Research Paper

Double stage converter with low current stress for low to high voltage conversion in nanogrid

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ABSTRACT

A low to high voltage conversion technique has been proposed in this paper using double stages of switched inductors for nanogrid applications. The proposed converter topology utilizes fewer components, achieves high voltage gain at a small value duty ratio, and has high efficiency. Moreover, the proposed converter provides a reduced switch current stress to obtain a stable constant boosted DC voltage. Therefore, it requires low-current rating switches and hence leads to cost reduction. Additionally, the load and the source end are connected to the same ground. The principle of operation, theoretical waveforms in Continuous Conduction Mode (CCM), and Discontinuous Conduction Mode (DCM) with steady-state analysis are discussed. A detailed discussion about the effect of non-idealities on the high voltage conversion, the design of components, and a comparison of the performance characteristics such as the number of components, Voltage Gain in CCM, switch current stress, normalized switch voltage stress, and efficiency of the proposed converter topology with other converters are presented. The experimental results of the 500W laboratory prototype are also shown to validate the operation of the proposed converter.

1. Introduction

The concept of nanogrid is comparatively new and pertains to a grid allocated to a distinct building or customer. Typically, there is a single generation unit within a Nanogrid, and it does not utilize either transmission or distribution lines and possibly will utilize a DC network. A Nanogrid is a small electrical system interfacing the grid of up to 100 kW capacity and confined to a solo building or major load or a system of loads up to 5 kW which are connected off-grid, both classifications representing devices (like Diesel Generator, smart loads, Electric Vehicles, and batteries) suitable for islanding and/or producing self-sufficient energy by incorporating an intelligent Distributed Energy Resources (DER) management/controls. Therefore, this combination of Renewable Energy Sources, Energy Storage Devices, and Intelligent control systems leads to improved home energy management, cost-effective solution, and income generation by providing grid support (Askarian et al., 2021). Many control strategies e.g. Control schemes for uncertain stochastic nonlinear system H-infinity (Hua et al., 2018), robust control scheme (Hua et al., 2019) are proposed to improve the Voltage strategy of a grid

system. In recent past years, a significant amount of research has been carried out to highlight the benefits of distributed generation. In a distributed generation, both the supply and storage are typically DC, and hence the benefits of a DC grid are often discussed in the literature. The need for increased efficiency in the DC power distribution system has led to this extensive research in the field of Microgrid and Nanogrid. Microgrids are mostly bigger than Nanogrids, and they normally work for the whole building or multiple buildings at a generation capacity of 1 kW to 50 kW. A Microgrid can function in both grid-connected as well as the off-grid mode by connecting and disconnecting itself from the grid. Comparatively complex energy systems with many energy sources are present in Microgrids. Microgrids work for a large number of customers and utilize the distribution lines also. Besides urban, rural, and industrial sectors Microgrids are also installed for the whole campus, like military establishments, business organizations, hospitals, and universities, etc.

Several technologies are associated with Nanogrids, but the Nanogrid literature is dominated by the research on converter topologies. Within the Nanogrid, it is the responsibility of the DC–DC converters to manipulate the voltages to fulfill the requirements of a particular task. DC–DC converters usually (but not necessarily) connect the sources of Nanogrid to the systems bus/the national grid and connect the bus to loads of Nanogrid. The output voltage of the converter can be lesser or greater in

amplitude than the input voltage. Reactive components such as capacitors and inductors, switching components such as diodes, MOSFETs, and IGBTs are utilized by the converters to achieve this variation in voltage amplitude (Burmester et al., 2017). The basic block diagram depicting the structure of the DC Nanogrid is shown in Fig. 1.

The function of a DC–DC converter is basically to either step up or step down the input voltage subject to the output voltage requirements. The converter Topology proposed here has to be used as the Source DC–DC Converter within a DC Nanogrid. It can be easily visualized that how a DC Nanogrid possibly will utilize the DC–DC converters. The DC voltage is supplied at the input of the DC to DC converters, and an improved DC voltage is obtained at the output. As shown in Fig. 1, the variable/low DC input voltage taken by the source converters is boosted to the required 400 V at the output for the DC bus. Several functions can be performed by using the source DC–DC converter, such as:

- Interfacing of different sources: Different kinds of sources can be connected to a Nanogrid at a time, such as a Solar PV array, Small Scale Wind Turbine, and Battery Storage providing power to the Nanogrid. Each of these sources has its operating characteristics. Therefore, each source needs a DC–DC Converter to assimilate the different sources into the Nanogrid. The regulation of the supply is guaranteed by the converter along with providing protection.
- Voltage at Bus: The source voltage can be converted up to a DC bus voltage level of 380 V using a DC–DC converter, which is nowadays the standard, intermediate dc voltage level for industry applications.

In general, the source voltage must be stepped up, so the boost or buck-boost type converters are typically used as the source DC–DC converter. These converters are required to have an efficiency greater than 85% and it is better to be more than 90%. The prime focus of the research being carried out in the field of Nanogrid is to find out the techniques to increase the efficiency of the DC–DC converters used inside the Nanogrid (Askarian et al., 2021; Burmester et al., 2017). The main motivations of DC–DC converters with a high voltage conversion ratio are power level, efficiency, power density, cost, complexity, and reliability (Bhaskar et al., 2019; Forouzesh et al., 2017).

To attain a high voltage conversion ratio at an appropriate duty cycle value, numerous topologies of high gain DC–DC converters have been proposed in the literature so far providing high efficiency and low component stress values (Forouzesh et al., 2017; Blaabjerg et al., 2021). A high step-up voltage is attained by employing the conventional DC–DC boost converter. Nevertheless, the switch voltage stress of a conventional DC–DC boost converter is the same as the output voltage. In addition, at high duty cycle values, the switch voltage/current stress limits the voltage conversion ratio, leading to a high value of conduction loss (Babaei et al., 2018). Besides, the parasitic resistance of the inductor/capacitor, severe reverse-recovery glitches related to the diode, high rating semiconductor components, and a high value of the conduction loss across the switch leads to a decline in the system efficiency and impose a limit to the maximum value of voltage conversion ratio (Bhaskar et al., 2017; Ioinovici, 2013; Sadaf et al., 2021b). To get rid of these issues, various structures of isolated converters have been proposed so far, including forward converters, push–pull, flyback, SEPIC, and full/half-bridge converters where the transformer or coupled inductor turns ratio is regulated to attain a high voltage conversion ratio (Alajmi et al., 2020; Kanamarlapudi et al., 2018; Azizkandi et al., 2020; Moradpour et al., 2018; Alajmi et al., 2021). The multiport type of Isolated DC–DC converters offer multiport structures without adding too many components, and they do not allow the flow

of circulating currents between the different input ports working at diverse PV voltages. Also, the duty cycle of the input port regulates the flow of power between the input and output ports, and hence phase-shift control is not required. Nonetheless, some drawbacks are also associated with isolated converter configurations. The main disadvantages of isolated converters are high power loss, high spikes in switch voltage, massive circuit structure, and saturation of transformer core. In addition, the leakage inductance of the transformer causes high voltage stress across the active switches of the converter. Moreover, the size and cost of the isolated type of DC–DC converters are more due to the necessity of an extra active clamping circuit, a transformer with high frequency, and a snubber circuit (non-dissipative) (Richard et al., 2019; Sadaf et al., 2021).

To overcome the issues mentioned above, the non-isolated type of DC–DC converter topologies can be incorporated to attain a high gain in voltage in the case of non-galvanic insulation applications. Thereby reducing the overall weight, size, and volume of the converter by eliminating the use of a high-frequency transformer, which in turn improves the efficiency (Tofoli et al., 2015; Sagar Bhaskar et al., 2020). Cascade/quadratic boosts are the most common high-gain non-isolated DC–DC converters (Mukherjee and Strickland, 2016; Andrade and Martins, 2017; Lee and Do, 2019). However, circuit complexity and cost are more in such converters due to two or more DC–DC converters' cascading. Furthermore, a highly non-linear voltage gain leads to complex control requirements, and integration of two or more power switches is not so useful (Sadaf et al., 2021c). The other possible solutions are switched inductor/capacitor, hybrid of switched-inductor/capacitor converter and a boost converter (Wang et al., 2019; Nguyen et al., 2018; Samiullah et al., 2021; Salvador et al., 2020). However, usually, the requirement of numerous power stages increases the circuit cost and complexity in these converters. On the other hand, the requirement of high-power rating switches and high current stress across the diodes are the main disadvantages of the switched capacitor/voltage lift cells based converters because of the capacitor networks present in such converters; resulting in a decrease in efficiency (Lakshmi and Hemamalini, 2018). A high step-up voltage can also be attained with the use of converters with capacitor/diode voltage multiplier or interleaved configurations (Meraj et al., 2020; Nouri et al., 2020; Zhu et al., 2021). However, these converters involve several converter stages leading to increased cost and complexity due to various converters connected in parallel. Furthermore, some other drawbacks associated with these converters are high energy dissipation and complex control (Sadaf et al., 2021a).

A new double stage converter for DC Nanogrid low to high voltage conversion is proposed in this paper to overcome the above-mentioned drawbacks. The proposed converter utilizes a very simple structure incorporating very few components and provides very high efficiency. The proposed converter draws a continuous input current from the input source with low ripple and achieves a higher voltage gain at a small value of duty ratio. The proposed converter provides a reduced switch current stress to obtain a constant DC step-up voltage. Therefore, it requires switches with low-current rating, since the two switches equally share the total input current. Normally, as the rating of a device increases its ON-state resistance increases. It is observed that lower rating components are required for the proposed converter and hence it is a low-cost design. The active switches of the proposed converter have low conduction loss, its design is transformer-less, and has a simplified control. Moreover, the load and source end of the proposed converter has a common ground connection. Therefore, for this converter to be used in PV systems, common-mode voltage and leakage reduction techniques are not
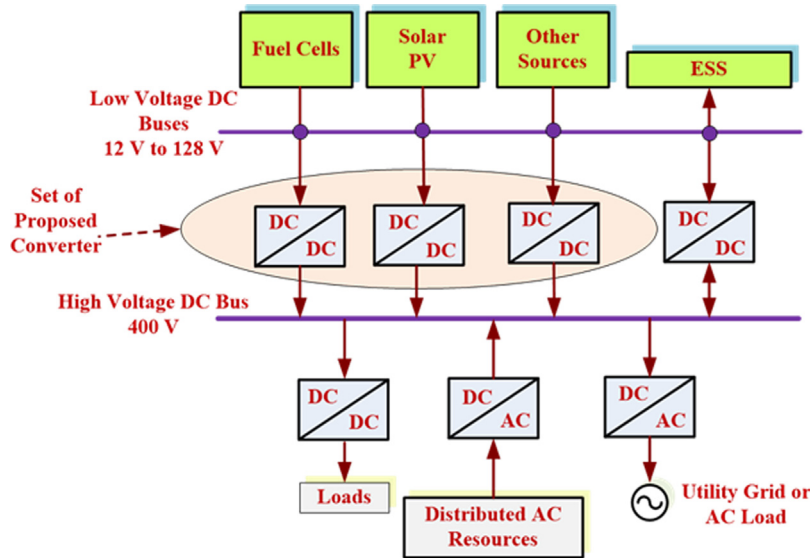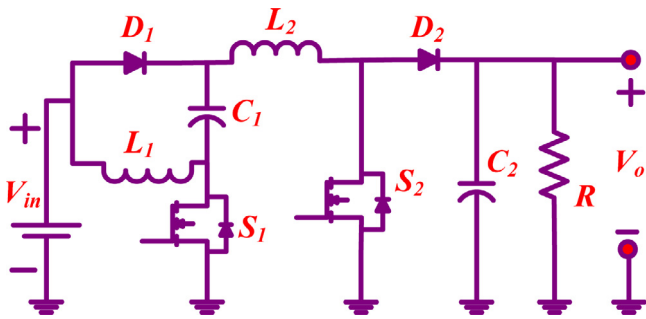
Fig. 1. Structure of DC nanogrid.

Fig. 2. Power circuitry of the proposed converter.

required, and hence making the proposed converter highly suitable for integration of solar PV panels with the DC Nanogrid system at the 400 V bus.

The manuscript is arranged as follows: Section 2 elaborates the power circuit and the operational theory of the proposed converter, followed by the mathematical analysis. Section 3 discusses how the non-idealities of different elements in the circuit affect the gain in voltage and efficiency calculation. The proposed converter topology is compared with various high gain DC–DC converters in Section 4, and a detailed comparison is provided. Section 5 gives the design of the circuit components. Section 6 presents the experimentally obtained results. Finally, the conclusion is given in Section 7.

2. Proposed converter topology

Fig. 2 shows the proposed double stage converter power circuitry for nanogrid low to high voltage conversion. It comprises two active switches S_1 and S_2, two inductors L_1 and L_2, diodes D_1 and D_2, two capacitors C_1 and C_2, and a load R. The switching frequency at which the switch S_1 and switch S_2 are being turned ON and OFF is indicated by f_S.

To discuss the steady-state operational theory of the proposed converter, the circuit elements are considered ideal. The equivalent series resistance (ESR) effects of the inductors and capacitors, ON-state switch resistance, and forward voltage drop across the diodes have not been taken into account. Also, for the output voltage to remain constant, the capacitance value of the

output capacitor C_2 is considered to be large enough. The value of inductance for both the inductors L_1 and L_2 is assumed to be equal. Therefore,

$$L = L_1 = L_2 \tag{1}$$

The steady-state mathematical analysis in CCM and DCM and the principle of operation are discussed below. The CCM and DCM characteristics waveforms for the proposed converter are displayed in Fig. 3.

2.1. Working principle (CCM)

The two working modes involved in the Continuous Conduction Mode (CCM) of the proposed converter are explained in this section, and the equivalent circuit is depicted in Fig. 4. During one switching period T_S, both the switches of the proposed converter are simultaneously operated using the same values of duty pulse as well as the duty ratio. Hence, there are two working modes in CCM: CCM_I and CCM_{II} for the proposed converter. Both the switches (S_1 and S_2) are ON in CCM_I, while switches (S_1 and S_2) are at OFF position in CCM_{II}.

CCM_I: Fig. 4(a) shows the power circuit for this mode. Both the switches S_1 and S_2 are at ON position during this mode. The input voltage supply (V_{in}) charges inductor L_1 (via switch S_1), the capacitor C_1 (via diode D_1 and switch S_1), and inductor L_2 (via D_1 and S_2), and the energy of the capacitor C_2 is supplied to the load (R). Diode D_1 is forward biased, and diode D_2 is reversed biased. It is observed that the input voltage (V_{in}) charges both the inductors (L_1 and L_2) and the capacitor C_1 in parallel. Therefore, in this mode, the inductors L_1 and L_2 voltages/currents are indicated by the following expressions:

$$V_L = V_{L1} = V_{L2} = V_{C1} = V_{in}, \ V_{C2} = V_o \tag{2}$$

$$I_{in} = I_{L1} + I_{L2} + I_{C1}, \ I_{C2} = -I_o \approx -\frac{V_o}{R} \tag{3}$$

where output voltage (average) is indicated by V_o, the input current is indicated by I_{in}, the output current is indicated by I_o, voltages across capacitors C_1 and C_2 are indicated by V_{C1} and V_{C2}, and currents through capacitors C_1 and C_2 are indicated by I_{C1} and I_{C2}, the currents through the inductors L_1 and L_2 are indicated by
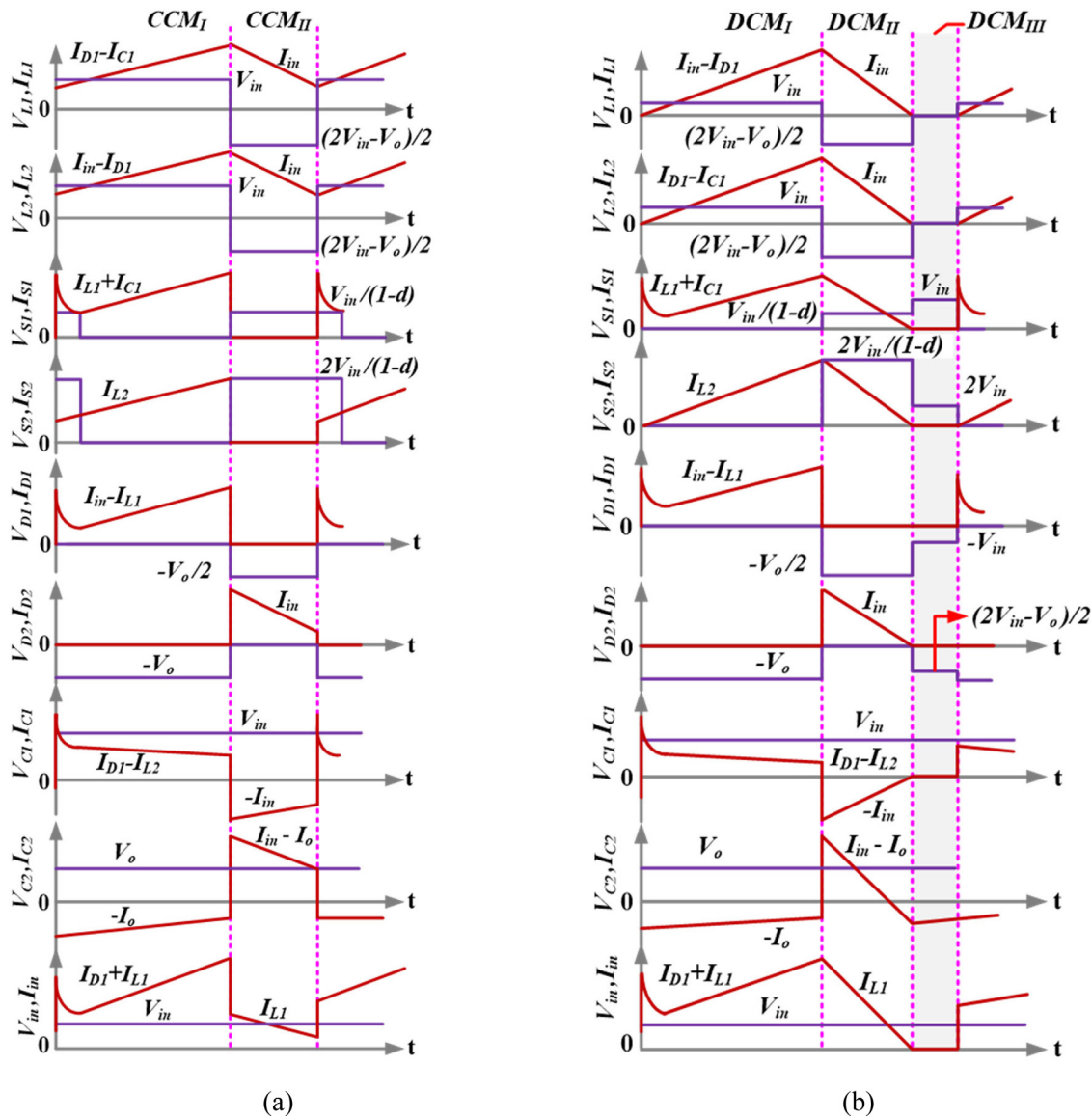
Fig. 3. Typical characteristics waveforms indicating the variations in voltages and currents for different circuit components with respect to time in (a) CCM, (b) DCM. *The units for all the given voltages are Volts, for all the given currents are Ampere, and for all the given times are Second.
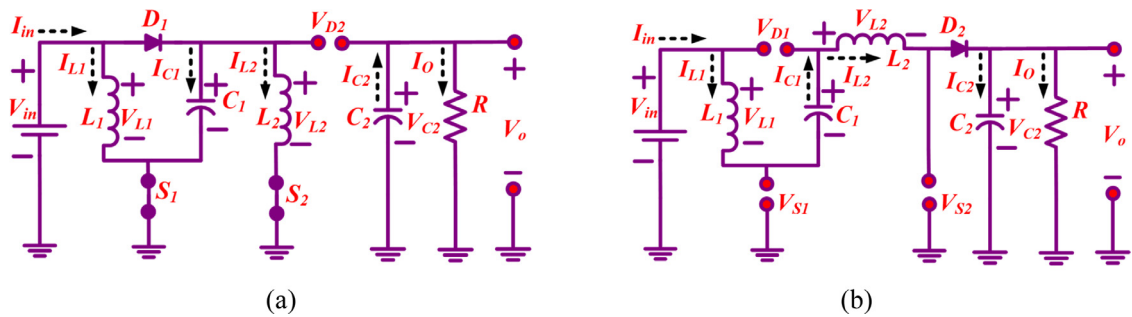

Fig. 4. Operating modes in CCM (a) CCM_I and (b) CCM_{II}.

I_{L1} and I_{L2}, the voltages across inductors L_1 and L_2 are indicated by V_{L1} and V_{L2}, respectively.

The switches S_1 and S_2 voltages/currents are indicated by the following expression:

$$V_S = V_{S1} = V_{S2} = 0, \ I_{S1} = I_{L1} + I_{C1}, I_{S2} = I_{L2} \quad (4)$$

CCM_{II}: The power circuitry of this mode is shown in Fig. 4(b). Both switch S_1 and switch S_2 are being turned OFF simultaneously during this mode. During this mode, the output capacitor C_2 is charged by the series combination of input voltage supply (V_{in}), inductor L_1, capacitor C_1, inductor L_2. Also, via diode D_2, the input

side energy is supplied to the load R. In this mode, Diode D_2 and diode D_1 are forward and reversed biased, respectively. Therefore, in this mode, inductors L_1 and L_2 voltages/currents are indicated by the following expressions:

$$V_L = V_{L1} = V_{L2} = \frac{2V_{in} - V_o}{2}, \ V_{C2} = V_o \tag{5}$$

$$I_L = I_{L1} = I_{L2} = I_{in} = I_{C1}, \ I_{C2} \approx I_L - \frac{V_o}{R} \tag{6}$$

The switches S_1 and S_2 voltages/currents are indicated by the following expressions:

$$\begin{cases} V_{S1} = \dfrac{V_{in}}{(1-d)}, \ V_{S2} = \dfrac{2V_{in}}{(1-d)}, \\ I_{S1} = I_{S2} = 0 \end{cases} \tag{7}$$

Therefore, the gain in voltage for the proposed converter in CCM is shown as,

$$M_{CCM} = V_o/V_{in} = 2/(1-d) \tag{8}$$

where (d) is the duty cycle of the proposed converter and (M) is the gain in voltage and the voltage gain for CCM (Continuous Conduction Mode) is indicated as M_{CCM}.

2.2. Working principle (DCM)

Discontinuous Conduction Mode (DCM) has three modes of operation: DCM_I, DCM_{II}, and DCM_{III} for the proposed converter. In DCM_I, both the switches S_1 and S_2 are at ON position, in DCM_{II} switches S_1 and S_2 are at OFF position with the inductor currents having a non-zero value, and in DCM_{III}, switch S_1 and switch S_2 are at OFF position with inductor current values equal to zero. The three working modes involved in the DCM of the proposed converter are explained in this section, and power circuitry for DCM_{III} is depicted in Fig. 5. The characteristic waveform of DCM is displayed in Fig. 3(b), where $K_I T_S$ is the time period for DCM_I, $K_{II} T_S$ is the time period for DCM_{II}, and $K_{III} T_S$ is the time period for DCM_{III}; K_I, K_{II}, and K_{III} are the constant multiples of the time period for DCM_I, DCM_{II}, and DCM_{III}, respectively.

DCM_I: The proposed converter's operating principle and power circuit in DCM_I are the same as that in CCM_I; both the switches (S_1 and S_2) are at ON position. The input voltage (V_{in}) is charging both the inductors (L_1 and L_2) and the capacitor C_1 in parallel. In this mode, the inductors (L_1 and L_2) currents initiated at zero value and reached a maximum value at the end. The maximum current values through L_1 and L_2 can be obtained from the following expression:

$$I_{L\max} = I_{L1\max} = I_{L2\max} = V_{in}K_I/Lf_s \tag{9}$$

where the maximum value of inductor (L_1 and L_2) currents are indicated by I_{L1max} and I_{L2max}, respectively, and $f_s = 1/T_S$ indicates the switching frequency. The inductors L_1 and L_2 ripple currents can be shown as,

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = V_{in}K_I/Lf_s \tag{10}$$

where the inductors (L_1 and L_2) ripple currents are indicated by ΔI_{L1} and ΔI_{L2}, respectively.

DCM_{II}: The proposed converter's operating principle and power circuit in DCM_{II} are the same as that in CCM_{II}; switch S_1 and switch S_2 are at OFF position with non-zero inductor currents. The output capacitor C_2 is charged by the series combination of input voltage supply (V_{in}), inductor L_1, capacitor C_1, inductor L_2. Via diode D_2, energy is supplied to the load R. In this mode, the inductors L_1 and L_2 currents started initially from a maximum
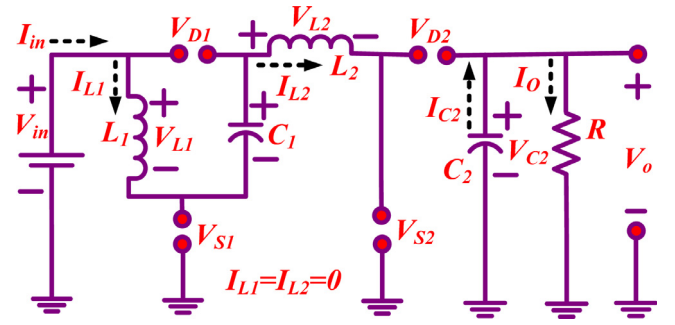

Fig. 5. Power circuitry of the proposed converter in DCM_{III}.

value and reached a zero value at the end. The maximum currents flowing through inductors L_1 and L_2 can be obtained from the following expression:

$$I_{L\max} = I_{L1\max} = I_{L2\max} = (2V_{in} - V_o)K_{II}/2Lf_s \tag{11}$$

The inductors L_1 and L_2 ripple currents can be shown as,

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = (2V_{in} - V_o)K_{II}/2Lf_s \tag{12}$$

DCM_{III}: The equivalent circuit of the proposed converter in DCM_{III} is displayed in Fig. 5. In this mode, switches S_1 and S_2 are at the OFF position with zero inductor current values. Therefore, both the inductors L_1 and L_2 are completely de-energized. Both the diodes (D_1 and D_2) are reversed biased in this mode and the energy stored in the output capacitor C_2 only is supplied to the load R. From Eqs. (9) and (11) K_{II} is shown by the following expression:

$$K_{II} = \frac{2V_{in}K_I}{(2V_{in} - V_o)} \tag{13}$$

The average current through the output capacitor C_2 for one switching period can be obtained as follows,

$$I_{C2} = \frac{1}{2}K_{II}I_{L\max} - I_o = \frac{1}{2}K_{II}I_{L\max} - \frac{V_o}{R_o} \tag{14}$$

From Eqs. (9), (13), & (14)

$$I_{C2} = \frac{(V_{in}K_I)^2 T_S}{(2V_{in} - V_o)L} - \frac{V_o}{R} \tag{15}$$

In steady-state conditions, the average current flowing through a capacitor is always zero, hence Eq. (15) can also be written as,

$$\frac{(V_{in}K_I)^2 T_S}{(2V_{in} - V_o)L} = \frac{V_o}{R} \tag{16}$$

From (16), the quadratic equation obtained is as follows,

$$\left(\frac{V_o}{V_{in}}\right)^2 - \frac{V_o}{V_{in}} - \frac{K_I{}^2}{\xi_L} = 0 \tag{17}$$

where normalized time constant (ξ_L) for the inductor L_1 and inductor L_2 and is expressed as $\xi_L = \frac{L}{RT_S}$. Hence, the value of (ξ_L) changes with the change in L, R, and T_S. The gain in voltage for the proposed converter in DCM is indicated by M_{DCM} and can be expressed as,

$$M_{DCM} = \frac{V_o}{V_{in}} = 1 + \left(\frac{\xi_L + K_I{}^2}{\xi_L}\right)^{1/2} = 1 + \left(1 + \frac{K_I{}^2 R}{Lf_s}\right)^{1/2} \tag{18}$$

The switching frequency is indicated by f_S. When the gain in CCM is equal to the gain in DCM, a boundary condition is reached.
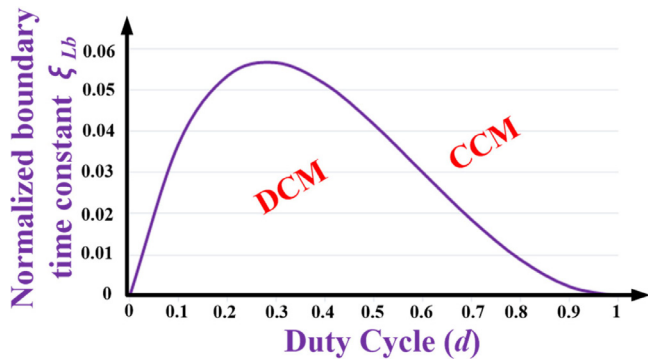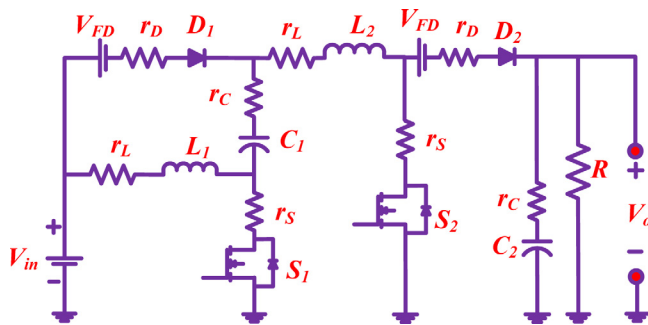
Fig. 6. Normalized boundary condition.

Fig. 7. Proposed converter with non-ideality characteristics.

Thus, from Eqs. (8) and (18),

$$1 + \left(1 + \frac{K_I{}^2 R}{L f_s}\right)^{1/2} = \frac{2}{1-d} \tag{19}$$

Now, as we know that the mode CCM_I is the same as that of mode DCM_I i.e. $d = K_I$. Therefore, the normalized time constant at the boundary conditions (ξ_{Lb}) for the inductors (L_1 and L_2) is shown by the following expression,

$$\xi_{Lb} = d \times \frac{\left(1 + d^2 - 2d\right)}{4} \tag{20}$$

Fig. 6 illustrates the variation of (ξ_{Lb}) with the variation in duty cycle (d) for the proposed converter. It is important to note that, the proposed converter works in CCM for the values of (ξ_L) greater than (ξ_{Lb}).

3. Non-idealities' effect of the circuit elements on voltage conversion ratio

The proposed converter's power circuit with consideration of the non-idealities of the circuit elements to study their effect on voltage gain is shown in Fig. 7. The ESR of inductors L_1 and L_2 is denoted as r_L. The non-ideality of the diodes is represented by their internal resistance (r_D) and the threshold voltage (V_{FD}). Hence, the non-ideality of diodes D_1 and D_2 is represented with their respective internal resistance and forward voltage drop as shown in Fig. 7. Similarly, switches S_1 and S_2 are represented with their internal resistance r_S. The ESR for the capacitors C_1 and C_2 are represented with their internal resistance r_C.

3.1. Effect of inductors L_1 & L_2 ESR

The effect of the inductor's ESR on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the ESR of both the inductors is assumed to be equal i.e. $r_{L1} \approx r_{L2} \approx r_L$. Therefore, the inductors L_1 and L_2 voltages in CCM_I and CCM_{II} can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in} - I_{L1} r_L, \, V_{L2} \approx V_{in} - I_{L2} r_L \tag{21}$$

$$CCM_{II} : V_{L1} \approx V_{in} - I_{L1} r_L - \frac{V_o}{2}, \, V_{L2} \approx V_{in} - I_{L2} r_L - \frac{V_o}{2} \tag{22}$$

From (21) and (22),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - I_{L1} r_L - I_{L2} r_L \tag{23}$$

$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - I_{L1} r_L - I_{L2} r_L - V_o \tag{24}$$

Considering inductor volt second balance principle and small approximation technique,

$$(2V_{in} - I_{L1} r_L - I_{L2} r_L) \, d = -(2V_{in} - I_{L1} r_L - I_{L2} r_L - V_o) (1 - d) \tag{25}$$

The expression of voltage gain for the proposed converter with consideration of the effect of the inductor's ESR is expressed as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_L} = \frac{2 - \frac{r_L}{V_{in}} (I_{L1} + I_{L2})}{1 - d} \tag{26}$$

Now, on the assumption of V_{DL} as the ESR voltage drop across the inductors (i.e. $I_{L1} r_L$ and $I_{L2} r_L$ are equal to V_{DL}), (26) can be expressed as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_L} = \frac{2\left(1 - \frac{V_{DL}}{V_{in}}\right)}{1 - d} = \frac{2}{1 - d} - \frac{2 (V_{DL})}{V_{in} (1 - d)} \tag{27}$$

It is noticed from (26)–(27) that, with greater values of V_{DL} and d the voltage gain declines drastically. It indicates that the duty cycle and inductor's ESR should have a small value.

3.2. Effect of diodes D_1 and D_2 ESR

The effect of the non-ideality of the diode on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the following non-idealities are assumed: $r_{D1} \approx r_{D2} \approx r_D$ and $V_{FD1} \approx V_{FD2} \approx V_{FD}$. Therefore, the voltages across the inductors L_1 and L_2 in CCM_I and CCM_{II} can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in}, \, V_{L2} \approx V_{in} - I_{D1} r_D - V_{FD} \tag{28}$$

$$CCM_{II} : V_{L1} \approx V_{L2} \approx V_{in} - \frac{I_{D2} r_D + V_{FD} + V_o}{2} \tag{29}$$

From (28) and (29),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - I_{D1} r_D - V_{FD} \tag{30}$$

$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - I_{D2} r_D - V_{FD} - V_o \tag{31}$$

Considering inductor-volt-second-balance principle and small-approximation technique,

$$(2V_{in} - I_{D1} r_D - V_{FD}) \, d = -(2V_{in} - I_{D2} r_D - V_{FD} - V_o) (1 - d) \tag{32}$$

The voltage gain expression for the proposed converter by considering the effect of diodes (D_1 and D_2) ESR can be obtained as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_D, \, V_{FD}} = \frac{2 - \frac{V_{FD}}{V_{in}} - d\frac{r_D}{V_{in}} I_{D1} - (1 - d)\frac{r_D}{V_{in}} I_{D2}}{1 - d} \tag{33}$$

Now, on the assumption of V_D as the forward resistance voltage drop across the diodes (i.e. $I_{D1}r_D$ and $I_{D2}r_D$ are equal to V_D), (33) can be shown as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_D,\, V_{FD}} = \frac{2 - \frac{1}{V_{in}}(V_{FD} + V_D)}{1 - d} = \frac{2}{1 - d} - \frac{(V_{FD} + V_D)}{V_{in}(1 - d)} \quad (34)$$

It is noticed from (33)–(34) that, with greater values of V_D and d the voltage gain declines drastically. It indicates that the threshold voltage (V_{FD}) and the internal forward resistance of the diodes should have a small value.

3.3. Effect of switches S_1 and S_2 ESR

The effect of ESR of switches on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the internal forward resistance of switches is assumed to be equal i.e. $r_{S1} \approx r_{S2} \approx r_S$. Therefore, the voltages across the inductors L_1 and L_2 in CCM_I and CCM_{II} can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in} - I_{S1}r_S, \quad V_{L2} \approx V_{in} - I_{S2}r_S \quad (35)$$

$$CCM_{II} : V_{L1} \approx V_{in} - \frac{V_o}{2}, \quad V_{L2} \approx V_{in} - \frac{V_o}{2} \quad (36)$$

From (35) and (36),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - (I_{S1} + I_{S2})\, r_S \quad (37)$$

$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - V_o \quad (38)$$

Considering inductor volt second balance principle and small approximation technique,

$$(2V_{in} - (I_{S1} + I_{S2})\, r_S)\, d = -(2V_{in} - V_o)(1 - d) \quad (39)$$

The expression of voltage gain for the proposed converter with consideration of the effect of switches S_1 and S_2 ESR can be obtained as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_S} = \frac{2 - \frac{r_S}{V_{in}}(I_{S1} + I_{S2})\, d}{(1 - d)} \quad (40)$$

Now, on the assumption of V_{DS} as the ESR voltage drop across the switches (i.e. $I_{S1}r_S$ and $I_{S2}r_S$ are equal to V_{DS}), (40) can be expressed as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_S} = \frac{2 - \frac{2V_{DS}}{V_{in}}d}{(1 - d)} = \frac{2}{(1 - d)} - \frac{2V_{DS}d}{V_{in}(1 - d)} \quad (41)$$

It is noticed from (40)–(41) that, with greater values of V_{DS}/V_{in} and d the voltage gain declines drastically. It indicates that the inductor's ESR should have a small value.

3.4. Effect of intermediate capacitor C_1 ESR

The voltage drop across the capacitor's internal resistance r_C is assumed as V_{DC}. The input voltage supply (V_{in}) charges the capacitor C_1 in CCM_I. The capacitor C_1 is being discharged by the current I_{L1} in CCM_{II}. Hence, it experiences a drop in voltage which is indicated by ΔV_{C1},

$$V_{C1} = V_{in} - V_{DC} - \Delta V_{C1} \approx V_{in} - \frac{t}{C_1}I_{L1} \quad (42)$$

The voltage across the capacitor C_1 at the end of CCM_{II} is expressed as,

$$V_{C1} = V_{in} - \frac{1}{C_1}\int_{dT_s}^{T_s} I_{L1}dt = V_{in} - \frac{1 - d}{C_1}T_s I_{L1} \quad (43)$$

The current I_{L1} during CCM_{II} can be shown by the following expression,

$$I_{L1} = I_o + I_{C2} = \frac{I_o}{1 - d} \quad (44)$$

From (43) and (44),

$$V_{C1} = V_{in} - \frac{1 - d}{C_1}T_s \frac{I_o}{1 - d} = V_{in} - \frac{V_o}{f_s R C_1} \quad (45)$$

As we know that the currents through the inductors in CCM_I and CCM_{II} modes increase and decrease, respectively. The comparison of the ripples in CCM_I and CCM_{II} shows that,

$$\frac{dT_s}{L_1}V_{in} = \frac{(1 - d)\, T_s}{L_1}(V_o - V_{in} - V_{C1}) \quad (46)$$

From (42), Eq. (46) can be written as

$$\frac{dT_s}{L_1}V_{in} = \frac{(1 - d)\, T_s}{L_1}(V_o - 2V_{in} + \Delta V_{C1}) \quad (47)$$

From (45)–(47), the voltage gain can be expressed as,

$$V_o|_{C_1} = \frac{2V_{in}}{(1 - d)\left(1 + \frac{t}{(1-d)RC_1}\right)} \quad (48)$$

From (48), the output voltage at the beginning of CCM_{II} is expressed as,

$$V_o = \frac{2V_{in}}{(1 - d)} \quad (49)$$

Also, the output voltage at the end of CCM_{II} is dropped down and expressed as,

$$V_o|_{C_1} = \frac{2V_{in}}{(1 - d)\left(1 + \frac{1}{f_s R C_1}\right)} = \frac{2V_{in}}{(1 - d)\left(\frac{f_s R C_1 + 1}{f_s R C_1}\right)} \quad (50)$$

Hence, the gain in voltage and the drop in output voltage is predictable for $f_s R C_1 \gg 1$,

$$\Delta V_o|_{C_1} = \frac{2V_{in}}{(1 - d)f_s R C_1} = \frac{V_o}{f_s R C_1} \quad (51)$$

From (51), the gain in voltage gain can be expected as,

$$\left.\frac{V_o}{V_{in}}\right|_{C_1} = \frac{2}{(1 - d)\left(1 + \frac{1}{f_s R C_1}\right)} \quad (52)$$

From the above expression, the values of switching frequency, load, and capacitor C_1 can be selected appropriately.

3.5. Effect of output capacitor C_2 ESR

The voltage drop across the capacitor C_2 due to internal resistance (r_C) is indicated as (V_{DC}). In CCM_I, the energy of capacitor C_2 is being released through (R). Therefore, the capacitor C_2 voltage being the same as the output voltage, also drops down and can be expressed as,

$$V_{C2} = V_o - V_{DC} - \frac{t}{C_2}I_o \approx V_o\left(1 - \frac{t}{RC_2}\right) \quad (53)$$

The final expression at the end of CCM_I is indicated by (ΔV_o) and can be written as,

$$\Delta V_o|_{C_2} = \frac{dV_o}{f_s R C_2} \quad (54)$$

It indicates that the switching frequency f_s, load R, and capacitance C_2 should be selected appropriately. The variation in the output voltage caused by the combination of both the capacitors C_1 and C_2 is expressed as,

$$\Delta V_o|_{C_1 + C_2} = \Delta V_o|_{C_1} + \Delta V_o|_{C_2} = \frac{V_o}{f_s R}\left(\frac{1}{C_1} + \frac{d}{C_2}\right) \quad (55)$$

3.6. Overall effect of non-idealities

The non-idealities associated with the inductors, diodes, the capacitors, and switches' ESR effect have been taken into account; the gain in voltage can be shown by using the following expression,

$$\frac{V_o}{V_{in}} \approx \frac{2}{1-d} - \frac{2(V_{DL})}{V_{in}(1-d)} - \frac{(V_{FD}+V_D)}{V_{in}(1-d)} - \frac{2V_{DS}d}{V_{in}(1-d)}$$
$$- \frac{2f_sRC_1C_2}{(1-d)(f_sRC_1C_2+dC_1+C_2)} \tag{56}$$

From Eq. (56), the gain in voltage is observed to be decreasing with the increasing values of voltage drop caused by each ESR and duty ratio. Therefore, for the proposed converter it is advisable to select semiconductor devices with the lower internal resistance and the duty ratio moderate values.

3.7. Evaluation of efficiency

The proposed converter's overall efficiency can be expressed as,

$$\eta = \frac{2 - \frac{2(V_{DL})}{V_{in}} - \frac{2V_{DS}d}{V_{in}} - \frac{(V_{FD}+V_D)}{V_{in}} - \frac{V_{DC}}{V_{in}} - V_{DC}}{2 + \frac{R(1-d)}{V_o \times V_{in}}P_{SW}} \tag{57}$$

where, P_{SW} indicates the overall switching loss during switching; P_{SW-S1} and P_{SW-S2} indicate the switching power losses for the switches S_1 and S_2, respectively. For switch S_1 and switch S_2, the rising and falling times are indicated by $t_{RS1/2}$, and $t_{FS1/2}$, respectively; I_{S1} and I_{S2} indicate the average currents through the switch S_1 and switch S_2; V_{S1} and V_{S2} indicate the voltages across the switch S_1 and switch S_2, respectively. The overall input/output power is obtained by using the following expressions,

$$P_{SW} = P_{SW-S1} + P_{SW-S2} = \frac{I_{S1}V_{S1}(t_{RS1}+t_{FS1}) + I_{S2}V_{S2}(t_{RS2}+t_{FS2})}{T_s} \tag{58}$$

4. Comparative Study

This section provides a detailed comparison of various high gain DC–DC converters with the proposed converter topology, like DDTM in Bhaskar et al. (2019), mSIBC in Sadaf et al. (2021b), converter in Sadaf et al. (2021c), Switched-Capacitor-Based Dual-Switch High-Boost DC–DC Converter (SCDS) (Nguyen et al., 2018), High Gain Switched-Inductor-Double-Leg Converter (HG-SIDL) (Samiullah et al., 2021), Non-isolated High-Step-Up DC–DC Converter Derived from Switched-Inductors and Switched-Capacitors (ASL-SU2C-VO) (Salvador et al., 2020), Converter in Lakshmi and Hemamalini (2018), and H-SLCs in Tang et al. (2015). Table 1 present the number of components, Voltage gain in CCM, switch current stress, normalized switch voltage stress, and efficiency for the various DC–DC converters being compared.

Only one switch is used in the classical boost converter. However, the switch voltage stress is higher, and the voltage conversion ratio is lesser than the proposed topology. The proposed converter utilizes fewer diodes than all the other converters except the converter proposed in Lakshmi and Hemamalini (2018) and the classical boost converter. It leads to lesser losses in the proposed circuit. Moreover, the total components count of the proposed converter is lesser than the converters proposed in Bhaskar et al. (2019), Nguyen et al. (2018), Samiullah et al. (2021), Salvador et al. (2020), and Tang et al. (2015), leading to an overall cost reduction of the circuit. The proposed converter achieves a higher voltage conversion ratio at a small value of duty cycle as compared to the traditional boost converter and the converter

topologies presented in Sadaf et al. (2021b,c), Nguyen et al. (2018) and Tang et al. (2015); while the gain in voltage is the same as the topology proposed in Samiullah et al. (2021) and Lakshmi and Hemamalini (2018). The source and load end of the converter in Sadaf et al. (2021b) and Sadaf et al. (2021c) are connected with the same ground, whereas all other converters are appropriate only for floating loads. It is observed from Table 1 that a lesser switch current stress is offered by the proposed converter topology in comparison to the rest of the converters except (Sadaf et al., 2021c; Salvador et al., 2020), and its value is half of the input current value. Therefore, lower current rating switches can be incorporated into the proposed circuit. The utilization of lower rating components in the proposed circuit offers a lesser ON-state resistance and a low-cost design as well. The efficiency of the proposed converter is greater than the converters in Bhaskar et al. (2019), Sadaf et al. (2021c), Nguyen et al. (2018), Samiullah et al. (2021), Salvador et al. (2020), Lakshmi and Hemamalini (2018), and Tang et al. (2015). Several factors influence the efficiency of a converter, such as voltage/current ratings of the components, their count, and types. Commonly, the device's ON-state resistance increases with an increase in its rating.

The converter topology proposed here develops a design with low cost and improved efficiency due to the usage of lower rating components. It is observed from the detailed comparative study that a high voltage conversion ratio, reduced current stress through the switches, and improved efficiency can be attained by the proposed converter topology by using fewer components. Moreover, the source and load end of the proposed converter has a common ground connection. Suppose we do not have a common ground between the source and load. In that case, there will be a potential difference between load and source ground, which will initiate a circulating current that is not suitable for the PV application. Therefore, for the proposed converter to be used in PV systems, common-mode voltage and leakage current reduction techniques are not required, and hence making the proposed converter highly suitable for integration of solar PV panels with the DC Nanogrid system at the 400 V bus.

5. Circuit components' design

A laboratory prototype of the proposed topology is developed to validate its operating principle and performance, where the typical input and output parameters are considered as follows: input voltage is 40 V, output voltage as 400 V, output power as 500 W, and the switching frequency as 100 kHz. The inductors are selected based on the current through the inductors, whereas the selection of capacitors is done based on the voltage across them. To obtain a better performance, the worst-case scenario has been considered to design the inductors and capacitors. Table 2 shows the specific values of various circuit components for the designed prototype.

5.1. Design of inductor

The 90% worst efficiency η(worst) has been selected to calculate the duty cycle.

$$d|_{\eta(worst)=90\%} = 1 - \frac{2}{M_{CCM}}\eta(worst) = 1 - \left(\frac{2}{10} \times 0.90\right) \approx 82\% \tag{59}$$

The critical values of the inductors L_1 and L_2 can be obtained as follows,

$$L_{1,C} = L_{2,C} = \frac{dV_{in}}{\Delta I_L f_s} = \frac{dV_{in}}{40\% \text{ of } I_L \times f_s} \tag{60}$$

Table 1
Comparison table.

Conv.	Number of reactive components		Semiconductor components count		Total	Voltage gain (M)	Normalized switch voltage stress	Switch current stress	Efficiency	Output port
	Inductor	Capacitor	Switches	Diodes						
A	1	1	1	1	4	$1/(1-d)$	1	I_{in}	98.33% at 200 W	Grounded
B	2	2	3	3	10	$(2-d_2)/(1-d_1-d_2)$	1/2, $(M-1)/M$	$I_{in}d_1/2$, $I_{in}d_2$	93.43% at 500 W	Floating
C	2	1	2	3	8	$(1+d)/(1-d)$	1/2, 1/2	$dI_{in}/2$, dI_{in}	97.17% at 500 W	Grounded
D	2	1	2	3	8	$(1+d)/(1-d)$	$(1+M)/2M$, 1	$I_{in}/2$, $I_{in}/2$	93.12% at 500 W	Grounded
E	1	3	2	4	10	$(3-2d)/(1-2d)$	$(1-M)/2$	$I_{in}/(3-2d)$	95.4% at 200 W	Floating
F	4	1	3	8	16	$(1+3d_1+d_2)/(1-d_1-d_2)$	$(1+M)/2M$, 1	$2I_{in}d_1/(1+3d_1+d_2)$, $2I_{in}d_2/(1+3d_1+d_2)$	94.69% at 500 W	Floating
G	2	3	2	3	10	$(3+d)/(1-d)$	$M/(3+d)$	$I_{in}/2$, $I_{in}/2$	94.53% at 200 W	Floating
H	2	1	3	2	8	$(1+d_1)/(1-d_1-d_2)$	$(1+M)/2M$, 1	$I_{in}/2$, I_{in}	93.60% at 100 W	Floating
I	2	1	2	4	9	$(1+2d)/(1-d)$	$(2+M)/3M$, $(1+2M)/3M$	–	93–95% at 200 W	Floating
J	4	1	2	7	14	$(1+3d)/(1-d)$	$(1+M)/2M$	–	93–95% at 200 W	Floating
K	2	2	2	2	8	$2/(1-d)$	$(1+M)/2M$, 1	$I_{in}/2$, $I_{in}/2$	96.9% at 500 W	Grounded

A: Traditional Boost Converter (Babaei et al., 2018), B: DDTM Converter (Bhaskar et al., 2019), C: modified SIBC (mSIBC) (Sadaf et al., 2021b), D: converter in Sadaf et al. (2021c), E: SCDS converter (Nguyen et al., 2018), F: HG-SIDL converter (Samiullah et al., 2021), G: ASL-SU2C-VO converter (Salvador et al., 2020), H: converter in Lakshmi and Hemamalini (2018), I: ASH-SLC in Tang et al. (2015), J: SH-SLC in Tang et al. (2015), K: proposed converter .

Therefore, using the given parameters, the critical values can be calculated as,

$$L_{1,C} = L_{2,C} = \frac{0.82 \times 40}{4.5 \text{ A} \times 100 \text{ kHz}} \approx 72.89 \text{ µH} \qquad (61)$$

Therefore, both the inductor values are selected based on (61), where 20% to 40% of the inductor current (average value) is indicated by ΔI_L and switching frequency for the switch control is indicated by f_s. The inductance values and the current rating of the inductors L_1 and L_2 should be more than the respective calculated values of input current and critical inductance. Therefore, inductors with the core of ferrite E-type rated at 1 mH/18 A have been selected for the designed prototype.

5.2. Design of capacitor

The current flowing through the capacitor C_1 is observed to be maximum when the switches are turned ON. Thus, the value of critical capacitance for the capacitor C_1 can be calculated as follows,

$$C_{1,C} = \frac{I_{in}(1-d)}{f_s \Delta V_{C1}} = \frac{12 \times 0.18}{100 \text{ kHz} \times 2 \text{ V}} = 10.8 \text{ µF} \qquad (62)$$

The capacitor C_1 voltage rating must be more than the input voltage value (40 V). Hence, a capacitor (film-type: rated at 22 µF/100 V) has been selected for the designed prototype. The value of critical capacitance for the capacitor C_2 can be calculated as follows,

$$C_{2,C} = \frac{dP_o}{V_o f_s \Delta V_{C2}} = \frac{0.82 \times 500}{400 \times 100 \text{ kHz} \times 4} \approx 2.56 \text{ µF} \qquad (63)$$

The capacitor C_2 voltage rating must be more than the output voltage value (i.e. 400 V). Hence, a capacitor (film-type: rated at 3.3 µF/450 V) has been selected for the designed prototype.

5.3. Diode selection

The critical value of diode D_1 voltage rating can be calculated as,

$$V_{D1,C} = \frac{V_o}{2} \text{ or } \frac{V_{in}}{1-d} \qquad (64)$$

The critical value of diode D_2 voltage rating can be calculated as,

$$V_{D2,C} = V_o \text{ or } \frac{2V_{in}}{1-d} \qquad (65)$$

The voltage ratings of the diodes D_1 and D_2 should be more than 200 V and 400 V, respectively for the selected parameters. The current ratings of the diodes D_1 and D_2 should be more than the input current i.e. I_{D1} and $I_{D2} > I_{in}$. Therefore, diodes STTH30R06 have been selected for the designed prototype.

5.4. Switch selection

The critical values of switches S_1 and S_2 voltage ratings can be calculated as,

$$V_{S1,C} = \frac{V_o}{2} \text{ or } \frac{V_{in}}{1-d}, \quad V_{S2,C} = V_o \text{ or } \frac{2V_{in}}{1-d} \qquad (66)$$

The voltage ratings of the switches should be more than 200 V and 400 V, respectively for the chosen parameters. The current ratings of switch S_1 and switch S_2 should be less than the input current value i.e. I_{S1} and $I_{S2} < I_{in}$. Therefore, switches C3M0065090 have been selected for the designed prototype.

6. Results and discussion

The working theory for the proposed converter is verified by developing a 500 W laboratory prototype. STTH30R06 is used for all the diodes, which is an ultra-fast recovery diode. To achieve higher efficiency and high switching operation, C3M0065090 silicon carbide MOSFET is used for the switches. Fig. 8(a) shows the output/input voltages and input/output currents waveforms
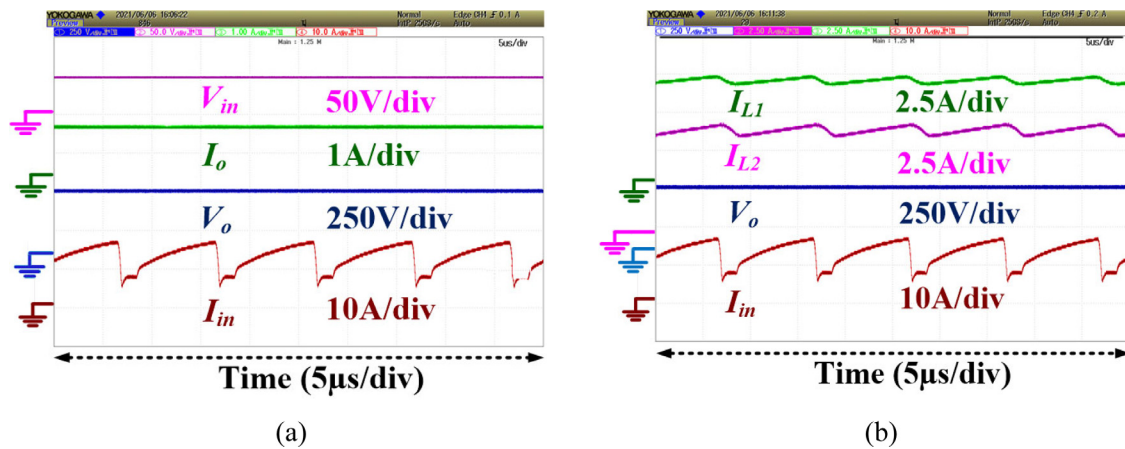
(a)   (b)

Fig. 8. Experimental results for (a) input voltage, output current, output voltage, and input current (b) inductor L_1 and inductor L_2 currents, input current, and output voltage.

obtained experimentally. It indicates that 400 V, 43 V, 1.25 A, and 12 A are the output voltage, input voltage, output current, and input current average values, respectively. It is important to note that the input current is continuous, and its slope is positive in the mode CCM_I due to the charging of the inductors L_1 and L_2. While the input current slope is negative in mode CCM_{II} due to the discharging of the inductor L_1 and inductor L_2. The peak value of efficiency for the proposed converter is observed as 96.9% at 500 W power. The waveforms for the inductors L_1 and L_2 currents obtained experimentally are presented in Fig. 8(b). The output voltage and input current waveforms are also shown for reference and to validate. It is important to note that the values of the average currents flowing through the inductors L_1 and L_2 are 6.72 A and 6.63 A, respectively.

The diodes D_1 and D_2 voltage waveforms obtained experimentally are displayed in Fig. 9(a). The waveforms of input current and output voltage are also shown for reference and to validate. It is important to note that, during the mode CCM_I the diode D_1 is forward biased whereas diode D_2 is reversed biased and vice-versa during the mode CCM_{II}. The diodes D_1 and D_2 PIV values are −200.1 V and −400.3 V, respectively. The fluctuations are observed in the PIV of diode D_1 and D_2 due to the parasitic capacitance of the switches and the practical mismatch of the inductor L_1 and inductor L_2. The waveform of the voltage for the capacitor C_1, and the voltages across both the switches S_1 and S_2, obtained experimentally are shown in Fig. 9(b); the input current waveform is also shown for reference and to validate. The voltage across the capacitor C_1 is found to be nearly equal to the input voltage (i.e. 42.4 V). The maximum switch voltage across the switches S_1 and S_2 are observed as 200.3 V and 399.4 V, respectively. The switch current waveforms of both the switches S_1 and S_2, obtained experimentally are shown in Fig. 9(c); the waveforms of the output voltage and input current are displayed for reference and to validate.

The maximum value of switch current through each of the switches S_1 and S_2 are observed as 6.61 A and 6.41 A, which is approximately equal to half of the input current value. Therefore, switches with a lesser current rating can be used in the proposed circuit. The utilization of lower rating components in the proposed circuit offers a lesser ON-state resistance and a low-cost design as well. The mathematical analysis shows that the decrease in voltage gain is in reverse proportion to the input voltage. Therefore, as the input voltage increases, the drop in output voltage automatically decreases. The conduction loss of the proposed converter is directly proportional to the current through each of the components, and these currents are directly

Table 2
Experimental parameters.

Parameters	Experimental values
Power	500 W
Input voltage (V_{in})	36 V to 48 V
Duty ratio	0.8 (for 40 V to 400 V conversion)
Output voltage (V_0)	400 V
Load	320 Ω
Switching frequency	100 kHz
Inductor L_1 and L_2	≈ 1 mH, 20 A (ferrite E core)
Capacitor C_1 , C_2	≈ 22 μF/100 V, 3.3 μF/450 V
Switches S_1, S_2	$V_{DS} = 900$ V, $i_D = 36$ A, $R_{ON} = 65$ mΩ (C3M0065090)
Diodes (D_1, D_2)	$V_{RRM} = 400$ V, $i_F = 30$ A, $R_{ON} = 0.01$ Ω, $V_F = 0.8$ V (STTH30R06)

proportional to the input current. Therefore, at a constant value of power, as the input voltage increases the input current decreases. The efficiency of the developed prototype is analyzed by studying the converter's performance at different values of input voltage and power. The efficiency curve of the developed prototype with the values of power varying from 100 W to 500 W, and variation in input voltage from 20 V to 43 V when the load is set at 320 Ω is shown in Fig. 9(d). When the input voltage is at 43 V, and the output power value is 500 W, the efficiency achieved by the designed prototype is 96.9%.

Fig. 10(a) shows the experimentally obtained waveform for the dynamically varying input and output voltage/current with the duty cycle variation from 0.5 to 0.8. The output voltage values are observed as 172 V, 215 V, 286 V, and 400 V approximately at the duty cycle values of 0.5, 0.6, 0.7, and 0.8, respectively. The experimentally obtained waveform for dynamically varying input and output voltage/current with the load variation is shown in Fig. 10(b). The experimental results show that the converter topology proposed here can develop steady input and output voltages/currents values.

7. Conclusion

A new double stage converter with low switch current stress for 400 V DC nanogrid low to high voltage conversion has been proposed in this paper. One of the main advantages of the proposed converter is that the switch current stress is reduced, as the current through both the switches is approximately half of the input current. Therefore, the proposed converter topology incorporates low current rating switches leading to cost reduction. The proposed converter topology utilizes fewer components,
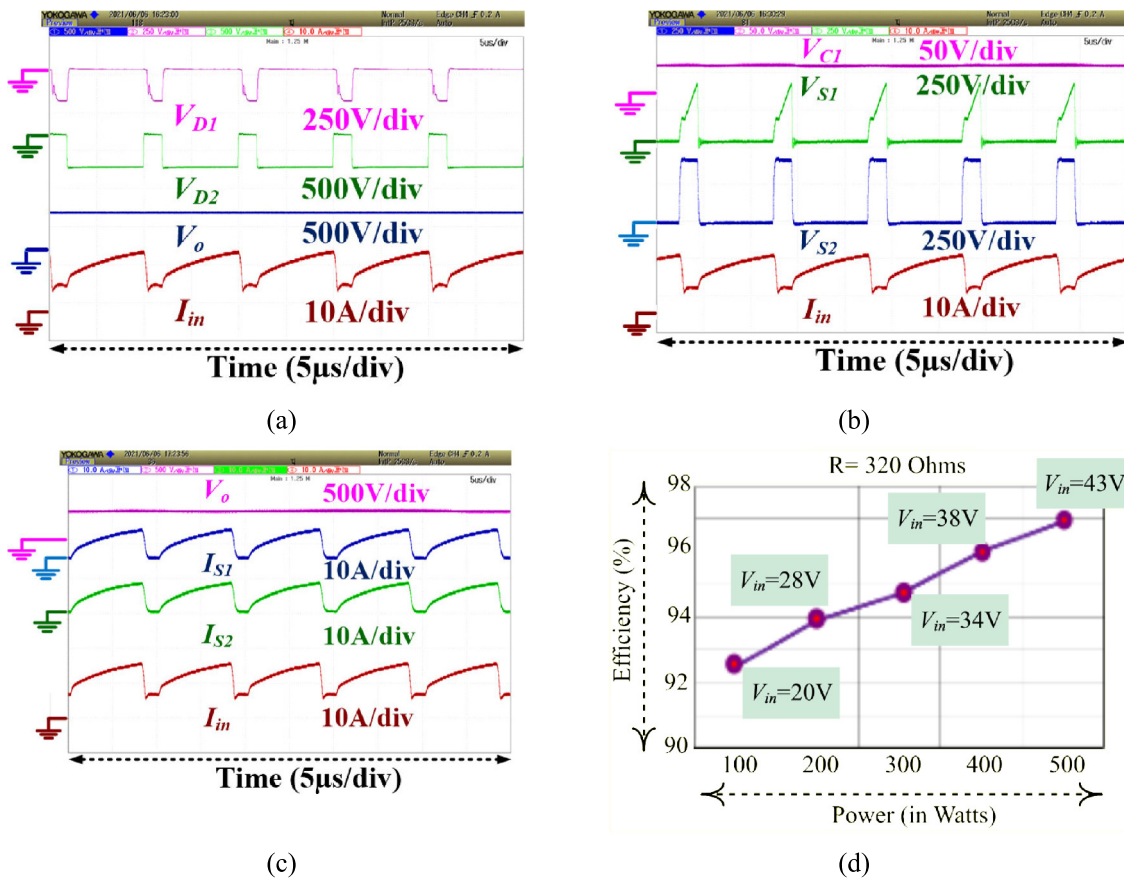
Fig. 9. The experimentally obtained waveform for (a) the diodes D_1, and D_2 voltages, output voltage, and input current (b) switch voltage for S_1 and S_2, the voltage across capacitor C_1, and input current, (c) switch current for S_1 and S_2, output voltage, and input current (d) Efficiency curve.
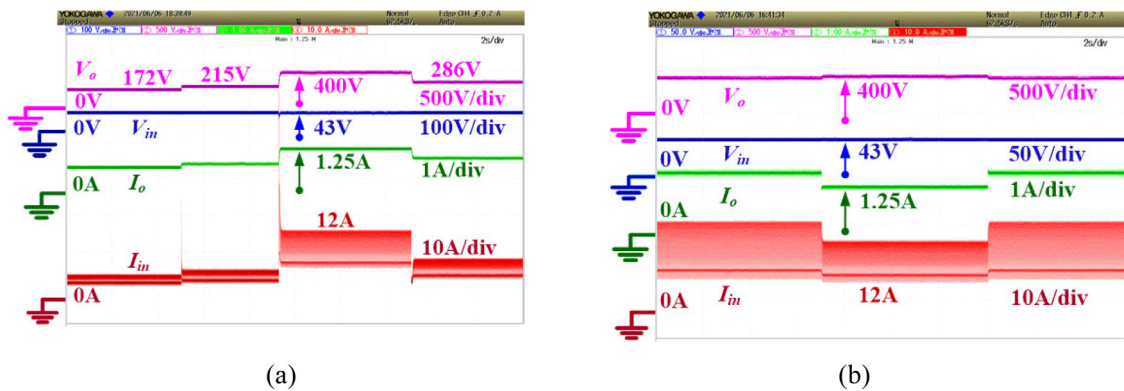

Fig. 10. The experimental waveforms for (a) dynamically varying input and output voltage/current with the duty cycle variation from 0.5 to 0.8, and (b) dynamically varying input and output voltage/current with the load variation.

achieves high voltage gain at a small value of duty ratio, and provides high efficiency. Also, the source and load end of the proposed converter circuit connected with a common ground makes it highly suitable for solar PV to be integrated with DC Nanogrid. The theoretical and mathematical analysis in both CCM and DCM is carried out for the proposed converter, and a formula for the voltage gain is obtained. Furthermore, a 500 W laboratory prototype is developed for the proposed converter and analyzed experimentally for its performance validation. With consideration of the physical constraints of the designed converter, the lower and upper limits of the duty cycle are set as 0.3–0.8. The direct connection of the pair of the diode and intermediate capacitor to the input supply and switch set a limitation on the proposed

converter. Due to this direct connection of the diode and intermediate capacitor with the input supply, it will experience a high transient peak current at the starting of the converter. The converter operation at different duty cycles and turn-on delay effect on the performance of the converter can be analyzed as future research work. Furthermore, there are multiple ways to extend the proposed configuration by using multiple switched inductors.

CRediT authorship contribution statement

Shima Sadaf: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Data curation, Writing –

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