

Received April 9, 2019, accepted April 22, 2019, date of publication May 3, 2019, date of current version May 16, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2914430

A New Multilevel Inverter Topology With Reduce Switch Count

MARIF DAULA SIDDIQUE¹, (Student Member, IEEE),
SAAD MEKHILEF^{1,2}, (Senior Member, IEEE),
NORAISYAH MOHAMED SHAH¹, ADIL SARWAR³,
ATIF IQBAL⁴, (Senior Member, IEEE), AND
MUDASIR AHMED MEMON¹

¹Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia

²Center of Research Excellence in Renewable Energy and Power Systems, King Abdulaziz University, Jeddah 21589, Saudi Arabia

³Department of Electrical Engineering, Aligarh Muslim University, Aligarh 202002, India

⁴Department of Electrical Engineering, Qatar University, Doha 2713, Qatar

Corresponding authors: Saad Mekhilef (saad@um.edu.my) and Atif Iqbal (atif.iqbal@qu.edu.qa)

This work was supported by the Qatar University through the QU High Impact Grant QUHI-CENG-19/20-2. The statements made herein are solely the responsibility of the authors. The publication charges are funded by the Qatar National Library, Doha, Qatar.

ABSTRACT Multilevel inverters are a new family of converters for dc–ac conversion for the medium and high voltage and power applications. In this paper, two new topologies for the staircase output voltage generations have been proposed with a lesser number of switch requirement. The first topology requires three dc voltage sources and ten switches to synthesize 15 levels across the load. The extension of the first topology has been proposed as the second topology, which consists of four dc voltage sources and 12 switches to achieve 25 levels at the output. Both topologies, apart from having lesser switch count, exhibit the merits in terms of reduced voltage stresses across the switches. In addition, a detailed comparative study of both topologies has been presented in this paper to demonstrate the features of the proposed topologies. Several experimental results have been included in this paper to validate the performances of the proposed topologies with different loading condition and dynamic changes in load and modulation indexes.

INDEX TERMS Asymmetric, hybrid inverter, inverter topology, multilevel inverter, MLI, nearest level control, power electronics, single-phase inverter, reduce switch count.

I. INTRODUCTION

Over the last few decades, multilevel inverter (MLI) topologies have gained popularity in industrial application because of the superior power quality compared to its conventional two-level counterpart. Lower harmonic distortion and better wave quality resembling a sinusoidal wave and lesser voltage stress on the switches have added to its popularity. For low and medium voltage/power applications, MLI find their applications in almost every field of electrical engineering including renewable energy systems, HVDC applications, distributed generation (DG) system, industrial drive applications, uninterruptible power supplies, etc [1]–[3]. They are widely used in drives and other allied areas in industries. MLI's are an assembly of power semiconductor devices along with different dc links to achieve staircase waveform close to sinusoidal at the output. Neutral Point Clamped (NPC),

The associate editor coordinating the review of this manuscript and approving it for publication was Tariq Masood.

Flying Capacitor (FC) and Cascade H-Bridge (CHB) are the three basic and popular MLI topologies used in commercial application since last few decades. Although there are few issues with the conventional MLI like a higher number of source requirement, voltage balancing of the capacitor and large switch requirement in CHB topology, FC topology and NPC topology respectively [4], [5]. Still, their advantages in terms of power quality supersede the shortcomings. Researchers have been trying to solve and mitigate the issues with MLI and have published a large number of papers over the last few years. They have mainly focused on reducing the switch count, source count and voltage balancing control of MLI. The design of MLI mainly depends upon the number of levels required at the output, number of semiconductor devices used, number of dc voltage sources and capacitors utilized, modularity of topology and the total standing voltage (TSV) of topology, etc. Based on these aspects, a number of MLI topologies have been presented and analyzed in the literature [2]–[7].

Another aspect of MLI has been the selection of magnitude of dc voltage sources used in the topology. Based on this, MLIs have been classified as symmetrical and asymmetrical. Symmetrical MLIs uses identical dc voltage sources whereas asymmetrical MLIs employs dc voltage sources having unequal magnitude. Symmetrical MLIs have more redundant states i.e. more number of switching combination are available to get same voltage level. This improves the performance of MLI in terms of balancing the voltage across capacitors and fault tolerant capabilities. However, at the same time symmetrical configured MLIs requires more number of switches, gate driver circuits, and dc voltage links. This increases the inverter size, cost and control complexity for a higher number of levels. Asymmetrical configuration increases the number of levels generated at the output compares to the symmetrical configuration using the same number of components and dc voltage sources [6], [7].

Various variants of conventional MLI have been reported in the literature to overcome the shortcomings while others have mentioned the shortcoming of a conventional multilevel inverter [8]. A higher number of switches are required to generate a staircase multilevel waveform. Moreover, even low rating switches require separate driver circuit along with necessary protective circuitry which adds to the complexity of the system. Authors of [8] have compared the work with several topologies. The results presented show that the number of IGBT required to realize a similar voltage level is lesser [8]. Moreover, the standing voltages are also lesser on the bidirectional switch. The topology of [8] has also been experimentally verified with a suitable design example.

The topology proposed in [9] utilized two novel cascaded multilevel inverters which contain five-level sub-module architecture. The proposed topology has been realized in both the asymmetrical and symmetrical mode of operation. The result shows the structure has advantages in levels of voltage generated for a given number of switches. The topology proposed in [10] requires eight switches to produce 15 level output. But the same voltage level can be achieved by PUC converter proposed in [11] and later in [12] with the lesser standing voltage on the switching devices. The proposed application of topology presented in [10] includes D-STATCOM, hybrid electric vehicle, and PV system.

Modular expendables symmetric and asymmetric structures with staircase cascading are reported in [13]. The topology has been compared with [14] and results presented claims to require lesser installation space and cost because of the reduced number of switching devices, switching and conduction losses and total standing voltage. The authors of [13] have also presented the simulation results which are validated by the experimental formulation of its prototype. The topologies of [15], [16] pointed out the disadvantage of H-bridge based multilevel converters topologies because of higher switching stress and total standing voltage. The ST topology is proposed in [16] contain two back to back connected T type switching arrangements (each T-section have two unidirectional and two bidirectional switches) joined

together to create a new structure which produces 17 levels without the H-Bridge circuitry for voltage polarity reversal. It utilizes 12 switches. The modules can be cascaded to produce a higher number of voltage level. An improved H-bridge based high step-up multilevel converter has been presented in [17]. The basic unit consists of two unidirectional switches, a capacitor, a power diode, and a dc voltage source. Control of switching devices ensures that the capacitor is charged to twice the voltage of dc source thereby developing output voltage higher than the input voltage. Two basic units along with the improved H-bridge unit constitutes the high step-up MLI. The topology proposed in [18] suggested another basic unit structure composed of four unidirectional switches, two bidirectional switches, and two dc sources. A modified H-Bridge is sandwiched between two such basic units forming a module with two dc sources on left of modified H-bridge and the remaining two are on the right side. The cascaded structure has also been presented. Various graphical representation of performance analysis points towards attractive features of the proposed multiple level converter. Similarly, some other upgraded topologies have been proposed in [19]–[29].

In this paper, work has been carried out with the aim of reducing the number of power semiconductor devices and dc voltage sources, while achieving a higher number of levels at the same time. This paper is organized as follows: Section II describes the proposed topology with its extension for a higher number of level. To set the benchmark of the proposed topology, Section III gives a quantitative comparison of the proposed topologies employing the same number of switches. Section IV elaborates the various experimental results and Section V summarizes the paper.

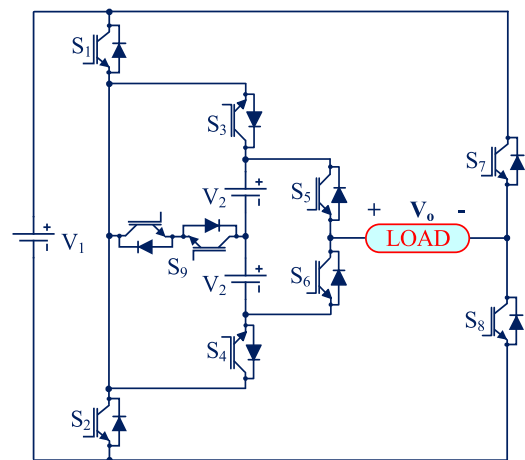


FIGURE 1. Proposed 3S-15L topology.

II. PROPOSED MULTILEVEL INVERTER

A. PROPOSED THREE SOURCE 15 LEVEL (3S-15L) TOPOLOGY

The proposed topology is depicted in Fig. 1. It consists of eight unidirectional switches from $S_1 - S_8$ along with one bidirectional switch S_9 . The switches $S_3 - S_6$ along with S_9 forms the inner part of the topology with two dc voltage

sources with a magnitude of V_2 . The remaining four switches i.e., $S_1 - S_2$ and $S_7 - S_8$ and one dc voltage source with magnitude of V_1 forms the outer portion of the proposed topology. The switches (S_1-S_2), (S_3-S_4), (S_5-S_6), and (S_7-S_8) need to operate in a complementary fashion to avoid short-circuiting of dc voltage sources.

The number of levels depends upon the magnitude of the dc voltage source, i.e., V_1 and V_2 the selection can be done in two ways as:

1) SYMMETRICAL CONFIGURATION

In this configuration, each dc voltage source has the same magnitude, i.e., $V_1 = V_2 = V_{dc}$. With such configuration, seven levels at the output are achieved.

2) ASYMMETRICAL CONFIGURATION

In the asymmetrical configuration, the magnitude of dc voltage sources have different magnitude, i.e., V_1 and V_2 have a different magnitude. For the proposed topology with asymmetrical configuration, the magnitude of dc voltage sources are chosen in tertiary mode, i.e., $V_1 = V_{dc}$, and $V_2 = 3V_{dc}$ (3S-15L Topology). With the tertiary configuration, the proposed topology generates 15 output voltage levels, i.e., zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, and $\pm 7V_{dc}$. The switching table for the proposed topology with the tertiary mode is given in Table 1. Furthermore, the different switching states for the proposed topology with tertiary mode are shown in Figs. 2 (a)-(h).

TABLE 1. Switching state for the proposed 3S-15L topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
1	0	0	1	1	0	0	1	0	$7V_{dc}$
0	1	0	1	1	0	0	1	0	$6V_{dc}$
0	1	0	1	1	0	1	0	0	$5V_{dc}$
1	0	0	0	1	0	0	1	1	$4V_{dc}$
0	1	0	0	1	0	0	1	1	$3V_{dc}$
0	1	0	0	1	0	1	0	1	$2V_{dc}$
1	0	1	0	1	0	0	1	0	V_{dc}
1	0	1	0	1	0	1	0	0	0
0	1	0	1	0	1	1	0	0	$-V_{dc}$
1	0	0	0	0	1	0	1	1	$-2V_{dc}$
1	0	0	0	0	1	1	0	1	$-3V_{dc}$
0	1	0	0	0	1	1	0	1	$-4V_{dc}$
1	0	1	0	0	1	0	1	0	$-5V_{dc}$
1	0	1	0	0	1	1	0	0	$-6V_{dc}$
0	1	1	0	0	1	1	0	0	$-7V_{dc}$

With tertiary mode, the maximum output voltage ($V_{o,max}$) of the proposed topology is:

$$V_{o,max} = (V_1 + 2V_2) = 7V_{dc} \tag{1}$$

The total standing voltage (TSV) is an important factor for the selection of switches. TSV is the addition of the maximum blocking voltage across each semiconductor device. The voltage stress across each pair of the complementary switch will

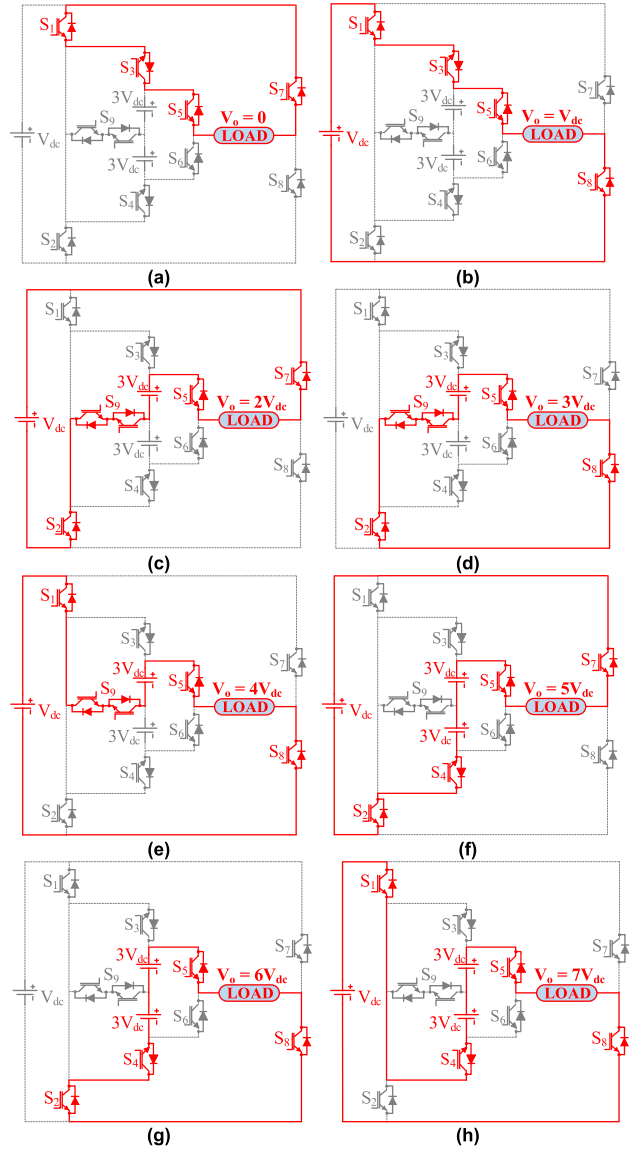


FIGURE 2. Different switching states of the proposed 3S-15L topology in positive half cycle. (a) $V_o = 0$. (b) $V_o = V_{dc}$. (c) $V_o = 2V_{dc}$. (d) $V_o = 3V_{dc}$. (e) $V_o = 4V_{dc}$. (f) $V_o = 5V_{dc}$. (g) $V_o = 6V_{dc}$. (h) $V_o = 7V_{dc}$.

be the same. Therefore,

$$\left. \begin{aligned} V_{S_1} &= V_{S_2} = V_1 = V_{dc} \\ V_{S_3} &= V_{S_4} = 2V_2 = 6V_{dc} \\ V_{S_5} &= V_{S_6} = 2V_2 = 6V_{dc} \\ V_{S_7} &= V_{S_8} = V_1 = V_{dc} \end{aligned} \right\} \tag{2}$$

The voltage stress across each unidirectional switch of the bidirectional switch S_9 is given as:

$$V_{S_9} = V_2 = 3V_{dc} \tag{3}$$

As two unidirectional switches are used for the bidirectional switch, each unidirectional switch needs to block the voltage of $3V_{dc}$. Therefore,

$$\begin{aligned} TSV &= 2(V_{S_1} + V_{S_3} + V_{S_5} + V_{S_7} + V_{S_9}) \\ &= 4V_1 + 10V_2 = 34V_{dc} \end{aligned} \tag{4}$$

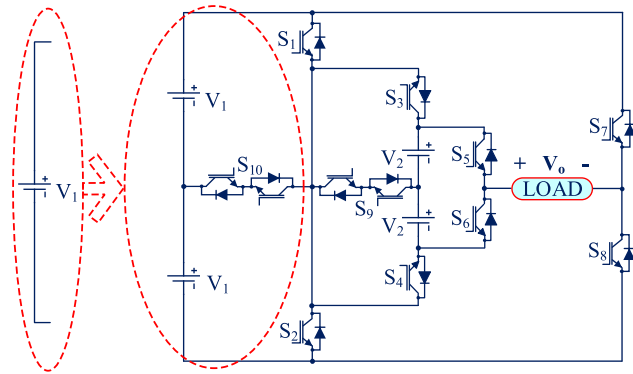


FIGURE 3. Proposed 4S-25L topology.

TABLE 2. Switching state for the proposed 4S-25L topology.

S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	V _o
1	0	0	1	1	0	0	1	0	0	12V _{dc}
0	0	0	1	1	0	0	1	0	1	11V _{dc}
1	0	0	1	1	0	1	0	0	0	10V _{dc}
0	0	0	1	1	0	1	0	0	1	9V _{dc}
0	1	0	1	1	0	1	0	0	0	8V _{dc}
1	0	0	0	1	0	0	1	1	0	7V _{dc}
0	0	0	0	1	0	0	1	1	1	6V _{dc}
1	0	0	0	1	0	1	0	1	0	5V _{dc}
0	0	0	0	1	0	1	0	1	1	4V _{dc}
0	1	0	0	1	0	1	0	1	0	3V _{dc}
1	0	1	0	1	0	0	1	0	0	2 _{dc}
0	0	1	0	1	0	0	1	0	1	V _{dc}
1	0	1	0	1	0	1	0	0	0	0
0	0	0	1	0	1	0	1	0	1	-V _{dc}
0	1	0	1	0	1	1	0	0	0	-2V _{dc}
1	0	0	0	0	1	0	1	1	0	-3V _{dc}
0	0	0	0	0	1	0	1	1	1	-4V _{dc}
0	1	0	0	0	1	0	1	1	0	-5V _{dc}
0	0	0	0	0	1	1	0	1	1	-6V _{dc}
0	1	0	0	0	1	1	0	1	0	-7V _{dc}
1	0	1	0	0	1	0	1	0	0	-8V _{dc}
0	0	1	0	0	1	0	1	0	1	-9V _{dc}
0	1	1	0	0	1	0	1	0	0	-10V _{dc}
0	0	1	0	0	1	1	0	0	1	-11V _{dc}
0	1	1	0	0	1	0	1	0	0	-12V _{dc}

B. PROPOSED FOUR SOURCE 25 LEVEL (4S-25L) TOPOLOGY

The proposed 3S-15L topology can be extended by replacing the single dc voltage source of magnitude V₁ with a T-configured two dc voltage sources with same magnitude V₁ as shown in Fig. 3. With the addition of one dc voltage source with magnitude V₁ and a bidirectional switch S₁₀, there is an addition in the number of levels. Again, for the symmetrical configuration, the proposed topology can generate nine levels. However, for asymmetrical configuration, the number of levels increases to 25. The 25 level output is achieved by selecting V₁ = V_{dc} and V₂ = 5V_{dc}. The different switching combination for the proposed topology with four dc voltage sources generating 25 levels is given in Table 2.

C. GENERALIZED STRUCTURE OF THE PROPOSED TOPOLOGY

In both proposed topologies with asymmetrical configuration, the magnitude of V₂ is higher compared to V₁.

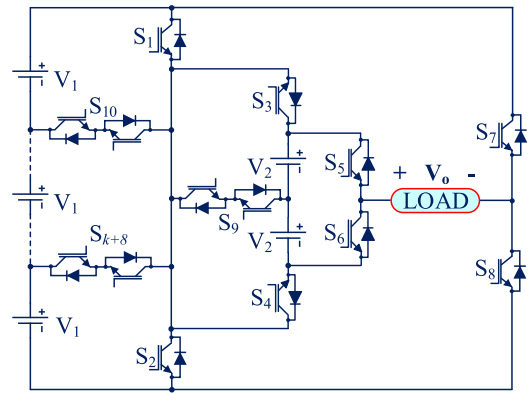


FIGURE 4. Extension I (E-I) of the proposed topology.

The proposed topology can be extended in two different ways as explained below.

1) EXTENSION WITH HIGHER NUMBER OF DC VOLTAGE SOURCES WITH MAGNITUDE V₁

In this method, the number of dc voltage sources with magnitude V₁ are increased in the outer T-section as shown in Fig. 4. For achieving higher number of levels, the selection of dc voltage sources is according to asymmetrical configuration. For the maximum number of levels, with k number of dc voltage sources of V₁ = V_{dc}, the magnitude magnitude of V₂ is selected as:

$$V_2 = (2k + 1) V_{dc} \tag{5}$$

The peak output voltage is given as

$$V_{o,max} = kV_1 + 2V_2 = kV_{dc} + 2(2k + 1) V_{dc} = (5k + 2)V_{dc} \tag{6}$$

The expression for number of switch requirement, gate driver, number of dc supply as a function of output voltage level is given by (7).

$$\left. \begin{aligned} N_{sw} &= 2k + 8 \\ N_{gd} &= k + 8 \\ N_{dc} &= k + 2 \\ N_l &= 10k + 5 \end{aligned} \right\} \tag{7}$$

The TSV for the proposed extension can be divided into two parts as:

$$TSV_{E-I} = TSV_T + TSV_{V_2} \tag{8}$$

where TSV_T is the TSV for the T-section of the proposed extension which is given as:

$$TSV_T = (4k + M)V_1 \tag{9}$$

where,

$$M = \begin{cases} \frac{3k^2 + 2k - 1}{4} & \text{for odd number of } k \\ \frac{3k^2 + 2k}{4} & \text{for even number of } k \end{cases}$$

TSV_{V₂} is the TSV of the topology with dc voltage sources of magnitude V₂ and is given by Eq. (4) which is:

$$TSV_{V_2} = 10V_2 \tag{10}$$

Therefore, from (8)-(10),

$$TSV_{E-I} = (4k + M)V_1 + 10V_2 \tag{11}$$

2) EXTENSION WITH HIGHER NUMBER OF DC VOLTAGE SOURCES WITH MAGNITUDE V₂

One main issue with the extension 1 (Ext-II) has been the magnitude of dc voltage source V₂ as its magnitude is dependent on k as given in Eq. (5). This problem can be solved by increasing the number of voltage source with magnitude V₂. Fig. 5 shows the Ext. II of the proposed topology. For a higher number of levels with asymmetrical configuration, the magnitude of dc voltages are selected as V₁ = V_{dc}, and V₂ = 5V_{dc}.

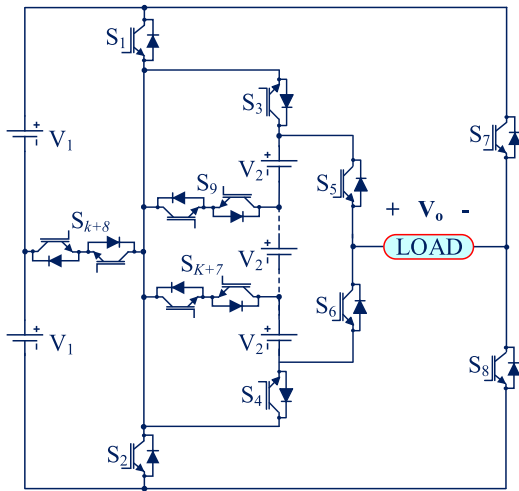


FIGURE 5. Extension II (E-II) of the proposed topology.

The different equations for the Ext. II remains the same as Ext. I as given in (7). The equation for TSV modifies as:

$$TSV_{E-II} = 10V_1 + (4k + M)V_2 \tag{12}$$

III. COMPARATIVE STUDY

In this section, a detailed comparative study is provided for the proposed topologies. The topology with three dc voltage source, four dc voltage source, and generalized structure have been compared separately with similar topologies. The proposed topologies with three and four dc voltage sources have been compared in terms of number of switches, number of gate driver circuit required, number of levels generated, number of diodes, TSV, and maximum blocking voltage (MBV) of any individual switch. The generalized structure has been compared in terms of number of switches, number of gate driver circuit, number of dc voltage sources and TSV against the number of levels at the output.

A. COMPARISON OF PROPOSED 3S-15L TOPOLOGY

The quantitative comparison among the topologies is given in Table 3. From the table, it is shown that the proposed MLI generates higher voltage levels compared to [13], [19], and [24] and have the same capability of voltage level generation as of [28]. However, proposed topology uses lesser gate driver circuits and have lower TSV and MBV than [28] which lower the cost of the MLI.

TABLE 3. Quantitative comparison of the proposed 3S-15L topology.

Topology	N _i	N _{sw}	N _{gd}	N _d	TSV	MBV
[13]	7	8	7	0	18	3
[19]	11	8	7	0	22	4
[24]	9	7	7	4	17	2
[28]	15	10	10	0	42	7
Proposed	15	10	9	0	34	6

TABLE 4. Quantitative comparison of the proposed 4S-25L topology.

Topology	N _i	N _{sw}	N _{gd}	N _d	MBV	TSV
[15]	13	10	8	0	8	32
[16]	17	12	10	0	8	48
[25]	17	12	10	0	8	40
[27]	17	10	8	0	8	40
[28]	25	10	10	8	10	78
Proposed	25	12	10	0	10	60

B. COMPARISON OF PROPOSED 4S-25L TOPOLOGY

In this comparison, similar topologies have been considered which have four dc voltage sources and configure in a symmetrical configuration. Table 4 gives a quantitative comparison of the proposed topology with other topologies. From the table, it can be deduced that the topologies presented in [15], [16], [27], and [25] generates fewer voltage levels compared to the proposed topology. In addition, the proposed topology utilizes a lesser number of gate driver circuits without any diodes compared to [28] which decreases the system cost and improves the conversion efficiency.

C. COMPARISON OF THE PROPOSED GENERALIZED STRUCTURE WITH OTHER TOPOLOGIES

Fig. 6 (a) shows the variation of number of power semiconductor switches required against the number of levels at the output. From Fig. 6 (a) it is shown that the proposed MLI generates higher voltage levels compared to all other topologies with number of levels more than 15. Furthermore, the proposed inverter utilized less number of driver circuits than all other topologies when voltage level are greater than 40 as shown in Fig. 6 (b). Moreover, with number of levels more than 22, only [29] requires less number of driver circuit compare to proposed topology. In addition, the variation of the number of dc voltage sources against the number of levels is illustrated in Fig. 6 (c). The proposed inverter utilized a

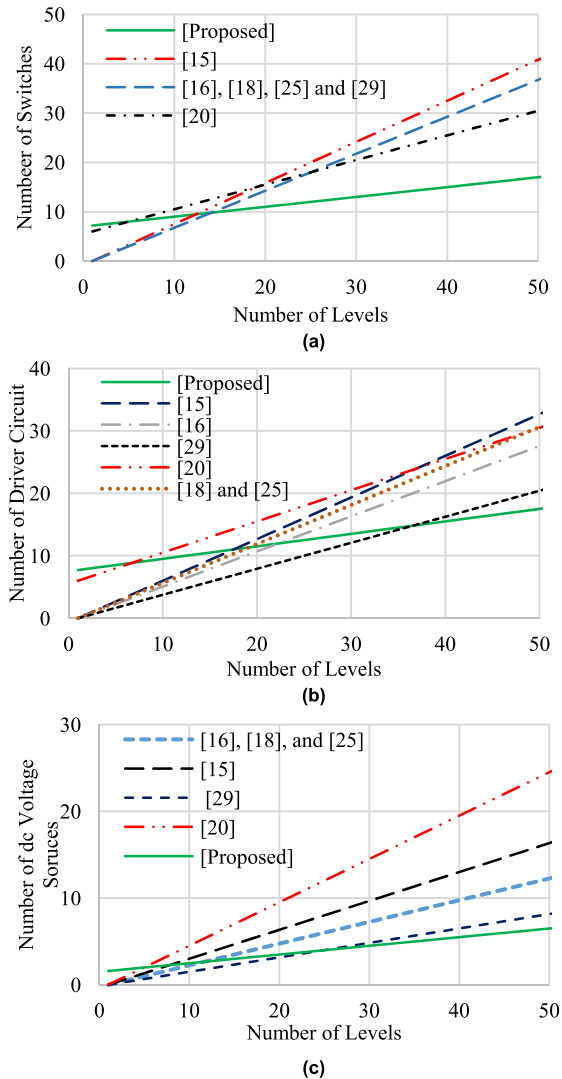


FIGURE 6. Variation of (a) number of switches, (b) number of gate driver circuit and (c) number of dc voltage sources with respect to number of levels.

lesser number of voltage sources than all other topologies when number of levels are higher than 28. The lower number of switches, driver circuit and dc voltage sources shows the superiority of the proposed topology with other topologies used for the comparison.

IV. RESULTS AND DISCUSSION

To verify the performance of the proposed topology, a laboratory prototype has been developed for the experimental results. In the experimental setup, TOSHIBA IGBT GT50J325 is used as a power switch. For the gate pulse generation of different switches, dSPACE 1104 controller is used. The modulation techniques are divided into two categories i.e. fundamental switching frequency techniques and high switching frequency techniques. The nearest level control (NLC) and selective harmonic elimination pulse width modulation (SHEPWM) are examples of fundamental switching frequency techniques. The sinusoidal pulse width modulation (SPWM) and space vector modulation are the

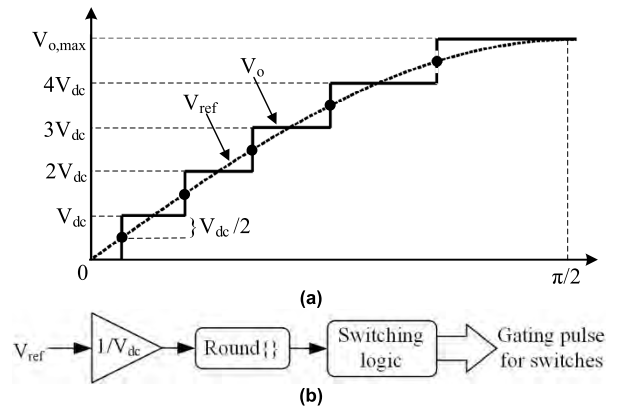


FIGURE 7. (a) Sampled reference voltage with NLC and (b) Implementation of NLC.

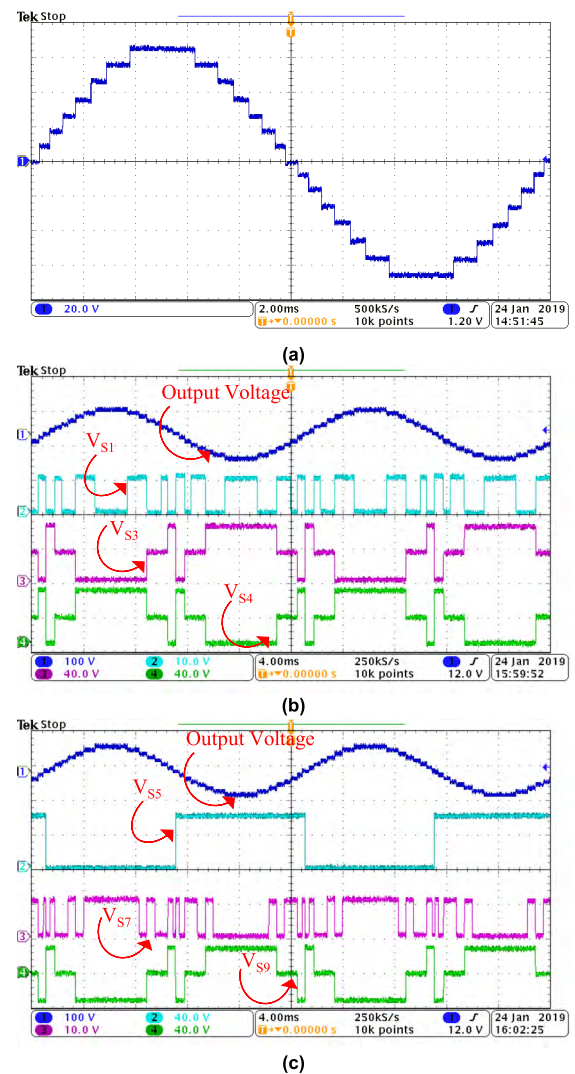


FIGURE 8. Experimental results for (a) 15 level output voltage, (b) voltage stress across switches S_1 , S_3 , S_4 , and (c) voltage stress across switches S_5 , S_7 , and S_9 .

examples of high switching frequency technique. The fundamental switching frequency techniques are more preferable than high switching frequency techniques due to its ability of achieving higher energy conversion with less system cost.

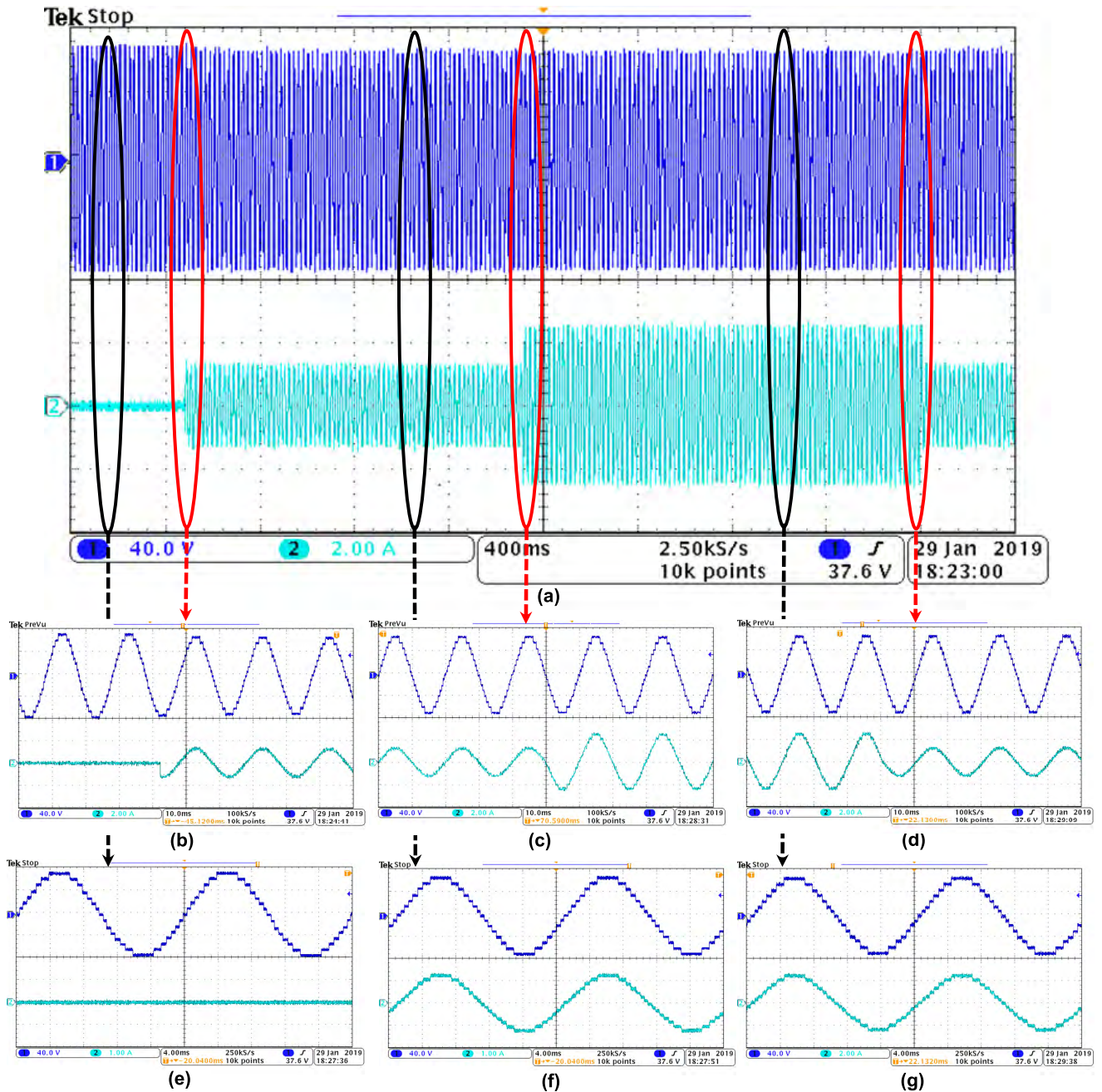


FIGURE 9. Experimental results for 15 levels output (a) output voltage and current waveform with different resistive load [scale: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$], (b) transient-state waveforms with change of load from $R=0$ to $R=60\ \Omega$, [scale: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$], (c) transient-state waveforms with change of load from $R=60\ \Omega$ to $R=30\ \Omega$, [scale: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$], (d) transient-state waveforms with change of load from $R=30\ \Omega$ to $R=60\ \Omega$, [scale: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$], (e) steady-state waveform with $R=0\ \Omega$ [scale: $v_o = 40\text{V/div}$, $i_o = 1\text{A/div}$], (f) steady-state waveform with $R=60\ \Omega$ [scale: $v_o = 40\text{V/div}$, $i_o = 1\text{A/div}$], (g) steady-state waveform with $R=30\ \Omega$ [scale: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$].

Among fundamental switching frequency techniques, the NLC is normally used due to its easy control and implementation when working on high level inverter.

In this paper, fundamental frequency modulation techniques based nearest level control (NLC) is used for the generation of gate pulse. With NLC, the sampled waveform is generated by comparing the reference signal with the existing voltage level as shown in Fig. 7 (a). Fig. 7 (b) shows the general control diagram for the NLC.

In this paper, the hardware results for the proposed topology with 3S-15L and 4S-25L configuration have been presented.

A. EXPERIMENTAL RESULTS FOR PROPOSED 4S-15L TOPOLOGY

As shown in Fig. 8, the proposed topology with three dc voltage sources generates 15 levels at the output having in Fig. 8 (a). Moreover, the voltage stress across different

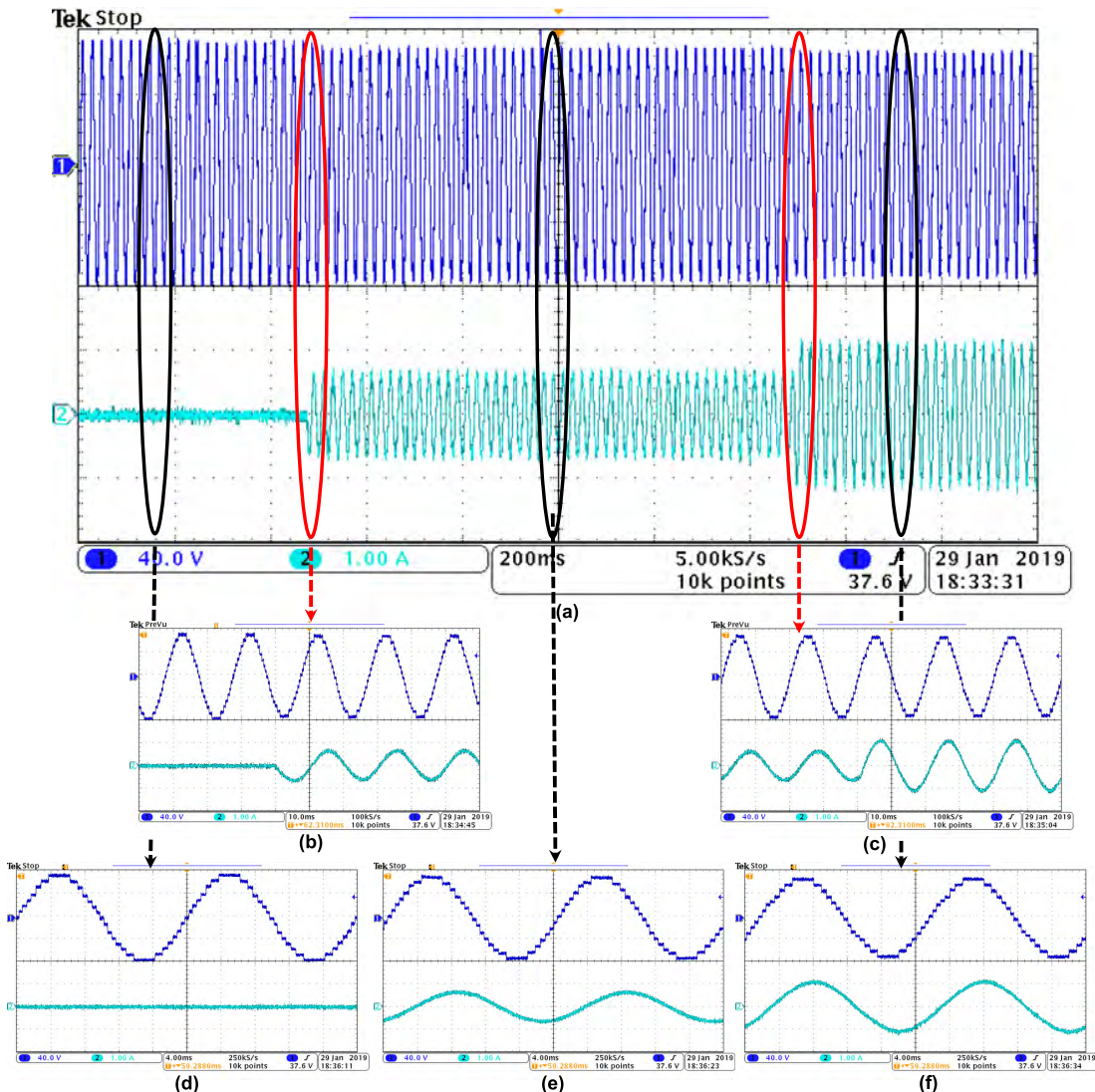


FIGURE 10. Experimental results for 15 levels output (a) output voltage and current waveform with different resistive-inductive load, (b) transient-state waveforms with change of load from $Z=0$ to $Z=60 \Omega + 100 \text{ mH}$, (c) transient-state waveforms with change of load from $Z=60 \Omega + 100 \text{ mH}$ to $Z=60 \Omega + 50 \text{ mH}$, (d) steady-state waveform with $Z=0 \Omega$, (e) steady-state waveform with $Z=60 \Omega + 100 \text{ mH}$, and (f) steady-state waveform with $Z=60 \Omega + 50 \text{ mH}$. [Scales: $v_o = 40\text{V/div}$, $i_o = 1\text{A/div}$].

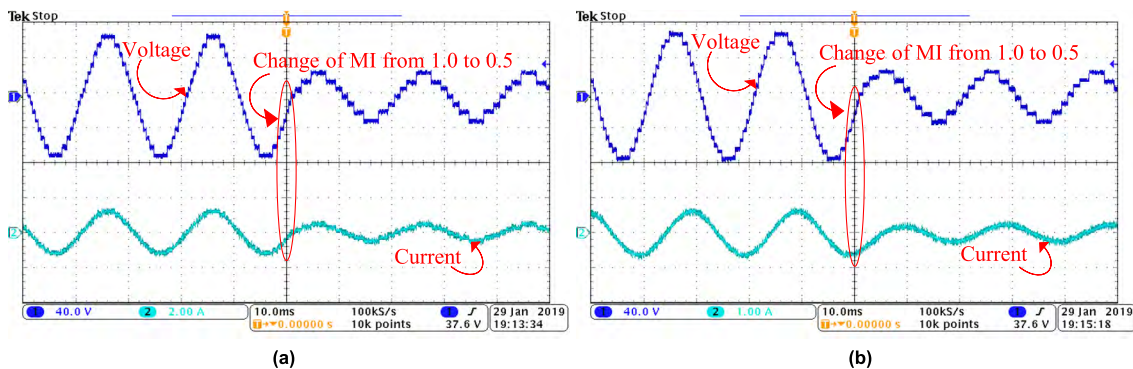


FIGURE 11. Output voltage and current waveform with change of modulation index from 1.0 to 0.5 with (a) $R = 100 \Omega$ [Scales: $v_o = 40\text{V/div}$, $i_o = 2\text{A/div}$], and (b) $R=100 \Omega, L=100\text{mH}$, [Scales: $v_o = 40\text{V/div}$, $i_o = 1\text{A/div}$].

switches are also shown in Fig. 8 (b) and (c). All these voltage stresses are in consistency with equation (2) and (3).

Furthermore, the proposed topology is tested with different types of loading conditions. Fig. 9 (a) shows the dynamic

response of the proposed topology with change in the magnitude of resistive load. Figs. 9 (b) - (d) gives the transient response i.e., showing the change of current as the load magnitude is changed. Furthermore, Fig. 9 (e) - (g) depicts

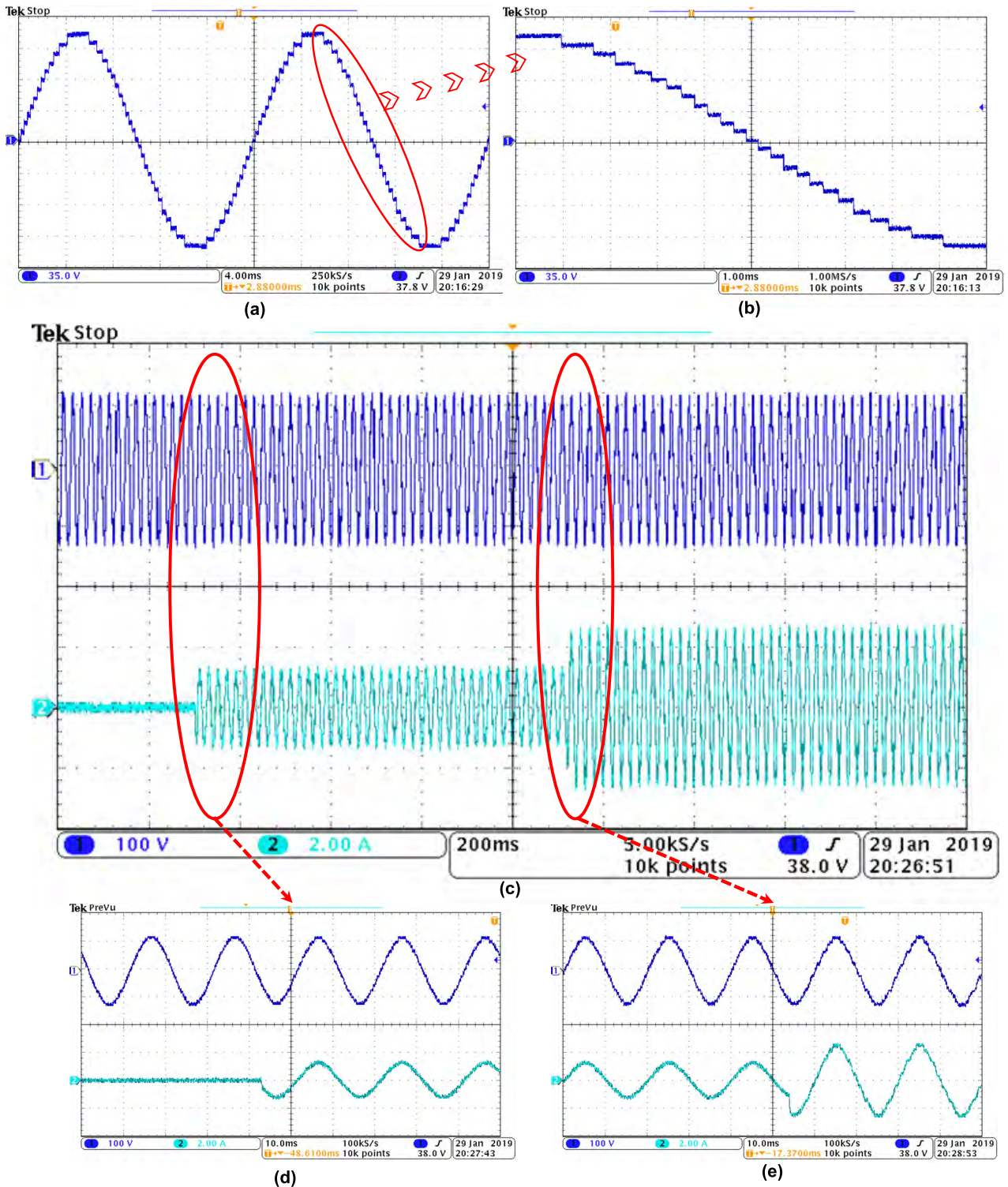


FIGURE 12. Experimental results for (a) 25 level output voltage waveform, (b) zoomed view of output voltage, (c) output voltage and current waveform with different resistive load [scale: $v_o = 100V/div$, $i_o = 2A/div$], (d) transient-state waveforms with change of load from $R=0$ to $R=100 \Omega$, [scale: $v_o = 100V/div$, $i_o = 2A/div$], (e) transient-state waveforms with change of load from $R=100 \Omega$ to $R=50 \Omega$, [scale: $v_o = 40V/div$, $i_o = 2A/div$].

the steady-state response with the resistive load. A similar test has been conducted with series connected the resistive-inductive load. Fig. 10 (a) – (f) shows the different transient and steady-state response for RL load.

A change of modulation index has also been considered while validating the performance of the proposed topology. Fig. 11 (a) illustrate the output voltage and current waveform with a change of modulation indexes from 1.0 to 0.5 with a

resistive load of 100 Ω . With the change of modulation index from 1.0 to 0.5, the number of levels is reduced to seven from fifteen. The smooth change of current and voltage waveform is shown in Fig. 11 (a). Similarly, with a resistive-inductive load, the change of modulation index has been depicted in Fig. 11 (b) with the waveform of voltage and current.

B. HARDWARE RESULTS FOR PROPOSED 4S-25L TOPOLOGY

The proposed 25 level topology has also been tested under various test conditions. As shown in Fig. 3, the topology for 25 level output voltage requires four dc voltage sources. The magnitude of V_1 is set to 10V and the magnitude of V_2 is selected as 50V. This selection results in an output voltage with a peak magnitude of 120V. The 12 voltage levels have a step voltage magnitude of 10V. Fig. 12 (a) shows the 25 level output voltage and to get a clearer view of the output voltage levels, Fig. 12 (b) shows a zoomed view of the output voltage.

Similar to 15 level output voltage, the proposed 25 level output voltage has been tested with the dynamic load variation. Fig. 12 (c) – (e) display the change of resistive load with 25 level output voltage. The load magnitude has been changed from zero to 100 Ω and this variation has been shown in Fig. 12 (d). Similarly, Fig. 12 (e) shows the change of resistance from 100 Ω to 50 Ω . From all these hardware results for 15 and 25 levels, the proposed topologies give satisfactory results under different dynamically changing load conditions.

V. CONCLUSION

This paper presents a new assembly of multilevel inverter topology with consideration of reduced switch count. The proposed topology has been discussed in details with the basic unit with 3S-15L configuration generating 15 levels, and the extension of the proposed topology with 4S-25L configuration to achieves 25 levels. Two generalized structure of the proposed topology has also been proposed. A detailed comparative study has been carried out with the proposed topology and recently reported topologies with three and four dc voltage sources. Finally, several experimental results proves the suitability and workability of the proposed topology with different type of loading combinations considering the change of modulation indexes.

REFERENCES

- [1] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.
- [2] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.
- [3] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [4] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [5] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248–1282, Sep. 2017.
- [6] M. Vijeh, M. Rezaeizadeh, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, to be published.
- [7] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016.
- [8] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.
- [9] M. A. Hosseinzadeh, M. Sarbanzadeh, E. Sarbanzadeh, M. Rivera, E. Babaei, and J. Riveros, "New cascaded multilevel converters based on switched-diode six-level configuration," in *Proc. IEEE Southern Power Electron. Conf. (SPEC)*, Dec. 2017, pp. 1–6.
- [10] K. Boora and J. Kumar, "General topology for asymmetrical multilevel inverter with reduced number of switches," *IET Power Electron.*, vol. 10, no. 15, pp. 2034–2041, Dec. 2017.
- [11] Y. Ounejjar, K. Al-Haddad, and L.-A. Gregoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.
- [12] H. Vahedi, M. Sharifzadeh, and K. Al-Haddad, "Modified seven-level pack U-cell inverter for photovoltaic applications," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1508–1516, Sep. 2018.
- [13] H. Samsami, A. Taheri, and R. Samanbakhsh, "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures," *IET Power Electron.*, vol. 10, no. 11, pp. 1315–1323, Sep. 2017.
- [14] E. Villanueva, P. Correa, J. Rodríguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
- [15] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7148–7156, Nov. 2016.
- [16] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-Type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.
- [17] R. S. Alishah, S. H. Hosseini, E. Babaei, M. Sabahi, and A. Zare, "Extended high step-up structure for multilevel converter," *IET Power Electron.*, vol. 9, no. 9, pp. 1894–1902, Jul. 2016.
- [18] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "A new general multilevel converter topology based on cascaded connection of sub-multilevel units with reduced switching components, DC sources, and blocked voltage by switches," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7157–7164, Nov. 2016.
- [19] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.
- [20] M. Jayabalan, B. Jeevarathinam, and T. Sandrasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electron.*, vol. 10, no. 1, pp. 10–17, Jan. 2017.
- [21] M. Saeedian, J. Adabi, and S. M. Hosseini, "Cascaded multilevel inverter based on symmetric-asymmetric DC sources with reduced number of components," *IET Power Electron.*, vol. 10, no. 12, pp. 1468–1478, Oct. 2017.
- [22] S. P. Gautam, S. Gupta, and L. K. Sahu, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," *IET Power Electron.*, vol. 9, no. 4, pp. 698–709, Mar. 2016.
- [23] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and H. M. Suryawanshi, "Hybrid control technique-based three-phase cascaded multilevel inverter topology," *IEEE Access*, vol. 5, pp. 26912–26921, 2017.
- [24] C. I. Odeh, E. S. Obe, and O. Ojo, "Topology for cascaded multilevel inverter," *IET Power Electron.*, vol. 9, no. 5, pp. 921–929, 2016.
- [25] C. Dhanamjayulu and S. Meikandasivam, "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads," *IEEE Access*, vol. 6, pp. 738–746, 2017.
- [26] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4530–4538, Jun. 2017.
- [27] R. S. Alishah, S. H. Hosseini, E. Babaei, M. Sabahi, and A. Z. Gharehkhoushan, "Optimal design of new cascade multilevel converter topology based on series connection of extended sub-multilevel units," *IET Power Electron.*, vol. 9, no. 7, pp. 1341–1349, 2016.

- [28] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2072–2080, Mar. 2017.
- [29] G.-J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May 2005.
- [30] M. D. Siddique and A. Sarwar, "Performance analysis of carrier based PWM technique for three level diode clamped multilevel inverter with different reference signals," in *Proc. IEEE 7th Power India Int. Conf. (PIICON)*, Nov. 2016, pp. 1–6.
- [31] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent PWM techniques," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 28–36, Feb. 2016.
- [32] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.
- [33] M. A. Memon, S. Mekhilef, and M. Mubin, "Selective harmonic elimination in multilevel inverter using hybrid APSO algorithm," *IET Power Electron.*, vol. 11, no. 10, pp. 1673–1680, Aug. 2018.



tronics converters (dc/ac and dc/dc), multilevel inverter topologies, and their control.

MARIF DAULA SIDDIQUE (S'18) was born in Chhapra, India, in 1992. He received the B.Tech. and M.Tech. degrees in electrical engineering from Aligarh Muslim University (AMU), in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia.

His research interests include step-up power elec-



He has authored or coauthored more than 400 publications in international journals and conference proceedings. His current research interests include power converter topologies, control of power converters, renewable energy, and energy efficiency.

SAAD MEKHILEF (M'01–SM'12) received the B.Eng. degree in electrical engineering from the University of Setif, Setif, Algeria, in 1995, and the master's degree in engineering science and the Ph.D. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively, where he is currently a Professor and the Director of the Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering.

His research interests include step-up power elec-



NORAI SYAH MOHAMED SHAH received the B.Eng. degree from the University of Malaya, in 1999, the M.Eng. degree from Oita University, Japan, in 2003, and the Ph.D. degree from George Mason University, Fairfax, VA, USA, in 2014. She is currently a Senior Lecturer with the Department of Electrical Engineering, University of Malaya. Her current research interests include signal processing and renewable energy.



power electronic converters, solar photovoltaic systems, and metaheuristic algorithms.

ADIL SARWAR received the bachelor's and master's degrees in technology and the Ph.D. degree from Aligarh Muslim University, in 2006, 2008, and 2012, respectively. He is currently an Assistant Professor with the Department of Electrical Engineering, Aligarh Muslim University, India. He has authored or coauthored more than 25 research papers. He has coauthored a chapter in *Power Electronics Handbook*, Fourth Edition edited by M. H. Rashid. His research interests include



He has been a Lecturer with the Department of Electrical Engineering, AMU, since 1991, where he served as Full Professor, until 2016. From 2009 to 2016, he was a Lecturer and then an Assistant Professor with the Institute of Information and Communication Technology, University of Sindh, Jamshoro, Pakistan. He has published widely in international journals and conferences, and his research findings are related to power electronics and renewable energy sources. He has authored or coauthored more than 350 research papers, one book, and three chapters in two other books. He has supervised several large R&D projects. His principal area of research interest is modeling and simulation of power electronic converters, control of multiphase motor drives, and renewable energy sources. His research interests include multilevel inverters, power quality, and control strategies. He is a Fellow of IET, U.K., and IE, India. He was a recipient of the Outstanding Faculty Merit Award, from 2014 to 2015, and the Research Excellence Award at Qatar University, Doha, Qatar. He was a recipient of the Maulana Tufail Ahmad Gold Medal for standing first at B.Sc. Eng. Exams from AMU, in 1991. He has received best research papers award at IEEE ICIT-2013, IET-SEISCON-2013, and SIGMA 2018. He is currently an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATION and the IEEE ACCESS and the Editor-in-Chief of i'manager's *Journal of Electrical Engineering*.

ATIF IQBAL (M'09–SM'11) received the B.Sc. Engineering (Gold Medal) and M.Sc. Engineering degrees in power system and drives from Aligarh Muslim University (AMU), Aligarh, India, in 1991 and 1996, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2006.

He is currently an Associate Professor in electrical engineering with Qatar University and a former Full Professor in electrical engineering with AMU.

His research interests include step-up power elec-



From 2009 to 2016, he was a Lecturer and then an Assistant Professor with the Institute of Information and Communication Technology, University of Sindh, Jamshoro, Pakistan. His research interests include multilevel inverters, power quality, and control strategies.

MUDASIR AHMED MEMON received the B.E. degree in electronics engineering and the M.E. degree in electronic systems engineering from the Mehran University of Engineering and Technology, Jamshoro, Pakistan, in 2009 and 2015, respectively. He is currently pursuing the Ph.D. degree in power electronics with the University of Malaya, Malaysia.