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Enhanced Deadbeat Control Approach for Grid-Tied Multilevel Flying Capacitors Inverter

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ABSTRACT This paper proposes an enhanced Deadbeat Controller (DBC) for a grid-tied Flying Capacitors Inverter (FCI). The proposed DBC guarantees the balancing of the capacitors' voltages while injecting current to the grid with lower Total Harmonics Distortion (THD). The proposed controller has the following advantages: 1) Improved current tracking quality even at zero crossing instants by using a weighted state-space model, 2) Superior steady-state performance (lower current THD) compared to other prediction-based control techniques such as Finite-Control-Set Model Predictive Control, 3) The generated duty cycles are normalized to the common base when the desired state is out of reach within the sampling time, 4) Voltage Ride-Through (VRT) capability, and 5) Robustness to parameters variation. Theoretical analysis, simulation, and experimental results are presented to show the effectiveness of the proposed control technique in ensuring uninterruptible and smooth transfer of energy to the grid during normal/abnormal operating conditions (severe voltage sags, parameters variation, etc.).

INDEX TERMS Flying capacitors inverter, grid connection, normalized deadbeat control, voltage ride through.

I. INTRODUCTION

Solar and wind energy systems have been getting an increasing interest due to their benefits such as abundance, sustainability, cleaner electricity production, and consideration for many applications [1]–[3]. In grid-connected PV systems, the power conditioning stage combines all the power converters that connect the power supply to the grid. These converters are needed to deal with the variation of the output voltage of the storage elements (depending on the state of charge) and PV modules (according to the connected system). Particularly, the performance and reliability of the inverters used are important parameters that can intensely affect the energy production and economic profitability of PV systems. Thus, PV inverters are moving in the direction of Multilevel Inverter (MLI) topologies to further improve the power quality, reduce the weight of passive filter components, and eliminate bulky transformers [4]–[10]. Among the widely used MLIs, the Flying Capacitors Inverter (FCI) is considered as an interesting topology due to the following advantages: 1) A single DC-source MLI where the number of output voltage levels can be expanded by connecting more cells in series; 2) Provides an extended range of control actions and improves filter bandwidth taking advantage from the switching state redundancy. 3) Provides more drive-through functionality through storage capacitors [11]–[15]. Nevertheless, like other grid-connected inverters, it is subject to grid voltage fluctuations (sags and swells) which might affect the sensitive loads [16], [17]. In addition, voltage drops are often accompanied by bad transient performances (current overshoot, voltage distortion, transients, and low power factor). In the international grid code, grid-connected inverters must provide low voltage ride-through (LVRT) capability during grid failures (reactive power injection). Moreover, fault-tolerant control techniques are generally applied. For instance, a vector current regulator with feedforward of

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negative sequence grid voltage was proposed in [18], while dual vector current regulators were presented in [19], [20] to generate the reactive power needed to meet the VRT requirements. In [21], the authors proposed a compensation control technique for positive and negative sequences of reactive currents.

Recently, prediction-based control techniques and particularly the Deadbeat Control (DBC) strategies have attracted an increasing research interest. Commonly, the DBC makes use of the discretized system model to calculate the control actions needed to reach the reference state values within the sampling time [22]–[27]. Thus, the DBC has been always considered as the fastest and most accurate discrete-time control technique[28].

In this paper, an enhanced DBC technique with VRT capability is proposed to control a grid-tied FCI. This paper provides contributions in the following areas: 1) Apply a DBC strategy to tackle the multi-objective control problem (control of the capacitors' voltages and the injected grid current) of a grid-connected FCI (to the best of our knowledge, this control technique has not been applied so far to this topology in the scientific literature); 2) Make use of a weighting factor in the state space model to improve the current tracking quality at the zero crossing instants; 3) Propose a normalization of the duty cycles quantities to the common base when the desired state is out of reach within the sampling time; 4) Provide extra VRT capability; 5) Compare the results obtained by the proposed DBC strategy with those attained when another prediction-based control technique (Finite-Control-Set Model Predictive Control) is applied to the studied system.

II. PROPOSED SYSTEM

Fig. 1 shows an overview of the considered three-cell FCI. Each cell consists of a pair of switching elements separated by a floating capacitor. The cell switches should be always controlled in a complimentary way to avoid shorting the voltage sources. At the output terminals, the voltage levels are generated according to the desired values $E_1{}^*$ and $E_2{}^*$ of the capacitors' voltages and the control actions u_j ($j = 1, 2, 3$). The eight possible switching configurations ($U_i(t)$, $i = 1, \ldots 8$) are presented in Table 1. For a stable operation, a multi-objective control approach should be applied to regulate the capacitor voltages $E_1(t)$ and $E_2(t)$

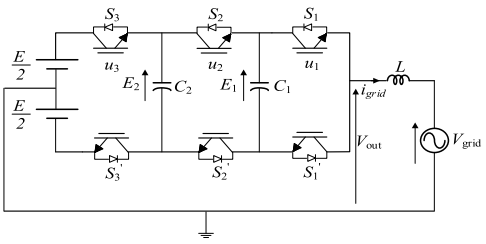

FIGURE 1. Circuit of the proposed 3-cell FCI.

TABLE 1. Possible switching states.

State	V_{out}	u_3	u_2	u_1
1	-E/2	0	0	0
2	-E/6	0	0	1
3	-E/6	0	1	0
4	E/6	0	1	1
5	-E/6	1	0	0
6	E/6	1	0	1
7	E/6	1	1	0
8	E/2	1	1	1

around their reference values while controlling the current $i_{grid}(t)$ injected to the grid. Obviously, traditional current regulators cannot satisfy these conditions and pre-charged circuits are conventionally employed with them to avoid the capacitors' voltages diverging. In the current study, the aim is to keep the voltages across the capacitors around their desired values of E/3 and 2E/3, respectively [22] and inject a line current with low THD and unity power factor (even under voltage dips).

A. MODELLING

By selecting the two capacitors' voltages and the injected grid current as the three state variables regrouped by $X(t) = [E_1(t)\, E_2(t)\, i_{grid}(t)]^T$ and the control actions (switching states) rearranged by the vector $U(t) = [u_3\ u_2\ u_1]^T$, the state-space representation could be computed by (1). For digital implementation purposes, the model presented in (1) should be discretised. Using the general forward Euler approximation in (2), the eight states (corresponding to the eight switching patterns $U_i(t)$, $i = 1, \ldots, 8$) can be derived at each sampling time by (3).

$$\dot{X}(t) = \begin{pmatrix} 0 & 0 & \frac{u_2 - u_1}{C_1} \\ 0 & 0 & \frac{u_3 - u_2}{C_2} \\ \frac{u_1 - u_2}{L} & \frac{u_2 - u_3}{L} & 0 \end{pmatrix} X(t) + \begin{pmatrix} 0 \\ 0 \\ \frac{E}{L}u_3 - \frac{E}{2L} - \frac{V_{grid}}{L} \end{pmatrix} \quad (1)$$

$$\frac{df(t)}{dt} = \frac{f(k+1) - f(k)}{T_s} \quad (2)$$

$$X_i(k+1) = X(k) + \dot{X}_i(t).T_s \quad (3)$$

where T_s is the sampling time and k is the sample number. Let the duty cycles $d_j(t)$ be the average of the switching states $u_j(t)$ calculated within a sampling period. The averaged state space model of the source-converter-grid is therefore derived by (4), as shown at the bottom of the next page. With

the aim of validating the average model, the state vectors $X(k+1)$ calculated by (3) and (4) are compared within a sampling period. A Pulse Width Modulator (PWM) stage is employed to generate the different switching patterns from the continuous duty cycles d_j. Three switching profiles could be identified for the generated pulses and the evolutions of the state variables planned for these profiles are studied in simulation (Fig. 2) using the following duty cycles' ratios: $d_3 = 0.25$, $d_2 = 0.5$, and $d_1 = 0.75$. As it can be noticed, the centred pulses (Fig. 2 (c)) give more flexibility and freedom for the state variables within the sampling time. This is due to a higher number of computed switching patterns (higher switching frequency with redundant switching states) compared to those considered within the other profiles (7 switching patterns with the centred pulses against 4 using the right and left profiles). Therefore, one can conclude that the centred pulses guarantee the best accuracy of the average model.

Hereafter, the centered profile will be adopted as the optimum profile and will be used for the validation tests. Equation (4) could be redrafted by (5), as shown at the bottom of the page, where $D(k)$ is the input vector, C is a constant matrix, and $B(X(k))$ is a variable matrix. Then, the duty cycles are computed by (6):

$$D(k) = B^{-1}(X(k))\left(\frac{1}{T_s}(X_{ref}(k) - X(k)) - C\right) \tag{6}$$

As well known, merging two or more variables in a single control law is not a simple task particularly when they are of different units and magnitude orders.

In this study, for proper operation of the proposed system, the three state variables (the grid current and the two capacitors' voltages) should be simultaneously controlled with equal importance. One of the novelties of the presented DBC is to make use of a weighting factor λ in the state-space model to compensate for the dissimilarity of the controlled variables. This results in enhancing the quality of current tracking especially during the current zero crossing instants.

B. NORMALIZATION

Conventionally, the duty cycles d_j must satisfy $d_j \epsilon [01]$, $j = \{1, 2, 3\}$. This constraint might be not satisfied when the desired state could not be reached within the selected sampling time. Therefore, this paper proposes a duty cycle quantities normalization to the common base [0 1]. The main idea of the normalization is to absorb large difference in absolute values into base relationships. The suggested algorithm (Fig. 3) consists of a series of Min-Max calculations to guarantee the normalization of duty cycles within the common base. The two main tests are performed to check if the computed duty cycles are within the common base [0 1]. If one of the duty cycles is negative, the minimum value is used to calculate the new positive duty cycles. Then the maximum value is computed. If the latter is less than 1, then the normalized duty cycles are output to the modulation stage. Otherwise, the positive duty cycles are divided by the maximum value to guarantee having all duty cycles less than 1. For a set desired state, the evolutions of the state variables were compared with and without normalization. Fig. 4 shows that the deviation or error between the desired and the reachable states using the normalized duty cycles is satisfactory.

It is worth to note that this error is mainly affected by the maximum variations of the state variables (7). The proposed overall control strategy is described in Fig. 5.

$$\begin{aligned} \Delta E_{1,2max} &= \frac{2i_{grid}}{C_{1,2}} T_s \\ \Delta i_{gridmax} &= \frac{E - 2V_{grid}}{L} T_s \end{aligned} \tag{7}$$

III. SIMULATION RESULTS

To validate the proposed controller, the Matlab/ Simulink software tool was used. For comparison purposes, a Finite-Control-Set Model Predictive Control (FCS-MPC) was also implemented to control the capacitors' voltage as well as the injected grid current of the studied FCI. The switching configuration that gives the minimum of the cost function J_i given by (8) is selected and then applied at the next

$$X_i(k+1) = X(k) + \left(\begin{pmatrix} 0 & 0 & \frac{d_2 - d_1}{C_1} \\ 0 & 0 & \frac{d_3 - d_2}{C_2} \\ \frac{d_1 - d_2}{L} & \frac{d_2 - d_3}{L} & 0 \end{pmatrix} X_i(t) + \begin{pmatrix} 0 \\ 0 \\ \frac{E}{L}d_3 - \frac{E}{2L} - \frac{V_{grid}}{L} \end{pmatrix} \right) .T_s \tag{4}$$

$$X_i(k+1) = X(k) + \left(\underbrace{\begin{pmatrix} -\lambda\frac{i_{grid}}{C_1} & \lambda\frac{i_{grid}}{C_1} & 0 \\ 0 & -\lambda\frac{i_{grid}}{C_2} & \lambda\frac{i_{grid}}{C_2} \\ \frac{E_1}{L} & \frac{E_2 - E_1}{L} & \frac{E - E_2}{L} \end{pmatrix}}_{B(X(k))} \underbrace{\begin{pmatrix} d_1 \\ d_2 \\ d_3 \end{pmatrix}}_{D(k)} + \underbrace{\begin{pmatrix} 0 \\ 0 \\ -\frac{E}{2L} - \frac{V_{grid}}{L} \end{pmatrix}}_{C(k)} \right) .T_s \tag{5}$$

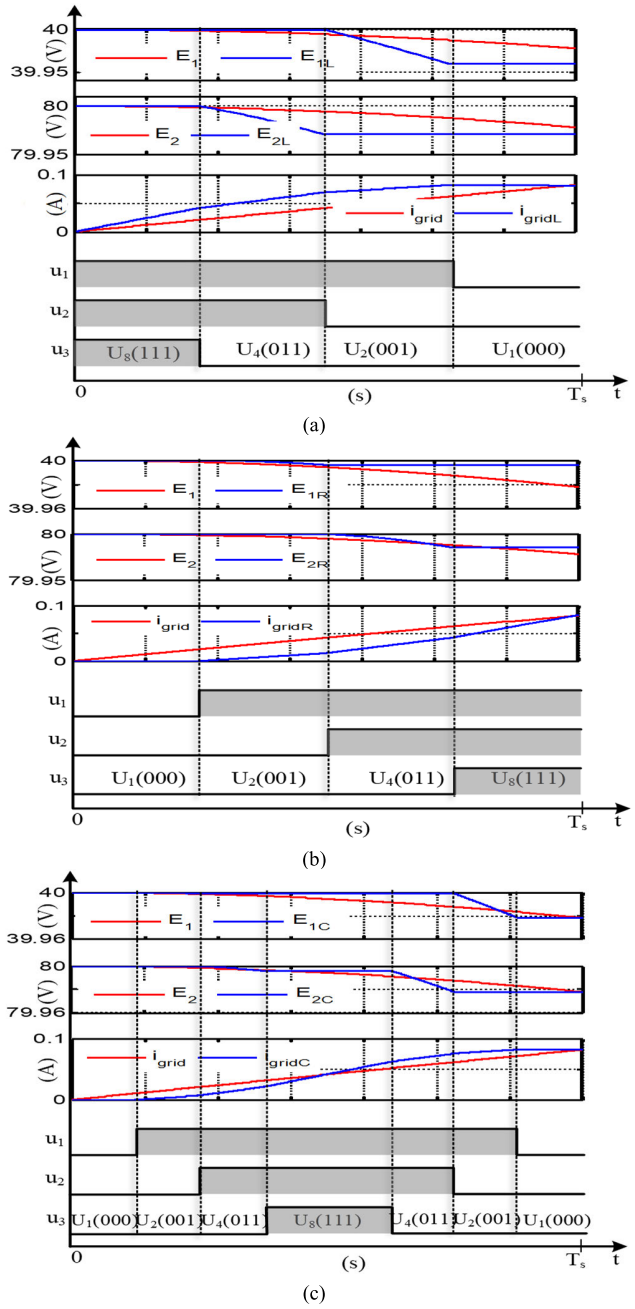

FIGURE 2. Evolution of the different state variables within a sampling period for different switching profiles; (a) Left switching profile (b) Right switching profile (c) Centered switching profile.

sampling period.

$$J_i^2 = \left(\frac{E_1^* - E_{1i}\,(k+1)}{\Delta E_1\,(k+1)}\right)^2 + \left(\frac{E_2^* - E_{2i}\,(k+1)}{\Delta E_2\,(k+1)}\right)^2 + \left(\frac{i_{grid}^* - i_{gridi}\,(k+1)}{\lambda.\Delta i_{grid}\,(k+1)}\right)^2 \tag{8}$$

Many scenarios were tested to compare the tracking quality (current THD) and explore the VRT capability (voltage sags). The considered system parameters are shown in Table 2.

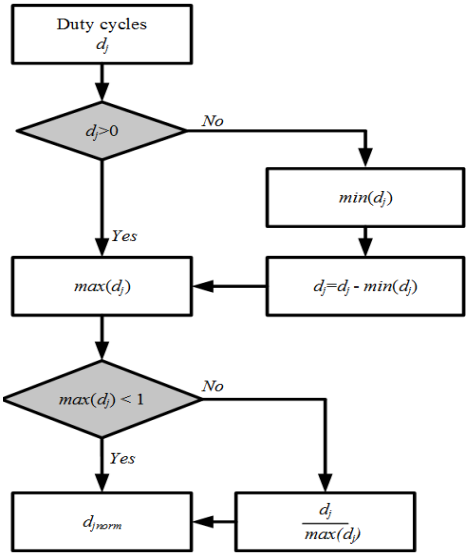

FIGURE 3. Algorithm of the duty cycles normalization to the common base when the desired state is out of reach during the sampling time.

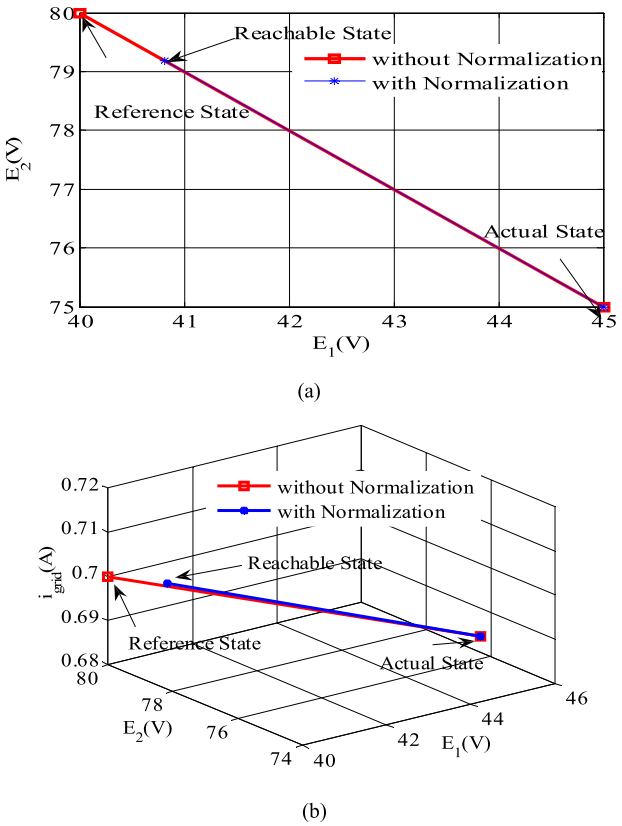

FIGURE 4. Evolutions of the state variables with and without normalization; (a) Capacitors voltage evolution (b) 3D state variables evolution.

The minimization of the grid current THD has been given the highest priority (for higher performance and stable operation) in the tuning process the weighting factor. Fig. 6 depicts the grid current THD variation as a function of the weighting

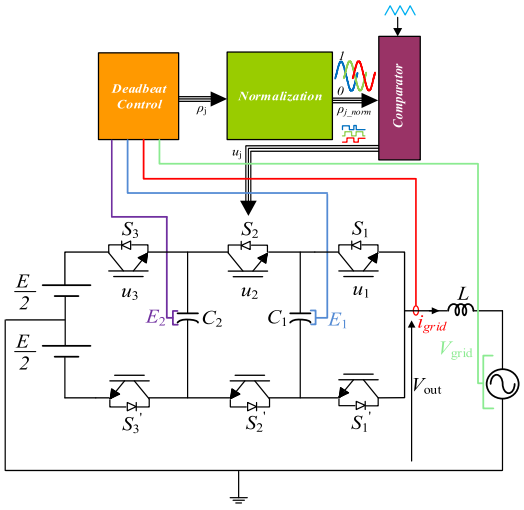

FIGURE 5. Proposed DBC strategy for the grid-tied 3-cell 4-level FCI.

TABLE 2. Simulation parameters.

Parameters	Values
DC-link voltage E	120 V
Sampling frequency f_s	14 kHz
Grid Voltage V_{grid}	50 V
Peak current i_{grid}	0.7 A
Capacitor C_1	100 µF
Capacitor C_2	100 µF
Inductor L	10 mH

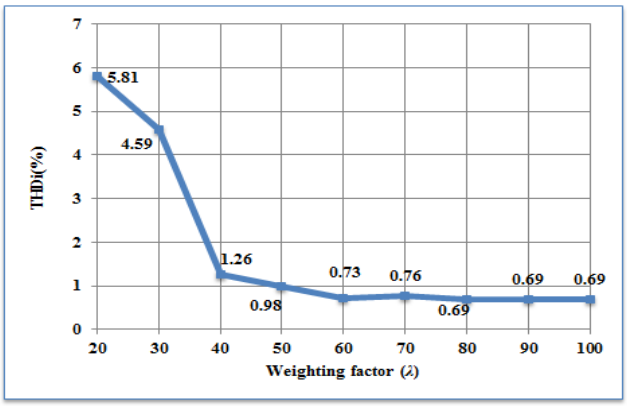

FIGURE 6. Grid current THD versus weighting factor λ.

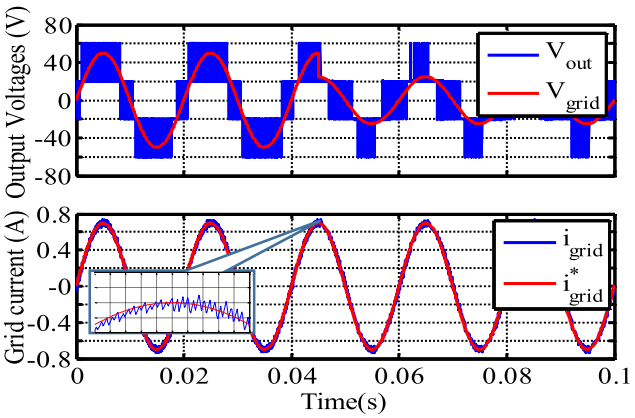

FIGURE 7. Transient performance of the proposed DBC during grid voltage sag (voltage sag occurs at t = 0.045s), Upper: Output and grid voltage waveforms, Lower: Injected grid current.

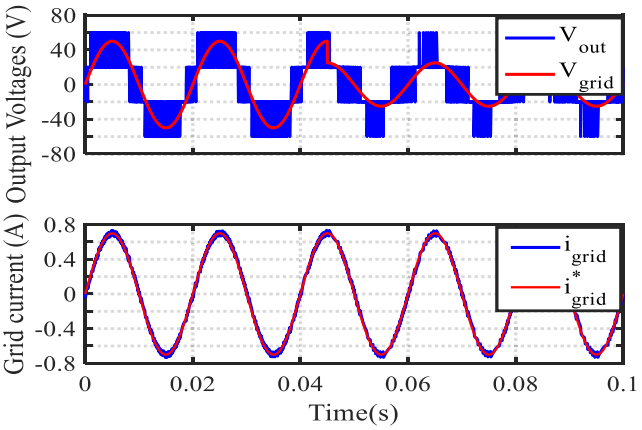

FIGURE 8. Transient performance of the MPC during grid voltage sag (voltage sag occurs at t = 0.045s), Upper: Output and grid voltage waveforms, Lower: Injected grid current.

factor λ. It is noted that the minimum THD of 0.69% is obtained for $\lambda \geq 80$. Hence, $\lambda = 80$ is selected as the optimum weighting factor. The upper part of Fig. 7 depicts the grid and the inverter 4-level output voltages. Note that at $t = 0.045$s, a 50% peak sag of the grid voltage is introduced. At this instant, the depicted zoom of the grid current (lower part) shows the high dynamic performance of the grid current confirming the very good VRT capability of the proposed controller. Similar results have been depicted by Fig. 8 where the FCS-MPC algorithm was applied.

Fig. 9 illustrates the weighting factor effect on the quality of the grid current tracking. Notice that for $\lambda = 30$, a clear current distortion appears around the zero crossing instants. Despite its stable operation, the inverter may overheat in a long run. Therefore, it is important to improve the tracking quality of the grid current by selecting the optimum value of the weighting factor ($\lambda = 80$), which minimizes the harmonic content as shown in Fig. 10. To further highlight the performance of the proposed DBC strategy, another test was performed by applying a tuned FCS-MPC algorithm to the studied FCI system. Fig. 11 shows the corresponding current THD of 3.44% which is very high compared to the THD obtained using the proposed DBC strategy (THD = 0.69%). Fig. 12 shows the Capacitors' voltages waveforms during transient and steady-state. Unlike standard current controllers, the proposed DBC ensures self-charging of the capacitors. According to this figure, the capacitors' voltages are well balanced around their reference values

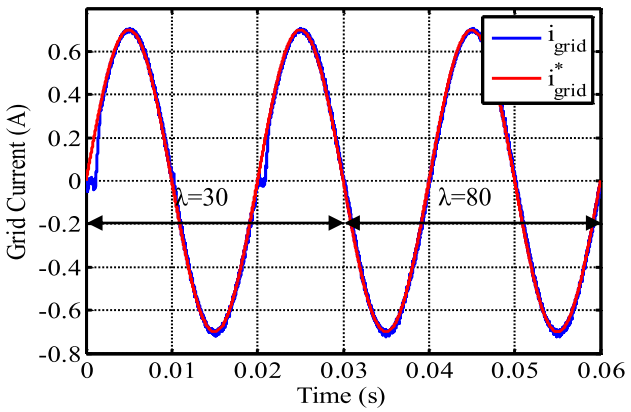

FIGURE 9. Tuning effect of the weighting factor on the injected grid current.

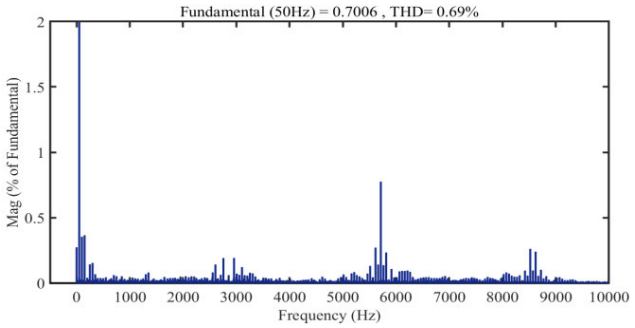

FIGURE 10. Harmonics content of the grid current using the proposed DBC ($\lambda = 80$).

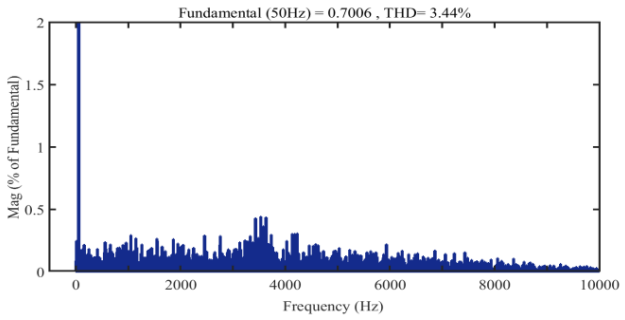

FIGURE 11. Harmonics content of the grid current using MPC.

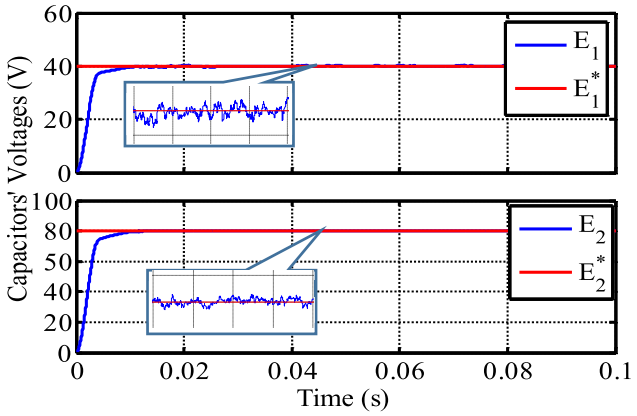

FIGURE 12. Capacitors' voltages waveforms (voltage sag occurs at t = 0.045s) with $\lambda = 80$.

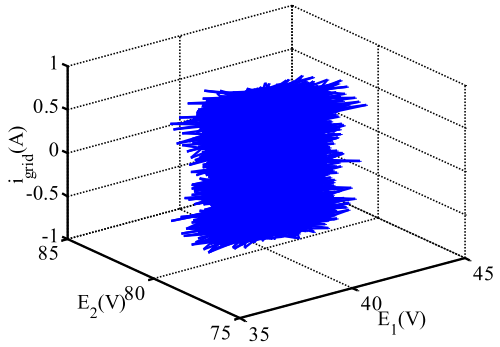

FIGURE 13. Closed-loop behavior of the system in the 3D state-plane.

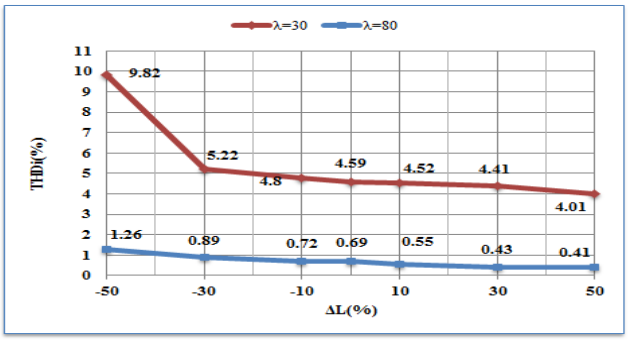

FIGURE 14. Grid current THD versus filtering inductor variation (ΔL) for λ equal 30 and 80.

($E/3$ and $2E/3$) with less than 1% voltage ripples. The closed-loop behavior of the system in the three-dimensional state-plane (Fig. 13) provides a better insight into the proposed DBC's dynamic performance and convergence.

Moreover, the robustness of the proposed DBC approach to the parameters variations is studied by varying separately the parameters (L and C_1) in the control algorithm (±50% of their rated values). The THD of the grid current and the average error in the capacitor voltage V_1 are chosen as performance indicators. Fig. 14 illustrates the effect of the inductor error, ΔL, on the current THD for two values of tuning factor. It is clear that the grid current THD is not much affected by the L variation for the tuned case ($\lambda = 80$). Fig. 15 shows the little deviation of the capacitor voltage error when C_1 is varied ($\lambda = 80$). These results show the robustness of the proposed DBC to parameters variations.

IV. EXPERIMENTAL RESULTS

A scaled 500 W (power rating available in the laboratory) experimental prototype was used to validate the proposed DBC (Fig. 16), where a step-up transformer was deployed to connect to the grid. The experimental parameters are given in Table 2.

To explore the effect of the weighting factor on the tracking quality of the state variables, tests were made using two

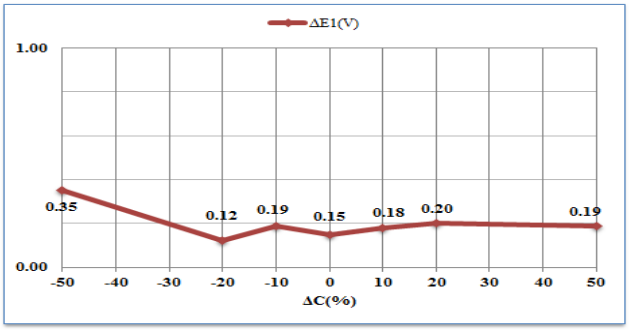

FIGURE 15. Sensitivity of the proposed DBC to the capacitor C_1 variation.

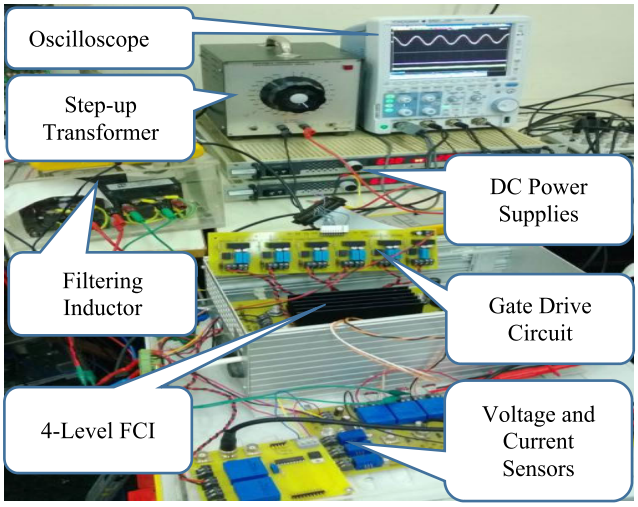

FIGURE 16. Scaled prototype of the grid-connected 3-cell 4-level FCI.

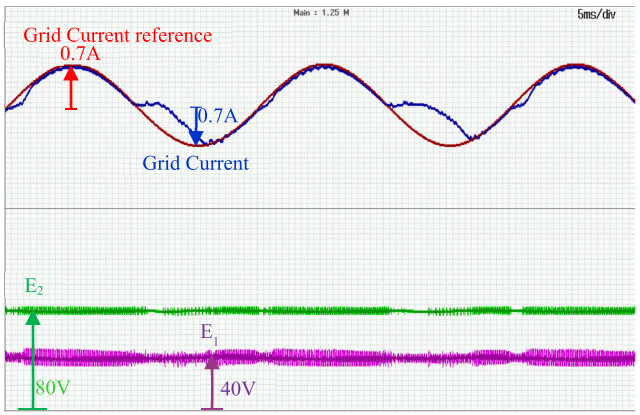

FIGURE 17. Effect of the untuned weighting factor ($\lambda = 30$) on the performance of the DBC. Upper reference and actual grid current (distortion at zero crossing instants); bottom capacitors' voltages.

different values. Notice that for $\lambda = 30$ (Fig. 17), a clear current distortion appears around the zero crossing instants. Despite its stable operation, the inverter may overheat in a long run. Therefore, it is important to improve the tracking quality of the grid current by selecting the optimum value of the weighting factor ($\lambda = 80$) as illustrated in Fig. 18. As it can be noticed that the tracking of the capacitors' voltages is robust to the variation of λ.

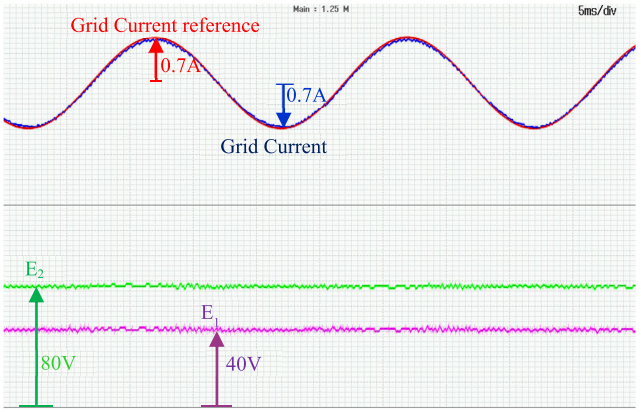

FIGURE 18. Effect of the optimum weighting factor ($\lambda = 80$) on the performance of the DBC. Upper reference and actual grid current (improved tracking quality); bottom capacitors' voltages.

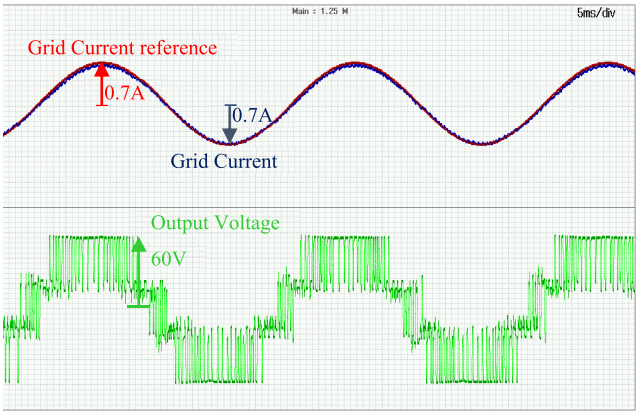

FIGURE 19. Experimental results; upper: grid reference and actual currents; lower: output voltage waveform.

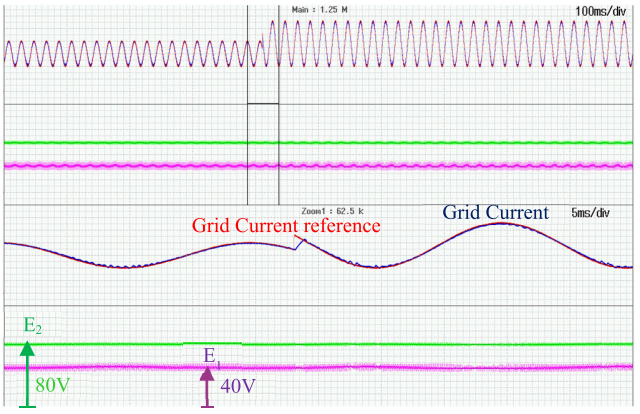

FIGURE 20. Transient performance of the DBC under a 100% reference current step change.

Fig. 18-Fig. 19 show the steady-state performance of the proposed DBC for the tuned scenario. Notice that the grid current and the capacitors' voltages are following accurately their references while the four levels of the output voltage are easily distinct.

Fig. 20 and Fig. 21 show the dynamic performances of the proposed DBC and FCS-MPC respectively, where a 100%

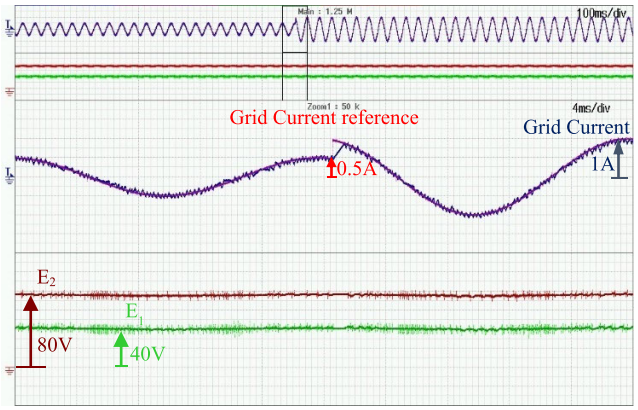

FIGURE 21. Transient performance of the FCS-MPC under a 100% reference current step change.

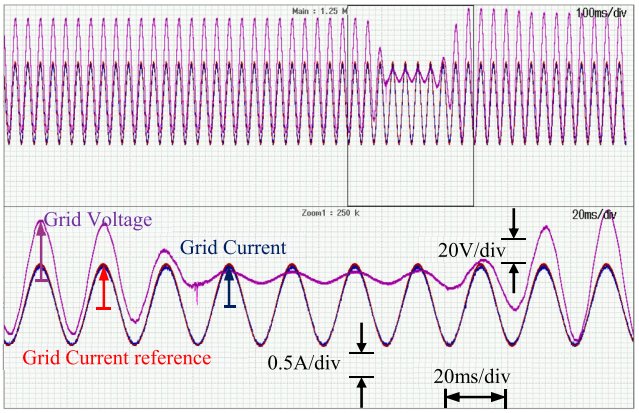

FIGURE 22. VRT performance of the DBC under 85% grid voltage sag.

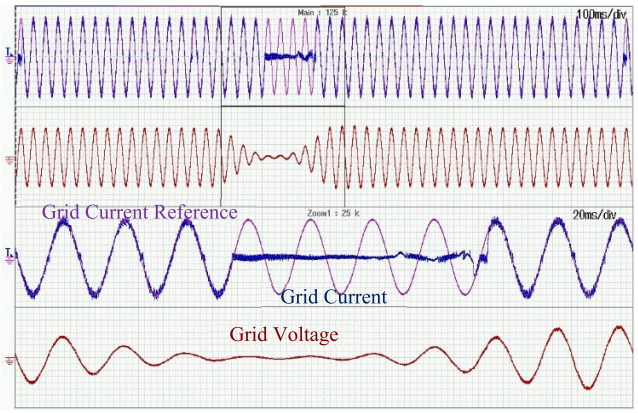

FIGURE 23. VRT performance of the FCS-MPC under 85% grid voltage sag.

step increase on the grid current reference was applied. One can notice that the measured currents are re-tracking rapidly (after 1ms) their references. However, the DBC case is obviously showing less distortions on the grid current tracking.

In order to test the VRT capability feature of the proposed controller, a grid voltage sag of 85% peak was led for few cycles. Fig. 22 shows a good grid current tracking (without peak current overshoot and phase shift) during the voltage sag using the proposed DBC strategy. From another side, when the weighting factor is not carefully selected, the reference grid current tracking might be lost during the voltage sag cycles when the FCS-MPC technique is applied as shown in Fig.23.

V. CONCLUSION

This paper proposed an enhanced DBC technique for a grid-tied Flying Capacitors Inverter (FCI). The proposed controller makes use of a weighting factor in the state space model to improve the current tracking quality at the zero crossing instants. Moreover, a normalization strategy of the duty cycles quantities to the common base was proposed when the desired state is out of reach within the sampling time. Digital simulation was performed on a 3-cell FCI. The presented results showed that the proposed DBC offers the possibility of controlling the grid current and the capacitors' voltages simultaneously with high dynamic performance. By selecting the optimized weighting coefficient value based on the minimization of the grid current THD, high performance (good tracking quality and fast transient response) and stable operation of the FCI were achieved. Moreover, the robustness of the proposed DBC approach to the parameters variations was proved. Finally, theoretical investigations and simulations were validated using a 500W experimental prototype. The presented results showed the high effectiveness of the proposed DBC in regulating the capacitors' voltages around their reference values while injecting a sinusoidal current to the grid with low THD and unity power factor even under severe voltage sags (VRT capability) and parameters variations.

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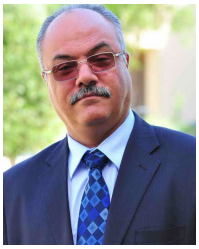

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