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# A Detailed Full-Order Discrete-Time Modeling and Stability Prediction of the Single-Phase Dual **Active Bridge DC-DC Converter**

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**ABSTRACT** The standard methodology to obtain the model of a power electronic converter is achieved by averaging the state-space dynamics of the converter's state variables. But the average of the transformer current is null over a switching cycle in the resonant dc-dc converter. Therefore, the conventional method is not suitable for resonant converters, including the phase-shifted bidirectional dual active bridge (PSBDAB) converter. The two-time scale discrete-type models can resolve the problem associated with the standard state-space averaging methodology. The time-scale segregates the dynamics of the PSBDAB converter into fast and slow state variables, which can be modeled separately and eases the analysis of the PSBDAB converter. The effect of the core-loss of the inductor, dead-time of the semiconductor devices, output filter capacitor's equivalent series resistance, semiconductor on-resistance, and the transformer copper loss components are included in the model to improve its steady-state and dynamics characteristics. Moreover, the stability analysis using a bifurcation diagram is carried out for the digitally controlled closed-loop of the system. Furthermore, the critical gain for the stable region with variations in the circuit parameters like load resistance, circuit equivalent inductance, and voltage demand is extensively studied. The modeling and stability analysis is validated in the simulation and experimental setup. The results verify that the proposed method accurately predicts the stable region with variations in the system circuit parameters. Thus this study provides a guide to select and tune the controller parameter to ensure the converter operates within the boundaries of the stable region.

**INDEX TERMS** Bidirectional converter, DC-DC converter, discrete-time model, dual active bridge, fullorder, modeling, phase-shift modulation, reduced-order, small-signal model, stability, time-scale model.

## I. INTRODUCTION

The phase-shifted bidirectional dual active bridge (PSBDAB) converter has been used extensively in various applications like a solid-state transformer (SST) [1], more-electric aircraft [2], automotive application [3], microgrid [4]. It is of utmost importance to properly analyze converter behavior and dynamic performance to get the best performance. A system's dynamics or behavior can be studied through detailed time-domain simulation (DTDS) software like MATLAB, PLECS, PSIM. However, the computation burden is much higher compared to its equivalent circuit model (ECM) [5]. Moreover, the converter's essential characteristics, like the critical gain of the closed-loop controller to ensure stability or the critical phase-shift between the bridge to ensure soft switching, can only be obtained by manually tuning the control parameters. This requires a lot of fine-tuning and becomes cumbersome when applied with

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varying circuit parameters. Therefore, there is necessary to obtain a simple but accurate model to study the system's behavior. Moreover, the model of the system assists in selecting and designing the semiconductor device, inductor, transformer, filter capacitor, and closed-loop controller. There are some modeling methodologies to obtain the ECM of the PSBDAB converter that is classified as continuous-time models and discrete-time models.

The simplest continuous-time model excluding input and output filter components from the system dynamics has two state variables. These two state variables (transformer current and output filter capacitor voltage) are used to study the nonlinear characteristics of the PSBDAB converter [2]. The average of the transformer current in a full cycle of the PSBDAB converter is zero [2]. Hence the PSBDAB converter can be modeled by ignoring the effect of the transformer current dynamics on the system behavior. The expression of the output voltage or output current (which is required for control) is obtained by studying the dynamics of rectified transformer current [1]. This kind of methodology where one of the state variables' dynamics is ignored is known as reduced-order modeling. The reduced-order-model of the PSBDAB can be classified as a continuous-time reduced-order model (CTROM) [6]-[11], Fourier series reduced-order-model (FSROM) [1], [12] and frequency domain reduced-order model (FDROM) [13]-[16]. Other methods use both state variables (full-order) to model and study the large and small-signal behavior of the system. These kinds of techniques to obtain the full-order model of the PSBDAB converter are known as a generalized average model (GAM) [17]–[22] and discrete-time model (DTM) [3], [23]-[27].

The CTROM of the PSBDAB converter is also known as average value modeling (AVM). Dependent current sources substitute the semiconductor devices of the converter. The expression of the dependent current source is the average value of the current flowing through the semiconductor devices over a time period of the converter. The AVM in [6] is obtained from the expression of the power by applying the conventional state-space averaging method [5], and then the output current is obtained for the ideal case. The exclusion of the system losses from the model reduced the overall efficacy of this model. The effect of all kinds of system losses except the core-loss of the inductor is considered in [7], [11] to improve the model accuracy. This method is extended to model a dual active half-bridge-converter in [8] by only considering the dynamics of the output voltage. The reduced-order modeling is also used to develop the model of a modular architecture of the PSBDAB converter [10], which helps to achieve the decoupled control strategies between the modules.

The behavior of the PSBDAB converter is identical to the synchronous machine model [1]. Therefore, its state variables can be expressed as the sum of the fundamental and higher-order switching frequency components. Since the primary and secondary voltages of the transformer are square waves or three-level pulse voltages, it can be expressed as a Fourier series [12], [28]. Likewise, the Fourier series expression can describe the transformer current, output power, and output voltage [12] of the system. The smallsignal model (SSM) and large-signal model (LSM) obtained through the FSROM is also a reduced-order type model due to the zero average of the transformer current or the inductor current.

The FDROM of the PSBDAB converter [13]–[16] is very identical to the FSROM [1], [12]. The difference between these two is that the current dynamics of the transformer current are not studied in the FDROM. The ripple in the transformer current and output voltage can be established in the FSROM. The output power of the PSBDAB converter is first computed using the infinite series sum followed by obtaining the expression of the output voltage. Similar to the CTROM [7], the equivalent SSM and LSM of the PSBDAB converter can be expressed through the dependent current source. The frequency-domain modeling in [14] is applied to model phase-shift, or duty cycle modulated control [29] of the PSBDAB converter. The same method has been applied to the three-phase PSBDAB converter [13]. A new frequency domain methodology based on the Floquet and Hill theory [30] is proposed to obtain the SSM and LSM of the PSBDAB converter [15]. The model in [15] also includes output and input filters in the system's model. In [16], the authors have analyzed the steady-state operation of a high-frequency PSBDAB converter whe0n the switching transition times cannot be neglected. It has been shown that expressions of power and the soft-switching range can be inaccurate if voltage transitions are considered instantaneous. This scenario is essential for the wide bandgap (WBG) devices that have low output capacitance.

The conventional continuous-time state-space based modeling of a power electronic converter system is based on the assumption that the DC part of its Fourier series dominates the behavior of the state variable. However, it is not true in the case of the resonant converter like the PSBDAB converter. Therefore, GAM includes the dc term, cosine term, and sine term of the Fourier series, which improves the dc-dc converter's modeling accuracy [17]. The averaging of the Fourier series is performed on the finite time duration of the state variables. The first literature to model a power electronic converter using GAM was proposed by Sanders at MIT [17]. The same methodology is then applied to the PSBDAB converter by Qin [18]. However, when the ESR of the input or output filter capacitor is added to the GAM, the number of state variables is increased from three to six. The accuracy of the GAM is compromised to simplify the model by disregarding cosine and sine components of the higher-order Fourier series term. The higher frequency Fourier series component of the switching frequency is added to GAM in [21] to improve the efficacy of the SSM and LSM. But the number of state variables is increased to nine. The performance of GAM is much better for the three-phase PSBDAB converter due to the absence of the odd multiples of the third harmonic switching frequency



FIGURE 1. Detailed diagram of the PSBDAB converter.

component in the Fourier series [9]. This helps to accurately predict the stable region of the three-phase PSBDAB dc-dc converter [22]. The efficacy of the single-phase PSBDAB converter can be improved by introducing a correcting factor that compensates for the error caused by the absence of the higher-order Fourier-series component [19]. The correcting factor uses the analytical solution of the power flow [28]. The accuracy can be further improved by introducing a second correcting factor to compensate for the system losses [20]. Moreover, the same methodology is applied to phase-shift, and advance modulation strategy [29]. GAM can also be used for the stability prediction of the three-phase PSBDAB converter [22]. However, GAM's accuracy is only good when two correction factors are introduced [20], or a high number of the state variable is included in the model [21].

The power electronic converter system modeling can be obtained through the discrete-time domain to predict the steady-state, and dynamic response of the pulse width modulated converters [31]. The discrete-time system can give the state variable's information at each sub-interval. The information of the transformer current at the switching time helps to study the zero voltage switching region of the PSBDAB converter [27]. The accuracy of the SSM obtained through DTM of a dc-dc converter is better than its continuous-time counterpart [32]. The DTM of a PSBDAB converter has been developed in [3], [23]–[27]. The modeling approach in [3], [24] does not explore the behavior of the systems at steadystate, open-loop, or the stability of the system. The bilinear DTM is used to predict the stability margin of a closed-loop system. However, bilinear DTM doesn't discuss the behavior of the converter's dynamics in the open-loop, which helps to integrate the battery with the PSBDAB converter [2]. The mixed system-based modeling of the PSBDAB converter is proposed in [27]. Although the modeling obtained in [27] discusses the LSM of the model unlike, [3], [23], [24], the system loss is neglected in the model. The mixed system model developed in [27] is lossless, which limits its accuracy at a higher frequency. Moreover, the absence of the transformer current dynamics limits its use in the stability analysis of the model. Therefore, a time-scale model considering the dead-time of the semiconductor devices, core-loss of the inductor, and other system non-linearity are included in



FIGURE 2. Operating waveform of a PSBDAB converter.

the proposed model to improve the LSM, SSM, and stability prediction PSBDAB converter.

The properties of the proposed two-time scale model for the PSBDAB converter and contributions of this paper are summarized as:

- The proposed two-time scale model (TTSM) incorporates output filter capacitor ESR. The model obtained from the time-scale model results in a full-order DTM. The inclusion of the filter ESR improves the stability prediction of the system.
- 2) The proposed TTSM includes the dead-time of the semiconductor devices and core-loss of the external inductor, which improves the SSM and LSM in the light and heavy load. The past work on the TTSM [27], [33]–[36] only provides an ideal model of the converter. The unavailability of the system loss component from the model affects its steady-state and dynamic accuracy.
- The effect of circuit parameters like load resistance, filter capacitance, external inductor inductance, and the voltage demand on the stability prediction is discussed.
- 4) A detailed analysis and comparison of proposed TTSM, FSM [1], [12], AVM [7], DTM [24], GAM [18] for the open and closed-loop behavior of the system have been presented. The proposed TTSM offers the best accuracy among the methods in the literature. Moreover, the proposed model can predict the critical gain to ensure the stable operation of the converter.

# **II. CONVERTER OPERATION AND ITS DESCRIPTION**

The PSBDAB converter consists of two H-bridges connected through the medium frequency ferrite transformer. There is an external inductor  $L_{ext}$  connected between the transformer and

one of the H-bridge, as shown in Fig. 1. The external inductor  $L_{ext}$  can be used as a control parameter to limit or manage the power flow in the PSBDAB converter [37]. The transformer primary to secondary turn ratio of the converter is denoted by  $N_{ps}$ . The output filter capacitance, switch conduction loss resistance, transformer input side & output-side resistance, the inductance of the external inductor, external inductor total loss resistance, and load resistance is denoted by  $C_o$ ,  $R_{sw}$ ,  $R_{pt}$ ,  $R_{st}$ ,  $L_{ext}$ ,  $R_{ext}$ , and R, respectively. The effective loss resistance of the inductor  $R_{ext}$  consists of the core loss component  $R_{co}$  and the copper loss component  $R_{cu}$ . The overall resistance and inductance of the PSBDAB converter referred to the output side of the transformer is denoted by  $r_{ef}$  and  $L_{ef}$ . The exact expression of  $r_{ef}$  and  $L_{ef}$  can be represented as,

$$r_{e_f} = 2R_{sw}(N_{ps}^2 + 1) + N_{ps}^2 R_{pt} + R_{ext} + R_{st}$$
(1)

$$L_{e_f} = L_{ext} + N_{ps}^2 L_{pt} + L_{st}$$
<sup>(2)</sup>

The wide bandgap semiconductor devices like SiC or GaN can be used to form an H-bridge, which improves the efficiency and power density of the converter. The signal from the controller given to the semiconductor devices  $S_{p1} - S_{p4}$ and  $S_{s1} - S_{s4}$  has a 50% duty cycle. The flow of power is controlled through the phase-shift difference between the primary and secondary side bridges  $V_p$  and  $V_s$ , respectively. The steady-state waveform of the primary-side bridge voltage, secondary-side bridge voltage, transformer current, rectifier transformer current, and output filter capacitor voltage of the converter are shown in Fig. 2. The phase difference between the bridges for the primary and secondary for the forward power flow is dT/2. The analysis and expression of the inductor current, output voltage, or other important characteristics of the system remains the same for input voltage greater than the output voltage or vice versa. The waveform in this paper shown in Fig. 2 assumes that the input voltage is greater than the output voltage. There are four sub-intervals in the phaseshifted controlled PSBDAB converter, as shown in Fig. 3. The description of each sub-interval for the forward power flow is as follows.

a) Sub-interval I  $[t_0, t_1]$ : The gating signals are applied to the primary side switches  $S_{p1}$  and  $S_{p4}$  to turn it on at  $t_0$ . The voltage across the input side H-bridge  $(V_P)$  for the first sub-interval is  $V_{in}$ . Since switches  $S_{s2}$  and  $S_{s3}$  are still conducting, the voltage across the H-bridge at the output side  $V_S$  will remain at  $-V_o$ . The voltage across the external inductor  $V_{ind}$  is more than zero in the first sub-interval; the transformer current i(t) increases from  $I_0$  to  $I_1$ . The negative transformer current at time-instant  $t_0$  illustrates the switch  $S_{p1}$ and  $S_{p4}$  are turned on with zero voltage switching.

b) Sub-interval II  $[t_1, t_2]$ : The secondary side switches  $S_{s1}$  and  $S_{s4}$  are turned on at  $t_1$ . The input side H-bridge voltage  $V_p$  remains the same at  $V_{in}$ . The polarity of the voltage across the H-bridge at the output side  $V_S$  changes from  $-V_o$  to  $V_o$ . The transformer current increases in this sub-interval from  $I_1$  to  $I_2$ . However, the transformer current will decrease from  $I_1$  to  $I_2$  when  $N_{ps}V_{in}$  is less than  $V_o$ . The positive transformer



FIGURE 3. Equivalent circuits during each sub-intervals.

current at time-instant  $t_1$  depicts the switches  $S_{s1}$  and  $S_{s4}$  are turned on with zero voltage switching.

c) Sub-interval  $[t_2, t_3]$ : The primary side switches  $S_{p1}$  and  $S_{p4}$  are turned off &  $S_{p2}$  and  $S_{p3}$  are turned on at  $t_2$ . Therefore, the polarity of the input side bridge voltage changes from  $V_{in}$  to  $-V_{in}$ , as shown in Fig. 2. The secondary side bridge voltage  $V_S$  remains the same at  $V_o$ . The voltage across the external inductor  $V_{ind}$  is less than zero, the transformer current decreases from  $I_2$  to  $I_3$ . The positive transformer current at time-instant  $t_2$  means that the switches  $S_{p2}$  and  $S_{p3}$  have been turned on with zero voltage switching.

d) Sub-interval IV  $[t_3, t_4]$ : The gating signal to the output side semiconductor devices  $S_{s1}$  and  $S_{s4}$  are removed, while gating signals are applied to the devices  $S_{s2}$  and  $S_{s3}$  at  $t_3$ . The input side bridge voltage for this sub-interval is the same as the last sub-interval at  $V_{in}$ . The output side bridge voltage  $V_s$  reverse its polarity from  $V_o$  to  $-V_o$ . The transformer current reduces from  $I_3$  to  $I_4$  for  $N_{ps}V_i > V_o$ . The negative transformer current at time instant  $t_3$  means that the devices  $S_{s1}$  and  $S_{s4}$  are turned on with zero voltage switching. The fourth sub-interval end at the switching period T.

#### **III. CONVENTIONAL DTM OF A PSBDAB CONVERTER**

The state variables of the PSBDAB converter are transformer current and capacitor voltage. The dynamics of the state-variable in each sub-intervals can be represented as [23],

$$\dot{x}_1(t) = A_1 x_1(t) + B_1 V_{in} \tag{3}$$

$$\dot{x}_2(t) = A_2 x_2(t) + B_2 V_{in} \tag{4}$$

$$\dot{x}_3(t) = A_3 x_3(t) + B_3 V_{in} \tag{5}$$

$$\dot{x}_4(t) = A_4 x_4(t) + B_4 V_{in} \tag{6}$$

where,  $\alpha = 1, 2, 3, 4$  denotes the sub-interval of the PSBDAB converter equivalent circuit as shown in Fig. 3.  $x_{\alpha}(t) = [i \ v_c]^T$  represent state-variables of the PSBDAB converter, while the variables  $A_{\alpha}$  and  $B_{\alpha}$  represents state matrices of the system. The expression of state matrices depends on the output filter capacitance, transformer turnratio, and other circuit parameters of the converter. The statematrices  $A_1 - A_4$  and  $B_1 - B_4$  in each sub-intervals can be expressed as [23],

$$A_{1} = \begin{bmatrix} -\frac{r_{e_{f}}}{L_{e_{f}}} & \frac{1}{L_{e_{f}}} \\ -\frac{1}{C_{e}} & \frac{-1}{RC_{e}} \end{bmatrix}, \quad A_{2} = \begin{bmatrix} -\frac{r_{e_{f}}}{L_{e_{f}}} & -\frac{1}{L_{e_{f}}} \\ \frac{1}{C_{e}} & -\frac{1}{RC_{e}} \end{bmatrix}$$
(7)

$$B_1 = \begin{bmatrix} \frac{N_{ps}}{L_e} \\ 0 \end{bmatrix}, \quad B_3 = \begin{bmatrix} -\frac{N_{ps}}{L_e} \\ 0 \end{bmatrix} x \tag{8}$$

$$A_3 = \overline{A_2}, \quad A_4 = A_1, \ \overline{B_2} = \overline{B_1}, \ B_4 = B_3$$
 (9)

The solution of differential equations given by (3) - (6) can be evaluated by the conventional method of linear algebra [38]. These differential equations can be solved with the help of the state variable initial value, matrix exponential that depends on the circuit parameters, and time-period of sub-interval and voltage at the input side of the converter  $V_{in}$  [38]. The unified solution of differential equations (3) - (6) is expressed as,

$$x_{k+1} = f(v_{in}, x_k) = e^{A_j t_{pj}} x_k + \Gamma_j V_{in}$$
(10)

where,

$$\Gamma_j = \int_0^{t_{pj}} e^{A_j t_{pj}} B_j dt = A_j^{-1} (e^{A_j t_{pj}} - I) B_j$$
(11)

where k = 0, 1, 2, 3 and j = k + 1 defines the statevector  $x_j$  for time-interval  $t_k$  to  $t_j$  as shown in Fig. 3. *I* is the two by two identity matrix. The phase-shift of the PSBDAB converter is unaltered in each switching period *T* as the gating signals to the semiconductor devices are supplied through the digital signal processor [39]. The solutions of the expressions (3) - (6) can be determined by using the standard linear algebra given by (10) as shown below,

$$x_1 = e^{A_1 t_{p1}} x_0 + \Gamma_1 V_{in} \tag{12}$$

$$x_2 = e^{A_2 t_{p2}} x_1 + \Gamma_2 V_{in} \tag{13}$$

$$x_3 = e^{A_3 t_{p3}} x_2 + \Gamma_3 V_{in} \tag{14}$$

$$x_4 = e^{A_4 t_{p4}} x_3 + \Gamma_4 V_{in} \tag{15}$$

where  $x_i$  represents the state variable at the end of the *i*<sup>th</sup> subinterval for i = 1,2,3,4.  $x_0$  and  $x_4$  are state variables at the start and end of the switching cycle with time-period *T*, as shown in Fig. 2. The sub-intervals I-IV of the PSBDAB converter repeats itself each switching cycle at the steady-state. Moreover, changes in the state variables during a switching cycle T add to zero. Therefore, the state variables at the start of the switching cycle  $x_0$  will equal the state variables at the end of the same switching cycle  $x_4$ . The expression of the state variable  $[i v_c]$  at time-instant  $t_4$  represented by  $x_4$  can be evaluated by substituting the exact expression of  $x_3$ ,  $x_2$ , and  $x_1$  from (12) - (14) into (15). The discrete-time expression of  $x_4$  can be written as,

$$x_4 = \xi(\Phi)x_0 + \zeta(\Phi)V_{in} \tag{16}$$

where

ξ

$$(\Phi) = e^{A_4 t_{p_4}} e^{A_3 t_{p_3}} e^{A_2 t_{p_2}} e^{A_1 t_{p_1}}$$
(17)

$$\zeta(\Phi) = e^{A_4 t_{p_4}} e^{A_3 t_{p_3}} e^{A_2 t_{p_2}} \Gamma_1 + e^{A_4 t_{p_4}} e^{A_3 t_{p_3}} \Gamma_2$$

$$+e^{A_4 t_{p_4}} \Gamma_3 + \Gamma_4 \tag{18}$$

The state variable  $x_4$  in (16) involves matrix-exponential that is cumbersome and hard to gain useful or important information about the PSBDAB converter's behavior. The model obtained through the conventional linear algebra method (16) is challenging to use for the controller design and tuning its parameters. The model given by (16) can be made simple by expanding the exponential matrix [3]. The simplest matrix exponential expansion is first-order or second-order approximation that can be represented as,

$$e^{A_j t_{pj}} = I + A_j t_{pj} \text{ or } I + A_j t_{pj} + \frac{A_j^2 t_{pj}^2}{2}$$
 (19)

The simplest first approximation of the exponential matrix approximation using (19) gives accurate information about the transformer current. However, there is a significant difference between the actual value and the predicted value from the first-order approximation in the output voltage  $v_o$ , as discussed in [40]. Therefore, most of the literature on the DTM uses a second-order approximation of the matrix exponential. Although the second-order approximation of the matrix experiential has good accuracy, the resultant model obtained is more complicated than the continuous-time models like CTROM, FSROM, or FDROM. The problem associated with the complexity of the model due to matrix exponential can be eased by a two-time scale model. The theory and the detailed explanation of the mixed system model, which includes timescale modeling, are well explained in [41].

## IV. DETAILED ANALYSIS OF THE PROPOSED TTSM FOR THE PSBDAB CONVERTER

The presence of a big filter capacitor at the load side does not allow the output voltage of the PSBDAB converter to vary significantly in a short period of time. But, the transformer current i(t) has a large ripple change from the negative peak to the positive peak in a switching cycle of T. The output voltage of the PSBDAB converter acts as a slow state variable (SSV), while the transformer current behaves as a fast state variable (FSV). After the SSV and FSV are defined based on their inherent properties, the time-scale-based generalized theory proposed in [42] can be used. The analysis is carried out in the existing literature [27], [33]-[36] by ignoring the loss component of the system (copper loss and semiconductor on the resistor, filter capacitor ESR), which in turn reduces the accuracy of the SSM.

The core loss of the transformer is neglected in this paper because it does not have a significant impact on the accuracy of the SSM or on the stability analysis of the PSBDAB converter [7], [23]. However, it does affect the efficiency of the system, especially at the light load in the phase-shift modulation. Moreover, the efficiency of the phase-shifted controlled PSBDAB converter is thoroughly studied in [7]. Therefore, the study of the efficiency of the converter is not included in this paper.

The transformer current (FSV) dynamics will be evaluated in the beginning, while the SSV (input and output voltage) will be considered as fixed variables in one particular subinterval. Subsequently, the dynamics of the SSV will be solved. The circuit state equation of the transformer current and the output voltage in the first ( $t_0,t_1$ ) and second subinterval ( $t_1,t_2$ ) can be represented as,

$$r_{e_f}i(t) + L_{e_f}\frac{di(t)}{dt} = N_{ps}V_{in}(t) + v_o(t) \quad \forall t \in (t_0, t_1) \quad (20)$$

$$r_{e_f}i(t) + L_{e_f}\frac{dt(t)}{dt} = N_{ps}V_{in}(t) - v_o(t) \quad \forall t \in (t_1, t_2) \quad (21)$$

$$v_o(t) = v_c(t) + i_d(t)R_c - i_o(t)R_c \quad \forall t \ \epsilon \ (t_0, t_2)$$
(22)

The rectified current  $i_d(t)$  flows opposite to the transformer current in the first sub-interval, i.e.,  $i_d(t) = -i(t)$  and in the same direction in the second sub-interval  $i_d(t) = i(t)$ . The expression of the output current  $i_o(t)$  is the same in all sub-intervals (I-IV) as,  $v_o(t)/R$ . It is important to express the dynamics of the transformer current as a function of state variable  $v_c(t)$  and input voltage  $v_{in}(t)$  for the first sub-interval I. The expression of i(t) w.r.t state variables is obtained from (20) - (22). The resultant expression of i(t) with  $i_o(t) = v_o(t)/R$  can be written as,

$$r_{ef}i(t) + L_e \frac{di(t)}{dt} = N_{ps}v_{in}(t) + \frac{Rv_c(t)}{R + R_c} - \frac{RR_c i(t)}{R + R_c}$$
(23)

The expression of the transformer current is further modified to make the modeling and analysis of the PSBDAB converter simpler and easier, as shown below,

$$ri(t) + L\frac{di(t)}{dt} = mv_{in}(t) + v_c(t)$$
(24)

where,

$$r = r_{e_f} + \frac{RR_c}{R + R_c} \{ 1 + \frac{R_c}{R} \},$$
(25)

$$m = N_{ps} \{ 1 + \frac{R_c}{R} \} \text{ and } L = L_e \{ 1 + \frac{R_c}{R} \}$$
 (26)

The expression of the transformer current for the first sub-interval is obtained by using the conventional first-order differential equation solution,

$$i(t) = i(t_0)e^{\frac{-t}{\tau}} + \frac{mv_i(t) + v_c(t)}{r} \left(1 - e^{-t/\tau}\right)$$
(27)

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where  $\tau = L/r$ .  $i(t_0)$  is the current at the start of the switching period or sub-interval I. Likewise, the dynamics of the transformer current for the second sub-interval II have been expressed in (28).  $i(t_1)$  is the current at the start of the sub-interval II.

$$i(t) = i(t_1)e^{\frac{-t}{\tau}} + \frac{mv_i(t) - v_c(t)}{r} \left(1 - e^{-t/\tau}\right)$$
(28)

Once the dynamics of the transformer current in the first and second sub-interval is obtained (27) - (28), the expression for the capacitor voltage  $v_c(t)$  can be obtained by averaging the transformer current dynamics over the first sub-interval as discussed in [33], [41]. The expression of the capacitor voltage for the first-sub-interval is denoted as,

$$C_o \frac{dv_c(t)}{dt} = i_d(t) - \frac{v_o(t)}{R}$$
(29)

The above expression of the capacitor voltage needs to be rewritten as a function of the state-variable  $[i \ v_c]^T$ . It can be obtained by substituting the expression of  $v_o$  from (22),  $i_o(t) = v_o(t)/R$  and  $i_d(t) = i(t)$  into (29),

$$C\frac{dv_c(t)}{dt} = -i(t) - \frac{v_c(t)}{R} \text{ with } C = C_o \left[1 + \frac{R_c}{R}\right] \quad (30)$$

The capacitor voltage at the end of the first sub-interval can be obtained by integrating (30) from zero to  $t_1$  [33], [41]. Therefore, the expression of the capacitor voltage for the first and second sub-intervals can be written as [33], [41],

$$v_c(t_1) = v_c(t_0) + \frac{1}{C} \int_0^{t_{p_1}} -i(t)dt - \frac{t_{p_1}v_c(t_0)}{CR}$$
(31)

and

$$v_c(t_2) = v_c(t_1) + \frac{1}{C} \int_0^{t_{p_2}} i(t)dt - \frac{t_{p_2}v_c(t_1)}{CR}$$
(32)

The exact expression of the transformer current at the end of the first and second sub-interval can be evaluated by substituting " $t = t_{p1}$ " and " $t = t_{p2}$ " in (27) and (28), respectively. The transformer current at the end of the first and second sub-interval as a function of the state variables and circuit parameters can be written as,

$$i(t_1) = i(t_0)e^{\frac{-t_{p1}}{\tau}} + \frac{mv_i(t_0) + v_c(t_0)}{r} \left(1 - e^{-t_{p1}/\tau}\right)$$
(33)

$$i(t_2) = i(t_1)e^{\frac{-t_{p2}}{\tau}} + \frac{mv_i(t_0) + v_c(t_0)}{r} \left(1 - e^{-t_{p2}/\tau}\right)$$
(34)

The converter dynamics of the SSV at the end of the sub-interval I and II can be evaluated by substituting the expression of the FSV from (27) and (28) into (31) and (32). The resulting capacitor voltage is expressed in (35) and (36).

$$v_{c}(t_{1}) = i(t_{0})\frac{\tau}{2C} \left(1 - e^{-t_{p1}/\tau}\right) + v_{c}(t_{0}) \left[1 - \frac{t_{p1}}{rC} - \frac{t_{p1}}{RC} + \frac{\tau}{rC} \left(1 - e^{-t_{p1}/\tau}\right)\right] - mv_{in} \left[\frac{t_{p1}}{rC} - \frac{\tau}{rC} \left(1 - e^{-t_{p1}/\tau}\right)\right]$$
(35)

and

$$v_c(t_2) = i(t_1) \frac{\tau}{2C} (1 - e^{-t_{p2}/\tau})$$

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$$+v_{c}(t_{1})\left[1-\frac{t_{p2}}{rC}-\frac{t_{p2}}{RC}+\frac{\tau}{rC}\left(1-e^{-t_{p2}/\tau}\right)\right]$$
$$+mv_{in}\left[\frac{t_{p2}}{rC}-\frac{\tau}{rC}\left(1-e^{-t_{p2}/\tau}\right)\right]$$
(36)

The SSV and FSV of the PSBDAB converter for the first two sub-intervals have been developed in (33) - (36). The PSBDAB converter's discrete-time model can be obtained using (33) - (36). The state-space model for the first and second sub-interval is represented as,

$$x(t_1) = \phi_1 x(t_0) + \psi_1 v_{in}(t_0)$$
(37)

where

$$\phi_{1} = \begin{bmatrix} e^{-t_{p_{1}}/\tau} & \frac{(1-e^{-t_{p_{1}}/\tau})}{r} \\ -\frac{\tau}{C}(1-e^{\frac{-t_{p_{1}}}{\tau}}) & 1-\frac{t_{p_{1}}}{rC} - \frac{t_{p_{1}}}{RC} + \frac{\tau}{rC}(1-e^{\frac{-t_{p_{1}}}{\tau}}) \end{bmatrix}$$
(38)

$$\psi_{1} = \begin{bmatrix} \frac{m(1-e^{-p_{1}/\tau})}{r} \\ m\left[\frac{t_{p_{1}}}{rC} - \frac{\tau}{rC}\left(1 - e^{-t_{p_{1}}/\tau}\right)\right] \end{bmatrix}$$
(39)

and

$$x(t_2) = \phi_2 x(t_1) + \psi_2 v_{in}(t_0)$$
(40)

where

$$\phi_{2} = \begin{bmatrix} e^{-t_{p_{2}}/\tau} & \frac{-(1-e^{-t_{p_{2}}/\tau})}{r} \\ \frac{\tau}{C}(1-e^{\frac{-t_{p_{2}}}{\tau}}) & 1-\frac{t_{p_{2}}}{rC} - \frac{t_{p_{2}}}{RC} + \frac{\tau}{rC}\left(1-e^{\frac{-t_{p_{1}}}{\tau}}\right) \end{bmatrix}$$
(41)

$$\psi_{2} = \begin{bmatrix} \frac{m(1-e^{-lp_{2}/t})}{r} \\ -m\left[\frac{t_{p_{2}}}{rC} - \frac{\tau}{rC}(1-e^{-t_{p_{2}}/\tau})\right] \end{bmatrix}$$
(42)

The standard state-space matrix for the first two sub-interval can be written as,

$$x(t_2) = \phi_{12}x(t_0) + \psi_{12}v_{in} \tag{43}$$

where

$$\phi_{12} = \phi_2 \phi_1 \text{ and } \psi_{12} = (\phi_2 \psi_1 + \psi_2) \tag{44}$$

Once the model is derived for the half-cycle, there are two methods to obtain the full model. Either by using the same methodology to achieve the state equation for the III and IV intervals as done in [23] or using the half-cycle symmetry proposed in [31]. In this paper, the half-cycle symmetry property of the resonant converter is exploited to obtain the state variable dynamics for the next two sub-intervals [31]. The in-depth explanation of the half-cycle symmetry is discussed in [31]. The final discrete-time model of the PSBDAB converter over a switching period in terms of the first two subintervals can be written as,

$$x(t_4) = \left\{ W\phi_{12} \right\}^2 x(t_0) + \left\{ W\phi_{12} + I \right\} W\psi_{12} v_{in}$$
(45)

where

$$W = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$$
(46)

## A. LARGE-SIGNAL MODEL

It is vital to develop the steady-state expressions of the transformer current and output voltage to study modeling and the stability prediction of the system [23]. The half-cycle symmetry is used to obtain the expression of the state variables [31]. The steady-state transformer current at time-instant  $t_2$  will have the same magnitude with an opposite polarity of the transformer current at the time-instant  $t_0$ . This is due to its odd half-cycle symmetric property, as shown in Fig. 2. But the capacitor voltage has an even half-cycle symmetric property. Therefore, the magnitude and polarity of the capacitor voltage at time-instant  $t_0$ , as shown in Fig. 2. Therefore, the steady-state expression of the FSV and SSV at the end of the second sub-interval w.r.t. start of the first sub-interval I can be written as,

$$\vec{v}_L(t_0) = -i_L(t_2) \text{ and } v_c(t_n) = v_o(t_c)$$
 (47)

The combination of (43) and (47) can be written as,

$$\begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i(t_2) \\ v_c(t_2) \end{bmatrix} = \phi_{12} \begin{bmatrix} i(t_0) \\ v_c(t_0) \end{bmatrix} + \psi_{12} v_{in} \quad (48)$$

$$\chi_{ss} = (W - \phi_{12})^{-1} \psi_{12} v_{in} \tag{49}$$

The state variable dynamics of the PSBDAB converter over a switching period *T* is expressed in (45). The LSM of the output voltage  $v_o(z)/d(z)$  can be achieved through z-transform on (45).

$$G(z) = [0 \ 1] \left\{ zI - (W\phi_{12})^2 \right\}^{-1} (W\phi_{12} + I) W\psi_{12} v_{in}$$
(50)

The transfer function (50) of the open-loop is essential to study the complex system, which involves the PSBDAB converter like modular structure [10]. The ECM of the PSBDAB converter given by (50) reduces the overall time to run a simulation compared to the DTDS. The reduced time required by ECM is beneficial to study the characteristics of the PSBDAB converter with the energy storage like battery, ultracapacitor [2] that need to operate for a long time around, an hour or more.

# **B. SMALL-SIGNAL MODEL**

It is vital to study the system's behavior around its equilibrium point. The study about its equilibrium point is also known as the SSM of the converter [5]. The SSM is required to select and design a controller to ensure stable operation throughout the operating range. The SSM is obtained by perturbing and linearizing the LSM (45) around its operating point.

The waveform of the PSBDAB converter shown in Fig. 2 is under the steady-state operation. However, it takes a number of cycles to reach equilibrium [5]. We assume in this study that the steady-state is reached at the  $\eta^{th}$  cycle. Therefore, it can be concluded that the state variables at the time-instant  $t_0$  are equivalent to the state variables at the start of the  $\eta^{th}$ cycle and the state variables at the time-instant  $t_4$  is equivalent to the state variables at the end of the  $\eta^{th}$  cycle or the start of the  $(\eta + 1)^{th}$  cycle, respectively. The state variable at the start and end of the  $\eta^{th}$  cycle is denoted by  $x_{\eta}$  and  $x_{\eta+1}$ . The phase-shift in the  $\eta^{th}$  is represented by  $d_{\eta}T_s/2$ . The non-linear state equation given by (45) can be rewritten separately for state variables as,

$$x_{1(\eta+1)} = g_1(x_{1\eta}, x_{2\eta}, v_{in}, d_\eta)$$
(51)

$$x_{2(\eta+1)} = g_2(x_{1\eta}, x_{2\eta}, v_{in}, d_\eta)$$
(52)

The above non-linear equations (51) and (52) need to linearized around the operating point by perturbing the state variables, control variable, and the input voltages as [5],

$$x_{1(\eta+1)} = X_{1ss} + \delta x_{1(\eta+1)} \tag{53}$$

$$x_{2(\eta+1)} = X_{2ss} + \delta x_{2(\eta+1)} \tag{54}$$

$$x_{1\eta} = X_{1ss} + \delta x_{1\eta}, \ x_{2\eta} = X_{2ss} + \delta x_{2\eta}$$
(55)

$$d_{\eta} = d + \delta d_{\eta}, \ v_{in\eta} = V_{in} + \delta v_{in} \tag{56}$$

 $X_{1ss}$ ,  $X_{2ss}$ , d, and  $V_{in}$  are the steady-state value of the transformer current, capacitor voltage, phase-shift, and the supplied voltage of the PSBDAB converter, respectively.  $\delta x_{1(\eta+1)}$  and  $\delta x_{2(\eta+1)}$  represent perturbation in the transformer current and capacitor voltage in the  $(\eta + 1)^{th}$  cycle, respectively.  $\delta x_{1\eta}$  and  $\delta x_{1\eta}$  represent perturbation in the transformer current and capacitor voltage in the  $\eta^{th}$  cycle, respectively.  $\delta d_{\eta}$  and  $\delta v_{in}$  represent the perturbation in the phase-shift and input voltage, respectively. The expressions given by (53) - (56) can be used to linearize (51) and (52) to form standard state-space SSM of the PSBDAB converter,

$$\begin{bmatrix} \delta x_{1(\eta+1)} \\ \delta x_{2(\eta+1)} \end{bmatrix} = \begin{bmatrix} \frac{\partial g_1}{\partial x_{1\eta}} & \frac{\partial g_1}{\partial x_{2\eta}} \\ \frac{\partial g_2}{\partial x_{2\eta}} & \frac{\partial g_2}{\partial x_{2\eta}} \end{bmatrix} \begin{bmatrix} \delta x_{1\eta} \\ \delta x_{2\eta} \end{bmatrix} \\ + \begin{bmatrix} \frac{\partial g_1}{\partial d_{\eta}} \\ \frac{\partial g_2}{\partial d_{\eta}} \end{bmatrix} \delta d_{\eta} + \begin{bmatrix} \frac{\partial g_1}{\partial v_{in\eta}} \\ \frac{\partial g_2}{\partial v_{in\eta}} \end{bmatrix} \delta v_{in} \quad (57)$$

The large-signal model of the PSDAB converter (45) is compared to (51) and (52). Subsequently, the generalized expression (57) is used to obtain the SSM of the PSDAB converter. The simplified expression of the SSM can be represented as,

$$\delta x_{\eta+1} = A_s \delta x_n + B_s \delta d_n + C_s \delta v_{in} \tag{58}$$

where,

$$A_s = (W\phi_{12})^2, \ C_s = (W\phi_{12} + I)W\psi_{12}$$
(59)

$$B_{s} = \frac{(W\phi_{12} + I)W\psi_{12}V_{in} + (W\phi_{12})^{2}X_{ss}}{\delta d}$$
(60)

The SSM of the PSDAB converter can be achieved by applying z-transform on (58), which results in control to capacitor voltage transfer function and input voltage to the capacitor voltage transfer function as,

$$G_{vd}(z) = \left| \frac{\delta v_{c\eta}(z)}{\delta d_{\eta}(z)} \right|_{\delta v_{in}=0} = [0\ 1](zI - A_s)^{-1} B_s \quad (61)$$

$$G_{vi}(z) = \left| \frac{\delta v_{c\eta}(z)}{\hat{v}_{in}(z)} \right|_{\delta d_n = 0} = [0 \ 1](zI - A_s)^{-1} C_s \quad (62)$$



FIGURE 4. Block diagram of a digital controller.

# C. STABILITY

The closed-loop block diagram of the digitally controlled PSBDAB converter is shown in Fig. 4. The study of the stability analysis for a proportional controller is taken as an example for its simplicity. The feedback output voltage from the ADC is sampled at the start of the switching period. Therefore, digital control implementation always causes a unit delay. The difference between the sensed output voltage and the reference voltage is fed to the proportional gain. The output of the proportional gain block gives the required phase-shift between the input and output side bridge voltages. The approach to obtain the stability prediction for proportional-integral (PI) control, proportional integral plus derivative (PID) control, or any other control is almost similar. The digitally controlled phase-shift (d) for the closed-loop block diagram of the PSBDAB converter shown in Fig. 4 can be represented as,

$$d_{\eta+1} = k_g(V_{ref} - V_{o\eta}) = k_g(V_{ref} - M_{esr}x_\eta)$$
(63)

where,

$$M_{esr} = \left[ -\frac{RR_C}{R+R_c} \frac{R}{R+R_c} \right] \quad \forall d \in (0, 0.5)$$

When output filter ESR is ignored, the output voltage equals the capacitor voltage, i.e.,  $M_{esr} = [0 \ 1]$ . However, output filter ESR is considered; the output voltage expression depends on both the output filter capacitor voltage and the rectified transformer current  $i_d$ . The voltage is sampled at the start of each cycle. Therefore, the output voltage's expression in terms of the state variable can be attained from (45), as shown in Fig. 4. The final discrete-model (45) and (63) can be used for the stability prediction of the DSP controlled closed-loop PSBDAB converter.

# V. EXPERIMENTAL VALIDATION OF THE TTSM

The circuit parameters of the experimental prototype are shown in Table 1. The low on-resistance MOSFETs are selected as semiconductor devices. The ETD core material of the transformer (ETD59) and external inductor (ETD49) is 3C90, developed by Ferroxcube. The inductor is designed with a magnetic flux density of 200 mT. The core loss per

Value
60 Volt
15 kHz
$100 \text{ m}\Omega$
$2.5 \ \mu \ \Omega$
0.975
$105 \ \mu H$
$50 \text{ m}\Omega$
$150 \text{ m}\Omega$
11 Ω
165 $\mu$ F
$150 \text{ m}\Omega$
$15 \text{ m}\Omega$
UCC5390
IRFP4321PBF

#### TABLE 1. Circuit parameters.

unit volume  $(\rho_d)$  of the inductor can be calculated as per the datasheet from the Ferroxcube [43]. The core-loss for ETD49 core and 3C90 material is around 150  $mW/cm^3$  [43]. The effective core volume ( $V_e$ ) of the ETD49 core is 24000 mm<sup>3</sup>. Therefore, the effective power loss due to the core loss, equal to  $\rho_d V_e$  in the external inductor, will be around 3.5 W. The transformer current's root means square (RMS) for the phase-shifted PSBDAB converter is around 5A with little variation around the light and heavy load. However, the RMS current is assumed to be constant in this paper for simplicity. The effective resistance due to core-loss can be calculated as around 150  $m\Omega$  as mentioned in Table 1. The digital implementation of the converter results in a unit delay of one switching period [14]. The unit delay can be approximated by a first-order pade approximation as given in (64). A low-cost analyzer (Digilent analog discovery 2), a part of the national instrument corporation, has been used to obtain the smallsignal response.

$$e^{-sT} = \frac{1 - sT/2}{1 + sT/2} \tag{64}$$

The dead-time of the semiconductor devices is 75 cycles of the 150 MHz DSP. The dead-time can be calculated as the product of the number of cycles and time-period of the oscillator of the digital processor, which corresponds to 500 ns. This dead-time causes the deviation in the phase-shift between the bridge voltages ( $v_{pr}$  and vsc) from dT/2 to ( $d + d_{dt}$ )T/2. The 500 ns dead-time causes the phase-shift of the converter to increase by  $d_{dt} = 0.015$ . However, the value of  $d_{dt}$  will change around the critical phase-shift  $d_{cr}$ . The critical phase-shift  $d_{cr}$  is the minimum phase-shift of the system to ensure the soft-switching operation of the converter. The value of the critical phase-shift can be calculated, as discussed in [44]. Moreover, the dead-time will not cause any deviation in the phase-shift for  $d > d_{cr}$ .



FIGURE 5. Steady-state bridge voltages and transformer current.







FIGURE 7. Comparative results of the root mean squared percent error (RMSPE) of the output voltage from the various model.

# A. EXPERIMENTAL VALIDATION OF THE LSM OF THE PSBDAB CONVERTER

The steady-state PSBDAB converter waveform of the transformer current, input, and output side bridge voltages at (d = 0.25) are shown in Fig. 5. The predicted comparative results and root mean squared percent error (RMSPE) of the output voltage from the various method in the literature along with the proposed method are shown in Fig. 6 and Fig. 7, respectively. The output voltage from hardware results, proposed TTSM, FDROM [14], CTROM [7], GAM [18], and FSROM [12] at d = 0.05 are 14 V, 13.9 V, 9.3 V, 10.6 V, 8 V and 12.5 V, respectively. The results from the proposed TTSM and hardware results are almost the same, with a percentage error of only 0.7 %. The FSROM provides a better prediction of the output voltage than the other models due to the incorporated dead-time effect while mod-



FIGURE 8. Open-loop response G(z) of the PSBDAB converter for a step increase in the control variable 'd' (a) from 0.05 to 0.075 (b) 0.25 to 0.35.

eling. The output voltage from hardware results, proposed TTSM, FDROM [14], CTROM model [7], GAM [18], and FSROM [12] at d = 0.45 are 46.1 V, 46.5 V, 48.2 V, 47.3 V, 48.8 V and, 48.1 V, respectively. Likewise to the light load performance, the proposed model has the best accuracy, with a percentage error of around 0.9 %. The RMSPE of the proposed TTSM, FDROM [14], CTROM [7], GAM [18], and FSROM [12] are 0.6 %, 12.9 %, 9.35 %, 17.8 % and 4.9 %, respectively as shown in Fig. 7.

The PSBDAB converter integration with the energy storage ( battery or ultra-capacitor) needs to be operated for a long time to study the charging and discharging behavior of the energy storage. The DTDS demands a very high computation and takes a longer time than the ECM simulation. Therefore, the model developed in this paper (50) can be used to study the charging and discharging behavior of the energy storage integrated with the PSBDAB converter. The open-loop transfer function (50) is implemented in MATLAB. Initially, the system was operating at light-load with d = 0.05. At t =0.5 s, the variable d is changed from the 0.05 to 0.075. The output voltage also increases due to a step-change in the variable d. The proposed model gives the best accuracy and predicts the response of the open-loop behavior with almost no error, as seen from Fig. 8 (a). The accuracy of the various models is compared at heavy load with step-increase in the variable d from 0.25 to 0.35, as shown in Fig. 8 (b). The proposed TTSM accurately predicts hardware results with almost no error compared to other models.

The output voltage open-loop response obtain from all models and experiment shows first-order behavior. This is due to the fact that the transformer current has a pole and zero very near to each other. Therefore, they cancel each other and have little impact on the open-loop behavior of the converter. The proposed method gives the best results compared to the other proposed model in the literature, as visible from Fig. 8.

# B. EXPERIMENTAL VALIDATION OF THE SSM OF THE PSBDAB CONVERTER

The comparative study of the existing literature and the proposed TTSM is studied in this subsection. The effect of the capacitor current dynamics on the SSM is ignored in this study for simplicity. The magnitude plot of the proposed model is obtained from (61). The frequency response at light load (d = 0.05) is shown in Fig. 9. The low-frequency gain at 10 Hz from the hardware, proposed TTSM, conventional DTM [3], [24], FDROM [14], CTROM [7], GAM [18], and FSROM [12] are 44.1 dB, 44 dB, 44.4 dB, 44.8 dB, 45.1 dB, 43.8 dB and, 44.6 dB, respectively. The high-frequency gain at 4 kHz from the hardware, proposed TTSM, conventional DTM [3], [24], FDROM [14], CTROM [7], GAM [18], and FSROM [12] are 12.4 dB, 12.4 dB, 11.7 dB, 10 dB, 12 dB, 11 dB and, 11.7 dB, respectively. The proposed TTSM has discrepancy of only 0.1 dB at 10 Hz and null at 4kHz, respectively.

The phase response is obtained using (61) in MATLAB. It is important to note that the phase caused by the sensor and the unit delay is omitted in the hardware results. Moreover, the discrete-model [3], [24] and the proposed model are converted from the discrete-model to the continuous model. A small phase is obtained at the low frequency (10 Hz) around -6°, as seen from Fig. 9. The phases at the higher frequency (4 kHz) from the experiment and the rest of the models are around  $-88.6^{\circ}$  and  $-92^{\circ}$ , respectively.

The frequency response at heavy load (d = 0.25) is shown in Fig 10. The low-frequency gain at 10 Hz for d = 0.25 from the hardware, proposed TTSM, conventional DTM [3], [24], FDROM [14], CTROM [7], GAM [18], and FSROM [12] are 37 dB, 38 dB, 39.2 dB, 39.72 dB, 39.72 dB, 40.7 dB and, 39.2 dB, respectively. The high-frequency gain at 4 kHz from the experiment, proposed model, conventional DTM [3], [24], FDROM [14], CTROM [7], GAM [18], and FSROM [12] are 7 dB, 6.9 dB, 6.4 dB, 6.6 dB, 6.6 dB, 8.2 dB and, 6.2 dB, respectively. The proposed TTSM has discrepancy of only 1 dB at 10 Hz and 0.1 at 4kHz, respectively. However, rest of the model has more than 2 dB error at the low frequency.

The phase response at d = 0.25 is shown in Fig. 10. Identical to the low phase-shift (d = 0.05), the phase-response of all models at d = 0.25 are identical. All models can predict the phase response correctly. There is a small discrepancy of around 3-4°. It can be seen from Fig. 9 and 10 that the proposed model provides better accuracy for the magnitude plot at low and high frequencies compared to other previously presented models.



**FIGURE 9.** Bode plot of  $G_{vd}(s)$  at d = 0.05.

# **VI. STABILITY ANALYSIS OF THE PSBDAB CONVERTER**

The circuit parameter of a system has significant effects on the system's stability and dynamic behavior. The output voltage and transformer current can have significant oscillation due to wrong choices of the system's parameters. The system's behavior can undergo regular instability because of a shift in the PSBDAB converter's circuit parameters. The system's behavior can be studied with the help of the bifurcation diagram, Jacobian matrix, stability curve, or Lyapunov exponent. The bifurcation diagram will be used in this paper to analyze the PSBDAB converter. The analysis, simulation, and experiment are conducted for the circuit parameter listed in Table 1.

A bifurcation diagram is a visual summary of the succession of period-doubling produced, as the gain of the controller  $k_g$ ' increases [26]. The periodic behavior of the transformer current's steady-state value at  $t_{\eta_1}$  can be plotted as a function of proportional gain  $k_g$ '. A singular point indicates that the transformer current's steady-state is settled at a fixed and stable point. The transformer current can undergo from a fixed and stable point to periodic double, periodic quadruple, or higher period [45].

The LSM of the PSBDAB converter given by (45) is established for one cycle. The LSM for the state variable in the  $(\eta + 1)^{th}$  cycle  $(x_{\eta+1})$  with respect to the state-variable in the  $\eta^{th}$  cycle  $(x_{\eta})$  can be written as (65). Moreover, the expression of the closed-loop control variable is modified as ( $\Phi$ ), which is represented in radian to have a better understanding of the phase-shift between the bridge voltages.

 $x_{\eta+1} = \{W\phi_{12}\}^2 x_{\eta} + \{W\phi_{12} + I\}W\psi_{12}v_{in}$ 

and

$$\Phi_{n+1} = k_o (V_{ref} - M_{esr} x_n) \quad \forall \ \Phi \ \epsilon \ (0, \pi/2) \tag{66}$$

(65)



**FIGURE 10.** Bode plot of  $G_{vd}(s)$  at d = 0.25.

The bifurcation map can be studied from (65) and (66). The control parameter  $k_{g}$  is varied from 0.01 to 10, as shown in Fig. 11 to Fig. 18. At first, the output capacitor ESR  $(R_c = 0)$  is neglected, and the proportional gain  $(k_g)$  is increased. It can be seen from Fig. 11 that the system goes to the unstable region when  $k_g$  is more than 1.71. When the capacitor ESR is included in the model, the critical value of  $k_g$  for the stable operation is reduced to 1.35, as shown in Fig. 12. The nature of the bifurcation diagram with the inclusion of capacitance ESR shown in Fig. 12 or exclusion of the capacitance ESR shown in Fig. 11 is similar. This contradicts with the explanation about the inclusion of the filter capacitor ESR  $(R_c)$  changes the transformer current variation swing [23]. Moreover, the ESR of the filter capacitor  $(R_c)$  is increased thrice to 0.45  $\Omega$ , and the bifurcation diagram is plotted in Fig. 13. The drift in the transformer current is identical to  $R_c = 0 \Omega$  or  $R_c = 0.15 \Omega$ . The critical gain to ensure stability  $k_{gc}$  is only reduced to 0.82 for  $R_c = 0.45 \Omega$ . Therefore, it can be interpreted that the drift in the transformer current not only depends on the filter capacitor ESR but also on other circuit parameters.

The standard electrolytic and film capacitor has a tolerance of around  $\pm 20\%$ . Therefore, the bifurcation diagram with 20% less capacitance of the output filter capacitor (132  $\mu$ F) is plotted in Fig. 14. There is not much difference in the behaviors of the inductor or its bifurcation diagram shape in this scenario. However, the critical gain has been reduced to 1.1. Moreover, the bifurcation diagram remains the same, with a 20% increase in capacitance. However, the actual plot is not shown in this paper due to repetitive behavior. Most of the work on the time-scale model [27], [33] [34], [36] does not include the system loss on the model. Therefore, the bifurcation with r = 0 is plotted in Fig. 15. It shows the



**FIGURE 11.** Bifurcation diagram using  $k_g$  as a parameter for (a)  $R_c = 0$ .



**FIGURE 12.** Bifurcation diagram using  $k_g$  as a parameter for  $R_c = 0.15$ .



**FIGURE 13.** Bifurcation diagram using  $k_g$  as a parameter for  $R_c = 0.45\Omega$ .



**FIGURE 14.** Bifurcation diagram using  $k_g$  as a parameter for  $C = 132 \mu F$ .

effect of the system loss resistance (r) on the stability of the system. The gain for the system to be stable should be less than 1.38 for the lossless model (r = 0). However, the effect



**FIGURE 15.** Bifurcation diagram using  $k_g$  as a parameter for  $r = 0 \ \Omega$ .



**FIGURE 16.** Bifurcation diagram using  $k_g$  as a parameter for  $L = 98\mu H$ .

of the capacitor ESR is considered for the lossless system, as shown in Fig. 15. When neither r nor  $R_c$  is considered [27], [33], [34], [36], the critical gain of the system increases to 1.46.

The bifurcation diagram with 90% of the equivalent inductance of the system ( $L = 98\mu H$ ), double load resistance ( $R = 22\Omega$ ), and around 85% of the reference voltage ( $V_{ref} =$ 38V) are shown in Fig. 16, Fig. 17 and Fig. 18, respectively. It can be seen that that unlike the previous case, the trends of the transformer current are different, as gain ( $k_g$  of the closes-loop is increased. The critical gain for  $L = 98\mu H$ ,  $R = 22\Omega$  and  $V_{ref} = 38V$  is 0.81, 0.55 and 0.84, respectively. It can be seen that each circuit parameter affects the critical proportion gain  $k_{gc}$  of the converter.

# A. SIMULATION VERIFICATION OF THE STABILITY ANALYSIS OF THE PSBDAB CONVERTER

The theory and analysis in Sections IV and VI are verified in simulation (MATLAB/Simulink) and experimental prototype. The system was operating with proportion gain  $k_g =$ 1.3 in a stable region of the converter. The closed-loop gain is increased from 1.3 to 1.4 at the time t = 0.01 s. It can be seen from Fig. 19 that the converter comes out of the stable region at  $k_g =$  1.4, as predicted from the bifurcation diagram in Fig. 12. The bifurcation diagram of the system for  $k_g =$  1.4, as shown in Fig. 12 comprises transformer current magnitude from 5.6 A to 8A. The same observation is also obtained through the simulation studies, as shown in Fig. 19(d). The oscillation in the transformer current increases as the gain



**FIGURE 17.** Bifurcation diagram using  $k_g$  as a parameter for  $R = 22\Omega$ .



**FIGURE 18.** Bifurcation diagram using  $k_g$  as a parameter for  $V_{ref} = 38 V$ .

of the closed-loop  $k_g$  is increased, as seen from Fig. 19. The output voltage and phase-shift  $\Phi$  waveform with the function of gain are shown in Fig. 19 (c). The ripple in the output voltage increase as the  $k_g$  is increased. The simulation results approve of the results obtained from the bifurcation diagram. It is important to note that the oscillation in the transformer current is increases slowly when  $k_g$  is increased, even with the inclusion of the capacitor ESR. However, it was claimed in [23] that the transformer current goes directly into the chaotic region when the system goes from stable to the unstable region when capacitor ESR is considered. However, such behavior depends on the circuit parameter of the system. The behavior of the system is the same in all cases shown from Fig. 11 to 18 except for load resistance  $R = 22\Omega$ .

The bifurcation diagram of the system with double load resistance shows different behavior than other cases. The instability of the system increases much faster than in other cases. The same statement is also verified through simulation results carried out in MATLAB/Simulink. The system was operating with proportion gain  $k_g = 0.54$  in a stable converter region. The closed-loop gain is increased from 0.54 to 0.56 at the time t = 0.01 s. It can be seen from Fig. 20 that the converter comes out of the stable region at  $k_g = 0.56$ , as obtained from the bifurcation diagram in Fig. 17. There is a small oscillation at  $k_g = 0.56$ . However, when the gain is increased marginally by 0.02, the system goes into chaotic behavior. The chaotic nature increases much faster at  $k_g = 0.56$ , as shown in Fig. 20(c). This nature is much more predominant when closed-loop gain  $k_g$  is moved only

by 0.04 from its critical gain  $k_{gc}$ . However, in the other cases shown in Fig. 11 to 16 and 18, the chaotic nature is relatively less even though the critical gain increases by 0.3 or more.

# B. EXPERIMENTAL VERIFICATION OF THE STABILITY ANALYSIS OF THE PSBDAB CONVERTER

The stability analysis of the converter is validated in the experimental setup with the same system parameters used in the analysis and the simulation studies. The hardware set-up for the closed-loop operation of the PSBDAB converter is shown in Fig. 21. The low resistance MOSFET IRFP4321PBF from Infineon is used as a semiconductor device. The voltage transducer LV25-P from LEM is used as a voltage sensor. The signal to the semiconductor is controlled through Texas Instrument TMS320F28335 experimental kit.

The experiment is conducted with load resistance R =11 $\Omega$ . Initially, the controller's gain is set at 1.3; the system remains in the stable region. There are no unwanted oscillation or dc components in the transformer current, as shown in Fig. 22. However, the oscillation starts to appear when the gain is increased more than 1.4. The system undergoes significant oscillation at gain of 1.7, as shown in Fig. 23. There are a small discrepancies between the theoretical and experimental value of the critical gain to obtain stability for  $R = 11\Omega$ . The control variable d to obtain the output voltage for  $R = 11\Omega$  is around  $d \approx 0.4$ , as shown in Fig. 19. The effective resistance of the system is increased at the higher value of d due to more conduction loss in the transformer, inductor, and turn-on loss of the semiconductor devices[7]. The increase in the effective resistance increases the critical gain of the close-loop for load resistance  $R = 11\Omega$ , as shown in Fig. 15. It was shown in Fig. 15 that the rise in the effective resistance increases the critical gain  $k_{cg}$  of the system and vice versa. The increase in the equivalent resistance r also reduces the maximum current in the unstable region.

The system is also validated with double load resistance (R = 22) to show how the oscillation of the transformer current varies at different loads. Initially, the converter was operated with the gain of the closed-loop  $k_g$  at 0.54. The system operated in the stable region with no unwanted oscillation in the transformer current or output voltage, as shown in Fig. 24. However, when  $k_g$  is increased to 0.6, a very high oscillation in the transformer, current and the output voltage, as observed in Fig. 25. The maximum current in the analysis (bifurcation diagram), detailed time-domain simulation, and the experimental results are the same to be around 8 A.

The comparative studies of the stability prediction between proposed TTSM and existing DTM in the literature have been listed under Table 2. The proposed model offers better accuracy than the other DTM proposed in the literature [3], [23] [24] [27]. There is a minor difference between all the models at  $R = 22\Omega$ . This is due to the low current required to obtain a reference voltage of 45 V at 22  $\Omega$  compared to the current requirement at 11  $\Omega$ . The same argument can be made when the reference voltage is reduced from 45 V to 38 V. The aging of the capacitor causes its ESR to increase with time.



**FIGURE 20.** Simulation results of the PSBDAB converter with load resistance  $R = 22\Omega$ .



**FIGURE 21.** Experimental prototype of the single-phase dual active bridge DC-DC converter.



**FIGURE 22.** Experimental results at  $k_g = 1.4$  for load resistance  $R = 11\Omega$ .



**FIGURE 23.** Experimental results at  $k_g = 1.7$  for load resistance  $R = 11\Omega$ .

The ESR of the capacitor can increase significantly than its normal value with prolonged usage [46]. There is a significant difference in the critical gain  $k_{cg}$  when the output filter capacitor ESR is higher (0.45  $\Omega$ ). The error in the predicted critical gain conventional DTM, lossless DTM is more than 50%. The contribution of this paper is again explained in the next section with the theory, simulation, and experimental results.

## **VII. DISCUSSION**

The TTSM for the PSBDAB converter is proposed in this paper. The procedure to obtain the LSM and SSM is simpler than the conventional DTM. The conventional DTM



**FIGURE 24.** Experimental results at  $k_g = 0.54$  for load resistance  $R = 22\Omega$ .



**FIGURE 25.** Experimental results at  $k_q = 0.6$  for load resistance  $R = 22\Omega$ .

presented in (16) comprises an exponential matrix, results in a complicated model. The complex model obtained from DTM fails to give insightful information about the converter's behavior. Moreover, the segregation of the state variables (transformer current and capacitor voltage) into fast and slow variables eases the analysis of the PSBDAB converter. The segregation into FSV and SSV helps to apply conventional mixed system-based time scale modeling to the system [41]. The segregation helps to decouple the dynamics of the transformer current given by (22) and (23), and capacitor voltage given by (26) and (27). Each of the state variable's behavior has been obtained separately, which eases the analysis of the system.

The proposed modeling in this paper incorporated deadtime, core-loss of the external inductor, and other kinds of converter's non-linearity. The inclusion of the dead-time improves the model's steady-state, LSM, and SSM. It can be seen from Fig. 6 that the inclusion of the dead-time improves the steady-state. Fig. 8 and 9 depict the improved accuracy of the proposed model compared with the other existing methods. Moreover, the inclusion of the core loss of the inductor improves the model accuracy at the light and heavy load operation of the system, as seen from Fig. 6 to 10.

The effect of the circuit parameters such as load resistance, the equivalent resistance of the model, the equivalent inductance of the model, output capacitor filter capacitance, and its ESR on the stability of the system are shown in Fig. 11 to 18. It has been observed that the load resistance

Model	Case I	Case II	Case III	Case IV	Case V	Case VI	Case VII	Case VIII
	$R_c = 0$	$R_c = 0.15$	$R_c = 0.45$	$C = 132 \mu F$	$r=0\;\Omega$	$L = 98 \mu H$	$R=22\Omega$	$V_{ref} = 38 V$
Conventional Discrete-time model [24]	1.62	1.62	1.62	1.27	1.45	0.93	0.6	0.93
Bilinear Discrete-time model [23]	1.62	1.35	0.88	1.11	1.39	0.84	0.57	0.87
Lossless time-scale model [27]	1.45	1.45	1.45	1.15	1.45	0.91	0.61	0.93
Proposed time-scale model (TTS)	1.71	1.37	0.86	1.12	1.39	0.83	0.56	0.86
Simulation model	1.76	1.38	0.85	1.13	1.39	0.83	0.56	0.86

TABLE 2. Comparison of the different critical gain top ensure stable operation of the system.

TABLE 3. Comparative study of different modeling strategies for PSBDAB converter.

Type of Model	Order of Model	Stead-state accuracy	Core-loss	Stability analysis	Dead-time
GAM [18]	Full-order	Low	Х	х	х
Ideal AVM [14]	Reduced-order	Low	Х	х	х
Non-ideal AVM [7]	Reduced-order	Good	Х	х	Х
FSM [12]	Reduced-order	Good	Х	х	$\checkmark$
Conventional DTM [3] [24]	Full-order	Not Discussed	Х	х	х
Bilinear DTM [23]	Full-order	Not Discussed	X	$\checkmark$	х
Proposed TTSM	Full-order	Best	$\checkmark$	$\checkmark$	$\checkmark$

of the converter has affected the nature of the transformer current more predominantly than the other circuit parameters, as shown in Fig. 17.

The comparative studies of the proposed TTSM and models developed in the literature for the steady-state, LSM, SSM are shown in Fig. 6, 8 and 9 & 10, respectively. Moreover, the comparative studies for the stability prediction among the discrete-time models are presented in Table 2. The characteristics of different modeling in the literature compared to the proposed model are listed in Table 3. The proposed model has the best accuracy among the full-order and the reduced-order model with RMSPE around half of a percent. The proposed model gives the best stability prediction compared to the existing literature on the stability analysis of the PSBDAB converter.

### **VIII. CONCLUSION**

This paper proposes a mixed system-based time-scale methodology of the phase-shifted bidirectional dual active bridge converter. The state variable of the PSBDAB converter (transformer current and capacitor voltage) are termed as fast and slow states. The separation of the fast and slow variables based on their inherited characteristics results in the decoupling of the state variable, which simplifies the analysis of the system. The steady-state, open-loop response, and frequency response (small-signal) of the output voltage is verified with experimental results. The inclusion of the dead-time and core-loss of the inductor in the model has been studied. The inclusion of the dead-time of the semiconductor devices and core-loss of the external inductor improves the model's overall accuracy at the light and heavy load operation. The proposed model can accurately predict the output power flowing through the system. The output voltage open-loop response with a variation in the control variable is verified with hardware results. The open-loop behavior from the proposed model is also compared with the existing model presented in the literature. The proposed model gives the closest behavior compared to the behavior obtained from the actual prototype. Similar to steady-state and the open-loop response, the control to output voltage frequency response from the proposed model provides the best accuracy than the other models. A detailed study about the stability of the closed-loop system with variation in circuit parameters is established. The critical gain to ensure the converter stays in the stable region is obtained and verified in the simulation and experimental setup.

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