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7L-SCBI topology with minimal semiconductor device count

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Abstract: In this work, a seven-level switched capacitor boost inverter (7L-SCBI) is proposed with minimal resource count. The proposed inverter requires only eight switches and two capacitors to generate a seven-level voltage. The proposed 7L-SCBI is capable of generating a multilevel voltage as well as boost the input DC-link voltage up to 1.5 times with a reduced blocking voltage of switches and capacitors. The comparison in terms of efficiency and device count with other switched capacitor topologies is presented in detail. The performance validation of the proposed 7L-SCBI is done with the help of a laboratory prototype.

1 Introduction

In high-power and high-voltage applications, the multilevel inverters (MLIs) are gaining remarkable interest in the industry as well as academia from the last three decades over two-level inverters. The MLIs have numerous advantages such as reduced dv/dt stress of the switches; improved power quality of the output voltages w.r.t. increased number of levels and minimised harmonic profile; reduced filter requirement; lower Electromagnetic interference (EMI) issues; minimised common-mode voltages etc. [1–3]. The renowned existing MLI configurations are namely, cascaded H-bridge (CHB), neutral point clamped (NPC), flying capacitor clamped (FCC), dual inverter (DI) and T-type-based MLIs. Even though these MLIs have several advantages, however they also have limitations of device count as the number of levels increases (number of switches, diodes, capacitors, isolated DC sources), in addition to capacitor balancing issues [1–3].

In [3], numerous hybrid topologies such as CHB topology with floating capacitors, active NPC, hybrid topologies with a combination of either NPC with CHB or FCC with CHB, packed U-cell etc. are discussed. However, the device count and output voltage gain are the major limitations with most of the topologies. A five-level MLI with switch boost capability is proposed in [4], where nine switches were used to attain the output voltage gain of 2. In [5], another five-level inverter topology is presented with ten switches and four capacitors; however, no additional gain is achieved. In these topologies [4, 5], the flying capacitor concepts with the combination of CHB circuits have been used, resultantly, these circuits require a higher number of devices. A new family of seven-level switched boost topologies has been presented in [6], with the help of CHB and T-type MLI concepts. However, this configuration requires four capacitors for clamping the DC-link voltage and for boosting the voltage to 1.5 times, ten switches were required.

Several seven-level inverter topologies have been presented in [7–11], where a higher number of switching devices as well as capacitors have been used, which makes the system costly. Some topologies achieving a higher number of voltage levels have also been proposed in [12–14]. However, these topologies suffer from higher voltage ratings of components. To overcome these issues, there is a necessity to implement an optimal seven-level configuration with a minimal number of switching devices and capacitors, meanwhile achieving a boost of the applied voltage. In this paper, a seven-level switched capacitor boost inverter (7L-SCBI) topology is proposed using only eight switches. The proposed 7L-SCBI requires only one DC source (with a magnitude of V_{dc}) and two capacitors for achieving a voltage boosting capability of 1.5.

2 Proposed 7L-SCBI and analysis

The proposed 7L-SCBI configuration is represented in Fig. 1*a*. In the proposed inverter, capacitors C_1 and C_2 are used effectively to boost up the DC input voltage as well as for clamping the DC-link

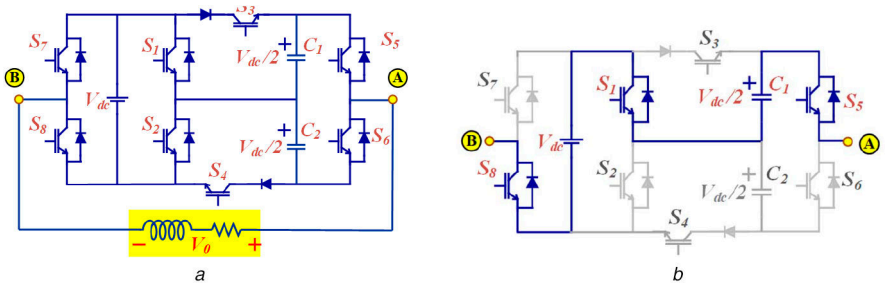


Fig. 1 *Proposed multilevel inverter configuration*
(a) 7L-SCBI, ***(b)*** Voltage state with $V_o = +3V_{dc}/2$

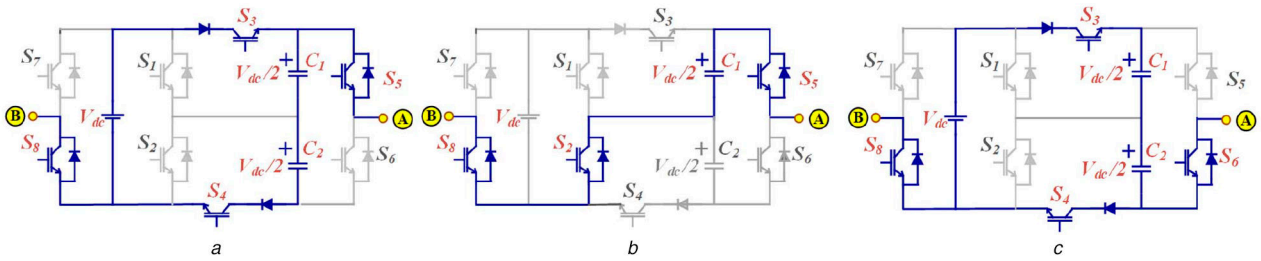


Fig. 2 *Voltage state of the proposed topology with*
(a) $V_o = V_{dc}$, *(b)* $V_o = +V_{dc}/2$ and $V_o = 0$

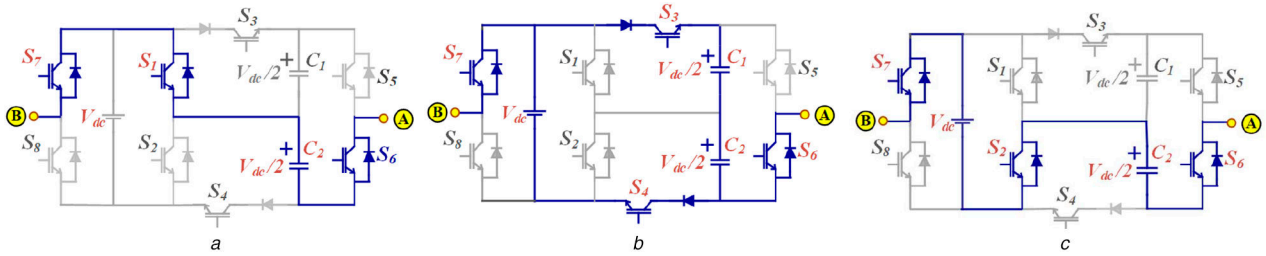


Fig. 3 *Voltage state of the proposed topology with*
(a) $V_o = -V_{dc}/2$, *(b)* $V_o = -V_{dc}$, *(c)* $V_o = -3V_{dc}/2$

Table 1 Possible switching states for proposed 7L-SCBI

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2
$3V_{dc}/2$	1	0	0	0	1	0	0	1	D	—
V_{dc}	0	0	1	1	1	0	0	1	C	C
$V_{dc}/2$	0	1	0	0	1	0	0	1	D	—
	1	0	0	0	1	0	1	0	D	—
	1	0	0	0	0	1	0	1	—	C
0	0	0	1	1	0	1	0	1	C	C
	0	0	1	1	1	0	1	0	C	C
$-V_{dc}/2$	1	0	0	0	0	1	1	0	—	D
	0	1	0	0	0	1	0	1	—	D
	0	1	0	0	1	0	1	0	C	—
$-V_{dc}$	0	0	1	1	0	1	1	0	C	C
$-3V_{dc}/2$	0	1	0	0	0	1	1	0	—	D

C = charging of capacitors; D = discharging of capacitors.

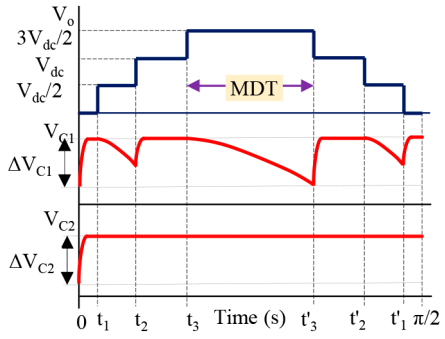


Fig. 4 *Capacitor voltage variation in worst condition*

voltage into two equal magnitudes. The two-switch inverter legs connected to the DC link will generate 0, V_{dc}, $-V_{dc}$ voltage levels and the capacitors branch along with clamping switches will generate $V_{dc}/2$, $-V_{dc}/2$, V_{dc}, $-V_{dc}$. As a result, the proposed 7L-SCBI is able to generate a 7L voltage across the load terminals (A and B). Conclusively, the levels $3V_{dc}/2$, V_{dc}, $V_{dc}/2$, $0V$, $-V_{dc}/2$, $-V_{dc}$, $-3V_{dc}/2$ are achieved here. The equivalent circuit for all the possible switching states for generating the 7L voltages across the load terminals A and B is shown in Figs. 1*b*, 2 and 3 as well as in Table 1.

The capacitors C_1 and C_2 are charged to $V_{dc}/2$ voltage equally by connecting this combination in parallel with the DC input source during the states of 0, V_{dc}, $-V_{dc}$ levels. Due to the higher number of switching state redundancies of the proposed 7L-SCBI, the charging of capacitors can also be done by connecting the individual capacitors in series with the DC source and load, i.e. C_1 is charged during $-V_{dc}/2$ level and C_2 is charged during $+V_{dc}/2$ level. From the switching Table 1 and Figs. 1–3, it can be observed that the capacitors are charged and discharged symmetrically which ensures that the capacitors are self-balanced. From Table 1, it can be observed that $+V_{dc}/2$ and $-V_{dc}/2$ voltage levels have a higher number of switching redundancies, which help in achieving the capacitor voltage balancing under disturbances or unbalanced conditions.

3 Determination of capacitance value

The selection of capacitance value for any capacitor has a significant role in the switched capacitor-based MLI topologies. In the proposed topology, only one capacitor is used in a one half-cycle, which gives a better voltage profile. The ratings of switched capacitors used in the MLI topologies are mainly depending on the capacitor voltage ripple, i.e. ΔV_c. Fig. 4 shows the output voltage along with the capacitor voltages when the carrier signals are replaced by a constant line. As depicted in Fig. 4, the maximum discharging time for capacitor C_1 is t_3 to t_3'. The capacitor C_2 is not

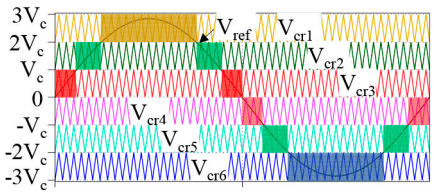


Fig. 5 *Level shifted PWM technique for seven level*

Table 2 ON state switches for each level

Logic	ON state switches	V_o
$V_{ref}>V_{cr1}$	S_1, S_5 and S_8	$3V_{in}/2$
$V_{cr1}>V_{ref}>V_{cr2}$	S_3, S_4, S_5 and S_8	V_{in}
$V_{cr2}>V_{ref}>V_{cr3}$	S_2, S_5 and S_8	$V_{dc}/2$
$V_{cr3}>V_{ref}>V_{cr4}$	S_3, S_4, S_6 and S_8	0
	S_3, S_4, S_5 and S_7	
$V_{cr4}>V_{ref}>V_{cr5}$	S_1, S_6 and S_7	$-V_{dc}/2$
$V_{cr5}>V_{ref}>V_{cr6}$	S_3, S_4, S_6 and S_7	$-V_{in}$
$V_{cr6}>V_{ref}$	S_2, S_6 and S_7	$-3V_{dc}/2$

Table 3 Comparison of the propsoed MLI

[7]	[6]	[7]	[9]	[10]	[11]	[12]	[13]	[*P*]
N_L	7	7	7	7	7	9	9	**7**
N_{sw}	10	10	9	9	10	17	10	**8**
N_d	0	0	0	0	0	0	0	**0**
N_{gd}	8	8	9	9	8	14	9	**8**
N_c	4	3	1	1	4	5	2	**2**
TSV	8	8	8	7	11	10	11	**7**
MBV	1	1.5	1	1	2	1	1	**1**
VB	✓	✓	✓	✓	✓	×	×	✓
gain	1.5	1.5	1.5	1.5	1.5	1	1	**1.5**

$N_L/N_{sw}/N_d/N_{gd}//N_c$ = number of levels/switches/diodes/gate drivers/capacitors; TSV = total standing voltage; MBV = maximum blocking voltage; VB = voltage boosting ability.

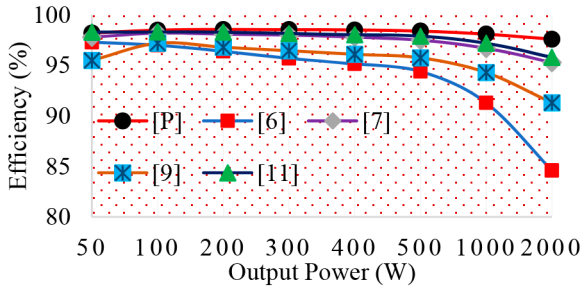


Fig. 6 *Efficiency comparison*

discharged during the positive half-cycle. During the negative half-cycle, the capacitor C_2 is discharged and the voltage of the capacitor C_1 does not change. Therefore, based on capacitor ripple voltage, the value of capacitance is given as

$$C_1 = C_2 = \frac{I_{pk}}{(\Delta V_C \times f_o)} \quad (1)$$

where I_{pk} is the peak load current and f_o is the output voltage frequency.

4 Modulation strategy

The proposed topology is modulated with the level-shifted pulse width modulation (LS-PWM) technique. In this LS-PWM for generating a seven-level voltage, six carrier signals (of magnitudes V_c) are compared with the sinusoidal reference signal as shown in Fig. 5. The control logic for different switches present in the proposed topology is generated according to the switching logic given in Tables 1 and 2.

5 Comparative study

To prove the superiority of the proposed inverter, a detailed comparative study of this inverter is done with other existing conventional inverters in terms of the number of devices, voltage stresses and other parameters for the different 7L topologies. Table 3 gives a detailed device comparison of the different SCBI topologies when compared to the proposed topology. Similar to the proposed MLI configuration, the topologies in [6, 7, 9–11] are capable of generating the 7L voltage as well as voltage boost capability of 1.5, but these topologies require a higher number of switching devices with higher values of total standing voltage (TSV). The topologies in [12, 13] can generate a nine-level output, but these topologies lack the boosting feature. Table 3 is evident that the proposed 7L topology gives a better design in terms of all aspects as compared to other topologies.

For analysing the efficiency comparison, in this work, the switched capacitor MLI topologies are considered which are having similar features such as 7L voltage with a gain of 1.5, as illustrated in Fig. 6. The proposed 7L topology has higher efficiency as compared to all other topologies due to the lower number of components used, i.e. switches as well as capacitors which result in reduced losses. In addition, as only one capacitor is used for each half-cycle a fundamental period will result in the reduction of ripple losses associated with the capacitors. From Fig. 6, it is observed that the proposed topology gives higher efficiency for different ratings of the output power as compared to the topologies in [6, 7, 9, 11].

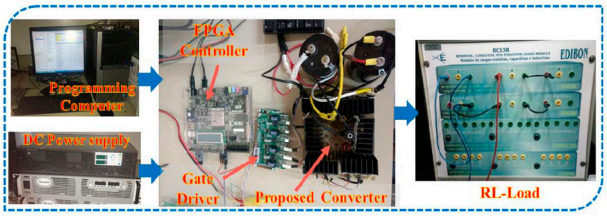
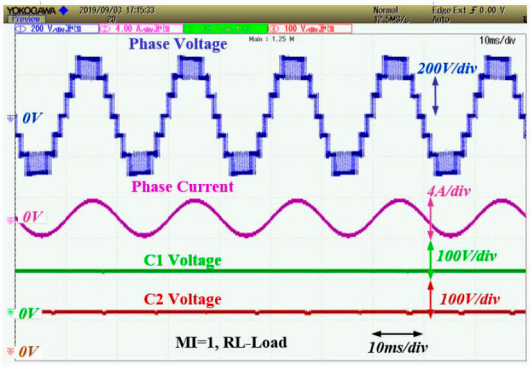


Fig. 7 *Experimental prototype of the proposed 7L-SCBI*

Table 4 Experimental prototype parameters

Parameters	Ratings or value
input voltage	200 V
switching frequency	5 kHz
modulating frequency	50 Hz
load resistor and inductor	150 Ω, 80 mH
capacitors	PG6DI, 450 V and 2200 μF



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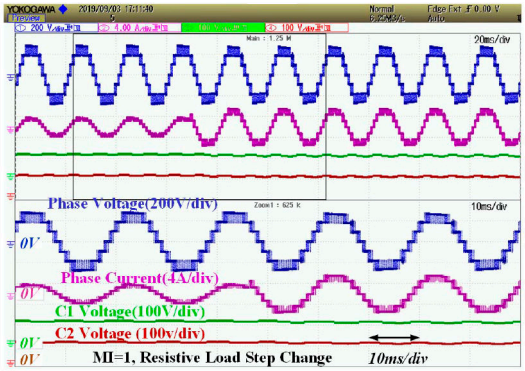


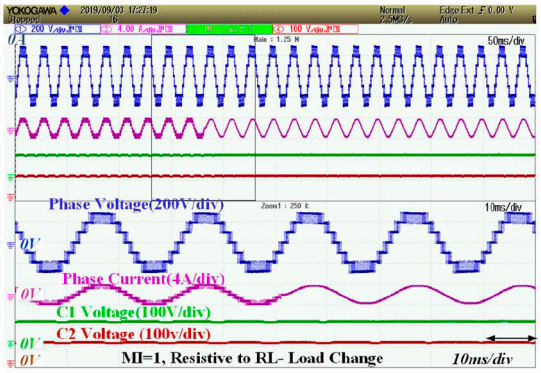
b

Fig. 8 *Experimental results with*
(a) RL load (150 Ω and 80 mH), ***(b)*** Step change in R-load

6 Results and discussion

The proposed 7L-SCBI is validated experimentally by using the laboratory prototype, as shown in Fig. 7. The parameters used for validating the experimental prototype are described in Table 4. The control logic pulses for proposed 7L-SCBI are generated with the help of Field Programmable Gate Array (FPGA) Vertix-5, XC5VLX50T controller. For avoiding the short-circuit possibilities of the DC source, 2 μs delay is provided between the complementary switches S_7 and S_8, S_5 and S_6.

The experimental result of the proposed 7L-SCBI with the resistive + inductive load (RL-Load, 150 Ω and 80 mH) is illustrated in Fig. 8*a*. The output voltage peak magnitude is 300 V for a given input voltage of 200 V, i.e. the boost factor is 1.5 as shown in Fig. 8*a*. The capacitors C_1 and C_2 are charged to 100 V equally, which is half of the input DC-link voltage. The experimental results of the proposed 7L-SCBI under the step change in the R-Load, i.e. two R-Loads (two 150 Ω loads) connected in parallel are given in Fig. 8*b*. The peak of the load



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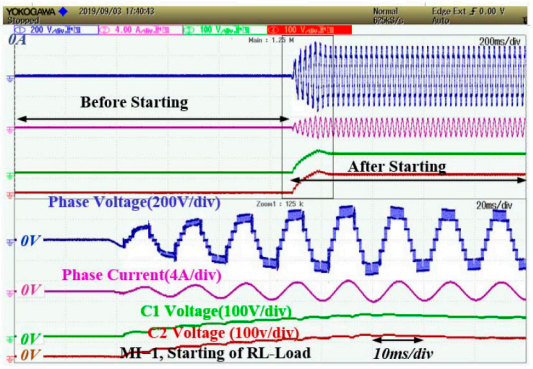

b

Fig. 9 *Experimental results with*
(a) Load change from 150 to 150 Ω + 80 mH, ***(b)*** Starting condition

current changes from 2 to 4 A which can be clearly observed from Fig. 8*b*. In this figure, zoomed version of the output voltage and currents is also presented.

The experimental results of the proposed inverter with the change in power factor (changing the load from R-Load to RL-Load) are shown in Fig. 9*a*. From this figure, it can be seen that with the R-Load the power factor is unity, after switching the load to RL-Load the power factor is reduced to 0.986 lagging [$\cos(X_L/R)$]. The experimental results during the starting time of the proposed 7L-SCBI prototype are presented in Fig. 9*b*. This figure is evident that the capacitors are charged slowly from 0 to 100 V in the first few cycles. During this time, the transients in output current and voltage of the inverter are minimal. It also shows that the proposed topology does not require any pre-charging circuit for the capacitors, and they are self-balanced without any auxiliary circuit.

7 Conclusion

A 7L-SCBI configuration is presented in this paper with the significant advantages that are essential for PV and fuel cell applications, such as voltage boosting capability, multilevel output voltage with the minimum order of switching device and passive components, and higher efficiency. At the output side, for achieving the voltage boost factor of 1.5 from the given input DC voltage the proposed inverter requires only two capacitors and eight power switches (voltage blocking rating is $\leq V_{dc}$). The experimental results are evidence for better performance under various operating conditions.

8 Acknowledgments

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