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Review on State-of-the-Art Unidirectional Non-Isolated Power Factor Correction Converters for Short-/Long-Distance Electric Vehicles

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ABSTRACT Electrification of the transportation sector has originated a worldwide demand towards green-based refueling infrastructure modernization. Global researches and efforts have been pondered to promote optimal Electric Vehicle (EV) charging stations. The EV power electronic systems can be classified into three main divisions: power charging station configuration (e.g., Level 1 (i.e., slow-speed charger), Level 2 (i.e., fast-speed charger), and Level 3 (i.e., ultra-fast speed charger)), the electric drive system, and the auxiliary EV loads. This paper emphasizes the recent development in Power Factor Correction (PFC) converters in the on-board charger system for short-distance EVs (e.g., e-bikes, e-trikes, e-rickshaw, and golf carts) and long-distance EVs (passenger e-cars, e-trucks, and e-buses). The EV battery voltage mainly ranges between 36 V and 900 V based on the EV application. The on-board battery charger consists of either a single-stage converter (a PFC converter that meets the demands of both the supply-side and the battery-side) or a two-stage converter (a PFC converter that meets the supply-side requirements and a DC-DC converter that meets the battery-side requirements). This paper focuses on the single-phase unidirectional non-isolated PFC converters for on-board battery chargers (i.e., Level 1 and Level 2 charging infrastructure). A comprehensive classification is provided for the PFC converters with two main categories: (1) the fundamental PFC topologies (i.e., Buck, Boost, Buck-Boost, SEPIC, Ćuk, and Zeta converters) and (2) the modified PFC topologies (i.e., improved power quality PFC converters derived from the fundamental topologies). This paper provides a review of up-to-date publications for PFC converters in short-/long-distance EV applications.

INDEX TERMS AC-DC converter, battery charger, charging infrastructure, DC-DC converter, electric vehicle, power factor correction.

NOMENCLATURE

CICM	Continuous Inductor Current Mode.
DBR	Diode Bridge Rectifier.
DICM	Discontinuous Inductor Current Mode.
DCVM	Discontinuous Capacitor Voltage Mode.
EV	Electric Vehicle.
V2G	Vehicle-to-Grid.
V2H	Vehicle-to-Home.
V2V	Vehicle-to-Vehicle.
V2B	Vehicle-to-Building.
V2X	Vehicle-to-Everything.
EVSE	EV supply Equipment.
PFSM	Power Flow and System Management.
PQDM	Power Quality and Devices Management.
PFC	Power Factor Correction.

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I. INTRODUCTION

The automotive sector's electrification empowers sustainable energy sources and mitigates noise and air pollution (i.e., diminishing dependence on conventional refueling infrastructure) [1]. According to the International Renewable Energy Agency (IRENA) analysis, it is predicted that

one billion Electric Vehicles (EVs) will be deployed on the roads by 2050, a growth of 200,000% compared to a decade ago [1]. In the past decade, China, United States, and the European markets had the largest share in light-duty EVs (i.e., cars and vans) sales. However, the penetration of heavy-duty EVs (i.e., e-buses and e-trucks) has been pinpointed in China with potential growth in other regions. Besides, the short-distance EVs category (i.e., e-bikes, e-trikes, and e-rickshaw) are emerging and competing against their conventional EVs [1]–[4].

A. ELECTRIC VEHICLES: CONTEMPORARY DEVELOPMENT

The penetration of EVs is expected to be on a high rise in the following decades, and by 2050, some countries such as Norway, Netherlands, France, United Kingdom, Japan, and China are planning to halt their fuel-based vehicle industry [1]. In the meantime, continuous technological development is anticipated in batteries technologies (e.g., high driving range and battery swapping), the maturity of smart charging (Vehicle-to-Grid (V2G), Vehicle-to-Home (V2H), Vehicle-to-Vehicle (V2V), Vehicle-to-Building (V2B), and Vehicle-to-Everything (V2X)), fast-charging stations (e.g., power up to 600 kW), and the ancillary power services provided by the EVs (e.g., peak load management, smart charging incentives, and EVs demand realization by renewable sources production) [1], [5].

EVs were introduced in the early 1800s; yet, in the last decade, despite EVs' sales over-estimation, the growing attention on clean energy and development of the energy storage technologies have advanced the global markets and governments towards the penetration of EVs [3], [5], [6]. Lithium-ion (Li-ion) battery-based EVs are the popular trend in markets due to their high energy density. Throughout the last 20 years, the price of Li-ion battery has fallen from US$ 1,000 per kWh to US$ 120 per kWh, while the energy density has improved from 90 Wh/kg to 300 Wh/kg (i.e., upgraded driving range distance) [5], [6]. Range anxiety represents a barrier against customers' purchase of EVs, and the up-to-date available practical driving range is around 620 miles/charge [7]. Li-ion and other types of batteries are in the evaluation and study phase to allow adaptation of mixed battery types in different highly-utilized automotive markets (e.g., trucks, trains, and buses) [6], [8]. In addition, intensive research has been pioneered towards battery management to estimate the batteries' State-of-Charge (SOC), State-of-Health (SOH), State-of-Power (SOP), and State-of-Life (SOL) in the EV application. These factors play an essential role in securing extended battery life, reduced operating cost, improved driving range, and avoidance of over-charge and over-discharge issues [9]–[12]. An illustration of the EV's battery charging speed (ideally) versus time and the SOC is presented in FIGURE 1 [13]. Besides, the lack of public charging infrastructure is another obstacle, which encompasses grid-connected and renewable sources-connected fast-charging stations.

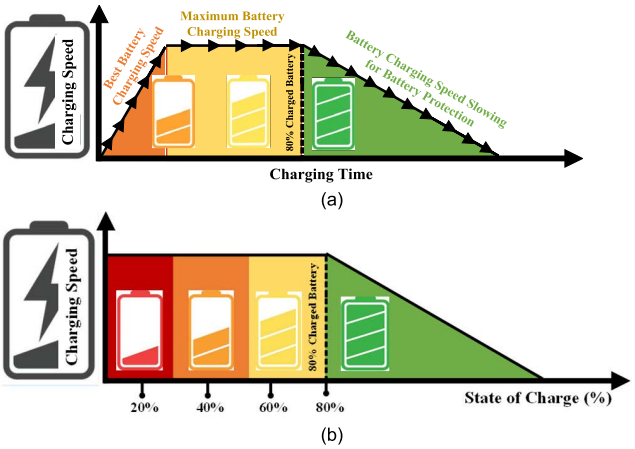

FIGURE 1. EV's battery charging speed versus (a) charging time and (b) state of charge.

B. ELECTRIC VEHICLES CHARGING INFRASTRUCTURE: CHALLENGES

The challenges in the EV charging infrastructure can be broadly layout into two main sectors: grid/charging station power management (i.e., Power Flow and System Management (PFSM) sector) and charging station power electronics (i.e., Power Quality and Devices Management (PQDM) sector). The challenges and issues related to each sector are declared in TABLE 1 [1]–[8], [14]–[20]. This paper focuses on the problems related to the power quality management part in EV charging infrastructure, specifically, the Power Factor Correction (PFC) converter in AC-based distribution network (i.e., the front-end AC-DC and DC-DC converter stages).

C. POWER FACTOR CORRECTION (PFC) CONVERTERS

In the last two decades, numerous on-board PFC converter topologies and design approaches have been devised for EV charging applications [4], [8], [10], [14], [17], [21], [22]. Unidirectional chargers offer simple and low-cost converter power flow, long battery life (i.e., avoidance of discharge), and moderate gird support (e.g., reactive power support) with minimized power infrastructure updates [14], [22]. On the other hand, bidirectional chargers involve advanced adjustments and coordination between the grid, charging station, and EV fleets [14], [22]. On-board chargers supply the EV's battery through a single-phase (i.e., Level 1 or Level 2 EV charging infrastructure) or three-phase supply (i.e., Level 2 EV charging infrastructure) that can be available in private locations (e.g., private residential houses), as presented in FIGURE 2. While the off-board charger (i.e., Level 3 EV charging infrastructure) is located in public charging stations, allowing fast or ultra-fast charging [5], [10], [14], [17], [19].

Active PFC converter is suitable for non-linear loads [23]. The PFC stage for the on-board charger consists of two conversion stages, an AC-DC converter (e.g., a Diode Bridge Rectifier (DBR)) and a single-stage isolated or non-isolated DC-DC converter [5], [22]. A single-stage non-isolated

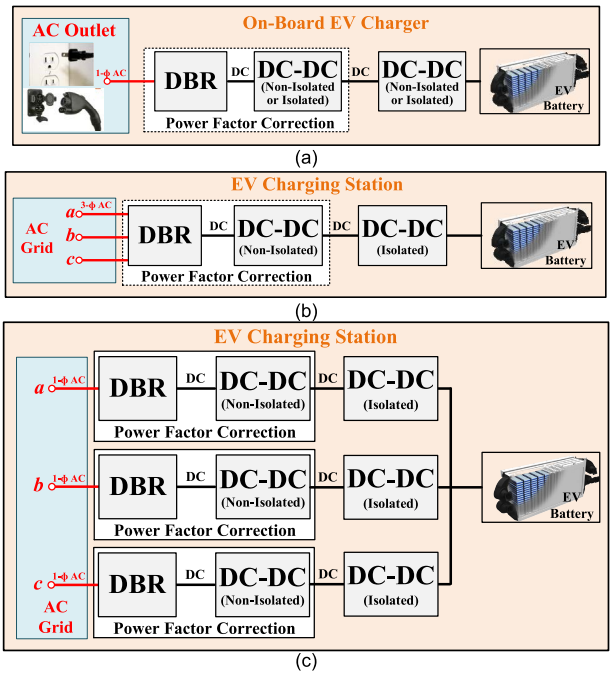

FIGURE 2. The conventional EV charging station in (a) single-phase configuration, (b) direct three-phase configuration, and (c) phase modular configuration.

DC-DC converter is feasible with the EV charging application due to the battery's floating ground with the EV body [24]. Also, the EV charging standards do not impose any obligation for the isolation interface [24]. Besides, a two-stage converter configuration for the EV charging is feasible by the DBR integration with an isolated or non-isolated DC-DC converter, a PFC converter as the first stage, which realizes the supply-side requirements. This is commonly followed by an isolated or non-isolated DC-DC converter, the second conversion stage, that attains the battery-side requirements, such as controlling the battery charging speed and providing an isolated or non-isolated interface between the grid and the battery, as shown in FIGURE 2(a) [22]. Meanwhile, the first DC-DC converter integrated with the DBR acts as a PFC converter to suppress the current harmonics injection and provide a near-unity power factor (*pf*) and low Total Harmonic Distortion (THD). The AC-DC conversion solely with a DBR and a bulky output capacitor is not practical for EV charging due to AC mains non-unity *pf*, high THD, and large DC-filter size [21].

Three-phase input active PFC systems can be achieved in two main converter configurations, direct three-phase configuration and phase modular configuration [23]. The former type (FIGURE 2(b)) is not practical as the PFC converter typically has a single fully-controlled semiconductor device that cannot unfold the three-phase signals. While in the latter type, the modular phase configuration (FIGURE 2(c)), each phase has a separate PFC converter and DC-DC converter stages. A single-phase active PFC converter configuration

TABLE 1. Challenges in the EV charging infrastructure.

Challenges and Issues	
Smart-controlled vehicle charging management:	**References**
1. Bidirectional and unidirectional charging management for V2G, V2H, V2V, V2B, and V2X power flow.	[1],[2],[5],[13],[14], [16],[19]
2. Optimal EV fleet charging patterns (e.g., considering charging location, charging speed, battery capacity and state of charge, vehicle type, and driving range) for monetary incentives.	[1],[2],[8],[15],[18], [19]
3. Smart charging interface for users for flexible and ease EV charging.	[1],[15]
4. Data collection and pattern forecasting for congestion management.	[1],[8],[15],[18]
5. Power-sharing among extreme-fast charging stations for robust charging infrastructure.	[1],[5],[8]
Distribution network management:	**References**
1. Voltage and frequency control for network stability during steady-state and dynamic conditions.	[1],[8],[15],[19]
2. Management of renewable sources in islanded micro-grids for intermittent power supply.	[1],[15],[17],[19]
3. Load and energy storage management for optimal supply utilization (e.g., peak shaving).	[1],[2],[8],[15],[17]
4. Cybersecurity and communication protection protocols.	[1],[8],[15]
Charging station design and management:	**References**
1. Charging cable interface (e.g., conductive charging and inductive charging).	[1],[13],[14],[20]
2. Energy storage technologies for back-up supply.	[1],[2],[17],[19]
3. Battery technologies, performance, and swapping.	[1],[3],[6],[8],[9], [11]-[14],[17],[19]
4. Grid-connected front-end converter (i.e., AC-DC) performance, efficiency, and cost.	[1],[2],[5],[8],[10], [14],[17],[21],[22]
5. Battery-side converter (i.e., DC-DC converter) performance, efficiency, and cost.	[1]-[3],[5],[8],[10], [14],[17],[21],[22]
6. Customer-side protection and safety.	[1],[2],[5],[7],[8]

(FIGURE 2(a)) is a typical structure for the on-board EV chargers in Level 1 and Level 2 charging infrastructure.

The conventional PFC converters for EVs charging employ the boost topology cascaded with a DBR. Besides, improved versions have been proposed (e.g., bridgeless boost, interleaved boost, and bridgeless interleaved boost topologies) to accommodate power levels above 3.5 kW [25]. In addition, the technological development in wide bandgap devices (e.g., Gallium Nitride (GaN) and Silicon Carbide (SiC)) advances the deployment of efficient PFC converters for high-power operating ranges [26]. The multilevel converters are commonly endorsed for Level 3 charging infrastructure. Also, the multilevel topology has been suggested for single-phase chargers, but at the cost of increased switching devices [14].

D. FOCUS AND CONTRIBUTION

EVs span a broad range of applications. It can be categorized in this paper into two main types: low-voltage battery EV applications (e.g., e-bikes, e-trikes, and e-rickshaw) with the battery voltage in the range of 36 V-120 V (i.e., low-speed EVs) and medium-voltage battery applications (e.g., passenger e-cars, e-trucks, and e-buses) with the battery voltage in the range of 230 V- 900 V (i.e., high-speed EVs) [7], [24].

TABLE 2. Examples of the available EV products in the market (e-bikes, passenger e-cars, and e-buses) and their battery characteristics.

EV (Mobility Type)	Battery Capacity	Driving Range	Battery Voltage	Charging Time*
Allant + 9.9S (e-bike) [27]	0.625 kWh 16.7 Ah	60 miles/charge	36 V	10.17 hour
Stromer ST3 (e-bike) [28]	0.814 kWh 15.9 Ah	87 miles/charge	48 V	10.33 hour
Gazelle C8 HMB (e-bike) [29]	0.5 kWh 13.4 Ah	43 miles/charge	36 V	10.15 hour
BMW i3s (e-car) [30]	42.2 kWh 120 Ah	153 mile-charge	352 V	9.53 hour
Tesla Model V 100D (e-car) [31]	100 kWh 285 Ah	295 miles/charge	350 V	17.40 hour
KIA Soul (e-car) [32]	64 kWh 180 Ah	243 miles/charge	356 V	11.07 hour
Design Line Eco-Smart I (e-bus) [33],[34]	262 kWh 78 Ah	99 miles/charge	Not Reported	NA for Level 1**

*The charging time is based on charging current 10% of the Ah battery rating limited to not exceeding 16 A (for Level 1 charging infrastructure), initial SOC 1%, and final SOC 100%.
**E-buses are charged in Level 2 and Level 3 EV charging infrastructures [34].

On-board chargers for the EVs are required for Level 1 and Level 2 charging infrastructure, where a single-phase source can be the power supply to the charger (i.e., the input AC voltage to the charger can be between 120 V-240 V). Based on the input AC voltage level, the on-board charger steps up/down the DC voltage to match the battery DC voltage level. This paper considers various battery voltage levels between 36 V-900 V with input AC voltage level between 120V-240V (i.e., Level 1 and Level 2 charging infrastructure). The battery capacity of the EV is directly proportional to the driving range. Therefore, low-speed EVs have less battery capacity and low driving range, yet, less battery charging time. While the fast-speed EVs have higher battery capacity and more extended driving range, yet, longer battery charging time. Hence, Level 1 and Level 2 charging infrastructure are recommended for the low-speed EVs, and Level 3 charging infrastructure is suitable for the high-speed EVs. TABLE 2 shows the battery capacity, driving range, battery voltage level, and charging time required with Level 1 charging infrastructure for different EV types [27]–[34].

Unidirectional on-board charger offers simple design and control, low cost, low maintenance, and power flow compatibility with all the charging levels (i.e., Level 1, Level 2, and Level 3 charging infrastructure) compared to the bidirectional charger [14]. A bidirectional on-board charger can be essential for economic benefits, and it is compatible with Level 2 and Level 3 charging infrastructure. This paper focuses on the unidirectional on-board chargers, while a comprehensive up-to-date review on bidirectional on-board chargers can be tackled in a separate review paper. In addition, this paper considers the non-isolated on-board charger for its simple design, low cost, high power density, and high energy density compared to the isolated topologies.

Several publications have tackled the categorization of the unidirectional non-isolated single-phase PFC converters (e.g., Buck, Boost, Buck-Boost converters, and their derivatives) [14], [25], [35]–[37], [40]. Besides, improved power quality versions of the fundamental topologies have been developed (e.g., modified bridge topologies, bridgeless topologies, interleaved topologies) either in Continuous Inductor Current Mode (CICM), Discontinuous Inductor Current Mode (DICM), and/or Discontinuous Capacitor Voltage Mode (DCVM) [17], [25], [35]–[40]. These studies focused on the converter structure, converter topology's pros and cons in terms of power quality factors, and optimal selection of the converter's components for a reduced converter size. However, an up-to-date classification, considering the recently developed unidirectional non-isolated single-phase modified PFC topologies, is unavailable. Also, these studies did not identify the battery's voltage level as a factor for appraising among the PFC converter topologies. This paper presents a categorization of the unidirectional non-isolated single-phase PFC converters and their up-to-date state-of-the-art development, their practical power quality performance (including power and voltage operating ranges), and converter topologies appraisal for EVs application (Level 1 and Level 2 EV charging infrastructures) (i.e., converter capability to process power between 0.3 kW-7 kW). Yet, the technical design analysis of the converters covered in this paper is out of the paper scope.

This paper delivers a review on the developed unidirectional non-isolated on-board PFC converters (i.e., G2V for low-speed and high-speed EVs). These EVs are run by low-voltage to medium-voltage battery packs (e.g., 36 V-900 V), and they are charged with power in the range of 0.3 kW to 7 kW in Level 1 and Level 2 charging infrastructure [7], [41]. The paper classifies the converter topologies into two main categories: fundamental PFC topologies (7 PFC topologies), modified PFC topologies (43 PFC topologies that are derived from the fundamental PFC topologies), and two main subcategories: single-stage PFC converters and two-stage PFC converters, as shown in FIGURE 3.

The main contribution of this paper is as follows.

- Capitalize the contemporary state-of-the-art single-phase PFC converters, unidirectional and non-isolated converters, towards comprehensive recommendation in the low-speed and high-speed EV (i.e., short-range and long-range mobility EV) applications, focusing on G2V integration.
- Performance evaluation for the addressed unidirectional non-isolated single-phase PFC converter topologies, practical assessment, in terms of power quality factors (e.g., power factor, THD, efficiency, and voltage and power operating ranges), cost and size.

The paper sections are organized as follows (FIGURE 4). Section II provides an overview of the three EV charging

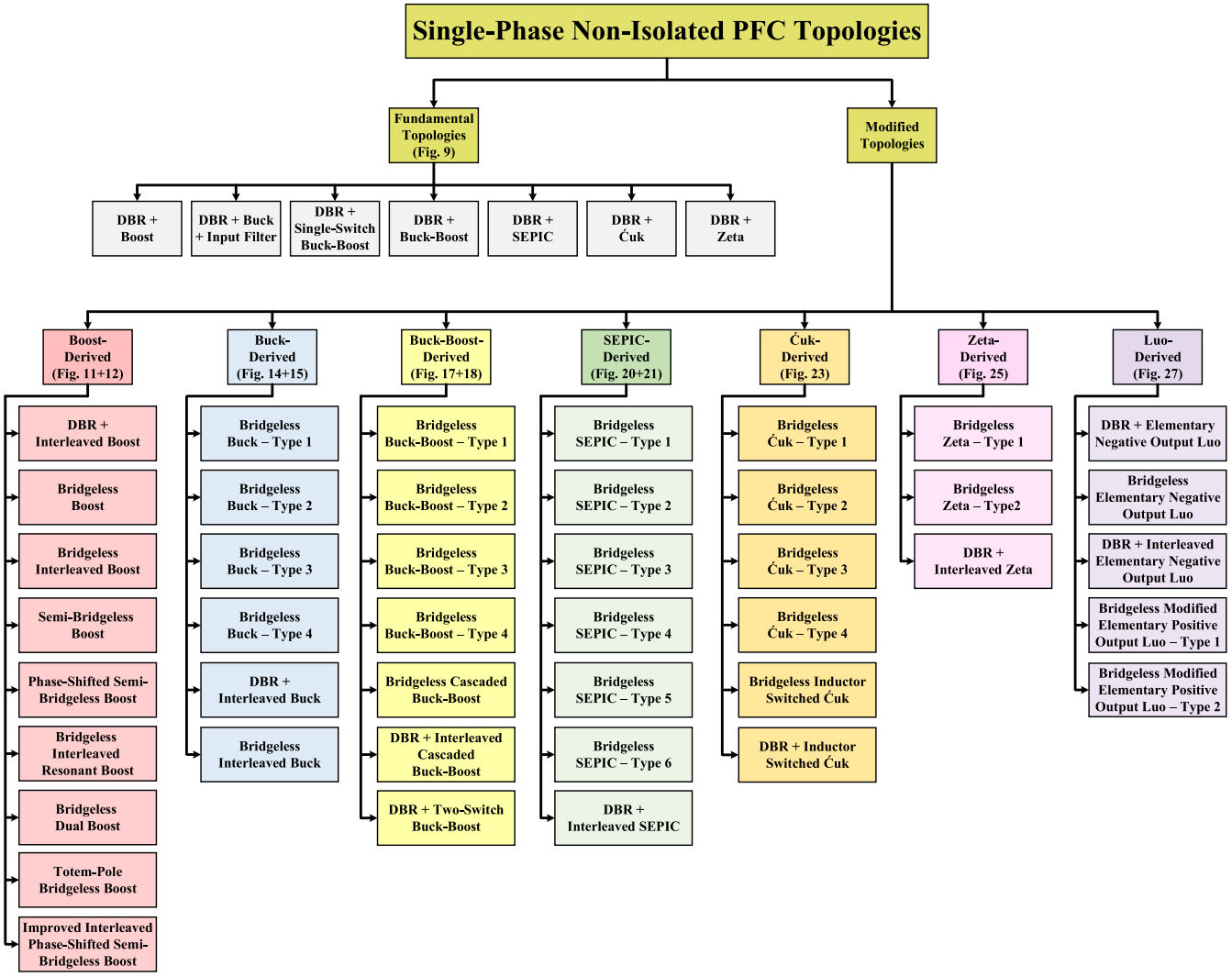

FIGURE 3. The classification of the single-phase unidirectional non-isolated PFC converter topologies in this paper.

levels infrastructure. Section III presents the power quality issues in the PFC converters for EV applications. Section IV delivers the first classification of the PFC converter, the fundamental PFC topologies. Section V presents the modified Boost-derived PFC converter topologies. Section VI covers the modified Buck-derived PFC converter topologies. Section VII covers the modified Buck-Boost-derived PFC converter topologies. Finally, Section VII provides an overall summary of the work.

II. EV CHARGING INFRASTRUCTURE: OVERVIEW OF THE 3-CHARGING LEVELS

Charging standards, workgroups, and organizations have been developed to allow flexible international EVs penetration and ease of multi-vendor integration [14], [42]. The charging standards entail three charging levels in both AC and DC distribution systems. The charging levels are classified based on the power level (i.e., power range), power type (i.e., single-phase AC, three-phase AC, or different DC voltage levels), charger location (i.e., on-board charger or off-board charger), charging speed (i.e., slow-speed, fast-speed, or extreme fast speed), and charging time [10], [13]–[17], [20]. The installation of the charging equipment is intrinsically related to the application environment. Level 1 and Level 2 AC require 120 V or 230 V and 240 V or 400 V, respectively. Meanwhile, Level 3 AC requires a voltage in a range of 208 V-600 V. Therefore, Level 1 and Level 2 can achieve home-based EV charging due to the accessibility of the conventional outlets and/or the commercialized EV Supply Equipment (EVSE). On the other hand, DC-based charging levels (Level 1 and Level 2: 200 V-450 V, Level 3: 200 V-600 V) and Level 3 AC require grid-connected supply mechanisms. The details of the maximum allowed power, voltage, and current for EV charging in the AC and DC distribution networks are clarified in TABLE 3 [5], [10], [14], [17], [19].

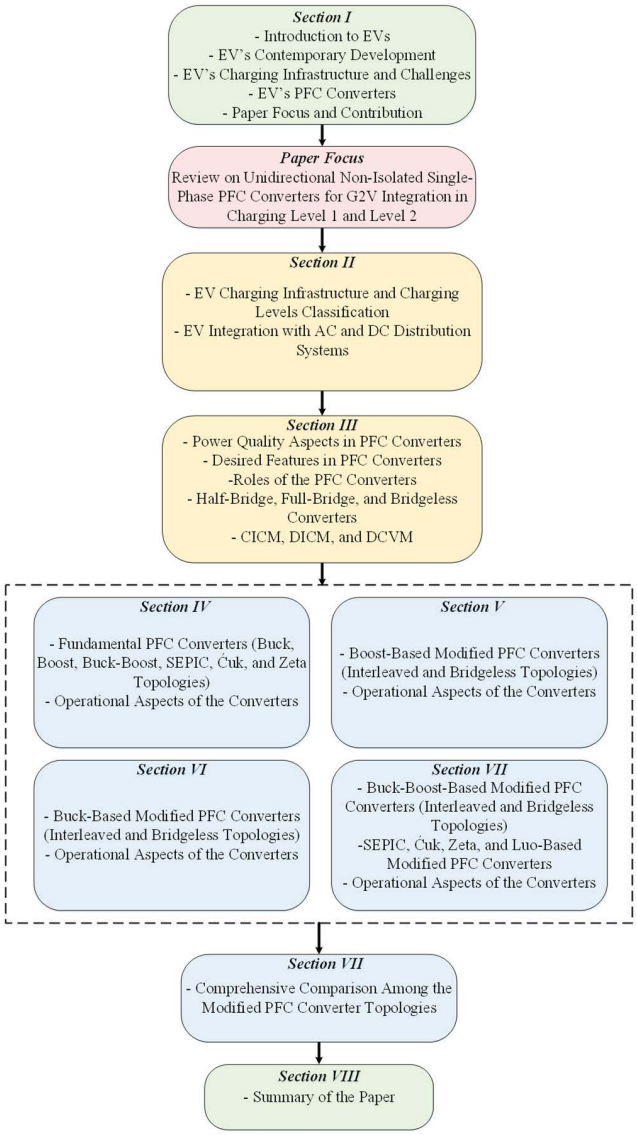

FIGURE 4. Graphical abstract of the paper.

TABLE 3. EV charging levels in AC and DC distribution grids.

Level #	Parameter	AC Grid	DC Grid
Level 1	Voltage	120 V-230 V	200 V-450 V
	Current	16 A	80 A
	Max. Power	2 kW	36 kW
Level 2	Voltage	240 V-400 V	200 V-450 V
	Current	80 A	200 A
	Max. Power	20 kW	90 kW
Level 3	Voltage	480 V-600 V	200 V-600 V
	Current	100 A	400 A
	Max. Power	50 kW	240 kW

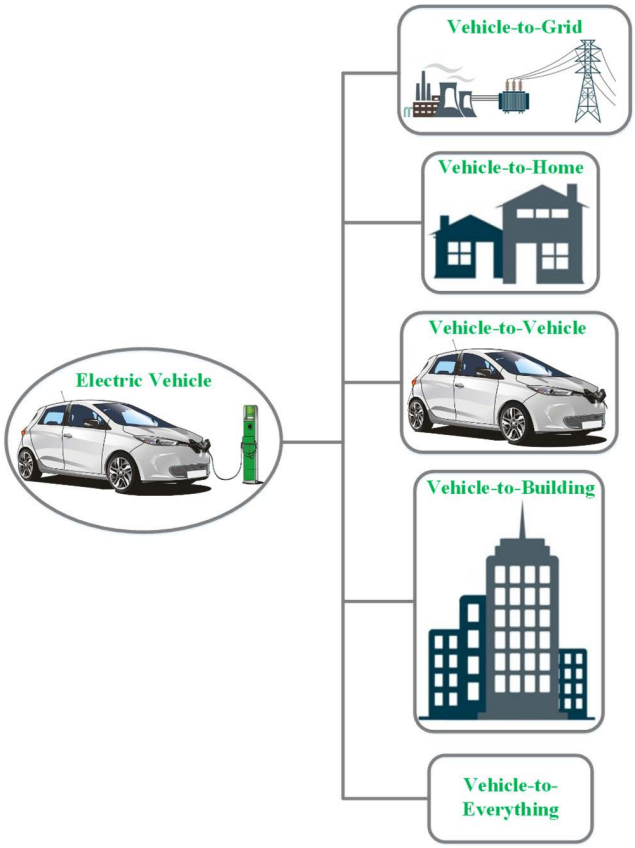

FIGURE 5. EV charging with various integrations (V2G, V2H, V2V, V2B, and V2X).

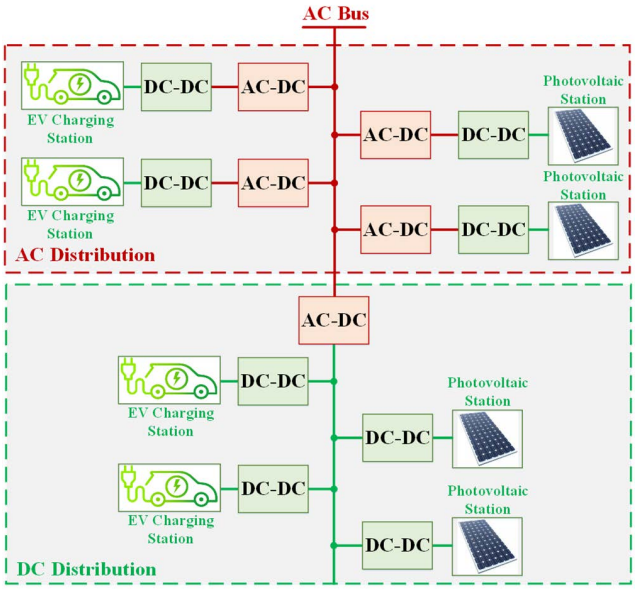

FIGURE 6. EV integration with the AC distribution and DC distribution systems.

On-board chargers can enable V2H, V2B, and V2V operation (FIGURE 5), facilitating smart charging and monetary benefits for both the customers and the grid. While off-board chargers can authorize V2G power flow (FIGURE 5), thus, providing ancillary services to the power distribution network [7], [14], [15], [18].

Today, charging stations based on the AC distribution network (FIGURE 6) is a common practice for EVs charging

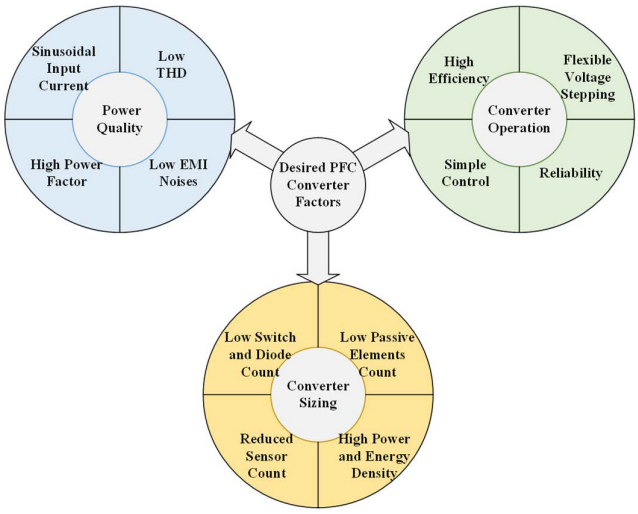

FIGURE 7. Desired design and operation aspects for a PFC converter.

infrastructure; however, the DC distribution network's (FIGURE 6) technology revolution can innovate DC-based EV charging infrastructure [5]. The AC-based power system's maturity (e.g., efficient AC-DC converter, protection, and metering) raises its reputation against DC systems. Nonetheless, a DC-based system has a reduced number of conversion stages (i.e., increased power efficiency), zero reactive power transfer (i.e., simplified control), and single-inverter interconnection with the grid (i.e., simplified islanding operation) [5]. Hence, the challenges of each system can emerge to hybrid AC and DC charging infrastructure.

III. PFC CONVERTERS: POWER QUALITY ASPECTS

The battery charger (i.e., the charging stations or charging converters) operation directly influences the battery's lifetime and charging time [14]. Besides, the PFC converters' penetration with nonlinear loads into the grid can degrade the power quality. The main desired features of a PFC converter are (FIGURE 7): continuous sinusoidal input current, low harmonics generation limited at THD $< 5\%$ (i.e. IEEE 519-2014 and IEC 61000-3-2 standards), high power factor ($pf \geq 0.9$), high efficiency ($\geq$95%) at varying load conditions and line voltage levels (i.e., IEEE 2030.1.1-2015 standard), flexible step-up and step-down chopper behavior, simplified control of input AC current and output DC voltage, reduced semiconductor devices (e.g., single-switch for a single-phase PFC), reduced passive elements, reduced filters size, reduced control sensors (e.g., DICM allows inherent unity power factor control and single control loop requirement; therefore, single sensor operation), reliability, cost-effective, reduced converter size, high power density, high energy density, reduced Electromagnetic Interface (EMI) noise (e.g., by mitigating the high-frequency harmonics generated from the switching devices, alleviating the rate of change in voltage and current signals produced due to the capacitive and inductive elements, replacing fast recovery diodes with slow diodes if applicable, and/or implementing zero crossing voltage or current for the switching devices (i.e., soft switching techniques)), and switching frequency selection based on the operating power range for cost-effective operation and filter mitigation [14], [23], [35], [43]–[45]. Usually, in high-power applications, passive and active filters are employed to meet the stringent grid requirement for power quality improvement. However, their bulky and costly nature degrades the overall system efficiency. Alternatively, in the low-power application, optimized size and controlled DC voltage, and power flow can be attained via the PFC converters [35].

The branding of the front-end AC-DC converter as a PFC converter can misrepresent its key factor integration purpose to *pf* correction, which can also be attained with a passive converter (i.e., $pf \geq 0.9$) [23]. The crucial roles of the PFC converter are THD minimization and output DC voltage control. On the other hand, the front-end passive AC-DC converter, DBR, operates as a unidirectional uncontrolled rectifier to convert the AC mains signal to an unregulated DC voltage or a bridgeless AC-DC rectification in combination with a DC-DC converter can achieve a regulated output voltage with significant losses mitigation. Brief advantages and disadvantages of the half-bridge, full-bridge, and bridgeless type PFC converters are presented in TABLE 4 [36], [38], [46]–[48].

The power quality of the PFC converter relies heavily on the practical components selection for the converter: semiconductor switches (e.g., high switching frequency for reduced components size, a limited upper frequency for inductor's magnetic losses mitigation and switching losses reduction, switch sizing based on the load current and breakdown voltage capability, and selection of the switch with minimum conduction losses for the operating power-level), inductors (e.g., selection of CICM or DICM for reliable and efficient conversion operation and size selection compromising between high-density design, ripple reduction, and fast transient response), capacitors (e.g., selection of the DCVM, selection of the output capacitor size for limited output voltage overshoot and ripples, and reduced losses with minimal internal series resistance), diodes (e.g., fast OFF/ON turn action), and control circuitry (e.g., feedback control for output regulation). PFC converters can operate in CICM, DICM, and/or DCVM. The advantages and disadvantages of each operating mode are described in TABLE 5 [38], [40], [48]–[52].

In the following sections, the PFC converter is presented in the following order: fundamental topologies, modified Boost-derived topologies, modified Buck-derived topologies, modified Buck-Boost-derived topologies, modified Single-Ended Primary-Inductor Converter (SEPIC)-derived topologies, modified Ćuk-derived topologies, modified Zeta-derived topologies, and modified Luo-derived topologies.

IV. FUNDAMENTAL PFC CONVERTER TOPOLOGIES

The conventional single-phase PFC converters for DC leveling up/down consists of the well-known fundamental topologies showcased in FIGURE 8. This category can be

TABLE 4. Comparison of the AC-DC conversion topologies.

Type	Half-Bridge	Full-Bridge	Bridgeless
Advantages	1. Reduced number of components. 2. Reduced cost. 3. Possible interleaved operation mode.	1. Reduced Components' stress. 2. Possible interleaved operation mode.	1. Elimination of DBR and simple design. 2. Improved efficiency and loss reduction. 3. Possible interleaved operation mode.
Disadvantages	1. Increased components' stress. 2. Inrush current issues. 3. Efficiency degradation & high DBR loss. 4. Bulky electrolytic capacitors requirement.	1. Increased components and cost. 2. Inrush current issues. 3. Efficiency degradation & high DBR loss.	1. Increased current stress. 2. Increased EMI filter requirement. 3. Complex input current sensing.

TABLE 5. Pros and cons of CICM, DICM, and DCVM in a PFC converter.

Type	CICM	DICM	DCVM
Advantages	1. Reduced component rating. 2. Endorsed in high-power applications. 3. Inductor current is not affected by the switch operation. 4. Simple control and high performance with the average current mode control. 5. High efficiency.	1. Endorsed in low-power applications (< 300W). 2. PFC can be inherently achieved. 3. Current shaping requires a single control loop. 4. Phase-Locked Loop (PLL) is not required. 5. Can achieve zero turn-on current in the switches and zero turn-off current in the output diodes.	1. Endorsed in low-power applications (< 300 W). 2. Continuous input current. 3. Soft turn-off switch capability. 4. Reduced input filter size and EMI noise. 5. PFC can be inherently achieved.
Disadvantages	1. Requirement of two control loops. 2. Requirement of PLL. 3. Higher number of sensors. 4. Not economic in low-power applications. 5. Additional circuitry requirement for soft-switching.	1. Requires interleaving for high-power applications. 2. Increased component rating. 3. High EMI noise. 4. High current stress on the switch. 5. Requirement of an additional LC filter. 6. Reduced efficiency.	1. Increased voltage stress on the switches in high-power applications. 2. Requires complex control for high-power applications. 3. Additional hardware requirement (one inductor and capacitor).

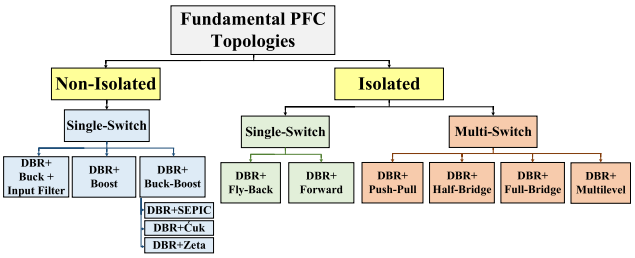

FIGURE 8. Fundamental PFC converters classification.

subdivided into a DBR in combination with the non-isolated single-switch converters (Buck, Boost, Buck-Boost, SEPIC, Ćuk, and Zeta topologies) (FIGURE 9), isolated single-switch converters (fly-back and forward topologies), and isolated multi-switch converters (push-pull, half-bridge, full-bridge, and multi-level topologies) [14], [15], [17], [21], [35]–[37], [53]–[56].

The fundamental Buck topology has major issues, namely inherent discontinuous input current (i.e., high ripples) due to the switch connected in series with the AC mains, limitation to voltage step-down mode, and dead-angle issue in the DICM when the input voltage is less than the output voltage (i.e., distorted input current with high THD and low *pf*) [57]. Therefore, an input filter is required for a practical application of the fundamental Buck topology (FIGURE 9(a)), and its application is limited. However, the Buck topology is an efficient option for low input/output voltage applications with unlimited lower limit voltage. Besides, it is efficient in open circuit operation. Also, it is resilient to inrush input current issues [35], [53], [58], [59]. The Buck topology is usually employed in low-power applications (< 300 W) where the converter can attain the input current' harmonic elements within the margins of the IEC 61000-3-2 requirements [50]. In [53], a practical performance evaluation of the fundamental Buck converter with an input LC filter has been presented for power rating set to 1.2 kW, input AC voltage by 100 V, considering both the Pulse-Width-Modulation (PWM) and Pulse-Space-Modulation (PSM). The *pf* was attained between 0.85-0.94 in PWM operation and 0.96-0.99 in PSM operation. The input current THD was between 26%-40% in PWM operation and between 0.5%-20% in PSM operation (i.e., high current harmonics content between half-load and full-load conditions in both operations; however, in PSM operation, increased inductor size can limit the harmonics below 5% between the half-load and full-load conditions).

The fundamental Boost topology (FIGURE 9(b)) offers a continuous input current. However, it has low efficiency during light-loading conditions. The charging of a fully discharged vehicle with the Boost topology commences with a low-efficiency converter. Also, the Boost topology is limited to the voltage step-up mode. Therefore, the converter design requires to be based on the maximum load voltage. Besides, the output capacitor current has high-ripples content and large inrush current [36], [37], [48]. Due to the high output voltage from the Boost topology, larger than the line voltage,

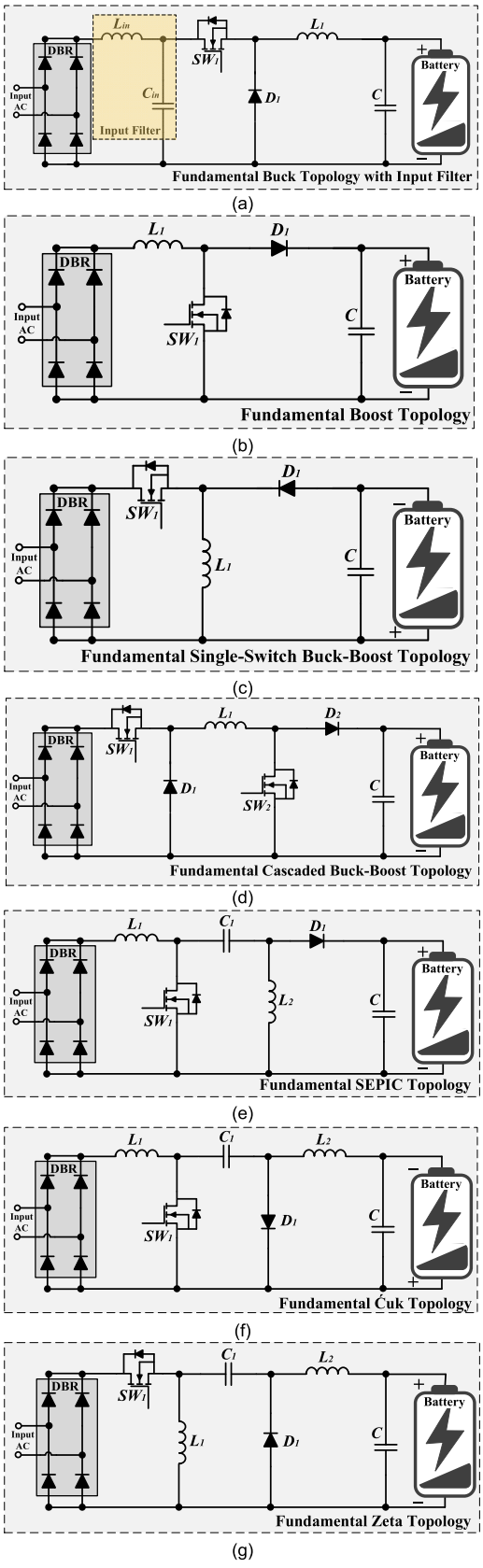

FIGURE 9. Fundamental single-phase unidirectional non-isolated PFC topologies with the DBR (a) Buck topology with input filter, (b) Boost topology, (c) Buck-Boost topology—single switch, (d) cascaded Buck-Boost topology, (e) SEPIC topology, (f) Cuk topology, and (g) Zeta topology.

the output capacitor is imposed to a high voltage rating (160 V – 400 V).

Nevertheless, the Boost topology excels in self-PFC in the DICM compared to the Buck topology, which poorly performs in the DICM. The practical performance of a fundamental Boost topology in CICM has been investigated in [36] for an input AC voltage in the range between 90 V and 265 V and power rating by 1.7 kW. The results showed that the converter's efficiency improves with the increase of the line voltage with an overall efficiency between 91% and 98%; however, the THD performance was not clarified. Besides, a 1 kW fundamental Boost converter prototype has been developed in [60] with an operating efficiency between 89%-96% for an input AC voltage between 90 V-265 V. Also, in [61], an efficient 3.3 kW Boost PFC converter prototype has been studied and realized with the fundamental Boost topology combined by an auxiliary circuit for high-switching frequency and losses minimization (i.e., zero-voltage switching for the Boost switch and zero-current switching for the auxiliary circuit switch).

The front-end AC-DC converter for the Nissan LEAF 2013 EV model is composed of a DBR in a combination of a fundamental Boost-based PFC converter [62]. The on-board charger of this model is compatible with two AC standard forms: 120 V/60 Hz and 240 V/50 Hz; besides, it has an additional charging access port for fast DC charging. The experimental data in [62] showed that the efficiency of the fundamental Boost PFC converter with the DBR was between 92%-96% for a power range between 3.3kW-6.6kW and the *pf* was between 0.92 to 0.99. The efficiency of the charger deviated largely with the input AC voltage variations. Nevertheless, a presentation of the THD performance, devices' stress, and generated noises for the PFC converter was not demonstrated.

The fundamental Buck-Boost topologies offer a variable input/output voltage stepping. Therefore, they are preferred for EV charging applications (i.e., suitable for various battery voltage levels). The fundamental single-switch Buck-Boost topology (FIGURE 9(c)) and the fundamental cascaded Buck-Boost topology (FIGURE 9(d)) suffer from a discontinuous input current and large inrush current. The fundamental SEPIC topology (FIGURE 9(e)) has a continuous input current and discontinuous output current (i.e., high output ripples). It does not have issues with large inrush current due to the capacitive isolation. The fundamental Ćuk topology (FIGURE 9(f)) is similar to the SEPIC topology. However, the output voltage of the Ćuk topology is negative (i.e., an additional circuit is required for polarity reversal), and both the input and output currents are continuous. Meanwhile, the fundamental Zeta topology's (FIGURE 9(g)) output voltage is positive. However, the input current is discontinuous.

An experimental performance assessment of the fundamental Buck-Boost PFC converter has been presented in [53] considering both the PWM and PSM operation with a power rating of 1.2 kW and input AC voltage by 100 V. The results showed that the Buck-Boost converter attained

pf between 0.88-0.98 (in PWM operation) and between 0.96-0.99 (in PSM operation). The achieved input current THD was between 14%-40% (in PWM operation) and between 0.6%-20% (in PSM operation). The THD was less than 5% between the half-load and full-load conditions with the PSM operation and low inductor sizing.

A diode-assist approach has been proposed in [63] to improve the voltage gain and reduce the voltage and current stress in the fundamental topologies (i.e., diode-assisted Buck, diode-assisted Boost, and diode-assisted Buck-Boost converters). Meanwhile, the isolated DC-DC converters can be employed to provide electric isolation between the input and output DC sides of the converter (i.e., DC isolation) for safety requirements. The isolation is achieved via an intermediate medium/or high-frequency transformer. The isolated PFC topologies differ in the number of switches, transformer size, voltage stepping operation, and components' stress. Both the fly-back and forward converter topologies possess a single-switch converter topology. However, they have poor transformer utilization. Advanced multi-switch topologies have been developed (e.g., push-pull, half-bridge, and full-bridge configurations) to lift the operating efficiency and reduce the filter size of the isolated converters in high-power applications. The PFC stage in the EV application does not necessarily require isolation, as its subsequent downstream DC-DC converter can handle the electrical isolation, battery voltage matching, and battery charging speed. Therefore, for a transformer-less PFC converter, the isolated topologies are not covered in this study.

Practically, the fundamental PFC converter topologies and their market products and vendors have been popular and employed for low-voltage and/or low-power applications [36], [37], [51], [57], [59], [62]–[71]. The foremost hindrances with the power leveling-up (for faster-charging levels) and high-frequency switching (for reduced converter size) operation are the amplified semiconductor conduction losses, diode recovery losses, and non-commitment to THD and *pf* standards. Consequently, the resultant is a converter operating with reduced efficiency and reliability [72]. Therefore, there has been a significant deficit in the performance evaluation and experimental data available of the fundamental PFC converter topologies for battery charging rates above 1 kW. Contrariwise, the current research is focused on abolishing the spontaneous and inherited issues in the fundamental topologies, approaching alternative PFC converter topologies, and/or utilizing advanced techniques (e.g., soft switching). To mitigate the disadvantages in the aforementioned fundamental topologies and reduce the significant losses generated by the DBR, due to the diodes drop losses (56% of the losses produced in the Boost-based PFC converter are reported to be from the DBR [36]), modified non-isolated DC-DC converters have been proposed to improve the performance of the fundamental PFC converters. That is while pursuing towards minimized usage of semiconductor devices. These developments are driven by the universal performance standards requiring high-efficiency at different capacity levels of the full-load (e.g., peak efficiency operation at 50% of the full-load) and high-efficiency across the line voltages 90V-264V, and controlled THD generation [73]. The high-voltage output from the fundamental Boost converter imposes high-voltage switches and bulky isolation transformers at the downstream converters (i.e., increased losses, cost, and size compared to low-voltage rated components). Hence, a fundamental Boost PFC converter's efficiency is integrated by a DBR drop at low-line voltages due to the losses in the high-voltage rated semiconductor devices. Relatively, the fundamental Buck converter succeeds in terms of high-efficiency at different line ranges; yet, current THD is high compared to the Boost topology [53], [73]. Meanwhile, the Buck-Boost topologies offer both Buck and Boost mode operations, yet they suffer from increased component stress and reduced efficiency. Besides, the voltage gain of the Buck-Boost topologies is limited in wide universal input AC voltage applications (limited step-down voltage gain) due to the low duty ratio and, consequently, limited switching frequency.

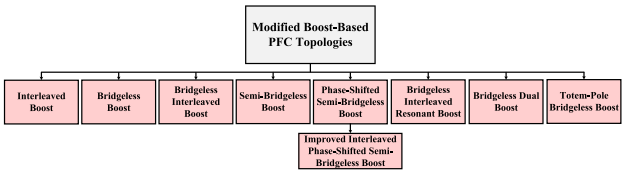

FIGURE 10. A classification for the Boost-based modified PFC topologies.

The following sections cover the modified versions of the fundamental unidirectional non-isolated PFC converters.

V. BOOST-BASED MODIFIED PFC CONVERTER TOPOLOGIES

The fundamental single-phase unidirectional Boost converter has been developed into nine modified topologies (FIGURE 10, FIGURE 11, and FIGURE 12): interleaved Boost, bridgeless Boost, bridgeless interleaved Boost, semi-bridgeless Boost, phase-shifted semi-bridgeless Boost, bridgeless interleaved resonant Boost, bridgeless dual Boost, totem-pole bridgeless Boost, and improved interleaved phase-shifted semi-bridgeless Boost. The interleaved topologies allow high-power operation ($\geq$1 kW) with improved power quality and efficiency. In the interleaved topology, two boost converters operate in parallel (interleaved) with a 180° phase shift, permitting a reduction in the inductor size, EMI filter size, and switching losses (with an increase in effective switching frequency). Regardless, an increased number of components and auxiliary circuits is inevitable. On the other hand, the bridgeless topologies have been introduced to eliminate the DBR losses and allow efficient power operation up to 7 kW. The Boost-based topologies can be sorted approximately in terms of their power processing (incrementally), EMI noise

(reduction), input ripple (reduction), and cost (incrementally) as follows: (1) bridgeless Boost topology, (2) bridgeless dual Boost topology, (3) totem-pole Boost topology,

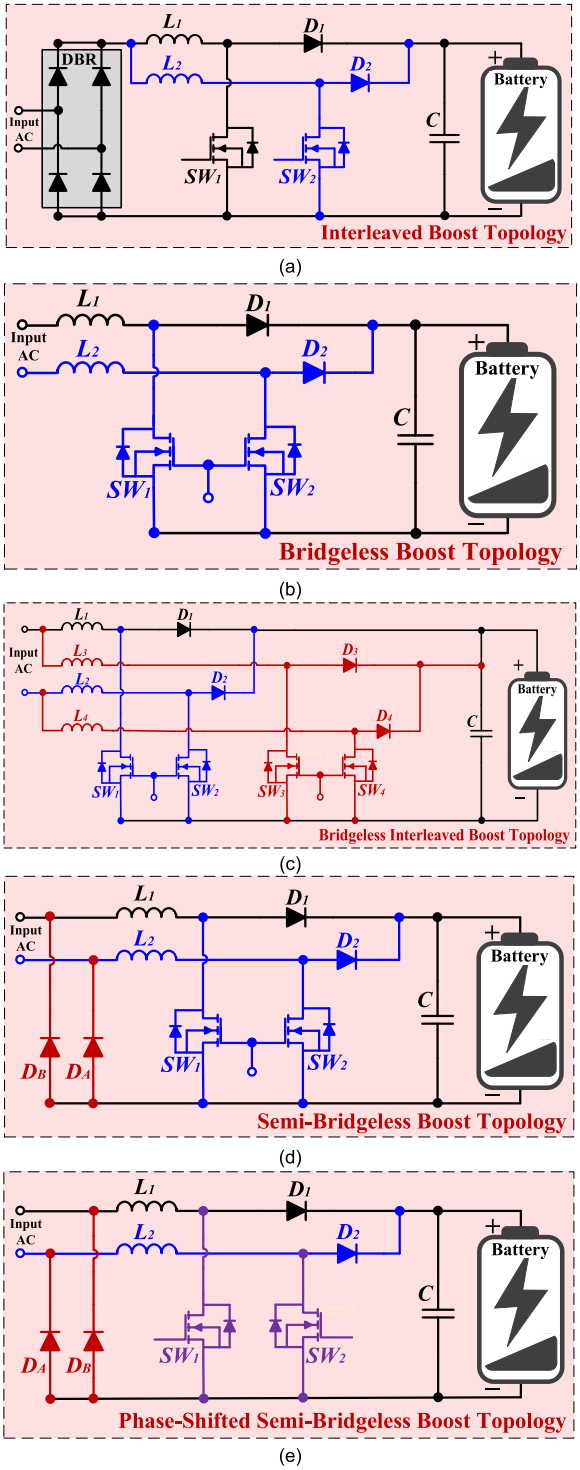

FIGURE 11. Boost-based modified PFC topologies (a) interleaved Boost topology with a DBR, (b) bridgeless Boost topology, (c) bridgeless interleaved Boost topology, (d) semi-bridgeless Boost topology, and (e) phase-shifted semi-bridgeless Boost topology.

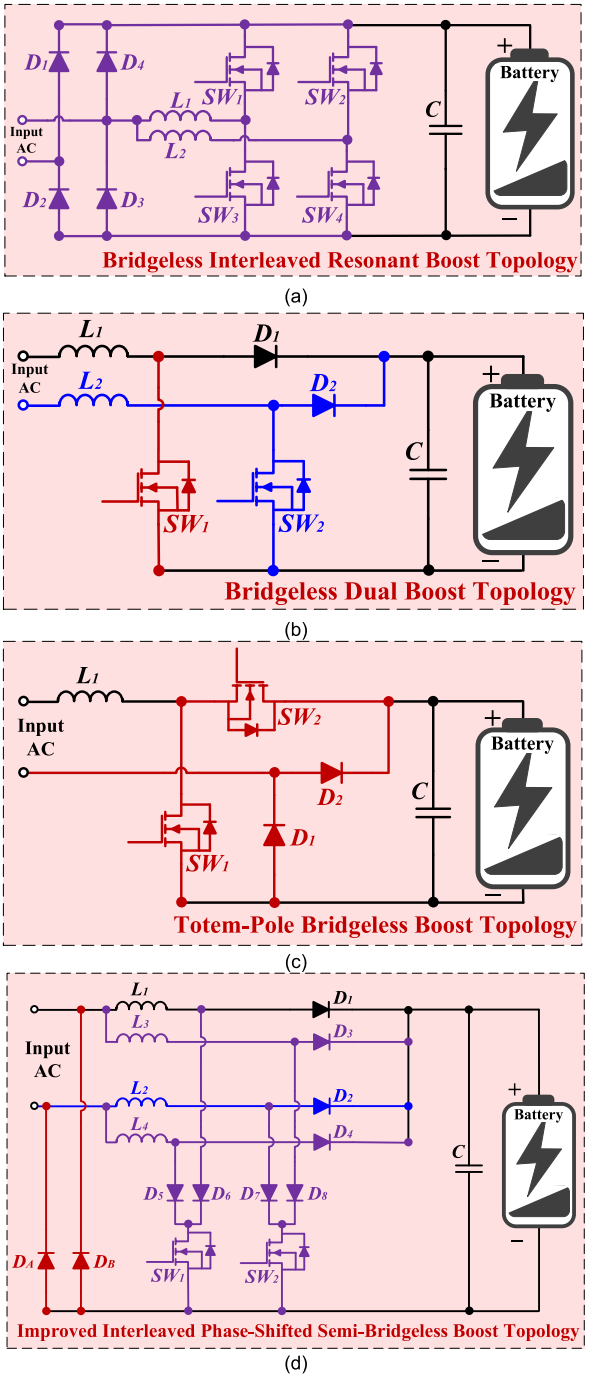

FIGURE 12. Continue Boost-based modified PFC topologies (a) bridgeless interleaved resonant Boost topology, (b) bridgeless dual Boost topology, (c) totem-pole bridgeless Boost topology, and (d) improved interleaved phase-shifted semi-bridgeless Boost topology.

(4) interleaved Boost topology, (5) semi-bridgeless Boost topology, (6) phase-shifted semi-bridgeless Boost topology, (7) bridgeless interleaved Boost topology, (8) bridgeless interleaved resonant Boost topology, and (9) improved interleaved phase-shifted semi-bridgeless Boost topology. The aforementioned topologies are showcased in FIGURE 11 and FIGURE 12, and they are discussed in TABLE 6 (merits versus demerits) and TABLE 7 (power rating, *pf*, and THD) [10], [19], [35]–[38], [40], [60], [74]–[92]. In addition, in [93], a zero-voltage transition switch for the bridgeless Boost topology was addressed with several types of auxiliary circuits of zero current switching switches operation.

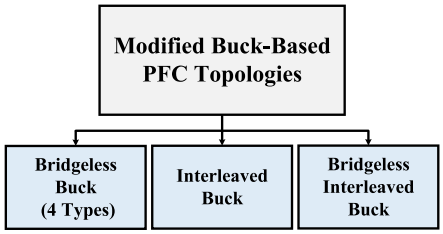

FIGURE 13. A classification for the Buck-based modified PFC topologies.

VI. BUCK-BASED MODIFIED PFC CONVERTER TOPOLOGIES

Similar to the improved Boost topologies, the fundamental Buck topology has been expanded to six modified topologies: bridgeless Buck topologies and interleaved Buck topologies (FIGURE 13, FIGURE 14, and FIGURE 15).

A bridgeless Buck topology (FIGURE 14(a)) has been proposed in [73] to improve the performance of the Buck converter as a PFC converter for high-power levels (around 1 kW). The bridgeless topologies offer current flow with a reduced number of switching devices, thus, minimizing the thermal stress. The topology in FIGURE 14(a) consists of two back-to-back fundamental Buck converters without the DBR. This bridgeless Buck topology allows higher efficiency operation with reduced input current THD compared to the fundamental Buck topology by reducing the number of simultaneous operating semiconductors and conduction losses generated from the DBR (i.e., DBR elimination). The deployed diodes at the output side, D_3 and D_4, are silicon diodes of low reverse recovery losses, while the boost topologies usually employ silicon-carbide diodes (i.e., increased cost and losses). The switches' location provides additional merit for start-up inrush current control. A trade-off exists between the output voltage selection and the THD and *pf* quality of the converter (e.g., power levels below 850 W must operate in output voltage below 160 V to meet the THD level requirement). Voltage balancing for the output capacitors is not an issue as automatic balancing is guaranteed. In terms of the input current and voltage sensing, complex methods and increased sensors are required (since the current flow is in two different paths in each half-cycle).

The input EMI filter size of the bridgeless Buck topology in FIGURE 14(a) is similar to the fundamental Boost topology due to the connection between the capacitors' midpoint and the input neutral line. Besides, modified versions of the bridgeless Buck converter (FIGURE 14(a)) have been presented in [40] and [73] (the topologies maintain the same features of the main topology in FIGURE 14(a)); yet, the performance of the modified versions have not been evaluated. The efficiency of FIGURE 14(a) has been evaluated practically over a power range between 70 W – 700 W with an input AC voltage of 115 V and 230 V and output DC voltage by 160 V. The results demonstrated high operating efficiency (between 93%-95%) for all the loading conditions and universal line voltages. However, for an input 115 V, the input current THD was between 31%-43%, and the *pf* was between 0.89-0.92. While for an input 230 V, the THD was between 19%-23%, and the *pf* was between 0.66-0.94. The high THD content in the presented design's input current and low *pf* remains an obstacle to applying the bridgeless Buck topology in FIGURE 14(a). The inherited dead-angle issue (i.e., distortion at the zero crossings) requires further investigation to reduce the harmonics content and improve the utilization of the active power.

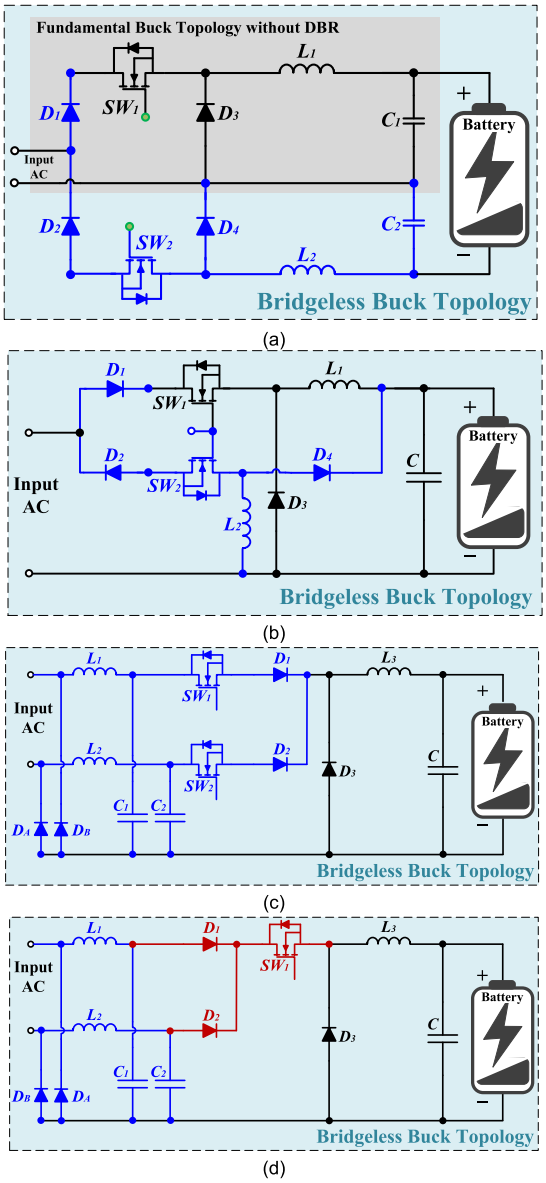

FIGURE 14. Buck-based modified PFC topologies (a) bridgeless Buck topology–type 1, (b) bridgeless Buck topology–type 2, (c) bridgeless Buck topology–type 3, and (d) bridgeless Buck topology–type 4.

A similar topology has been tackled in [94] (a bridgeless Buck converter (FIGURE 14(b))); yet, the performance evaluation was limited to 120 W. In [58], a modified bridgeless Buck topology has been developed to address the dead-angle issue by integrating a fly-back circuit;

TABLE 6. Merits and demerits of the Boost-based modified topologies (Figure 11 and Figure 12).

Topology	Merits	Demerits
Interleaved Boost (FIGURE 11(a)) - [10],[35]-[37], [74],[75],[78]-[81],[83],[84]	• Ripple current reduction and/or reduced inductor size. • Reduced input EMI filter size (due to reduced high-frequency components in input current ripples). • Reduced stress on the output capacitor (due to reduced output current ripples) compared to the non-interleaved configuration. • Increased efficiency for applications up to 3.5 kW. • Practical efficiency in CICM between 91% and 98% • Input current THD < 5% and unity *pf* between half-load and full-load.	• Significant DBR losses (compared to the fundamental Boost topology). • A decline in efficiency with an increase in power level. • Additional control requirement for the current sharing among the interleaved stages in CICM. DICM operation can avoid this issue. • Asymmetrical current sharing may reduce converter efficiency.
Bridgeless Boost (FIGURE 11(b)) - [36]-[38],[40], [74],[75],[77],[79], [82],[85],[88],[89], [90],[91]	• DBR elimination through using two switches. • High operating efficiency for applications up to 2 kW. • Similar gating signal for both switches. • A modified topology of the bridgeless Boost topology "totem-pole bridgeless Boost topology" is shown in FIGURE 12(c).	• Increased input EMI filter size (bulky and costly). • Complex input current measurement and sensing by sensing the current through the switches and diodes path separately (due to non-unified grounds during each half-cycle. • Requirement of current transformer (bulky and costly), Hall effect (costly), or differential amplifier (signal with noise) sensors for the switches and diodes current sensing (further elaboration in [75]). • Requirement of low-frequency transformer or optical coupler for input voltage sensing (due to floating input line with respect to the converter ground). • Large input filter size (due to high THD in the input current).
Bridgeless Interleaved Boost (FIGURE 11(c)) - [10],[36]-[38],[79]	• DBR elimination. • Ripple current reduction and/or reduced inductor size. • Reduced input EMI filter size. • Reduced stress on the output capacitor. • Efficient operation for application up to 6 kW. • Practical efficiency in CICM between 93% and 99%. • Input current THD < 5% and unity *pf* between half-load and full-load.	• Complex input current and input voltage measurement and sensing (similar to the bridgeless Boost topology). • Increased number of components. • Additional control requirement for the current sharing among the interleaved stages in CICM. DICM operation can avoid this issue. • Asymmetrical current sharing may reduce converter efficiency.
Semi-Bridgeless Boost (FIGURE 11(d)) - [10],[36]-[38],[40],[75],[77], [82]	• Reduced DBR losses (two slow-diodes at the input side). • Reduced input EMI filter size. • Simplified input voltage sensing compared to the bridgeless topologies (due to avoidance of floating ground issue). • Practical efficiency in CICM between 96% and 99%.	• Complex input current measurement and sensing. • Increased diode losses. • High diodes (output side) reverse recovery losses and increased EMI noises at an increased switching frequency.
Phase-Shifted Semi-Bridgeless Boost (FIGURE 11(e)) - [25],[36]-[38], [40],[75],[92]	• Reduced DBR losses. • Ripple reduction in the input current. • Reduced input EMI filter size. • High efficiency during the light load operation. • Simplified input voltage and input current sensing (by using resistances). • Practical efficiency in CICM between 94% and 99%. • Improved light-loading efficiency (97%) compared to the interleaved Boost topology (95%) and the fundamental Boost topology (95%) at 240 V line voltage. • Input current THD < 5% and unity *pf* between half-load and full-load.	• Low efficiency during full load operation (due to high-power stress on the switches). • Increased diode losses compared to the bridgeless Boost topology (due to the two slow-speed diodes at the input side). • High diodes (output side) reverse recovery losses and increased EMI noises at an increased switching frequency. • Undesired circulating current in the inductors at each cycle. Solved by the improved topology in FIGURE 12(d).
Bridgeless Interleaved Resonant Boost (FIGURE 12(a)) - [36],[86]	• Reduced diodes losses (four slow diodes) compared to the bridgeless interleaved Boost topology (four fast diodes). • Efficient for application up to 6 kW. • Reduced input EMI filter size. • Practical efficiency in CICM between 96% and 98%.	• Complex input current sensing. • Additional control requirement for the current sharing among the interleaved stages in CICM. DICM operation can avoid this issue. • Asymmetrical current sharing may reduce converter efficiency.
Bridgeless Dual Boost (FIGURE 12(b)) - [37],[38],[40], [75],[76],[92]	• DBR elimination. • Efficient operation during light-loading conditions (decoupled gating signals with synchronous switching behavior, enabling reduced switching and conduction losses). • Higher efficiency in wide-range input AC voltage compared to the fundamental Boost topology.	• Complex input current and input voltage measurement and sensing (similar to the bridgeless Boost topology). • High diodes reverse recovery losses and increased input EMI filter size compared to the fundamental Boost topology. • Undesired circulating current in the inductors at each cycle.

nonetheless, the proposed design was limited to a low-power range (up to 100 W). Also, a bridgeless Buck topology with dual-switch (FIGURE 14(c)) and single-switch (FIGURE 14(d)) configurations in DCVM (i.e., bridgeless Buck with additional LC input circuit) has been addressed in [50] to achieve the advantages of both the CICM and DICM (i.e., simple control and reduced current stress)with high operating efficiency for applications up to 100 W.

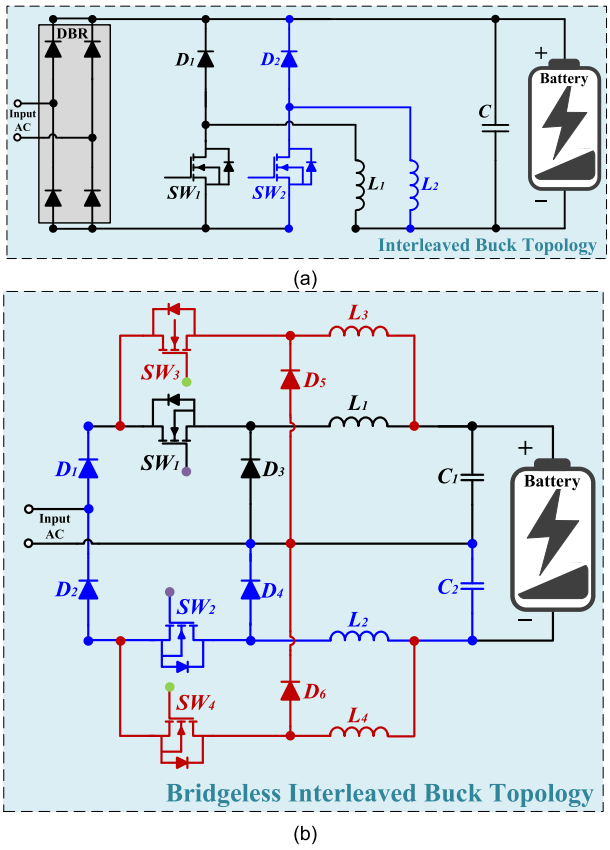

FIGURE 15. Continue Buck-based modified PFC topologies (a) interleaved Buck topology with a DBR and (b) bridgeless interleaved Buck topology.

Besides, an interleaved Buck topology (FIGURE 15(a)) has been addressed in [67] and [95], which has advantages similar to the interleaved Boost topology (i.e., reduced EMI filter size, reduced input current ripples, and reduced component stress). Nevertheless, the presented converter operating performance was limited to 300 W with good *pf* and efficiency at all loading conditions. While the current THD was between 10%-15% for input AC voltage by 230 V, and the current THD was between 30%-40% for input AC voltage by 115 V. A bridgeless interleaved Buck topology (FIGURE 15(b)) has been introduced in [97] to increase the power level of the bridgeless Buck converter and merge the benefits of the DBR elimination and the interleaved operation. This topology is a replication of the bridgeless Buck topology in FIGURE 14(a) with a parallel configuration. The bridgeless interleaved topology gives a high operating efficiency from light-load to full-load operating conditions (95%-97 efficiency with input AC voltage by 85 V and 264 V) for power applications between 30 W and 700 W. Nevertheless, similar to the rest of the Buck-based modified topologies, the harmonics quality of the input current is a drawback to this topology.

A summary of the operating performance conditions of the above-mentioned Buck-based topologies is presented in TABLE 8.

TABLE 7. The power limit, *pf*, and current THD of the Boost-based modified topologies (Figure 11 and Figure 12).

Topology	Power Rating	*pf**	THD*
Interleaved Boost with a DBR [80]	100 W-3.4 kW	120 V: 0.989-0.996	120 V: 4%-12%**
		240 V: 0.97-0.996	240 V: 3%-24%**
Bridgeless Boost [85]	300 W-1.4 kW	120 V: 0.84-0.99	120 V: 5.5%-64%
Bridgeless Interleaved Boost [79]	100 W-3.4 kW	120 V: 0.98-0.99	120 V: 4%-14%**
		240 V: 0.86-0.99	240 V: 4%-41%-**
Semi-Bridgeless Boost [82]	50 W-750 W	85 V-264 V (Power: 750W): 0.991-0.999	85 V-264 V (Power: 750W): 3.5%-8%
Phase-Shifted Semi-Bridgeless Boost [75]	100 W-3.4 kW	120 V: 0.85-0.99	120 V: 4%-45%**
		240 V: 0.97-0.99	240 V: 4%-24%**
Bridgeless Dual Boost [76]	500 W	Not reported.	115 V (Power: 500W): 3.7%
Totem-Pole Bridgeless Boost [91]	350 W	90 V-265 V: 0.96-0.97	Not Reported
Improved Interleaved Phase-Shifted Semi-Bridgeless Boost [92]	20 W-600 W	85 V: 0.98-0.99	85 V: 2%-4%
		265 V: 0.90-0.99	265 V: 3%-20%-**

*The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

VII. BUCK-BOOST-BASED MODIFIED PFC CONVERTER TOPOLOGIES

The limited output voltage from the Boost topologies, output DC voltage consistently higher than the input peak voltage, imposes a two-stage converter charger (PFC converter and a step-down DC-DC converter), therefore, increasing the size and reducing the reliability of the on-board charger. Although the Boost topologies can offer 99% efficiency still, the overall efficiency of the system will suffer in case of operating the subsequent converter (e.g., Inductor-Inductor-Capacitor (LLC) resonance converter [98], [99]) in non-optimal conditions due to the varying range of the load-side such as the battery of the EVs. When the battery's SOC is low (i.e., the DC link voltage is lower than the input grid), then the Boost topologies are not practical, and they can threaten the overall converters' efficiency, in the case of a two-stage battery charger. The Buck topologies have a tradeoff between the *pf* and output voltage selection due to the dead-angle problem. The Buck-Boost topologies can establish a single-stage converter or two-stage converters for EV's battery charging with high-performance PFC capability, battery voltage matching, wide output voltage operating, and high converter efficiency.

TABLE 8. The power limit, *pf*, and current THD of the Buck-based modified topologies (Figure 14 and Figure 15).

Topology	Power Rating	*pf**	THD*
Bridgeless Buck – Type 1 [73]	40 W-700 W	115 V: 0.89-0.92 230 V: 0.66-0.94	115 V: 31%-43% 230 V: 19%-23%
Bridgeless Buck – Type 2 [94]	40 W-120 W	120 V: 0.95-0.96	Not Reported**
Bridgeless Buck – Type 3 [50]	100 W	100 V (Power: 100W): 0.89-0.99	100 V (Power: 100W): 8%-49%**
Bridgeless Buck [58]	35 W-100 W	90 V-270 V (Power: 35 W): 0.77-0.95 90 V-270 V (Power: 100W): 0.93-0.95	Not Reported**
Interleaved Buck with a DBR [67],[95],[96]	30 W-300 W	115 V: 0.93-0.95 230 V: 0.96-0.99	115 V: 30%-40% 230 V: 10%-15%
Bridgeless Interleaved Buck [97]	30 W-700 W	115 V: 0.962-0.967 230 V: 0.951-0.957	115 V: 30%-33% 230 V: 11%-23%

*The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

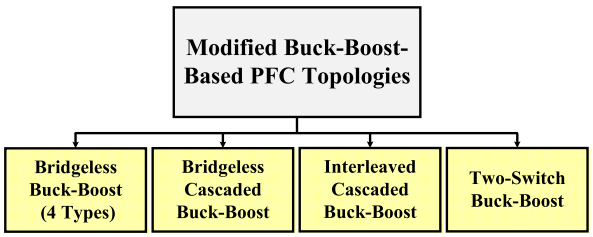

FIGURE 16. A classification for the Buck-Boost-based modified PFC topologies.

Meanwhile, for the case of a two-stage converter battery charger, the battery charging speed can be controlled by integrating a high-power density DC-DC converter of low-rated devices (i.e., reduced losses generation).

A. BUCK-BOOST-BASED DERIVED PFC TOPOLOGIES (FIGURE 17-FIGURE 18)

The bridgeless rectification trend has been developed into the Buck-Boost converter family (i.e., bridgeless Buck-Boost, SEPIC, Ćuk, and Zeta topologies). The fundamental Buck-Boost topology with a DBR elimination (FIGURE 17(a)) has been developed in [100] and [101] with a prototype rated at 350 W and 850 W, respectively, and operating in the DICM. The bridgeless Buck-Boost topology in FIGURE 17(a) consists of two standard single-switch Buck-Boost converters, with each single converter operating over a half-cycle of the line voltage. The converter in [101] offered high-power quality performance with the current

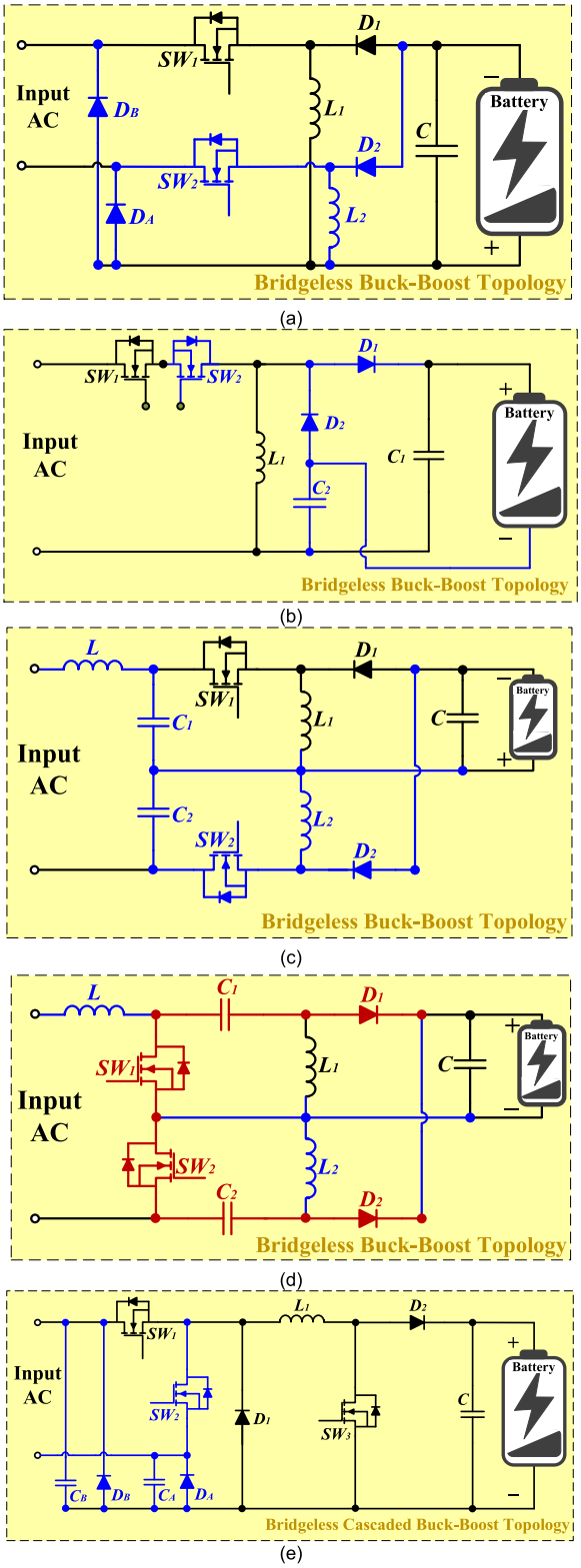

FIGURE 17. Buck-Boost-based modified PFC topologies (a) bridgeless Buck-Boost topology—type 1, (b) bridgeless Buck-Boost topology—type 2, (c) bridgeless Buck-Boost topology—type 3, (d) bridgeless Buck-Boost topology—type 4, and (e) bridgeless cascaded Buck-Boost topology.

THD between 2.3%-5% and almost unity power factor for a line voltage between 170 V-255 V and loading conditions between 100 W-600W. However, the converter's efficiency

for the previous loading conditions was between 45%-82%, while higher efficiency is expected for an increased power range. This topology relies on two-switch and two-gate drive circuitry (i.e., less reliability). Besides, the converter involves complex voltage and current measurements and separate current sensors for each half-cycle of the line. Also, this topology suffers from high EMI filter requirements due to the discontinuous input current. Another bridgeless Buck-Boost topology in DICM (FIGURE 17(b)) has been proposed in [38] for a 1 kW power charging EV application. This topology demonstrated high-power quality performance at 110 V input AC voltage and 400 V output DC voltage, where the input current THD was between 3.1%-4.1%, and unity *pf* was observed for power application in the range of 250 W-1 kW. The operating efficiency of the converter was between 90%-96% for an input AC voltage between 80 V-110 V, where the switches were the main contributors to the emitted losses due to operating the converter in the DICM. However, the proposed topology in FIGURE 17(b) also suffers from a discontinuous input current, increasing the EMI filter requirement. Nevertheless, in the previous studies, the soft-switching technique was deployed to mitigate the EMI emissions. Also, similar bridgeless Buck-Boost topologies in DICM have been introduced in [70] (FIGURE 17(c) and FIGURE 17(d)). Still, the performance evaluation was limited to 300 W with input AC voltage by 110 V and the output DC voltage by 48 V. An inductor was introduced at the input-side of the bridgeless topologies in FIGURE 17(c) and FIGURE 17(d) to mitigate the EMI filter size. A family of bridgeless Buck-Boost topologies has been introduced in [102]; yet, the topologies are complex, and the application was limited to 200 W. Also, the power quality performance was not quantified.

The fundamental cascaded Buck-Boost topology (FIGURE 9(d)) has been developed into a bridgeless configuration in [103]. The bridgeless cascaded Buck-Boost topology (FIGURE 17(e)) offers a reduced number of conducted semiconductors (3 devices) compared to its fundamental topology with the DBR (4 devices). The bridgeless topology escalates the EMI interference and raises the difficulty in voltage sensing. Nonetheless, the study in [103] showed that the efficiency of the cascaded Buck-Boost converter in bridgeless topology (FIGURE 17(e)) was between 95%-97% for power demand between 200 W-600 W, while the efficiency of the topology with DBR (FIGURE 9 (d)) was between 93%-95.5%. Almost unity power factor (0.98-0.99) was achieved, and current THD between 8.22%-9.89% were recorded with an input AC voltage between 200 V-400V. Nevertheless, the converter operation was limited to Boost operation, neglecting the merits of Buck operation. In [24], a single-stage (DBR and a PFC converter) single-phase on-board battery charger has been recommended with an interleaved cascaded Buck-Boost topology (FIGURE 18(a)). The study emphasized eliminating the isolated DC-DC converter stage due to its impact on reducing the overall operating efficiency of the charger and increasing the converter size (i.e., neglecting the isolation between the AC-side and the battery-side as it is not enforced by the EVs standards). However, the topology has the disadvantage of discontinuous current nature of the input-side due to the switches operation and the DBR, requiring an EMI filter at the input-side of the converter. The topology in FIGURE 18(a) can operate in Buck and Boost modes with high operating efficiency. A 3.7 kW prototype was developed to test the interleaved cascaded Buck-Boost converter with an input AC voltage between 120 V-240 V. The recorded operating efficiency and *pf* for power rating between 100 W-3.7 kW were between 86%-98% and 0.91-1, respectively, for input AC voltage by 120 V. While the operating efficiency and *pf* were between 91%-98% and 0.93-1, respectively, for input AC voltage by 208 V. Meanwhile the operating efficiency and *pf* were between 91%-98% and 0.95-1, respectively, for input AC voltage by 240 V. Almost unity power factor was achieved for all the previous conditions between half-loading and full-loading settings. However, the study lacks harmonics content justification. Besides, the high-power rating comes with the compromise of increased components count, yet, with reduced component voltage and current stress.

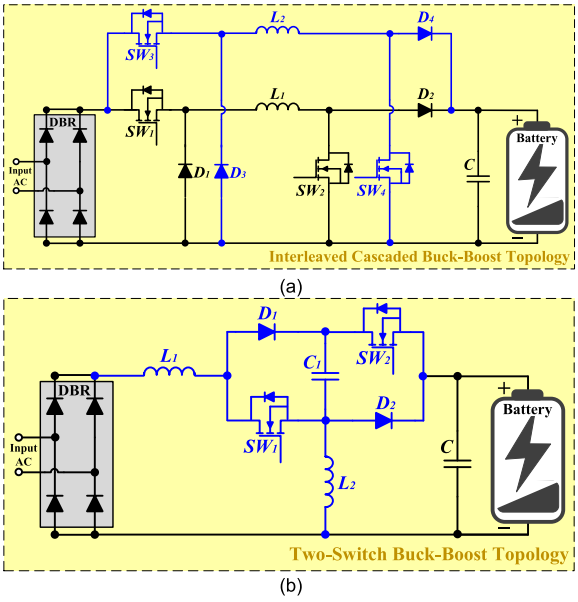

FIGURE 18. Continue Buck-Boost-based modified PFC topologies (a) interleaved cascaded Buck-Boost topology with a DBR and (b) two-switch Buck-Boost topology with a DBR.

In [104], a Buck-Boost topology with the DBR integration in CICM (FIGURE 18(b)) has been proposed with two switches controlled via a transition mode control logic with independent step-up and step-down switches of unique duty ratios for controlled output DC voltage. In the Buck mode, the switch *SW1* is controlled to be in the off state with a zero duty ratio setting, while the duty ratio of *SW2* is controlled to obtain a regulated output voltage. Meanwhile, in the Boost mode, the duty ratio of *SW2* is set to one, while the duty ratio of *SW1* is controlled to regulate the output voltage. A practical prototype for the topology in

TABLE 9. The power limit, *pf*, and current THD of the Buck-Boost-based modified topologies (Figure 17 and Figure 18).

Topology	Power Rating	*pf**	THD*
Bridgeless Buck-Boost – Type 1 [100],[101]	100 W-850 W	170 V-255 V: 0.999	170 V-255 V: 2.3%-5%**
Bridgeless Buck-Boost – Type 2 [38]	250 W-1 kW	110 V: 0.999	110 V: 3.1%-4.1%
Bridgeless Buck-Boost – Type 3 [70]	60 W-300 W	110 V: 0.985-0.998	110 V: 2.02%-2.45%
Bridgeless Buck-Boost – Type 4 [70]	60 W-300 W	110 V: 0.972-0.992	110 V 9.7%-20.8%
Bridgeless Cascaded Buck-Boost [103]	200 W-600 W	200 V-400 V: 0.981-0.999	220 V-380 V: 8.22%-9.89%
Interleaved Cascaded Buck-Boost [24]	100 W-3.7 kW	120 V-240 V: 0.91-0.999	Not Reported
Two-Switch Buck-Boost with a DBR [104]	300 W-1 kW	85 V-265 V: 0.991-0.998	85 V-265 V: 3%-5%

*The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

FIGURE 18(b) was developed for applications up to 1 kW with an input AC voltage between 85 V-265 V and the output DC voltage between 150 V-450 V (i.e., both step-down and step-down operation). The prototype exhibited good power quality performance with an efficiency between 91%-96%, *pf* between 0.991-0.998, and current THD between 3%-5% at universal line inputs and 300 W to 1 kW power operating range. However, the DBR losses counted 24% of the losses generated by the converter.

A summary of the operating performance conditions of the above-mentioned Buck-Boost-based topologies is presented in TABLE 9.

B. SEPIC-BASED DERIVED PFC TOPOLOGIES (FIGURE 20 and FIGURE 21)

The fundamental SEPIC topology has a higher voltage and current stress on the switches and diodes compared to the Boost topologies. Therefore, its utilization has been limited to low-power applications. Nonetheless, the SEPIC topology in DICM allows continuous input current compared to the Boost topology in DICM (i.e., large input filter requirement for the Boost topology) due to the two inductors in the SEPIC topology. The implementation of the bridgeless topologies has been extended to the SEPIC converter (FIGURE 19). A bridgeless SEPIC topology (FIGURE 20(a)) has been proposed in [105] operating in the DICM. In addition to the bridgeless topology and DICM advantages, this topology offers a single or

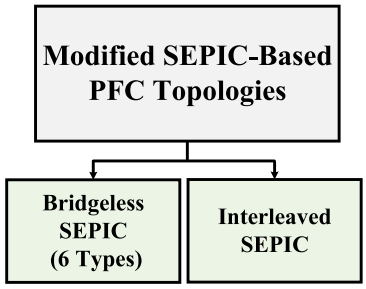

FIGURE 19. A classification for the SEPIC-based modified PFC topologies.

two semiconductors operating during each half-cycle (i.e., reduced conduction losses) and reduced voltage stress on semiconductor devices compared to the fundamental SEPIC topology with the DBR. Three inductors are required for the bridgeless SEPIC topology in FIGURE 20(a), yet, for optimal cost and design sizing, a single magnetic core can be utilized for the three inductors. Besides, an isolated gate drive is required, due to the series switches interconnection, compared to the fundamental SEPIC topology. The major limitation of the topology implementation is the floating output terminal between the two capacitors and the voltage conversion restriction to step-up operation (i.e., step-down and Buck operation is not applicable). The power quality of a simulated-based bridgeless SEPIC topology (FIGURE 20(a)) for power rating 200 W and experimental-based for power rating 60 W were studied in [105]. The study showed that with an input AC voltage of 120 V and output DC voltage of 400 V, the simulated-based outcomes resulted in 2.16% current THD and 97% efficiency. Meanwhile, the practical prototype was tested with an input AC voltage of 30 V and output DC voltage of 200 V, which achieved a current THD of 2.5% and 91% efficiency without an input filter. An improved version of the topology in FIGURE 20(a) has been introduced in [106] for applications up to 100 W.

Another type of bridgeless SEPIC topology operating in the DICM has been introduced in [52] (FIGURE 20(b)) to avoid the requirement of the isolated gate drive in [105]. The topology in FIGURE 20(b) consists of an interleaved SEPIC converter, where each stage operates in half-cycle of the line voltage. This topology has a larger component number, fewer conducting semiconductors per half-cycle, and similar overall switching losses compared to the fundamental SEPIC topology. Besides, similar voltage and current stress compared to the fundamental SEPIC topology, yet, lower Root-Mean-Square (RMS) current stress is achieved for the interleaved components in the bridgeless topology. The bridgeless SEPIC topology in FIGURE 20(b) was developed practically for low-power rating, power between 20 W-100 W, input AC voltage by 85 V and 220 V, and output DC voltage of 48 V, without a filter at the input side. The recorded results showed an operating efficiency between 92.5%-93.5%. While with an input AC voltage of 100 V, the current THD was 1.6% at an operating power of 65 W. A similar bridgeless SEPIC

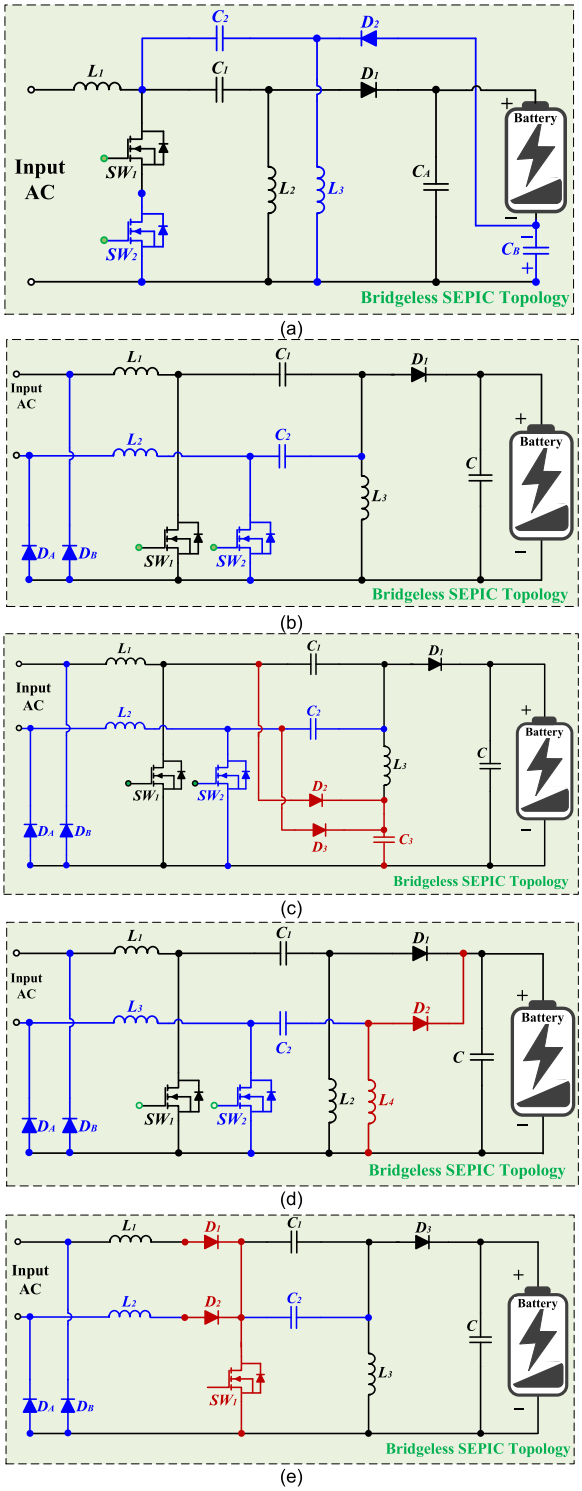

FIGURE 20. SEPIC-based modified PFC topologies (a) bridgeless SEPIC topology–type 1, (b) bridgeless SEPIC topology–type 2, (c) bridgeless SEPIC topology–type 3, (d) bridgeless SEPIC topology–type 4, and (e) bridgeless SEPIC topology–type 5.

topology has been studied in [107] for applications up to 350 W. In addition, similarly to the bridgeless-Boost topology configuration in [85], a bridgeless SEPIC topology has

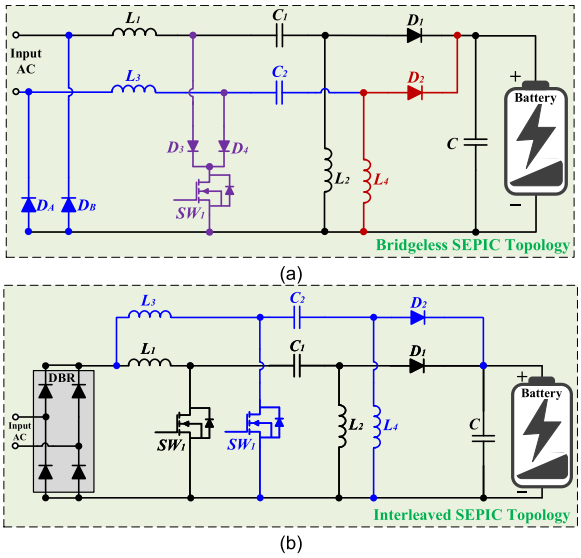

FIGURE 21. Continue SEPIC-based modified PFC topologies (a) bridgeless SEPIC topology–type 6 and (b) interleaved SEPIC topology with a DBR.

been introduced in [108] and [109] for applications up to 130-150 W. Besides, an improved bridgeless SEPIC topology (FIGURE 20(c)) in DICM has been studied in [110], which allows increased voltage gain, reduced switch stress, and improved operating efficiency for universal input AC voltage by the integration of a multiplier cell for applications up to 200 W. However, the topology in FIGURE 20(c) is limited to Boost-mode operation, and it suffers from similar characteristics and disadvantages as the fundamental Boost topology (e.g., output DC voltage always higher than the input-side voltage and high inrush current). Moreover, the bridgeless SEPIC topology in FIGURE 20(c), including the topologies in FIGURE 20(b) and [107], suffer from circulating current at the output inductor (i.e., increased losses) with the output inductor operating in DICM. An experimental prototype has been developed for the topology in FIGURE 20(c) with the input AC voltage between 120 V-220 V and output DC voltage by 400 V. The current THD, *pf*, and efficiency were between 9.7%-27.2%, 0.965-0.995, and 95.7%-96.5%, respectively, for a power range between 100 W and 200 W. An improved bridgeless SEPIC topology for circulating current mitigation (i.e., efficiency improvement) (FIGURE 20(d)) has been addressed in [111] for applications up to 100 W in CICM and without input voltage sensing (i.e., increased control reliability). The efficiency of the topology in FIGURE 20(d) was between 89%-94% for an input AC voltage between 85 V-135 V and the DC output voltage by 60 V. Furthermore, in [112] (FIGURE 20(e)) and [113] (FIGURE 21(a)), a single-switch bridgeless SEPIC topology has been introduced for applications between 100 W-160 W, which eliminates the circulating current losses with the condition that both the input interleaved inductors and output inductor operate in DICM. Nevertheless, the power quality performance of the topologies requires further clarifications.

An increased power processing SEPIC topology has been introduced in [114] with an interleaved configuration and DBR integration (FIGURE 21(b)). The issue withthe power-sharing mismatch among the interleaved branches was solved by utilizing coupled inductors. The switches of the interleaved branches are phase-shifted by 180° to reduce current ripples, harmonics, and EMI filter size. The studied topology in [114] holds the following benefits compared to the fundamental SEPIC topology and the interleaved non-coupled SEPIC topology: current ripple cancelation and reduced THD, reduced switching losses in both CICM and DICM, reduced output voltage ripples, reduced power-sharing mismatch, and improved resistivity against duty cycle mismatch. Simulated-based results for the interleaved inductor coupled SEPIC topology was presented in [114] for 3.3 kW rated power. The results showed the impact of varying the battery's SOC from 420 DC voltage to 200 DC voltage with an input AC voltage of 240 V. Through stepping the DC voltage down, the current THD went from 2% to 3.4% with a unity power factor at both operating conditions. Besides, the power quality with input AC voltage by 120 V and power by 1.6 kW was examined, and the results presented prominent outcomes (current THD at 1.37% and almost unity power factor), yet, the converter's operating efficiency was not elucidated. The work on the interleaved coupled inductor SEPIC topology (FIGURE 21(b)) has been extended in [115]. To avoid the switching losses, the study considered DICM to realize zero voltage switching for the switches (i.e., reduced turn-on switching losses) and zero current switching for the diodes (i.e., reduced turn-off reverse recovery losses). An experimental prototype was developed for the interleaved inductor coupled SEPIC topology, with two interleaved phases, considering both DC voltage stepping-up (190 V) and stepping-down (90 V) with input AC voltage by 110 V and rated power 500 W. The overall operating efficiency and current THD were between 91%-97% and 5.7%-10.3%, respectively, with unity *pf* for the power range between 100 W-500W. At the rated power (500 W), the operating efficiency was 96%, and the current THD was 5.7%. The EMI filter at the input side was eliminated by the proper design of the coupled inductors in the two phases for current ripple mitigation. Also, the work of [114] has been expanded in [116] for applications up to 1 kW with an experimental prototype of high power quality performance and high operating efficiency. A bridgeless interleaved SEPIC topology is also a potential solution for increased power processing while mitigating the DBR losses [117], [118], yet, the research work on this topic is limited.

A summary of the operating performance conditions of the above-mentioned SEPIC-based topologies is presented in TABLE 10.

TABLE 10. The power limit, *pf*, and current THD of the SEPIC-based modified topologies (Figure 20 and Figure 21).

Topology	Power Rating	*pf**	THD*
Bridgeless SEPIC – Type 1 [105]	60 W-200 W	120 V: 0.999	120 V: 2.16%
Bridgeless SEPIC – Type 2 [52]	20 W-100 W	100 V (Power: 65 W): 0.999	100 V (Power: 65 W): 1.6%
Bridgeless SEPIC – Type 3 [110]	100 W-200 W	120 V-220 V: 0.965-0.995	120 V-220 V: 9.7%-27.2%**
Bridgeless SEPIC – Type 4 [111]	100 W	85 V-135 V: 0.994-0.999	Not Reported**
Bridgeless SEPIC – Type 5 [112]	160 W	50 V-100 V: 0.999	50 V-100 V: 4.9%**
Bridgeless SEPIC – Type 6 [113]	100 W	110 V: 0.98	Not Reported**
Interleaved SEPIC with a DBR [114]	1.5 kW-3.3 kW	120 V-240 V: 0.999	120 V-240 V: 1.37%-3.43%
Interleaved SEPIC with a DBR [115]	100 W-500 W	120 V: 0.999	120 V: 5.7%-10.3%

*The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

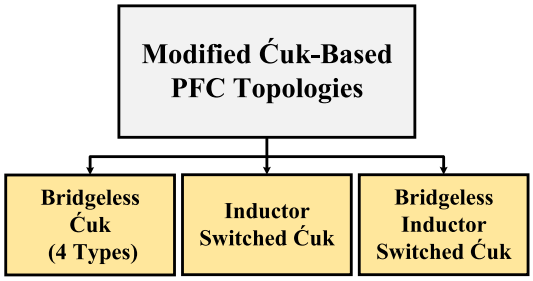

FIGURE 22. A classification for the Cuk-based modified PFC topologies.

C. ĆUK-BASED DERIVED PFC TOPOLOGIES (FIGURE 23)

Besides the SEPIC topology, the Ćuk topology (FIGURE 9(f)) has better current ripples mitigation due to the continuous input current and continuous output current operation. Therefore, the bridgeless configuration has been applied to the Ćuk topology to evade the DBR losses and improve the converter's efficiency (FIGURE 22). The bridgeless Ćuk topology (FIGURE 23(a)) has been first introduced together with the bridgeless SEPIC topology (FIGURE 20(b)) in [52]; however, the work focused on the SEPIC topology only. In [119], three bridgeless Ćuk topologies (FIGURE 23(a), FIGURE 23(b), and FIGURE 23(c)) in DICM have been introduced and studied, including the bridgeless Ćuk topology that was introduced in [52]. Due to the similarity between the bridgeless SEPIC topologies and bridgeless Ćuk topologies, the advantages of the former can be extended to the latter. The gate signals of the bridgeless Ćuk topologies are driven by a similar signal (i.e., simplified control). Besides, the input EMI filter size and output ripples can be reduced considerably with the input/output inductors in coupled core configuration and non-floating

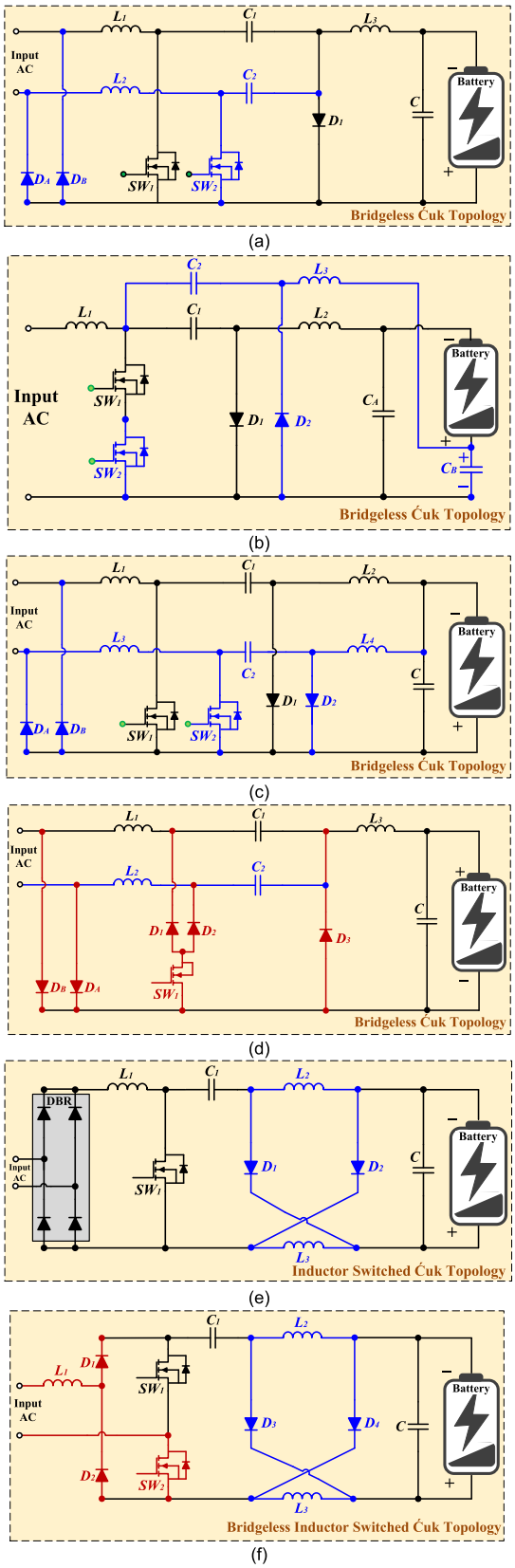

FIGURE 23. Ćuk-based modified PFC topologies (a) bridgeless Ćuk topology–type 1, (b) bridgeless Cuk topology–type 2, (c) bridgeless Cuk topology–type 3, (d) bridgeless Ćuk topology–type 4, (e) inductor switched Ćuk topology with a DBR, and (f) bridgeless inductor switched Ćuk topology.

ground configuration at the input-side of the converters. The application of the bridgeless Ćuk topologies in [119] has been limited to power between 10 W-150 W with DICM and with simulated-based and practical-based performance evaluation for the topologies in FIGURE 23(a) and FIGURE 23(c). The simulated-based results obtained the efficiency and the current THD between 94%-95% and 1%-1.5%, respectively, with the input AC voltage by 120 V and the output DC voltage by 48 V. Meanwhile, the practical prototype demonstrated efficiency and current THD near the simulated results. However, the output voltage from the topologies in FIGURE 23(a), FIGURE 23(b), and FIGURE 23(c) require inverting circuits to reverse the output voltage polarity. Besides, the topologies in FIGURE 23(a) and FIGURE 23(c) both allow step-up and step-down operation, while the topology in FIGURE 23(b) is limited to step-up operation. The bridgeless Ćuk topology in FIGURE 23(a) suffers from circulating current in the interleaved inductors during each half-cycle due to the interconnection of two interleaved capacitors thus, reducing the effective power transfer (i.e., redundant power losses). Meanwhile, the bridgeless Ćuk topology in FIGURE 23(b) has a high number of components (two capacitors at the output side). Besides, the load-side has a floating terminal due to the capacitor connection. Also, a floating ground exists for the upper switch due to the series switches arrangement. The bridgeless Ćuk topology in FIGURE 23(c) avoids the issues associated with FIGURE 23(a) and FIGURE 23(b), yet, it has additional diode losses across the inactive switches as the diodes operate as a return path for the current during each half-cycle. Furthermore, to abolish the issue of the output voltage negative polarity in the bridgeless Ćuk topologies, a non-inverted output voltage bridgeless Ćuk topology (FIGURE 23(d)) has been introduced in [120] without imposing additional inverting circuitry. Unity *pf*, low current THD, and high operating efficiency (90%-97%) in DICM were achieved with the bridgeless non-inverting Ćuk topology, yet, the application was limited to a power rating of 150 W.

An improved bridgeless Ćuk topology has been introduced in [121] with a topology similar to FIGURE 23(c) to avoid the problems encountered by type 1 (FIGURE 23(a)) and type 2 (FIGURE 23(b)). Also, it eliminates the diode losses associated with the inactive switches in type 3 (FIGURE 23(c)) by applying a control signal to the inactive switch to disable the diodes' operation as a return path. A single gate driver signal is provided to both switches in synchronism at each half-cycle. Therefore, the bridgeless Ćuk topology in [121] avoids the circulating current in the interleaved inductors, eliminates floating neutral points, and improves the converter efficiency by reducing the diode losses. An experimental prototype of the improved bridgeless Ćuk topology was developed in [121] for battery charging application up to 900W in DICM with input AC voltage between 110 V-220 V and output DC voltage by 300 V. The presented results showed an operating efficiency between 88%-92%, current THD less than 5%, and unity power factor for power between 150W and 850 W. In addition, the bridgeless Ćuk topology type 3

TABLE 11. The power limit, *pf*, and current THD of the Ćuk-based modified topologies (Figure 23).

Topology	Power Rating	*pf**	THD*
Bridgeless Ćuk – Type 1 [119]	10 W-150 W	100 V-120 V: 0.999	100 V-120 V: 1%-1.5%
Bridgeless Ćuk – Type 3 [119],[121]	10 W-850 W	100 V-220 V: 0.98-0.999	100 V-220 V: 1.25%-1.5%**
Improved Bridgeless Ćuk – Type 3 [121]	150 W-850 W	110 V-220 V: 0.999	110 V-220 V: <5%**
Bridgeless Ćuk – Type 4 [120]	30 W-150 W	110 V: 0.991-0.996	110 V: 2.66%-7.66%**
Inductor Switched Ćuk with a DBR [122],[125]	300 W-500 W	85 V-265 V (Power: 500 W): 0.98-0.999	85 V-265 V (Power: 500 W): 4.8%-7.3%
Bridgeless Inductor Switched Ćuk [125]	130 W-850 W	130 V-260 V: 0.999	130 V-260 V: 2.5%-5.5%

* The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

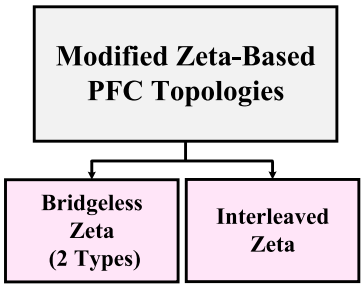

FIGURE 24. A classification for the Zeta-based modified PFC topologies.

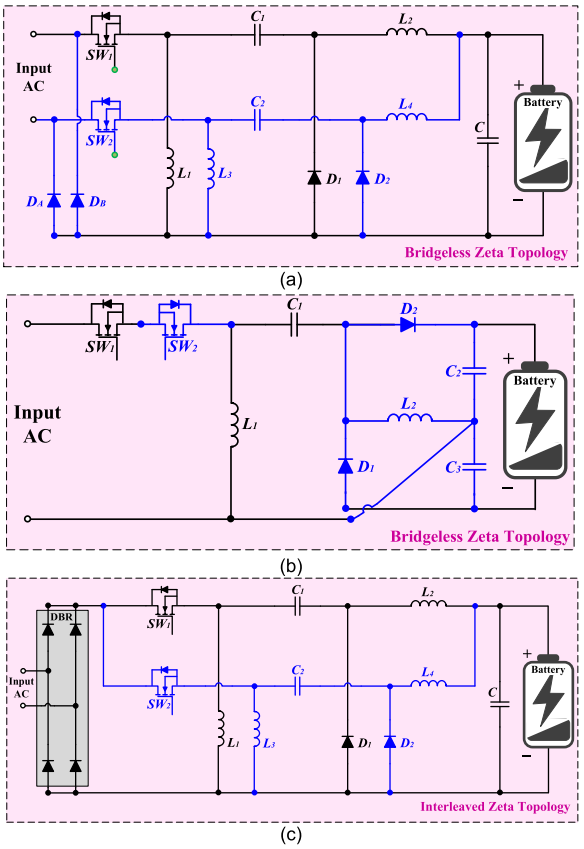

FIGURE 25. Zeta-based modified PFC topologies (a) bridgeless Zeta topology–type 1, (b) bridgeless Zeta topology–type 2, and (c) interleaved Zeta topology with a DBR.

(FIGURE 23(c)) in [119] was compared to the topology in [121] for the same power range application. The topology in FIGURE 23(c) showed operating efficiency between 87%-90%, current THD below 5%, and *pf* between 0.98-1 for power range between 150 W-850 W. Therefore, the improved bridgeless Ćuk topology in [121] achieved higher power quality performance than the topology in FIGURE 23(c). Nevertheless, the topology in [121] still requires inverting circuitry for a positive output voltage.

A single-stage Ćuk topology with a DBR (FIGURE 23(e)) has been addressed in [122] for electric bike battery charging with rated output power by 500 W and DC voltage by 48 V. The topology proposed in [122] considers a robust Ćuk topology with switched inductor operation (by splitting the output inductors and diodes to half) for improved efficiency at steep voltage step-down (i.e., improved static gain) from input AC voltage between 85 V-265 V to output DC voltage by 48 V. Several works have recommended methods for boosting the voltage gain of the fundamental DC-DC converters (e.g., coupled inductors utilization, cascaded converter operation, quadratic converter utilization, and switched inductor or switched capacitor configurations) [84], [122]–[124]. The switched inductor or switched capacitor method modifies the fundamental converter by splitting the inductor or splitting the capacitor with two to three diodes. The network splitting lifts the converter's DC gain through series and/or parallel charging and discharging of the inductors or capacitors. The switched inductor Ćuk topology in [122] (FIGURE 23(e)) demonstrated a practical prototype in CICM with reduced losses, unity power factor operation, and current THD between 4.8%-7.3%. The work in [125] pioneered its study towards a single-stage converter charger (i.e., directly feeding the battery from the front-end PFC converter) with an improved version of the PFC converter topology presented in [122]. A bridgeless inductor switched Ćuk topology (FIGURE 23(f)) operating in DICM for the output inductors has been addressed in [125] for applications up to 850 W, input AC voltage between 130 V-260 V, and output DC voltage between 45 V-65 V. The two switches in FIGURE 23(f) operate simultaneously for reduced control complexity while the inductor at the input side operates in CICM for ripples mitigation. The prototype of the bridgeless switched inductor Ćuk topology (FIGURE 23(f)) in [125] achieved

TABLE 12. The power limit, *pf*, and current THD of the Zeta-based modified topologies (Figure 25).

Topology	Power Rating	*pf**	THD*
Bridgeless Zeta – Type 1 [127]	40 W	50 V-100 V: 0.9-0.99	50 V-100 V: 1.2%-3.5%
Bridgeless Zeta – Type 2 [129]	1 kW	110 V: 0.999	110 V (Power: 1 kW): 3.39%
Interleaved Zeta with a DBR [130]	50 W-400 W	90 V-264 V: 0.89-0.99	90 V-264 V: <10%

* The voltage values are the input AC voltage.

TABLE 13. The power limit, *pf*, and current THD of the Luo-based modified topologies (Figure 27).

Topology	Power Rating	*pf**	THD*
Bridgeless Elementary Negative Output Luo [135]	100 W-400 W	173 V-267 V: 0.98-0.99	173 V-267 V: 4%-9.9%**
Interleaved Elementary Negative Output Luo with a DBR [136]	100 W-750 W	160 V-260 V (Power: 750 W): 0.999	160 V-260 V (Power: 750 W): 1.5%-2%
Bridgeless Modified Elementary Positive Output Luo – Type 1 [138]	100 W	90 V-260 V (Power: 100 W): 0.993-0.999	90 V-260 V (Power: 100 W): 1.2%-1.8%
Bridgeless Modified Elementary Positive Output Luo – Type 2 [139]	150 W-850 W	170 V-260 V: 0.999	170 V-260 V: 1.8%-2.3%

* The voltage values are the input AC voltage.
**Satisfied the IEC 61000-3-2 class D limits.

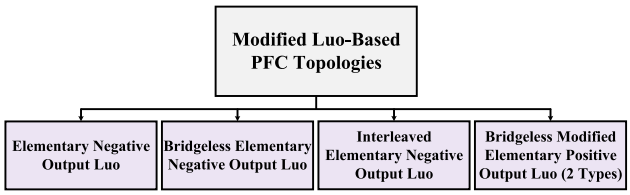

FIGURE 26. A classification for the Luo-based modified PFC topologies.

a good power quality performance with unity power factor, current THD between 2.5%-5.5%, and efficiency between 79%-87% for power between 130 W-850 W and input AC voltage between 130 V-260 V. Meanwhile, under the same testing conditions, the efficiency of the single-stage DBR-based switched inductor Ćuk topology (FIGURE 23(e)) was recorded as 78%-84%. On the other hand, the efficiency of the DBR-based fundamental Ćuk topology with a two-stage converter configuration [126] (i.e., considering the integration of an isolated DC-DC converter) was recorded at 76%-83%.

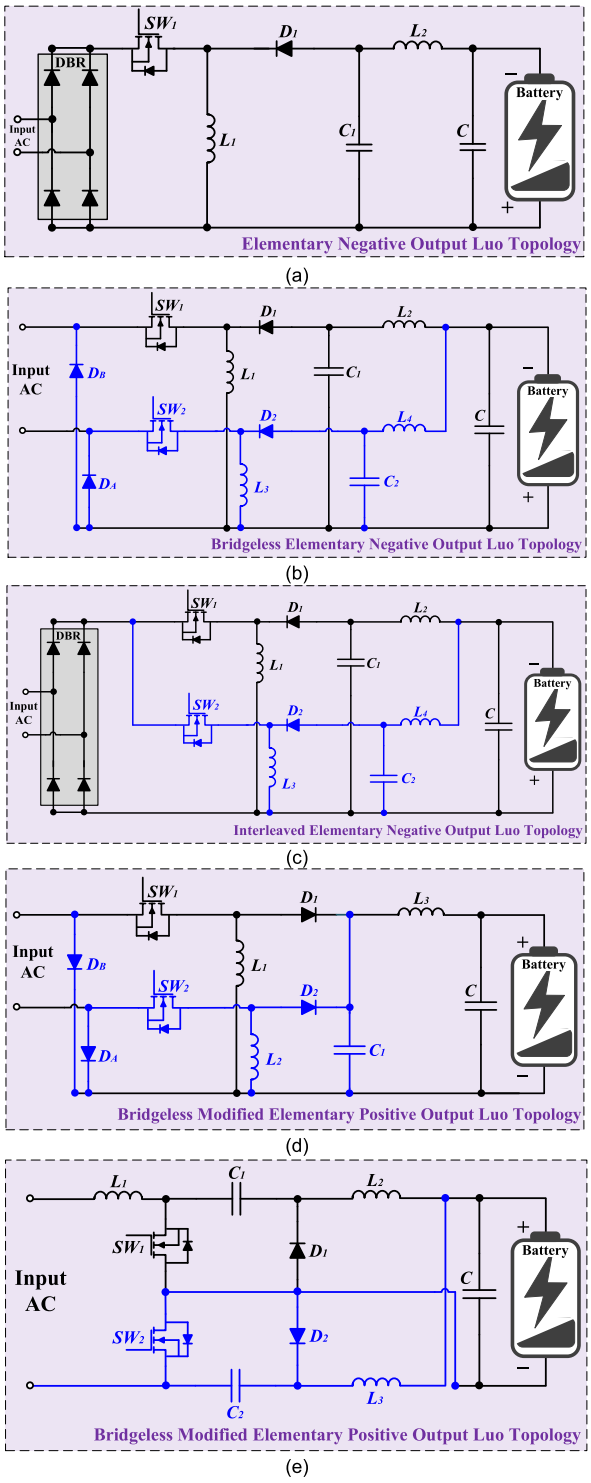

FIGURE 27. Luo-based modified PFC topologies (a) elementary negative output Luo topology with a DBR, (b) bridgeless elementary negative output Luo topology, (c) interleaved elementary negative output Luo topology with a DBR, (d) bridgeless modified elementary positive output Luo topology–type 1, and (e) bridgeless modified elementary positive output Luo topology–type 2.

A summary of the operating performance conditions of the above-mentioned Ćuk-based topologies is presented in TABLE 11.

TABLE 14. Appraisal among the single-phase unidirectional Boost-derived modified PFC topologies (Figure 11 and Figure 12).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Interleaved Boost with a DBR (FIGURE 11(a)) [36],[80]	L: 2 C: 1 SW: 2 SD: 4 FD: 2 **Total: 11**	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	CICM	400 V	400 µH at 3.4 kW f_{SW} at 70 kHz C_{DC} at 82 µF	Low (Inductors' Current Ripple 180° Phase-Shifted)	91%-97% at 100 W-3.4 kW	Medium
Bridgeless Boost (FIGURE 11(b)) [88]	L: 2 C: 1 SW: 2 SD: 0 FD: 2 **Total: 7**	L: 1 C: 1 SW: 1 SD: 0 FD: 1 **Total: 4**	CICM	Not Reported	f_{SW} at 100 kHz L and C Values Not Reported	High (V_{in} Always Floating with Respect to V_{out})	96%-94% at 150 W-500 W	Low
Bridgeless Interleaved Boost (FIGURE 11(c)) [36],[79]	L: 4 C: 1 SW: 4 SD: 0 FD: 4 **Total: 13**	L: 2 C: 1 SW: 2 SD: 0 FD: 2 **Total: 7**	CICM	400 V	400 µH at 3.4 kW f_{SW} at 70 kHz C_{DC} at 82 µF	Low (Inductors' Current Ripple 180° Phase-Shifted)	94%-99% at 100 W-4.5 kW	High
Semi-Bridgeless Boost (FIGURE 11(d)) [82]	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	L: 1 C: 1 SW: 1 SD: 1 FD: 1 **Total: 5**	CICM	400 V	1.08 mH at 750 W f_{SW} at 110 kHz C_{DC} at 470 µF	Medium (V_{in} and V_{out} Share the Same Ground)	96%-99% at 50 W-750 W	Medium
Phase-Shifted Semi-Bridgeless Boost (FIGURE 11 (e)) [36]	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	L: 1 C: 1 SW: 1 SD: 1 FD: 1 **Total: 5**	CICM	400 V	400 µH at 3.4 kW f_{SW} at 70 kHz C_{DC} at 82 µF	Medium (V_{in} and V_{out} Share the Same Ground)	93%-99% at 100 W-3.4 kW	Medium
Bridgeless Dual Boost (FIGURE 12(b)) [76]	L: 2 C: 0 SW: 2 SD: 0 FD: 2 **Total: 6**	L: 1 C: 0 SW: 1 SD: 0 FD: 1 **Total: 3**	CICM	200 V	550 µH at 500 W f_{SW} at 130 kHz C_{DC} Not Reported	High (V_{in} Always Floating with Respect to V_{out})	Not Reported	Low
Totem-Pole Bridgeless Boost (FIGURE 12(c)) [91]	L: 1 C: 1 SW: 2 SD: 2 FD: 0 **Total: 6**	L: 1 C: 1 SW: 1 SD: 1 FD: 0 **Total: 4**	DICM	400 V	135 µH at 350 W f_{SW} at 30 kHz – 250 kHz C_{DC} at 470 µF	High (DICM Operation)	96%-98% at 350 W	Low
Improved Interleaved Phase-Shifted Semi-Bridgeless Boost (FIGURE 12(d)) [92]	L: 4 C: 1 SW: 2 SD: 2 FD: 8 **Total: 17**	L: 2 C: 1 SW: 2 SD: 1 FD: 4 **Total: 10**	Critical Conduction Mode	388 V	210 µH at 600 W f_{SW} Not Reported C_{DC} at 500 µF	Low (Inductors' Current Ripple 180° Phase-Shifted)	93%-98 at 600 W	High

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches. V_{in} is the input AC voltage. V_{out} is the output DC voltage.
*The number of devices operating per half-cycle.

D. ZETA-BASED DERIVED PFC TOPOLOGIES (FIGURE 25)

The fundamental Zeta topology has been modified in [127] to eliminate the DBR stage and develop a bridgeless Zeta PFC converter via an interleaved Zeta configuration (FIGURE 25(a)). Each interleaved phase operates either in the positive cycle or the negative cycle. The main drawback of the bridgeless Zeta topology in FIGURE 25(a), including the fundamental Zeta topology, is the direct series connection of the AC supply with a switch (i.e., increased harmonics level and EMI noise). Nevertheless, compared to the Ćuk topologies, positive output DC voltage is attained in the Zeta topologies without auxiliary circuitry. The design of the bridgeless Zeta converter in [127] was limited to low-power applications, 40 W, with DICM and operating

TABLE 15. Appraisal among the single-phase unidirectional Buck-derived modified PFC topologies (Figure 14 and Figure 15).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless Buck – Type 1 (FIGURE 14(a)) [73]	L: 2 C: 2 SW: 2 SD: 2 FD: 2 **Total: 10**	L: 1 C: 1 SW: 1 SD: 1 FD: 1 **Total: 5**	CICM	160 V	60 µH at 700 W f_{SW} at 65 kHz C_{DC} at 3000 µF	High (Dead Angle Issue)	93%-95% at 70 W-700 W	Medium
Bridgeless Buck – Type 2 (FIGURE 14(b)) [94]	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	L: 1 C: 1 SW: 1 SD: 1 FD: 1 **Total: 5**	DICM	85 V	150 µH and 300 µH at 120 W f_{SW} at 20 kHz C_{DC} at 470 µF	High (DICM Operation)	85%-90% at 120 W	Medium
Bridgeless Buck – Type 3 (FIGURE 14(c)) [50]	L: 3 C: 3 SW: 2 SD: 2 FD: 1 **Total: 11**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DCVM	48 V	2.2 mH and 180 µH at 100 W f_{SW} at 50 kHz 47 nF and C_{DC} at 3000 µF	Low (DCVM Operation)	95%-96% at 100 W	Medium
Bridgeless Buck [58]	L: 4 C: 2 SW: 4 SD: 4 FD: 2 **Total: 16**	L: 2 C: 2 SW: 2 SD: 2 FD: 1 **Total: 9**	DICM	130 V	0.1 mH and 0.4 mH at 100 W f_{SW} at 50 kHz C_{DC} at 470 µF	High (DICM Operation)	82%-91% at 100 W	High
Interleaved Buck with a DBR (FIGURE 15(a)) [67]	L: 2 C: 1 SW: 2 SD: 4 FD: 2 **Total: 11**	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	CICM	80 V	24.7 µH at 300 W f_{SW} at 300 kHz C_{DC} at 2200 µF	Low (Inductors' Current Ripple 180º Phase-Shifted)	89%-96% at 30 W-300 W	Medium
Bridgeless Interleaved Buck (FIGURE 15(b)) [97]	L: 4 C: 2 SW: 4 SD: 2 FD: 4 **Total: 16**	L: 2 C: 1 SW: 2 SD: 1 FD: 2 **Total: 8**	CICM	160 V	80 µH at 700 W f_{SW} at 65 kHz C_{DC} at 1000 µF	Low (Inductors' Current Ripple 180º Phase-Shifted)	95%-97% at 70 W-700 W	High

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches. V_{in} is the input AC voltage. V_{out} is the output DC voltage.
*The number of devices operating per half-cycle.

efficiency between 87%-95%. The bridgeless Zeta topology has been expanded in [128] for EV charging applications up to 780 W, yet, the design considered isolated Zeta converter configuration, which increases the size of the PFC converter. A non-isolated bridgeless Zeta PFC topology in DICM with reduced components count (FIGURE 25(b)) has been introduced in [129] for EV charging application up to 1 kW, yet, the power quality performance of the converter needs additional investigation. An interleaved Zeta topology in DICM with the DBR integration (FIGURE 25(c)) has been studied in [130] for power applications up to 400 W. The topology in FIGURE 25(c) suffers from a discontinuous input current, high EMI noise, high harmonics content, and high DBR losses with an increased power processing level. The interleaved Zeta topology was tested in wide universal input AC voltage between 90 V-264 V, output DC voltage by 200 V, and power demand between 50 W- 400 W. The efficiency of the topology in FIGURE 25(c) was between 77%-91%, the *pf* was between 0.89-0.99, while the current THD was below 10%. Further topologies can be derived from the fundamental Zeta topology, such as an interleaved bridgeless Zeta topology, to eliminate the DBR losses and enhance the conversion efficiency. Therefore, bridgeless Zeta topologies can be a potential choice for EV charging as a PFC converter. However, the research on the Zeta PFC topologies development for EV charging applications has been extremely limited [127]–[132].

A summary of the operating performance conditions of the above-mentioned Zeta-based topologies is presented in TABLE 12.

TABLE 16. Appraisal among the single-phase unidirectional Buck-Boost-derived modified PFC topologies (Figure 17 and Figure 18).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless Buck-Boost Type 1 (FIGURE 17(a)) [101]	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	L: 1 C: 1 SW: 1 SD: 1 FD: 1 **Total: 5**	DICM	48 V	150 µH at 850 W f_{SW} at 20 kHz C_{DC} Not Reported	High (DICM Operation)	45%-82% at 100 W-600 W	Medium
Bridgeless Buck-Boost Type 2 (FIGURE 17(b)) [38]	L: 1 C: 2 SW: 2 SD: 0 FD: 2 **Total: 7**	L: 1 C: 2 SW: 2 SD: 0 FD: 1 **Total: 6**	DICM	400 V	24.45 µH at 1 kW f_{SW} at 50 kHz C_{DC} at 824 µF	High (DICM Operation)	90%-96% at 250 W-1 kW	Low
Bridgeless Buck-Boost Type 3 (FIGURE 17(c)) [70]	L: 3 C: 3 SW: 2 SD: 0 FD: 2 **Total: 10**	L: 3 C: 2 SW: 1 SD: 0 FD: 1 **Total: 7**	DICM	48 V	16 µH and 450 µH at 300 W f_{SW} at 60 kHz C_{DC} at 6800 µF 1 µF	High (DICM Operation)	89%-93% at 60 W-300 W	Medium
Bridgeless Buck-Boost Type 4 (FIGURE 17(d)) [70]	L: 3 C: 3 SW: 2 SD: 0 FD: 2 **Total: 10**	L: 2 C: 2 SW: 1 SD: 0 FD: 1 **Total: 6**	DICM	48 V	16 µH and 450 µH at 300 W f_{SW} at 60 kHz C_{DC} at 6800 µF 1 µF	High (DICM Operation)	89%-94% at 60 W-300 W	Medium
Bridgeless Cascaded Buck-Boost (FIGURE 17(e)) [103]	L: 1 C: 3 SW: 3 SD: 2 FD: 2 **Total: 11**	L: 1 C: 1 SW: 2 SD: 1 FD: 2 **Total: 7**	CICM	400 V	f_{SW} at 50 kHz L and C Values Not Reported	Medium (V_{in} and V_{out} Share the Same Ground)	95%-97% at 200 W-600 W	Medium
Interleaved Cascaded Buck-Boost (FIGURE 18(a)) [24]	L: 2 C: 1 SW: 4 SD: 4 FD: 4 **Total: 15**	L: 2 C: 1 SW: 2 SD: 2 FD: 2 **Total: 9**	CICM	270 V-430 V	800 µH at 3.7 kW f_{SW} Not Reported C_{DC} at 80 µF	Medium (V_{in} and V_{out} Share the Same Ground)	93%-98% at 370 W-3.7 kW	High
Two-Switch Buck-Boost with a DBR (FIGURE 18(b)) [104]	L: 2 C: 2 SW: 2 SD: 4 FD: 2 **Total: 12**	L: 2 C: 2 SW: 1 SD: 2 FD: 1 **Total: 8**	CICM	150 V-450 V	30 mH and 2.52 mH at 1 kW f_{SW} at 30 kHz C_{DC} at 950 µF 8 µF	Medium (V_{in} and V_{out} Share the Same Ground)	91%-96% at 300 W-1 kW	Medium

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches. V_{in} is the input AC voltage. V_{out} is the output DC voltage.
*The number of devices operating per half-cycle.

E. LUO-BASED DERIVED PFC TOPOLOGIES (FIGURE 27)

In efforts to improve the voltage gain of the Zeta topology, the Luo family converters have been derived (positive output Luo converters) with several circuit topologies, in the succeeding voltage gain, passive elements count, and semiconductor devices count proliferation order: elementary circuit (the fundamental Zeta topology (single-switch)), self-lift circuit (single-switch), re-lift circuit (two-switches), triple-lift circuit (two-switches), and quadruple-lift circuit (two-switches) [133], [134]. The step-up and step-down modes are attained solely by the elementary circuit. Meanwhile, the other aforementioned circuit topologies are derived from the elementary circuit, and they are limited to the Boost mode with an increased voltage gain compared to the elementary circuit. Besides, a modified version of the positive output Luo converters has been introduced for the aforementioned

TABLE 17. Appraisal among the single-phase unidirectional SEPIC-derived modified PFC topologies (Figure 20 and Figure 21).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless SEPIC – Type 1 (FIGURE 20(a)) [105]	L: 3 C: 4 SW: 2 SD: 0 FD: 2 **Total: 11**	L: 3 C: 4 SW: 1 SD: 0 FD: 1 **Total: 9**	DICM	200 V-400 V	3.6 mH and 377 µH at 200 W f_{SW} at 50 kHz C_{DC} at 440 µF	Low (Three/or Four Inductors Can be Coupled on the Same Magnetic Core)	91%-97% at 60 W-200 W	Medium
Bridgeless SEPIC – Type 2 (FIGURE 20(b)) [52]	L: 3 C: 3 SW: 2 SD: 2 FD: 1 **Total: 11**	L: 3 C: 3 SW: 1 SD: 1 FD: 1 **Total: 9**	DICM	48 V	2.2 mH and 68 µH at 65 W f_{SW} at 50 kHz C_{DC} at 2200 µF 1 µF		91%-93% at 20 W-100 W	Medium
Bridgeless SEPIC – Type 3 (FIGURE 20(c)) [110]	L: 3 C: 4 SW: 2 SD: 2 FD: 3 **Total: 14**	L: 3 C: 3 SW: 1 SD: 1 FD: 2 **Total: 10**	DICM	400 V	2.2 mH and 180 µH at 200 W f_{SW} at 50 kHz C_{DC} at 1000 µF 1.2 µF		96%-97% at 50 W-200 W	High
Bridgeless SEPIC – Type 4 (FIGURE 20(d)) [111]	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	CICM	60 V	600 µH and 200 µH at 100 W f_{SW} at 65 kHz C_{DC} at 1.8 mF 1 µF		89%-94% at 20 W-100 W	High
Bridgeless SEPIC – Type 5 (FIGURE 20(e)) [112]	L: 3 C: 3 SW: 1 SD: 4 FD: 1 **Total: 12**	L: 2 C: 3 SW: 1 SD: 3 FD: 1 **Total: 10**	DICM	48 V	2.2 mH and 22 µH at 160 W f_{SW} at 50 kHz C_{DC} at 3300 µF 1 µF		Not Reported	Medium
Bridgeless SEPIC – Type 6 (FIGURE 21(a)) [113]	L: 4 C: 3 SW: 1 SD: 2 FD: 4 **Total: 14**	L: 2 C: 2 SW: 1 SD: 1 FD: 2 **Total: 8**	CICM	50 V	f_{SW} at 100 kHz L and C Values Not Reported		91% at 100 W	High
Interleaved SEPIC with a DBR (FIGURE 21(b)) [114]	L: 4 C: 3 SW: 2 SD: 4 FD: 2 **Total: 15**	L: 1 C: 1 SW: 1 SD: 1 FD: 0 **Total: 4**	CICM	200 V-420 V	600 µH and 480 µH at 3.3 kW f_{SW} at 100 kHz C_{DC} at 2 mF 10 µF		Not Reported	High
Interleaved SEPIC with a DBR (FIGURE 21(b)) [115]	L: 4 C: 3 SW: 2 SD: 4 FD: 2 **Total: 15**	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	DICM	50 V-200 V	400 µH at 500 W f_{SW} at 150 kHz C_{DC} at 2 mF 1 µF		91%-97% at 100 W-500 W	High

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches.
*The number of devices operating per half-cycle.

positive output Luo circuits with a single-switch converter configuration. Also, double output Luo converters have been introduced by an interleaved symmetrical circuit configuration to enable double-positive supply. Besides the self-lift technique, which enhances the voltage gain in arithmetic progression, a powerful voltage boosting technique known as the super-lift has been introduced to Luo converters to escalate the voltage gain in geometric progression. Several circuit configurations have been introduced for the super-lift positive output Luo converter, which has a higher voltage boosting capability compared to the positive output Luo converters. However, due to the limited step-up functionality, the

TABLE 18. Appraisal among the single-phase unidirectional Cuk-derived modified PFC topologies (Figure 23).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless Ćuk – Type 1 (FIGURE 23(a)) [119]	L: 3 C: 3 SW: 2 SD: 2 FD: 1 **Total: 11**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DICM	48 V	1 mH and 22 µH at 300 W f_{SW} at 50 kHz C_{DC} at 12000 µF 1 µF	High (DICM Operation)	94%-95% at 10 W-300 W	Medium
Bridgeless Ćuk – Type 3 (FIGURE 23(c)) [121]	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DICM	300 V	1 mH and 22 µH at 300 W f_{SW} at 50 kHz C_{DC} at 12000 µF 1 µF	High (DICM Operation)	87%-90% at 150 W-850 W	High
Improved Bridgeless Ćuk – Type 3 (FIGURE 23(c)) [121]	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	Input Inductors in CICM and Output Inductors in DICM	300 V	4 mH and 150 µH at 900 W f_{SW} at 50 kHz C_{DC} at 2000 µF 3 µF	Medium (CICM and DICM Operation)	88%-92% at 150 W-850 W	High
Bridgeless Ćuk – Type 4 (FIGURE 23(d)) [120]	L: 3 C: 3 SW: 1 SD: 2 FD: 3 **Total: 12**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DICM	48 V	1 mH and 22 µH at 150 W f_{SW} at 100 kHz C_{DC} at 2 mF 1 µF	High (DICM Operation)	90%-97% at 150 W	Medium
Inductor Switched Ćuk with a DBR (FIGURE 23(e)) [122],[125]	L: 3 C: 2 SW: 1 SD: 4 FD: 2 **Total: 12**	L: 2 C: 2 SW: 1 SD: 2 FD: 2 **Total: 9**	CICM	48 V	15 mH and 4.5 mH at 500 W f_{SW} at 25 kHz C_{DC} at 8000 µF 4.5 µF	Medium (CICM Operation)	78%-84% at 200 W-850 W	Medium
Bridgeless Inductor Switched Ćuk (FIGURE 23(f)) [125]	L: 3 C: 2 SW: 2 SD: 2 FD: 2 **Total: 11**	L: 3 C: 2 SW: 2 SD: 1 FD: 2 **Total: 10**	Input Inductor in CICM and Output Inductors in DICM	45 V-65 V	6 mH and 40 µH at 850 W f_{SW} at 20 kHz C_{DC} at 11.75 mF 0.94 µF	Medium (CICM Operation)	79%-87% at 200 W-850 W	Medium

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches.
*The number of devices operating per half-cycle.

positive output Luo PFC converters suffer from a similar disadvantage as the Boost PFC topologies (i.e., the requirement of additional step-down DC-DC integration for the battery voltage matching and high-stress in the components at the down-stream stages). In addition, negative output Luo converters (derived from the fundamental single-switch Buck-Boost topology (FIGURE 9(c))) have been introduced. The elementary negative output Luo converter (FIGURE 27(a)) has an additional capacitor and inductor at the output side compared to the fundamental single-switch Buck-Boost converter.

A bridgeless elementary negative output Luo PFC topology (FIGURE 27(b)) in DICM has been studied in [135] for applications up to 400 W. The bridgeless elementary negative output Luo PFC topology has a discontinuous input current at both the positive and negative cycles (i.e., increased harmonics flow and EMI interference) due to the direct input connection to a switch. While continuous output current is achieved with the output inductor. Besides, an auxiliary inverting circuit is required for the negative output DC voltage. A performance evaluation of the bridgeless elementary negative output Luo topology was conducted under the following testing conditions: input AC voltage between 173 V-267 V, output DC voltage between 50 V-200 V, and power demand between 100 W-400 W. The current THD was between 4%-9.9%, the *pf* was between 0.98-0.99, and the IEC 61000-3-2 limits were met and were below the standards. However, the converter's efficiency performance was not remarked. An interleaved elementary negative output Luo PFC converter (FIGURE 27(c)) in DICM has been addressed in [136] for EV charging applications with power upto 750 W. The two interleaved branches in

TABLE 19. Appraisal among the single-phase unidirectional Zeta-derived modified PFC topologies (Figure 25).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless Zeta – Type 1 (FIGURE 25(a)) [127]	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DICM	60 V	500 µH and 500 µH at 150 W f_{SW} at 30 kHz C_{DC} at 990 µF 1 µF	High (DICM Operation)	87%-95% at 20 W-40 W	High
Bridgeless Zeta – Type 2 (FIGURE 25(b)) [129]	L: 2 C: 3 SW: 2 SD: 0 FD: 2 **Total: 9**	L: 2 C: 2 SW: 1 SD: 0 FD: 1 **Total: 6**	DICM	300 V-400 V	1 mH and 25 µH at 1 kW f_{SW} at 20 kHz C_{DC} at 400 µF 10 µF	High (DICM Operation)	Not Reported	Medium
Interleaved Zeta with a DBR (FIGURE 25(c)) [130]	L: 4 C: 3 SW: 2 SD: 4 FD: 2 **Total: 15**	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	Input Inductors in CICM and Output Inductors in DICM	200 V	698 µH and 189 µH at 400 W f_{SW} at 50 kHz C_{DC} at 480 µF 940 nF	Medium (CICM Operation)	77%-91% at 50 W-400 W	High

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches.
*The number of devices operating per half-cycle.

TABLE 20. Appraisal among the single-phase unidirectional Luo-derived modified PFC topologies (Figure 27).

Topology	Device Count	Devices Operating*	Operating Mode	Output Voltage	Sizing	EMI Noise	Efficiency	Cost
Bridgeless Elementary Negative Output Luo (FIGURE 27(b)) [135]	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	Input Inductors in DICM and Output Inductors in CICM	50 V-200 V	1.78 mH and 189 µH at 400 W f_{SW} at 20 kHz C_{DC} at 2200 µF 0.44 µF	High (DICM Operation)	Not Reported	High
Interleaved Elementary Negative Output Luo with a DBR (FIGURE 27(c)) [136]	L: 4 C: 3 SW: 2 SD: 4 FD: 2 **Total: 15**	L: 4 C: 3 SW: 2 SD: 2 FD: 2 **Total: 13**	Input Inductors in DICM and Output Inductors in CICM	300 V	50 µH and 2.35 mH at 750 W f_{SW} at 20 kHz C_{DC} at 800 µF 440 nF	Low (Inductors' Current Ripple 180° Phase-Shifted)	60%-90% ar 100 W-750 W	High
Bridgeless Modified Elementary Positive Output Luo – Type 1 (FIGURE 27(d)) [138]	L: 3 C: 2 SW: 2 SD: 2 FD: 2 **Total: 11**	L: 2 C: 2 SW: 1 SD: 1 FD: 1 **Total: 7**	DICM	48 V	50 µH and 288 µH at 100 W f_{SW} at 20 kHz C_{DC} at 2200 µF 1.1 µF	High (DICM Operation)	Not Reported	Medium
Bridgeless Modified Elementary Positive Output Luo – Type 2 (FIGURE 27(e)) [139]	L: 3 C: 3 SW: 2 SD: 0 FD: 2 **Total: 10**	L: 2 C: 2 SW: 1 SD: 0 FD: 1 **Total: 6**	Input Inductors in DICM and Output Inductors in CICM	300 V	4 mH and 0.15 mH at 850 W f_{SW} at 20 kHz C_{DC} at 2 mF 3 µF	Medium (CICM Operation)	60%-90% at 150 W-850 W	Medium

Where C is the number of capacitors, L is the number of inductors, SW is the number of switches, SD is the number of slow diodes, and SF is the number of fast diodes. C_{DC} is the DC link capacitor across the battery. f_{SW} is the switching frequency of the switches.
*The number of devices operating per half-cycle.

FIGURE 27(c) operate in a 180° phase shift with respect to each other. The interleaved elementary negative output Luo PFC topology was tested under the following testing conditions: input AC voltage between 160 V-260 V, output DC voltage by 300 V, and power demand between 100 W-750 W. Unity *pf* was achieved with an efficiency between 60%-90% for the aforementioned power range, while the current THD was between 1.5%-2% at the full-loading condition.

In [137], an isolated positive output Luo PFC converter with DBR integration (i.e., bulky transformer requirement)

has been studied for EV charging and power up to 750 W, yet, the efficiency of the PFC converter was between 70%-90-% for applications between 350 W-750 W. A bridgeless configuration for a non-isolated modified elementary positive output Luo topology (FIGURE 27(d)) in DICM has been investigated in [138] for power applications up to 100 W. Compared to the bridgeless elementary negative output Luo topology, the inverting circuitry is eliminated, yet, a bulky AC filter is attended at the input side due to the EMI emissions from the discontinuous input current (direct switch connection to the input AC supply). Besides, the elementary positive output Luo converter is modified to allow Buck mode operation. The topology in FIGURE 27(d) was tested for input AC voltage between 90 V-260 V, output DC voltage by 48 V, and power demand at 100 W. The performance evaluation of the converter showed that the current THD was between 1.2%-1.8% and *pf* was between 0.993-0.999. However, no data was provided for the converter's efficiency performance. Another type of bridgeless modified elementary positive output Luo topology (FIGURE 27(e)) has been introduced in [139] for EV charging applications with power up to 850 W. The topology in FIGURE 27(e) is similar to the bridgeless Buck-Boost PFC topology in FIGURE 17(d). Two Luo converters are interleaved, and each converter operates for a half-cycle. The input current and output currents in the bridgeless topology in FIGURE 27(e) are continuous. Therefore, the current THD is mitigated, and the EMI filter size is reduced. Nevertheless, the series switch connection complicates the gate drive design. For control simplicity and alleviated input filter, the input inductor can operate in CICM, while the output inductor can operate in DICM. The bridgeless topology in FIGURE 27(e) was tested under the following testing conditions: input AC voltage between 170V-260 V, output DC voltage by 300 V, and power demand between 150 W-850 W. Unity *pf* was achieved with the current THD between 1.8%-2.3%. While the PFC converter efficiency integrated by a fly-back DC-DC converter was between 60%-90%.

A summary of the operating performance conditions of the above-mentioned Luo-based topologies is presented in TABLE 13.

A summarized appraisal among the covered modified PFC topologies is presented in TABLE 14 to TABLE 20. Nevertheless, a proper performance assessment among the presented unidirectional non-isolated PFC topologies requires designing and benchmarking the topologies under similar testing conditions and design requirements. However, the overall PFC topologies configuration, merits, and demerits can give an initial overlook over the converter control complexity, the number of the passive elements and semiconductor devices, the operating modes (step-up and/or step down), devices' voltage and current stress, down-stream converter requirement, EMI interference, harmonics contamination level, gate drives' design, thermal cooling, power density, and converter sizing.

VIII. CONCLUSION

Pure electrified transportation, electric-based vehicles, and clearance of diesel-based vehicles are the present and future visions for many developed countries. Power electronics play the main role in replacing diesel-based vehicle charging with battery-based vehicle charging. This work focused on the EV charging infrastructure Level 1 and Level 2 with a single-phase and unidirectional supply. To maintain the power quality of the grid to the international standards while charging the EV from the grid, an on-board PFC converter of high power factor, low harmonics content, and high efficiency at variable operating conditions (e.g., different supply levels and different battery voltages) is required with high power density and energy density for optimized losses, size, and cost consideration. A classification of the non-isolated single-phase unidirectional PFC converters was provided, and a comprehensive review of different topologies was showcased.

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