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COLLEGE OF ENGINEERING

QUASI IMPEDANCE SOURCE BASED HIGH POWER MEDIUM VOLTAGE CONVERTER FOR GRID INTEGRATION OF DISTRIBUTED ENERGY SOURCES

BY

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ABSTRACT

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Title, Quasi Impedance Source Based High Power Medium Voltage Converter for Grid Integration of Distributed Energy Sources

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The next generation of Power Electronics systems would need to be able to work at higher power levels, higher switching frequencies, compact size, and higher ambient temperatures, as well as should have improved energy efficiency than existing Silicon (Si) devices. As a result, new wide bandgap semiconductor technologies must be introduced to address Si's physical limitations. Silicon Carbide (SiC) devices are becoming popular because of their outstanding properties that address all the requirements of the next generation Power Electronics system.

On the other hand, the converter topology still plays a major role in deciding the overall system performance. Hence the major objective of this dissertation is to devise new multilevel quasi impedance source (qZS) based converter topologies using SiC devices to achieve a compact, highly efficient, and modular solution for grid integration of Solar PV Energy Source to the utility grid. Other objectives include modification in the PWM methods to address the problem of unequal power-sharing in Solar PV multilevel converters. By using qZS as the front-end power converter several different power converter topologies have been developed and presented in this dissertation. The

detailed design, modulation, loss analysis, and control have been developed for multi-module cascaded structure. Level-shifted PWM technique is developed at first for two cascaded modules which are similar to the standard Phase opposed disposed Pulse width modulation (PODPWM). However, this control method cannot be directly applied to a higher number of modules. For more than two cascaded modules a unified combined hybrid PWM technique is developed and presented. During normal balanced operation, the power among the modules is unequal. To address the unequal power-sharing problem, further modification in the PWM technique is done called the 'Carrier rotation' technique. For providing the isolation between the low voltage PV panels and the high voltage AC grid, a modified Inverter topology, and a new modulation technique is developed. The presented technique, however, is limited to a single module, and more research is needed to implement for cascaded structure.

Front-end qZS based single-stage DC-AC-DC converter is developed as an alternative of one of the most popular conventional dual active bridge (DAB) converter. The proposed converter offers reduced component count while maintaining the continuous input current. The detailed operation, modulation technique, simulation, and experimental result are presented to show the superiority of the developed qZS-Cascaded Multilevel Converter. The developed power converter has strong commercialization potential.

DEDICATION

To my family, friends and mentors who supported me throughout the duration of my studies.

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TABLE OF CONTENT

DEDICATION v

ACKNOWLEDGMENTS vi

LIST OF TABLES xiv

LIST OF FIGURES xv

ABBREVIATIONS xxi

CHAPTER 1: INTRODUCTION 1

1.1. Background/Motivations 1

1.2. The identified problems/shortcoming/drawbacks 6

1.3. Research Objective, ... 6

1.4. Advantages of the Proposed New Modulation Techniques and Converter Topologies 7

1.5. Research Problem and Literature Review 7

1.6. Research Contribution and Methodology, ... 11

1.7. Dissertation organization, ... 14

CHAPTER 2: OPERATION OF QUAZI Z- SOURCE POWER CONVERTERS 17

2.1. Introduction 17

2.2. Modulation and Operation principle of qZS Inverter 18

2.2.1. Active State Operation 19

2.2.2. Zero State Operation 19

2.2.3. Shoot-through State Operation 20

2.3. Inductor design and selection 21

2.4. Capacitor Design and Selection 21

2.5. Implementation of qZSI connected with PV panels 22

2.6. Experimental Results 24

2.7. Summary 25

CHAPTER 3: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR 5 LEVEL QUASI Z SOURCE INVERTER FOR PV SYSTEMS 27

3.1. Introduction 27

3.2. PS-PWM FOR qZS-CMI 28

3.2.1. Single Phase qZS-CMI, operation of qZSI 28

3.2.2. The relation between PS-PWM & APOD-PWM for qZS-CMI 29

3.3. Proposed APOD-PWM for qZS-CMI 31

3.3.1. Proposed APOD-PWM for Unequal Power-sharing 31

3.3.2. Proposed APOD-PWM for Equal Power-sharing 32

3.4. Switching Loss Analysis of Proposed PWM Methods 35

3.4.1. Switching loss analysis for PODPSPWM with carrier rotation (PODPS – I) 35

3.4.1.1. Switching losses in the active state 38

3.4.1.2. Switching losses in shoot-through states 39

3.4.2. Switching loss analysis for PODPS-PWM without carrier rotation (PODPS – II) 40

3.4.2.1. Switching losses in active state 41

3.4.2.2. Switching losses in shoot-through states 41

3.5. Simulation Results and Discussions 43

3.6. Experimental Verification of the proposed Modulation Scheme 46

3.7. Summary 50

CHAPTER 4: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR CASCADED MULTILEVEL QUASI IMPEDANCE SOURCE INVERTER 52

4.1. Introduction 52

4.2. System Description 53

4.3. Proposed PODPS-PWM for Multilevel qZSI 54

4.3.1. PODPS-PWM Modulation 54

4.3.2. The relation between PS-PWM & PODPS-PWM 56

4.4. Comparison of Switching losses 58

4.4.1. Switching losses in the active state 59

4.4.2. Switching losses in shoot-through state 60

4.5. Experimental Results and Discussion 61

4.5.1. THD Performance of proposed PWM switching 62

4.5.2. Multilevel Operation with PODPS-PWM, ... 63

4.5.3. Unequal Power-sharing with PODPS-PWM 64

4.5.4. Validation of switching losses with switching pulses..... 65

4.6. Summary 67

CHAPTER 5: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR EQUAL POWER-SHARING AMONG QUASI Z SOURCE MODULES IN CASCADED MULTILEVEL INVERTER 68

5.1. Introduction, ... 68

5.2. Single Phase qZS-CMI, Characteristics of qZSI..... 69

5.3. PODPS-PWM for Single Phase QZS-CMI 70

5.3.1. PODPS-PWM for qZS-CMI 70

5.3.2. Relation between PS-PWM & PODPS-PWM for qZS-CMI..... 71

5.4. Proposed Modified PODPS-PWM for QZS-CMI..... 74

5.4.1. Method 1, Single Cycle Carrier Rotation 74

5.4.2. Method 2, Two Cycle Carrier Rotation 76

5.4.3. Method 3, Three Cycle Carrier Rotation 76

5.5. Switching Loss Analysis 77

5.5.1. Power loss in Equal power distribution 78

5.5.1.1. Switching losses in active state 78

5.5.1.2. Switching losses in shoot-through states..... 79

5.5.2. Power loss in Un-Equal power distribution 80

5.5.2.1. Switching losses in active state 80

5.5.2.2. Switching losses in shoot – through state..... 81

5.6. Detailed Simulation Results and Discussions 82

5.7. Experimental Verification of the proposed Modulation Scheme 84

5.8. Summary 90

CHAPTER 6: A 4-MW CASCADED MULTILEVEL INVERTER FOR SOLAR PV POWER CONVERSION SYSTEM 91

6.1. Introduction, ... 91

6.2. Modulation and Mathematical Analysis 92

6.3. Control strategy 93

6.4. Simulation Results..... 95

6.5. Summary 98

CHAPTER 7: NOVEL ISOLATED QUASI Z-SOURCE INVERTER FOR TRANSFORMERLESS GRID-CONNECTED SOLAR PV APPLICATIONS..... 100

7.1. Introduction, ... 100

7.2. QZSI for Transformerless Grid Integration 102

7.3. PWM Generation and Operating Modes of QZSI..... 103

7.4. Common-mode Voltage Analysis 107

7.5. Losses in The Semiconductor Devices..... 109

7.5.1. HB module loss..... 110

7.5.2. Auxiliary switch loss....110
7.5.3. qZS network diode loss....111
7.6. Experimental Results....111
7.7. Summary....116
CHAPTER 8: ISOLATED QUAZI Z-SOURCE NETWORK-BASED POWER CONVERTER 118
8.1. Introduction....118
8.2. Isolated QZS based Conversion system....120
8.2.1. Operating modes and circuit analysis....120
8.3. Components Design....124
8.3.1. Inductor design and selection....124
8.3.2. Capacitor design and selection....125
8.3.3. Transformer design....125
8.4. Simulation results and discussion....128
8.5. Summary....130
CHAPTER 9: HIGH VOLTAGE HIGH POWER MULTILEVEL CONVERTER FOR SOLAR PV APPLICATIONS TO THE UTILITY GRID....132
9.1. Introduction....132
9.2. qZS-CMC based PV power system....133
9.2.1. System Configuration....133

9.2.2. Operating Principle 135

9.3. 4 MW Isolated Quasi Powered Multilevel Converter, Control Algorithm, 136

9.3.1. Controller Unit 136

9.3.2. Modular Sine PWM Generation 138

9.4. Simulation results and discussion 139

9.5. Summary 142

CHAPTER 10: CONCLUSION AND FUTURE WORK 143

10.1. Conclusion 143

10.2. Future Work 146

CHAPTER 11: Appendix 148

11.1. Under equal power distribution condition 148

11.2. Under un-equal power distribution condition 149

11.3. Published Research Papers 150

References, ... 151

LIST OF TABLES

Table 2.1. Simulation parameters……. 22

Table 3.1. Active and shoot – through switching over a fundamental cycle.. 37

Table 3.2 Active and shoot – through switching over a fundamental cycle for PODPS – II…… 41

Table 3.3 Comparison of proposed PWM methods with PSPWM……. 42

Table 3.4. Component specifications for qZSI-CMI…… 43

Table 4.1. Active and shoot-through pulses for a modulating cycle…… 59

Table 4.2. Switching losses comparison for different modulations…… 61

Table 4.3 Quasi Impedance Source Inverter parameters ……. 62

Table 5.1. Comparison of switching losses in different modulation methods. 80

Table 5.2. Comparison of switching losses in different modulations…… 82

Table 5.3. Component specifications for qZSI-CMI…… 82

Table 6.1. Simulation Parameters…… 96

Table 7.1. Simulation parameters…… 111

Table 8.1 Simulation parameters for proposed isolated qZS inverter……. 128

Table 9.1 Simulation setup parameters for multilevel qZS inverter connected to utility grid…….. 139

Table A. Characteristics of different switches in different modulation region.. 148

Table B. Active and shoot-through pulses for a modulating cycle……. 149

LIST OF FIGURES

Figure 1.1. Distributed energy system with grid interface…….. 1

Figure 1.2. Investigated scheme in the dissertation, Solar PV to Grid via DC-DC and then DC-AC power converters…… 2

Figure 1.3. Z-Source Inverter…….. 4

Figure 1.4. Different LS-PWM schemes…… 10

Figure 1.5. Block diagram of the proposed two-stage power conversion….. 13

Figure 1.6. Proposed Cascaded MLI…….. 13

Figure 1.7. Proposed Interleaved qZS based Converter…… 14

Figure 2.1. PV to Ac grid-connected qZS Inverter……. 17

Figure 2.2. Modulation comparison and Operating states……. 18

Figure 2.3. Simulation results at 120V, 1.2kw and 0.99pf…….. 22

Figure 2.4. Performance Analysis of qZSI system with proposed PWM…… 24

Figure 2.5. Hardware setup……. 25

Figure 2.6 Performance of qZSI system……. 26

Figure 3.1. Conventional LS-PWM Techniques……. 27

Figure 3.2. Single phase qZS-CMI PV power system…… 29

Figure 3.3. Geometrical analysis for the relation between the PS-PWM and PODPS-PWM…… 29

Figure 3.4. Proposed APOD-PWM for unequal power……. 32

Figure 3.5 Proposed carrier rotation techniques of the APOD-PWM for Equal power distribution between the qZS-CMI modules…… 33

Figure 3.6. Detailed switching gate pulse of the proposed three carrier rotation techniques of the APOD-PWM for Equal power distribution between the qZS-CMI modules…….. 35

Figure 3.7. Identification of different regions of switching during carrier rotation for bottom module……. 36

Figure 3.8. Identification of different regions of switching for bottom module switches…….. 40

Figure 3.9. Harmonic spectra of load voltage and load current with different proposed APOD-PWM techniques……. 44

Figure 3.10. Shows the photograph of the experimental setup…… 46

Figure 3.11. APOD-PWM for unequal power-sharing between modules…… 47

Figure 3.12. APOD-PWM for equal power-sharing between modules for single cycle carrier rotation……. 47

Figure 3.13. APOD-PWM for equal power-sharing between modules for two cycle carrier rotation…… 49

Figure 3.14. APOD-PWM for equal power-sharing between modules for three cycle carrier rotation…….. 49

Figure 3.15. Per module Efficiency comparison…… 50

Figure 4.1. Three – phase seven-level qZSI connected to RL load……. 53

Figure 4.2. PSPWM and LS PWM…… 55

Figure 4.3. Graphical analysis for the relation between the PS-PWM and PODPS-PWM……. 57

Figure 4.4. Output voltage levels and the output current with FFTs ……. 62

Figure 4.5. Voltage waveforms for line voltage (blue), module output voltages, top (pink), middle (green) and bottom (red)…… 63

Figure 4.6. Module level waveforms of CMLI output voltage (pink), inductor current (red), input voltage (blue) and bridge output voltage (green)……. 64

Figure 4.7. Switching pulses waveforms for the four switches showing S_{n1} (blue), S_{n2} (pink), S_{n3} (green), S_{n4} (red) where n =1 (bottom), 2 (middle) and 3(top)……... 66

Figure 5.1. Different LS-PWM schemes……. 68

Figure 5.2. Single phase qZS-CMI PV power system…… 70

Figure 5.3. PODPS-PWM for qZS-CMI……. 71

Figure 5.4. Graphical analysis for the relation between the PS-PWM and PODPS-PWM……. 72

Figure 5.5. Different carrier rotation techniques of the PODPS-PWM for the qZS-CMI…….. 75

Figure 5.6. Harmonic spectra of load voltage with (a) PODPS-PWM, proposed method…… 83

Figure 5.7. Shows the photograph of the experimental setup……. 84

Figure 5.8. Seven-level qZS-CMI output voltage and output load current waveforms along input qZS inductor current and HB input voltage……. 85

Figure 5.9. Equal Power distribution, The bottom, middle and top modules three level output voltages along with their cascaded seven level output voltage…… 86

Figure 5.10. Unequal Power Distribution, Voltage waveforms for output voltage (blue), module output voltages, top (pink), middle (green) and bottom (red)…… 86

Figure 5.11. Steady state operation of the individual modules while generating seven – level output voltage collectively…….. 88

Figure 5.12. Equal power-sharing between the modules during the different load currents……... 89

Figure 6.1. Proposed 4MW qZS-CMI, 16 modules per phase…… 92

Figure 6.2. qZS CMI PV power control system algorithm……. 93

Figure 6.3. Control algorithm for the DC-link control…… 94

Figure 6.4. Block diagram for the grid current control…….. 94

Figure 6.5. qZS DC-link voltages…… 96

Figure 6.6. qZS inductor currents……..... 96

Figure 6.7. qZS inductor currents and DC-link voltages……. 97

Figure 6.8. Three phase grid currents and voltages……. 97

Figure 6.9. Grid current THD…… 98

Figure 6.10. 33 level qZS CMI output voltage…… 98

Figure 6.11. Total output active and reactive power…… 98

Figure 7.1. Connection topologies of PV systems …….. 101

Figure 7.2 Proposed QZSI with additional switches. ……. 102

Figure 7.3. Proposed Modified PWM signals for the transformer-less grid-connected QZSI topology…… 104

Figure 7.4. All six operating modes of proposed Quasi Z-Source Inverter with additional switches…….. 106

Figure 7.5. Common-mode current flow in PV system…… 107

Figure 7.6. Common-mode current paths in positive half cycle……. 108

Figure 7.7. Hardware setup……. 112

Figure 7.8. Experimental results of proposed qZSI…… 112

Figure 7.9. Switching cycle showing all operating states 1,powering 2,freewheeling 3,shoot-through 4,freewheeling 5,powering……. 113

Figure 7.10. Switching currents validating the proposed PWM algorithm…. 114

Figure 7.11. Switching current in (a) positive half cycle (b) negative half cycle…… 115

Figure 7.12 qZSI performance (a) unity power factor (b) lagging power factor……... 115

Figure 7.13. Efficiency of the proposed QZSI converter…… 116

Figure 8.1. PV output to the 1-phase AC conversion system…….. 119

Figure 8.2. Proposed single-stage DC-AC conversion system…… 120

Figure 8.3. Switching logic of the proposed system…… 120

Figure 8.4. All the operating modes of the proposed isolated converter…… 121

Figure 8.5. Flowchart showing design process of the high-frequency transformer……... 126

Figure 8.6. qZS network component voltages and currents…… 129

Figure 8.7. HFT primary and secondary side voltages and currents respectively…….. 129

Figure 8.8. VDR diode voltages and capacitor voltages along with the DC-link voltage with the HB current……. 130

Figure 8.9. Output AC voltage and the load current of the proposed converter……. 130

Figure 9.1. Configuration of the qZS-CMC PV power system…… 134

Figure 9.2. Submodule of the proposed qZS-CMC…….. 135

Figure 9.3 Control algorithm of proposed converter consisting of controller unit, signal processing unit and modular switching signal generation unit…. 137

Figure 9.4. Transient response of system for change in active and reactive power references…… 140

Figure 9.5 Tracking performance of active and reactive power producing d and q axes currents……... 140

Figure 9.6. Grid voltage, current and converter voltage waveforms for unity pf operation……. 140

Figure 9.7 Grid voltage/current and converter voltage waveforms for lagging pf operation……. 141

Figure 9.8. Grid voltage/current and converter voltage waveforms for leading pf operation……. 141

ABBREVIATIONS

AC	Alternating Current
APOD-PWM	Alternate Phase apposed disposed Pulse width modulation
CHB	Cascaded H Bridge
CML-qZSI	Cascaded multilevel quazi Z-source inverter
CR-PWM	Carrier rotation Pulse width modulation
CR	Carrier rotation
DC	Direct Current
HB	H bridge
kHz	Kilo hertz
KVA	Kilo Volt-ampere
KVAR	Kilo Volt-ampere reactance
KW	Kilo Watt
LS-PWM	Level Shift pulse width modulation
M	Modulation index
MLI	Multilevel inverter
MOSFET	Metal Oxide semiconductor field effect transistor
MPPT	Maximum Power point Tracking
MVA	Mega Volt-ampere
MVAR	Mega Volt-ampere reactance
MW	Mega watt
PWM	Pulse width modulation
PD-PWM	Phase disposed pulse width modulation

POD-PWM	Phase opposed disposed pulse width modulation
PODPS-PWM	Phase opposed disposed phase shifted pulse width modulation
PS-PWM	Phase shifted pulse width modulation
PV	Photovoltaic
qZS-CMI	quazi Z-source Cascaded multilevel inverter
qZS	quazi Z-source
qZSI	quazi Z-source inverter
THD	Total harmonic distortion
VDR	Voltage double rectifier

CHAPTER 1: INTRODUCTION

1.1. Background/Motivations

The depleting fossil fuel and environmental concerns have led to the development of alternative clean sources of electrical energy, more popularly known as renewable energy sources (RES). These sources are mostly in the form of distributed energy sources (DES). Among several developed DES, solar Photovoltaic and Wind energy systems are more promising sources of energy. The electrical energy share by Solar PV and Wind sources is increasing steadily due to wide acceptability across the globe. The form of electrical energy sources produced by DES needs some form of processing by Power converters. The power converter transforms the generated energy by DES in compatible form that suits the utility grid system. The integration of DES with utility grid using Power Converters poses several challenges. A huge amount of work is done and reported in the literature to resolve the upcoming challenges. A typical distributed energy system with different power converters is shown in Figure 1.1. The Figure 1.2

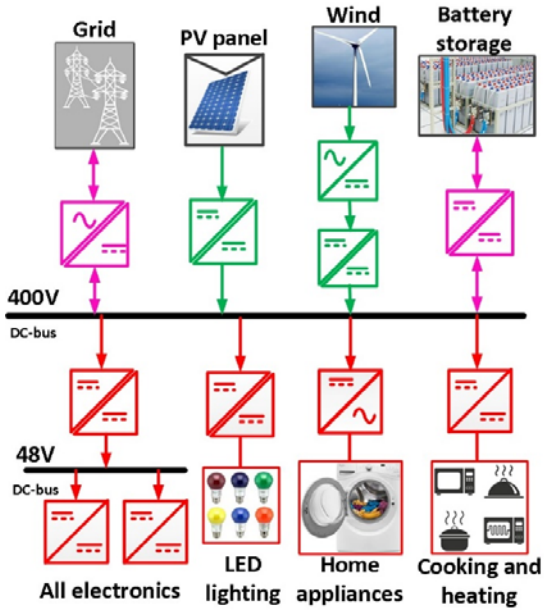


Figure 1.1. Distributed energy system with grid interface.

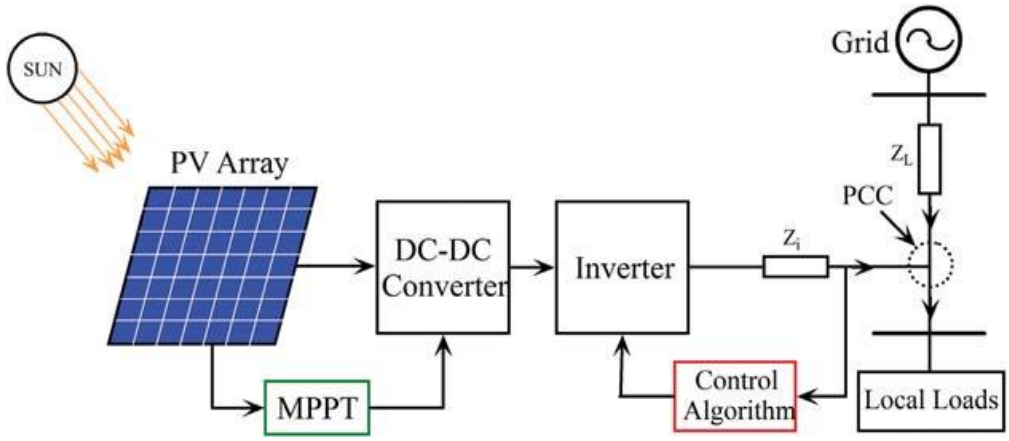


Figure 1.2. Investigated scheme in the dissertation, Solar PV to Grid via DC-DC and then DC-AC power converters.

shows the Investigated scheme in the dissertation. Which takes the input from the Solar PV feeds the generated power to the AC Grid by utilizing the DC-DC and then DC-AC power converters.

The most commonly used Power conversion systems in Solar PV grid integration consist of a boost converter, and a three-leg three-phase voltage source converter connected to the electric grid via a mains transformer (50 Hz) with a delta-star winding connection. The use of a transformer is necessary because of the inability to control three-phase three-leg converters in the case of an asymmetric load, which causes current to flow in the neutral conductor (common-mode current). This current is confined in the transformer windings connected in delta, without burdening further circuit elements. Hence it is inevitable to avoid bulky transformers in grid interfacing.

Due to the drawback of low efficiency, large volume and weight, and high cost, the transformer in the grid-connected PV system is being removed gradually. The inverter without a transformer is becoming popular in grid-connected distributed PV systems due to its high efficiency and low cost. However, the galvanic connection between the grid and PV array and the parasitic capacitance between the ground and PV panels

results in the appearance of a common-mode leakage current. The leakage current would decrease the conversion efficiency, and reduce the grid current quality, and induce the severe conducted and radiated EMI. To eliminate the common-mode current, its inducing principle is well studied and a model of common-mode current circuit is given in the literature. Basing on this model, several kinds of topologies and modulation methods have been proposed in the recent past. However, a limited study is done on the effect of common-mode leakage current in the cascaded multilevel inverter.

Transformerless topologies especially deserve more attention because of their higher efficiency, smaller size and weight, and cheap solution for the PV system (the price of the separating transformer reaches the price of the inverter). Hence, the proposed Ph.D. dissertation having one of the tasks as developing a transformerless power electronics solution for interfacing with renewable energy sources. The problems at hand are to address these two requirements, especially for the medium voltage grid. Although in the literature these problems are tackled using different hardware and software reconfiguration. The most common solution is to use a high-frequency transformer (HFT) to provide isolation between grid and solar PV. This is a cost-effective solution, since the use size, weight, and volume of high-frequency transformer is much smaller compared to the line frequency transformer. Additionally, PWM modification is also employed to address the common-mode voltage reduction.

The quality of the injected current is a prime concern in grid-interactive distributed energy sources. Hence to improve the quality of the output waveform, and to achieve high voltage, multilevel Inverter (MLI) are, therefore, employed. Multilevel inverters synthesize the voltage from several levels of voltages. Three popular topologies are evolved for multilevel inverters; namely, diode-clamped, flying capacitor, and cascaded H-Bridge. The major advantages of the multilevel inverters include low distortion in

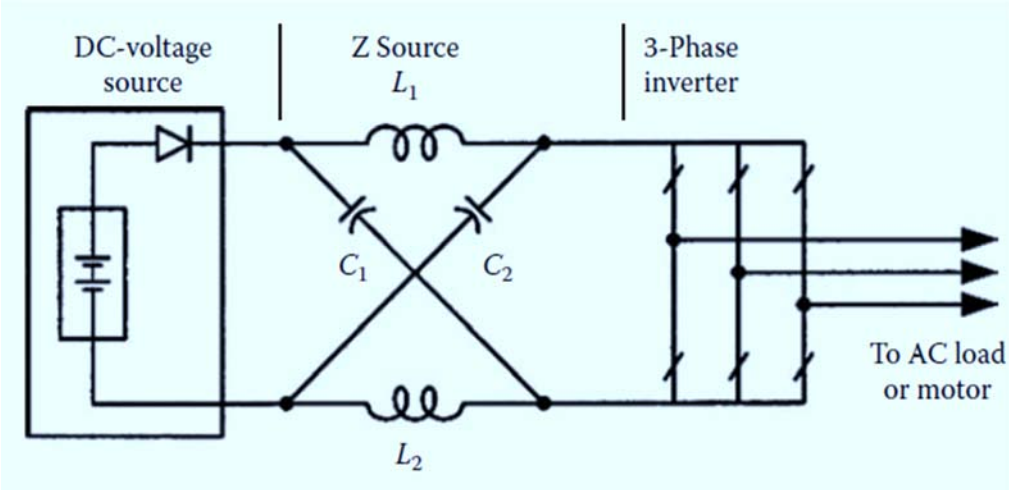


Figure 1.3. Z-Source Inverter

the output voltage waveform, reduced common-mode voltage, and improved input side current with lower filter requirement and possible to achieve high voltage. With all these attractive features, the control becomes complex, and reliability issues arise due to a large number of power devices being used. All these topologies have their relative advantages and disadvantages. This Ph.D. dissertation will also propose a new MLI topology and will address the aforementioned issues.

The conventional Power conversion between DES and utility grid is comprised of a DC-DC converter followed by a DC-AC inverter. The DC-DC converter is used to boost the small voltage produced by Solar PV. Also, the maximum power point tracking is done using the DC-DC converter. The Z-source inverter (ZSI) topology was first introduced as an alternative, shown in Fig. 1.2. It has the ability to buck or boost and invert the input dc voltage in a single-stage. It has gained tremendous interest in PV-grid-connected applications. The ZSI topology uses two capacitors and two inductors to boost the input dc voltage to match the inverter-side ac output voltage requirements. The operation of a ZSI is heavily dependent on the passive components. It presents an opportunity to integrate energy storage units into such a system. However, this suffers

from the drawback of discontinuous source side current. To overcome this a variant of ZSI, called quasi Z- Source Inverter (qZSI) was proposed. This evolved as a strong alternative to the conventional inverter. The cascaded structure of qZSI is reported in the literature to achieve a multilevel inverter. The proposed work will utilize the qZS module to come up with new converter topologies, which effectively feeds PV generated power to the utility grid at the medium voltage level. So a cascaded multilevel converter by utilizing the qZSI modules for the 4MW power rating has been detailed in the dissertation.

Intermittent input power availability is inescapable for distributed energy sources as it depends upon different environmental factors. Multilevel qZSI is popularly being used for the integration of distributed energy sources to the grid. These multilevel qZSI based converters also face the challenge of unequal power-sharing among different modules due to different factors like for PV – partial shading, dust accumulation, humidity, high temperature, and for wind depending upon different wind speeds. The main reason for this issue is the cascaded connection (used for achieving high voltage and high power) and implementation of the Phase-shifted Carrier-based PWM technique (PSCPWM) resulting in uneven distribution of power among various cascaded modules. During partial shading of at least one of the connected modules, healthy modules (not partially shaded) are pulled down to extract lower power due to cascaded connection and PSCPWM technique.

Usually, the generators used in wind energy generation system voltage are rated for a few kV while the power rating is high (in the range of MW). Thus huge current is produced, which poses several challenges on the power converter side. The available switch rating is not sufficient to handle such a huge amount of current. To address this issue, parallel-connected converters are employed. This problem will be addressed in

the presented dissertation. by developing novel interleaved power converters based on qZSI.

1.2. The identified problems/shortcoming/drawbacks

The identified problems/shortcoming/drawbacks with the existing transformerless Inverters based on qZS are;

1. The high-frequency Transformer (HFT) used in the existing solutions are underutilized
2. Since the turn ratio of HFT is 1,n, the design is more complex, such as the device ratings will be different at different stages of the converter
3. The current stress in the switches are high and non-uniform leading to a complex heat sink design
4. Limited range of operation (since the shoot-through duty can be varied for small values)
5. Most of the reported work uses Si-based switches hence are restricted to limited switching frequency operation
6. Each unit of cascaded modules in MLI, generate different power when level-shifted PWM is used in a solar PV grid integrated inverter system

1.3. Research Objective,

The objectives of the dissertation are to address the aforementioned drawbacks of the existing solution in isolated converters. Emerging semiconductor technologies like silicon carbide may play an important role in the referred developments as operation at higher switching frequencies without significant prejudice on the efficiency will be feasible, leading to the possibility of reducing the size of passive components and consequently the cost and volume of the converter circuit. On the other hand, the

converter topology still plays a major role in deciding the overall system performance. Hence the proposal is to devise new multilevel qZS based converter topologies using SiC devices to achieve a compact, highly efficient, and modular solution for grid integration of Solar PV Energy Sources. Other objectives include modification in PWM methods to address the problem of unequal power-sharing in Solar PV converters.

1.4. Advantages of the Proposed New Modulation Techniques and Converter Topologies

The envisaged advantages of the new converter Modulation Techniques and topologies are,

- Highly modular in nature
- Reduced cost due to use of equal rating devices (easy for batch processing)
- High gain (higher than the existing solutions)
- Use of 1,1 High-Frequency Transformer for isolation purpose
- Compact solution (reduced volume and cost)
- Fault-tolerant structure
- High efficiency
- Wide range of operation (shoot-through duty can be varied for large range)
- Equal Power-sharing among cascaded modules (due to modified PWM algorithm)
- High power quality due to interleaved and multilevel structures etc.

1.5. Research Problem and Literature Review

Currently, using cascaded multilevel H-bridge (CML-HB) inverter to the solar photovoltaic systems has become a widespread research topic, because of its many advantageous features like low dV/dt, medium voltage (MV)/ high voltage (HV) high

power transformerless solutions, distributed maximum power point tracking (D-MPPT), low total harmonic distortion (THD) and high modularity in nature [1, 2]. However, in conventional CML-HB-based solar PV power generating systems, every module operates as a voltage buck inverter and lacks a voltage boosting feature resulting in a greater number of modules to reach the rated voltage in MV/HV applications. Furthermore, each module (HB's) PV voltage variation leads to unbalancing of the dc-link voltage of the entire system. To add voltage boosting ability, a DC-DC converter has been employed in each HB module [3, 4]. Due to this, the system conventionally consists of two-stage conversion with complex circuitry, difficult control, and decreased system efficiency.

Recently proposed qZSI having the ability of single-stage power conversion had been used to build a single-stage cascaded multilevel topology [5]. It provides bucking and boosting of the applied input voltage while ensuring a continuous input current from the PV panels [6-10]. The qZS-CMI's proposed in [6, 7], adds the advantages of both conventional CML-HB and qZSI. The detailed comparison between qZS-CMI and CML-HB presented in [11], shows the superiority of the former resulting in the saving of one-third of modules (when compared to CML-HB).

In [6, 7, 12], PSCPWM was proposed for the qZS-CMI. This modulation is a standard sine-triangle comparison to generate the active and zero state switching signals. For the generation of the shoot-through state (ST), the carrier signal is compared with the constant duty. These shoot-through pulses are inserted between the active states (during zero output voltage vector). Furthermore, in [13] PI controllers-based DC-link voltage control is employed within the closed-loop control in all the modules. The semiconductors switch in all the modules share equal power. However, the switching is not optimal because all the modules are operating with the same switching frequency

for active pulses and twice the switching frequency for shoot-through pulses resulting in higher switching losses. For reducing the switching loss and increasing the boosting gain, phase-shifted pulse width amplitude modulation (PS-PWAM) was proposed in [6]. PS-PWAM implementation is complex and all the switches share different switching power loss which leads to different size requirements of heat sinks for different modules. Modular multilevel space vector pulse width modulation (MMSV-PWM) is reported in [14] for the three-phase qZS-CMI. MMSV-PWM is applied to three-phase systems which are computationally intensive (to continuously compute the coordinate transformation and the triangular functions). Application of shoot-through for a small duration requires high sampling to achieve smoother boosting gain control, which leads to high mathematical burden and can cause phase delay errors [14-16]. Model predictive control (MPC) is also reported for the qZSI in [17, 18], it achieved one control loop-based voltage and power control. However, MPC for multicell CMLI needs a high computational burden and a very difficult weight selection process hindering the practical applications. It is difficult to implement and it has been a bottleneck for researchers to implement it for the qZS-CMI applications. Multidimensional pulse width modulation (MD-PWM) [19], was proposed to improve the voltage control of the modules at a higher speed and accuracy by using the hysteresis controller. This results in unequal switching frequency leading to filter design complexity.

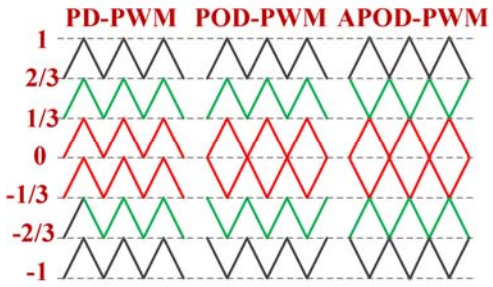


Figure 1.4. Different LS-PWM schemes

Furthermore, H-Bridge-based CMIs are also controlled with '2n' carrier signals, which are uniformly displaced vertically between '-1' to '+1'. This method is known as LS-PWM [20]. Mainly, LS-PWM includes phase disposition (PD-PWM), phase opposition disposition (POD-PWM), and alternative phase opposition disposition (APOD-PWM) methods. These different LS-PWM methods are shown in Figure 1.4. In [21], an attempt has been made to apply these LS-PWM techniques to five-level qZS-CMIs. The rotating carrier PWM technique applied to the CML-HB is reported in [22, 23]. Therefore, it can be observed from [21-23], that power distribution among the operating modules is uneven and the switching sequence is different for different modules resulting in increased input current distortion and higher THD. For high power applications, these harmonics consume a significant amount of power thereby limiting the practical applications. To address this power imbalance problem authors in [24-27] have proposed a novel technique by rotating the carriers for CML-HBI. To date, no such LS – PWM technique is applied to qZSI based CMI.

In view of the PV insulation demand, which is within the 1kilovolt (kV), the isolated converters have to be incorporated into the power conversion stage without compromising the efficiency and reliability at high power levels. Basic DC-DC isolated converters with qZS network- current source capability have been proposed in [28-30]. The variant of the different topologies with the qZS have been proposed and clearly

discussed in [30], they discussed the resonance phenomena, coupling of the transformers, symmetricity, number of inputs for increasing the efficiency and gain of the system. For reaching the transmission voltage level, a large number of modules have to be cascaded in series from the output side. It requires a large number of inputs; they can be achieved from the distributed PV panels. Improvements to this input parallel and output series (IPOS) cascaded converters are gaining popularity, especially for high input currents [31, 32]. The previously published chapters focused on the application of the boost half-bridge isolated current fed (CF) topology to the IPOS architecture, due to its simple structure and continuous input current. The impedance converters are capable of outperforming their CF counterparts in the recent emerging applications. However, the scarce chapters regarding the IPOS cascaded of the ISCs are minimal and deal with the wind power generation applications [33, 34]. While the solar PV [34], fuel cell, and battery energy storage applications are more demanding in terms of the input voltage range and DC voltage gain. In [35], a high gain DC-DC converter based on the Quazi Switched boost converter topology has been presented. Mahshid Amirabadi has extensively worked on the single-stage DC-AC and AC-AC power conversion with and without high-frequency isolation [36-41]. The single-stage multi-string inverter with a high-frequency AC link and soft-switching operation was discussed [42]. These single-stage converters do not require any electrolytic capacitors. Therefore, these converters are expected to have high efficiency, high power density and high reliability. The size of the converter is reduced by using high-frequency transformer. By considering these, the single-stage single-phase converters are proposed to work on for the dissertation. The major aims of the proposed work are to develop new converter topologies with isolation and without isolation.

1.6. Research Contribution and Methodology,

The methodology is based on a comprehensive literature review for understanding the gap in existing knowledge, proposing new converter topologies, mathematical modeling of the proposed converters, simulation studies, and experimental validation by developing laboratory prototypes. The focus of thesis research work lies in the development of high voltage and high-power converters for grid integration of solar PV energy systems. The key tasks that will be carried out are listed below,

1. Modulation, control, and implementation of the proposed isolated qZS based (Current Fed) DC-DC-AC converter (two-stage conversion).
2. Modulation, control and implementation of the single-stage isolated qZS based (Current Fed) DC-AC converter.
3. Modulation, control, and implementation of the cascaded qZSI for the distributed Maximum Power Point Tracking for the different irradiation conditions by using two-stage and single-stage isolated qZSI for the high-power High voltage applications (Input Series Output series Cascaded qZS converters).
4. Modulation, control and implementation of the Input Parallel Output Series isolated Quasi Z-source (i-qZSI) grid-connected inverter for wind energy sources applications.
5. The major issue of unequal power-sharing among cascaded modules in Solar PV applications is a well-known problem if level-shifted PWM is used. To address this concern, the PWM technique with unequal power distribution is proposed in this work which is not yet reported in the literature. Here, a novel LS – PWM technique will be developed for maximum power extraction from PV panels during partial shading. However, unequal power-sharing becomes a concern during normal full isolation operation (healthy condition) in terms of unequal component ratings and

PV side capacitor rating. To eliminate this, carrier rotation of novel LS – PWM technique is done to achieve equal power-sharing operation.

6. Active and reactive power control for grid-connected converters will be developed and implemented for zero and non-zero reactive power cases.
7. Experimental prototype development and testing of various power converters

The block diagram of the novel proposed converters is presented in Figure 1.5.

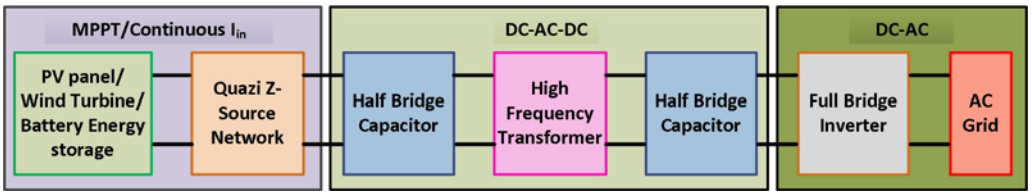


Figure 1.5. Block diagram of the proposed two-stage power conversion.

To achieve a high voltage high power modular structure, several units of Figure 1.5 are cascaded as shown in Figure 1.6.

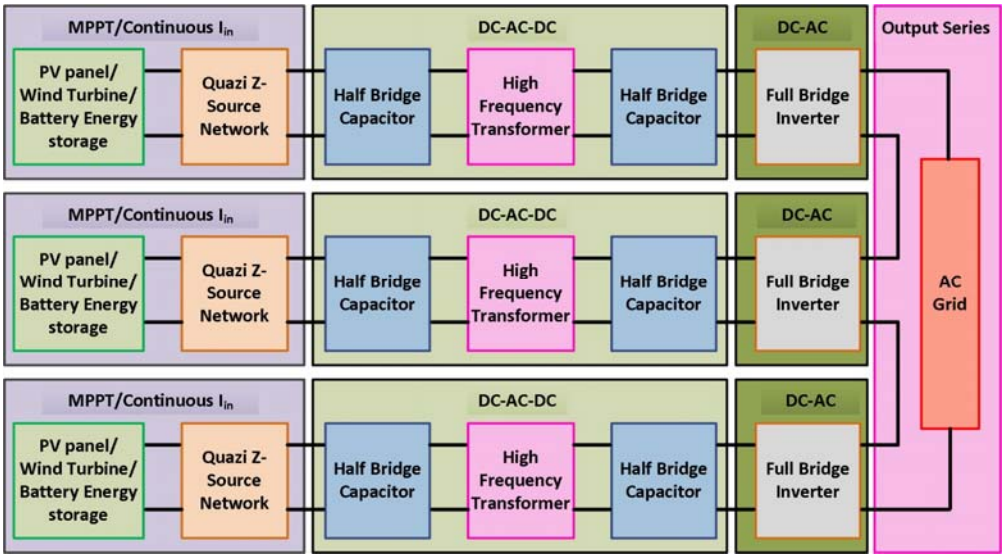


Figure 1.6. Proposed Cascaded MLI.

To address the high current sharing especially in the wind energy generation system,

several units of Figure 1.5 are used as interleaved structures as shown in Figure 1.7.

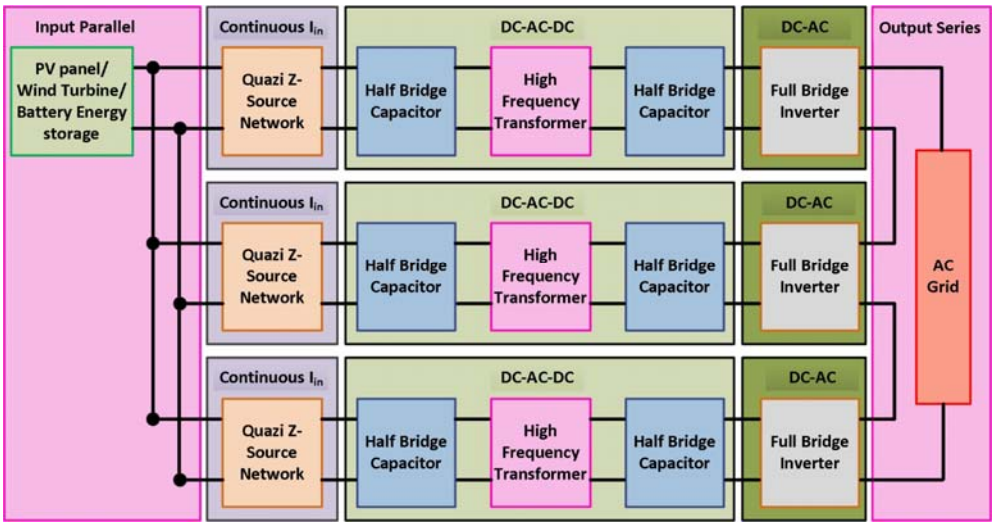


Figure 1.7. Proposed Interleaved qZS based Converter.

1.7. Dissertation organization,

The dissertation has been organized into the following chapters,

- Chapter 2, Covers the basic operation and design of the single-phase quasi z-source inverter. Where the mathematical analysis, design, simulation and experimental validation are detailed. PV integration is also discussed.
- Chapter 3, PS-PWM scheme causes higher switching losses and creates electromagnetic interference (EMI) problems for a higher number of cascaded modules. To address these issues, a novel modified LS-PWM technique is proposed to obtain equal power from cascaded modules under abnormal conditions. The direct use of the APOD-PWM results in unequal power-sharing between the qZSI modules, under all operating conditions. An effective carrier rotation is incorporated in the conventional APOD-PWM to make equal power-sharing between the qZSI modules. The proposed scheme is an excellent solution for the PV systems to address the problem of partial or complete

shading, temperature variation, PV module failure, and dust accumulation on the PV panels.

- Chapter 4, The developed PWM in chapter 3 is applicable only for the 2-cscaded modules and fails for more than the three modules. With this aim, a novel hybrid PODPS-PWM technique is proposed in this chapter for 3 to n number of modules. With the proposed PWM method reduced switching losses are achieved. A mathematical relation between the PSPWM and the proposed PODPSPWM has been deduced.
- Chapter 5, The above developed PODPS-PWM ensures optimal switching but suffers from uneven distribution of power among all the operating modules and also all the semiconductors of the same module, of qZSI. This chapter proposes a novel switching technique that combines the advantages of both PS-PWM and LS-PWM such as equal power distribution (among operating modules) and optimal switching sequence along with equal switch utilization. The proposed method is PODPS-PWM.
- Chapter 6, In this chapter a 4 MW grid-tied PV system by connecting qZS network into cascaded H-bridge (CHB) inverter. The proposed power conditioning system consists of 3-phase, 48 Module of HB inverters connected each with the qZS passive network.
- Chapter 7, Due to its single-stage conversion, the qZSI can be used as an efficient transformerless grid-tie inverter. However, the common-mode current is a major problem in transformerless topologies due to the absence of galvanic isolation. This chapter proposes a modified PWM technique to control the qZSI, along with two extra semiconductor switches, to reduce the common-mode current. The proposed topology can efficiently control the reactive power

and the suitable PWM scheme is also reported. Simulation results have been performed with the Standard Test conditions of the PV panel. Experimental results for a single-phase 500W prototype are presented to validate the proposed PWM scheme for the qZSI topology.

- Chapter 8, In this chapter, an Isolated Quazi Z-Source converter system has been proposed for the high-frequency operation, for the distributed power generation system. This system consists of PV side qZSI network, thus creates the continuous input current; High-frequency Transformer (HFT) for the isolation between the PV and AC side; Voltage Doubler Rectifier (VDR) for boosting the input voltage; finally HB for the DC-AC conversion. The high-frequency AC small-signal analysis for the qZS network has been presented with the effect of its passive components and its passive components affect on the operation of the entire system. The HFT design details presented as the special type of techniques needed to reduce the impact of skin effect and proximity effect. In the end, the simulation results validated the proposed system.
- Chapter 9, In this chapter, by utilizing the above-developed topology a QZS based Cascaded Modular Converter was proposed for the high power and high voltage PV systems. The proposed systems operating principle, control mechanism, and modulation have been discussed in detail. The Matlab/Simulink simulation results reported the suitability for the PV systems.
- Chapter 10, Conclusion is provided in Chapter 10 where all the results are summarized and recommendations are made. The future scope of work is also given.

CHAPTER 2: OPERATION OF QUAZI Z- SOURCE POWER CONVERTERS

2.1. Introduction

Figure 2.1, represents the qZS Inverter connected between the solar PV panels and the single-phase AC-grid. Here the PV is grounded through the standard grounding procedures. As the current in the input is continuous, small PV capacitor is needed. The capacitor voltage and the inductor current are utilized to operate the entire system at the Maximum Power Point (MPP). There are two inductors, two capacitors and one diode, altogether known as the Quazi Z-Source (qZS) network. The Output of the qZS network is connected to the standard H-Bridge (HB) semiconductor switches. In order to reduce the size of the passive components, high switching frequency is required. MOSFETs based on SiC technology can be operated at tens to hundreds of Kilo Hertz (kHz) switching frequency thereby reducing the size of the passive elements connected in the qZS network. The output for the HB is connected to the single-phase AC- grid through passive filters. Since the operating switching frequency is significantly high, the output filter size is also considerably reduced. This chapter discusses the basic operating principles of a qZSI. The modulation and control is elaborated. A novel PWM based on level shifted scheme is developed and reported. The developed PWM technique is the foundation of multilevel operation of cascaded qZSI that is further presented in the

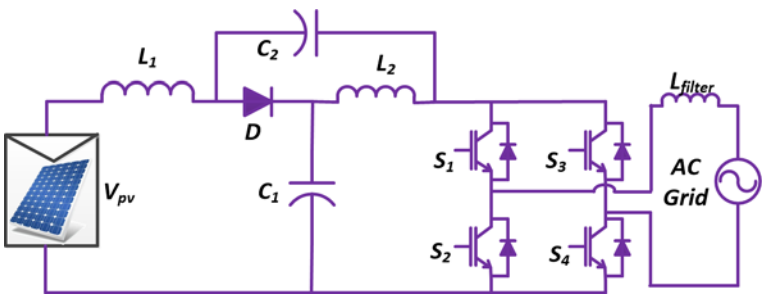


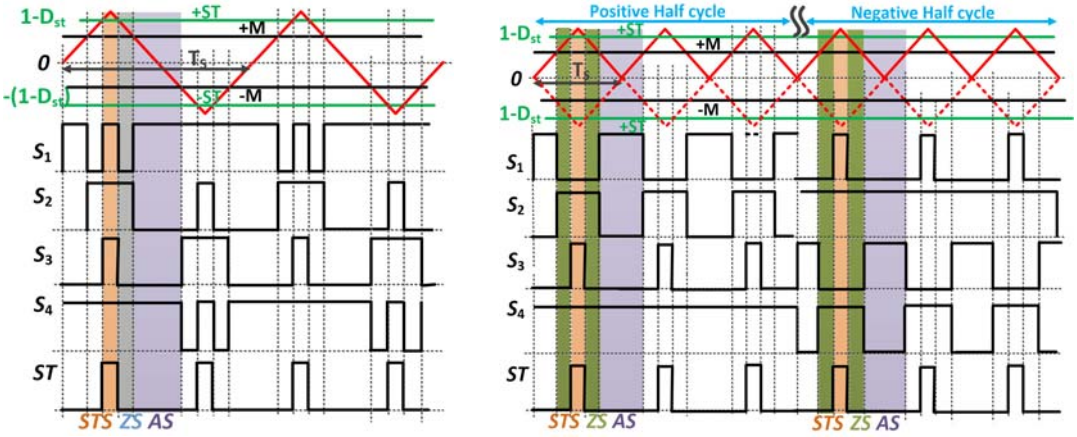
Figure 2.1. PV to Ac grid-connected qZS Inverter.

subsequent chapters.

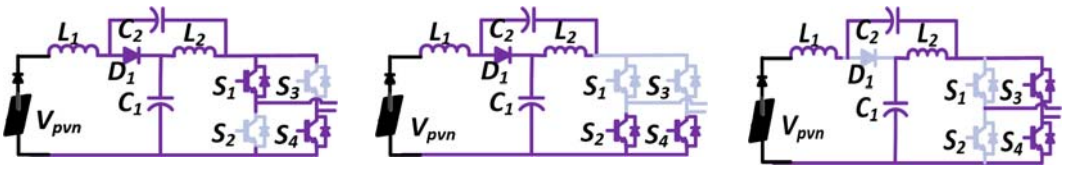
2.2. Modulation and Operation principle of qZS Inverter

A qZS inverter operate in two modes, i) shoot-through and ii) non-shoot-through. Figure 2.2, represents all the operating modes of the qZS Inverter along with its detailed modulation comparison between the proposed and the conventional algorithm/technique.

Figure 2.2(a) represents the conventional PWM technique and Figure 2.2(b) proposed modified PWM technique. In Figure 2.2(a)&(b) the red lines triangles are the carrier signals, black is the sinusoidal modulation signal (M), it is visible as a straight line because the switching frequency is very high and is shown for a small time, green lines are the shoot-through reference ($1\text{-}D_{st}$) and T_s represents the switching frequency of the carrier signal. The gate signals for the MOSFETs can be represented as the G_{S1}, G_{S2},



(a) Conventional Modulation (b) Novel Modulation technique



(c) Active State (AS) (d) Zero State (ZS) (e) Shoot-through State (STS) as S_3 and S_4 are ON

Figure 2.2. Modulation comparison and Operating states.

G_{S3} and G_{S4} and the shoot-through duty is represented by the D_{st}. It can be observed from both modulations that there are three operating modes as; i) active state, ii) zero state, and iii) the shoot-through state. However, the proposed modulation has the equal number of turn ON switching's states as that of carrier signals, however, in the conventional modulation, it is twice the number of switching carrier signals. So the proposed modulation will be having lesser number of switching losses than the conventional modulation. Below is the discussion for the operating states,

2.2.1. Active State Operation

In the positive active mode as shown in Figure 2.2(c), S_1 & S_4 are ON. At this mode, the output voltage of the QZS network becomes the summation of the voltages of the capacitors C_1 and C_2 which appear across the HB. During this mode, the qZS network diode will be turned ON. During this mode the mathematical equations can be represented as below,

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = i_{L1}(t) - i_{out} \\ C_2 \dfrac{dV_{C2}}{dt} = i_{L2}(t) - i_{out} \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) - V_{C1}(t) \\ L_2 \dfrac{di_{L2}}{dt} = -V_{C2}(t) \end{cases} \tag{2.1}$$

2.2.2. Zero State Operation

In the Zero state mode as shown in Figure 2.2(d), upper MOSFET switches (S_1 and S_3) or bottom MOSFET switches (S_2 and S_4) are ON. During this mode, the diode D_1 in the QZS becomes forward biased. During this mode input source and inductor L_1 is discharged which energizes the capacitor C_1. L_2 is discharged and energizes the capacitor C_2. The related mathematical equations can be represented as below,

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = i_{L1}(t) \\ C_2 \dfrac{dV_{C2}}{dt} = i_{L2}(t) \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) - V_{C1}(t) \\ L_2 \dfrac{di_{L2}}{dt} = -V_{C2}(t) \end{cases} \tag{2.2}$$

2.2.3. Shoot-through State Operation

In the shoot-through mode as shown in Figure 2.2(e), one of the HB legs becomes conducting (MOSFET switches (S_1 & S_2 or S_3 & S_4) are ON. The diode D_1 in the QZS becomes reverse biased. During this mode inductor, L_1 is charged by the input and the capacitor C_2 and L_2 are charged from the capacitor C_1.

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = -i_{L2}(t) + i_{out} \\ C_2 \dfrac{dV_{C2}}{dt} = -i_{L1}(t) \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) + V_{C2}(t) \\ L_2 \dfrac{di_{L2}}{dt} = V_{C1}(t) \end{cases} \tag{2.3}$$

As the filter inductor is present at the output terminals of the inverter so the current during the Active state and the zero states can be the same. So that the three states can be reduced to only two states such as shoot-through and non-shoot-through state. So it can be observed that only there are two modes one as the shoot-through state (D_{st}*T) and the other as the non-shoot-through state ((1- D_{st})*T) by simplifying the above equations (2.1) and (2.3) below is obtained,

$$\begin{cases} V_{C1} = \dfrac{1-D_{st}}{1-2D_{st}} V_{pv} \\ V_{C2} = \dfrac{D_{st}}{1-2D_{st}} V_{pv} \\ V_{C1} + V_{C2} = \dfrac{1}{1-2D_{st}} V_{pv} = BV_{pv} \end{cases} \tag{2.4}$$

From the power balance equation, the following expression is obtained,

$$\begin{cases} V_{out} I_{out} = I_{pv} V_{pv} \\ I_{pv} = I_{L1} = \dfrac{1}{(1-2D_{st})} I_{out} \end{cases} \tag{2.5}$$

Where all the currents and the voltages are the average values.

2.3. Inductor design and selection

The inductors in the proposed qZS based isolated converter are selected based on the peak-to-peak current ripple flowing through the inductors. The peak to peak inductor current ripple can be observed from the above equations, as given below,

$$\begin{cases} \Delta I_L = \Delta I_{L1} = \Delta I_{L2} \\ \Delta I_L = \dfrac{(1-D_{st}) D_{st} T}{2(1-2D_{st}) L} V_{pv} \end{cases} \tag{2.6}$$

The ripple current passing through the inductor during the shoot-through state. If the inductor current ripple is chosen, so that $\Delta I_{L1} = \Delta I_{L2} < \%xI_L$, the required inductance should be,

$$\begin{cases} L = \dfrac{(1-D_{st}) D_{st} T}{x\%(1-2D_{st}) 2P_{out}} V^2{}_{pv} \end{cases} \tag{2.7}$$

2.4. Capacitor Design and Selection

The capacitors are designed according to the capacitor voltage ripple. The current flowing through the capacitor during the shoot-through state in the proposed converter is calculated as,

Table 2.1. Simulation parameters

Input DC voltage	100V
Output grid voltage	120Vac
Grid frequency	50Hz
Output power	500W
Switching frequency	10kHz
$L_1 = L_2$	2mH
$C_1 = C_2$	2000uF
L_{0ilter}	2mH

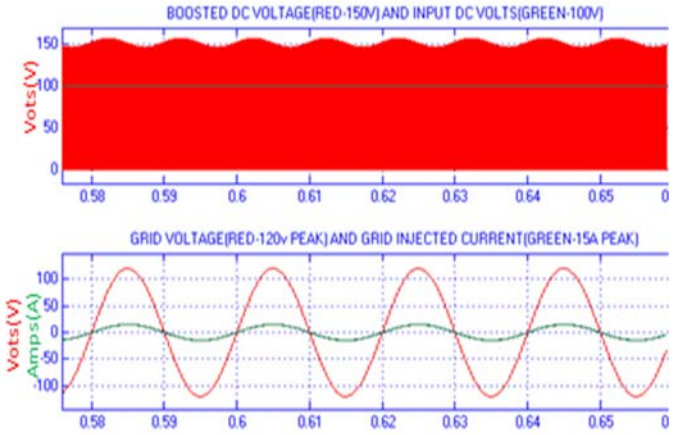


Figure 2.3. Simulation results at 120V, 1.2kW and 0.99pf.

$$C_1 \frac{\Delta V_{C1}}{D_{st} T} = 2I_{s\_tx} + I_{L1} \tag{2.8}$$

Then final values can be obtained as follows,

$$\begin{cases} C_1 = \dfrac{(1-2D_{st})D_{st}T}{2y\%(1-D_{st})V^2{}_{pv}} P_{out} \\ C_2 = \dfrac{(1-2D_{st})T}{2y\%V^2{}_{pv}} P_{out} \end{cases} \tag{2.9}$$

Here the peak-to-peak capacitor voltage ripple is considered as y%.

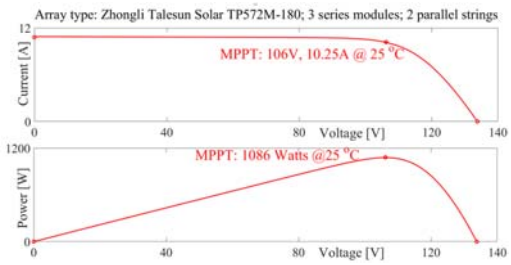
2.5. Implementation of qZSI connected with PV panels

The proposed qZSI is simulated using Matlab/Simulink. The parameters used for the simulation purpose are given in Table 2.1. The simulation results are presented in

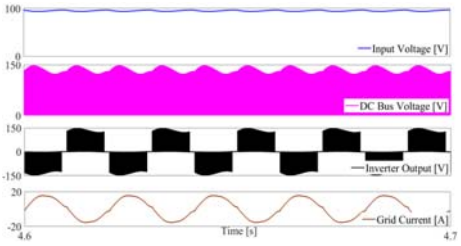
Figure 2.3. The DC-link voltage is boosted to 150 V (dc source voltage from PV is 100 V), with a small ripple 10 V peak-peak and the ripple can be further reduced by increasing the capacitor size. The grid voltage is 120V peak and the injected current is in phase with the voltage offering almost unity power factor operation. The common-mode voltage is seen to have the same magnitude and frequency as that of the grid supply. However, it is noticed that the common-mode voltage is indirectly applied to the stray capacitors of very high impedance. Hence, the common-mode current is almost zero.

Implementation of the proposed system is carried out with PV panels having part number TP572M – 180 manufactured by Zhongli Talesun Solar. To achieve the desired performance, two parallel strings are used with each string consisting of three series modules giving peak power of 1086 Watts when operating at MPPT (106V, 9.25A at 25^0C) as shown in Figure 2.4(a). MPPT algorithm is employed to operate the PV panels near the MPPT point. Figure 2.4(b) shows the performance of qZSI with the proposed PWM. Operation of MPPT is ensured by observing the input voltage of 100V applied to qZSI, which is close to the MPPT operating point of 106V. This input voltage is boosted by controlling the shoot-through duty cycle generated by the MPPT algorithm. Here, the voltage is boosted approximately 1.5 times i.e., from 100V to 150V. Inverter output voltage and grid current are also shown. Figure 2.4(c) shows controlled active power injection from PV-generated power into the utility grid. In addition to this, the power generated from the panel is also shown, which is near the MPPT point.

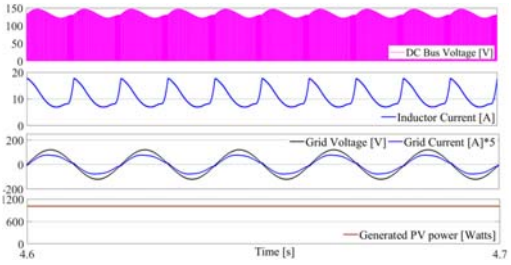
Management of active and reactive power by the solar PV stations with the utility grid is essential in advanced distribution systems. To address this, the operation of qZSI at the lagging power factor is shown in Figure 2.4(d). Phase displacement change between grid voltage and grid current calls for modified PWM as discussed in the previous



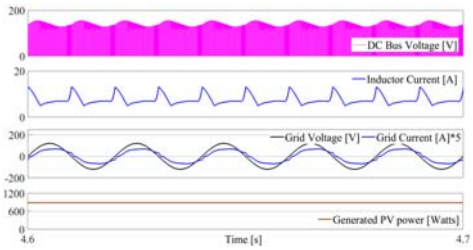
(a) Maximum Power Point Tracking (MPPT) tracking point.



(b) Performance of qZSI when operated with above mentioned PV panel.



(c) Performance of grid current qZSI controlled at unity power factor.



(d) Performance of grid current qZSI controlled at lagging power factor.

Figure 2.4. Performance Analysis of qZSI system with proposed PWM.

section 2.2. This reflects as a change in grid current requirement, thereby invoking the MPPT algorithm. As a result, a shift in the operating point of solar PV panels can be observed in Figure 2.4(d) where the power generated now is lesser than its operation at unity power factor. This means, for extraction of maximum power from solar PV panels, operation of qZSI at unity power factor is preferred.

2.6. Experimental Results

An experimental prototype of 500 Watts is built in the laboratory as shown in Figure 2.5. The H-bridge inverter is built using Semikron SKM100GB12T4. The qZS network is built using inductor $L_1 = L_2 = 1$mH, $C_1 = C_2 = 470$uF. The control code is written in a system generator and built using FPGA VIRTEX-5 XC5VLX50T. The switching frequency is kept at 10 kHz.

Figure 2.6, shows the performance of qZSI controlled with the proposed PWM

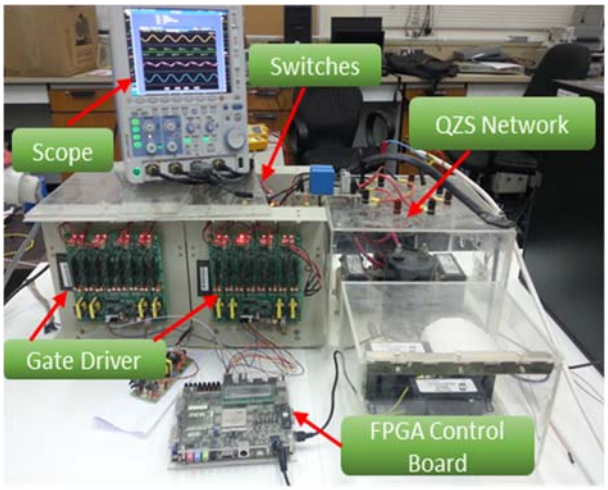
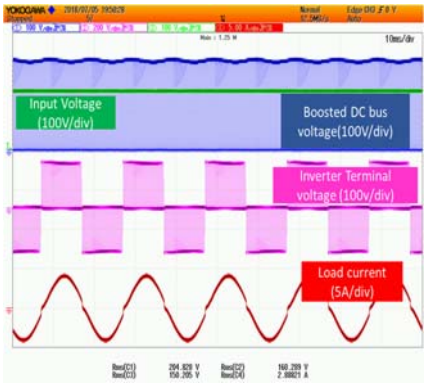


Figure 2.5. Hardware setup.

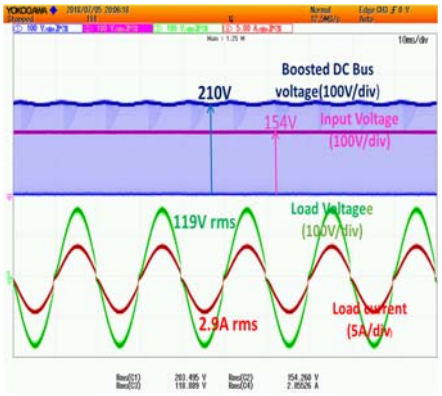
algorithm. Figure 2.6(a) shows inverter output performance. The input voltage of 100V is applied to the system. Quasi network boosts the applied input voltage to 150V. This forms the DC-link voltage for the H – Bridge whose output voltage is shown along with load current. Figure 2.6(b) shows the operation of qZSI at the unity power factor. Figure 2.6(c) shows the inductor current during the steady-state operation of qZSI.

2.7. Summary

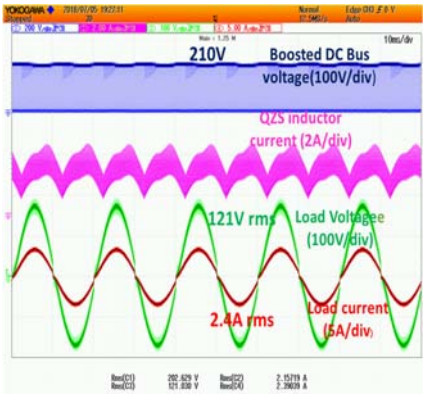
A novel PWM technique has been presented in this chapter, which has similar results as the conventional PWM technique for the grid-connected single-phase qZSI. The detailed operating modes and components design methodology has been presented here. Simulations were carried out at different power factors. For validating its suitability for PV applications, simulation results with commercialized PV panels are also presented. An experimental prototype of 500 Watts is developed in the laboratory and hardware results are presented. The proposed inverter topology, controlled by the



(a) Performance of proposed qZSI with proposed PWM algorithm



(b) Operation of qZSI at unity power factor



(c) Boosting of applied input voltage by qZSI

Figure 2.6. Performance of qZSI system

novel modified PWM technique, is suitable for PV inverter grid-connected applications.

The PWM technique developed and elaborated in this chapter is further utilized in the next chapter for obtaining multilevel operation of cascaded qZSI. The single unit operation and control is described in this chapter while the cascaded structure is illustrated in the next chapter.

CHAPTER 3: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR 5 LEVEL QUASI Z SOURCE INVERTER FOR PV SYSTEMS

3.1. Introduction

Multilevel Inverters (MLI) are used for the higher voltage and high-power applications, due to lower dV/dt, almost sinusoidal output voltage, and better current THD [1, 2, 43]. The most examined and commercialized topologies are Cascaded H-Bridge inverter (CHB) [3, 44], Neutral Point Clamped Inverter (NPC) [45, 46], Flying Capacitor Inverter (FC) [47, 48], and Modular Multilevel Converter (MMC) [49, 50]-[6, 14, 51, 52]. Several modulation schemes in [6, 18, 19, 21-23, 54] have been reported for achieving the optimal switching and equal power-sharing between the operating modules. In [55], Phase-Shifted Pulse Width Amplitude Modulation (PS-PWAM) is proposed which achieves optimal switching for the semiconductors but loses modularity. Since different switches of a given module switch at different times (i.e., at different frequencies), this causes an oversized heat sink selection. Furthermore, the switching pulse generation is complex and not suitable for the higher number of modules.

MLI is also controlled with the LS-PWM technique, which includes POD PWM, PD PWM, and APOD PWM [21]. All the existing LS-PWM methods are shown in Figure 3.1. In [21], the direct application of these methods to qZS-CMI is carried out which fails to address the advantages (optimal switching) of LS-PWM. LS-PWM applied to

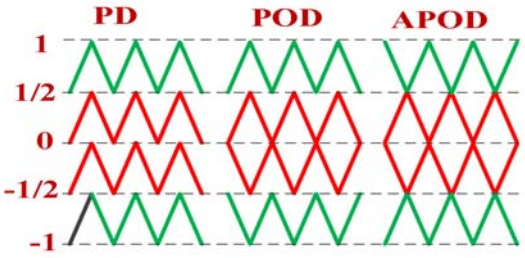


Figure 3.1. Conventional LS-PWM Techniques for five-level output

the CMIs is presented in [22, 23]. Furthermore, it is observed that this PWM method causes unequal power distribution among operating modules, and hence not suitable for PV systems application. Also, the uneven switching sequence is created at the module's semiconductors thereby prohibiting the harmonic cancellation at the input, which further deteriorates the THD. For MW power applications these harmonics will consume a substantial amount of power thereby preventing its practical applications. For the CMI, a novel carrier rotation is applied in [24-27] to achieve equal power distribution between the modules. The effort of this chapter is to apply the APOD-PWM to the qZS-CMI to improve the switching sequence generation which reduces the switching power loss in the semiconductors, however, this leads to unequal power distribution between the two operating modules. To address the issue of unequal power distribution, another carrier rotation PWM is developed and applied to the APOD-PWM to ensure the equal power between the operating modules.

3.2. PS-PWM FOR qZS-CMI

3.2.1. Single Phase qZS-CMI, operation of qZSI

A qZS-CMI based single-phase solar PV system is shown in Figure 3.2. There are two qZSI modules connected in cascade denoted as upper and lower. Each qZSI module comprises PV panels as the input source, two capacitors C_{n1} and C_{n2}, two inductors L_{n1} and L_{n2}, , one diode in qZS network, and four MOSFETs based HB module, where n∈ module number (1 to 2). Every module operates in three different states, AS, STS, and ZS. The qZSI is presumed to be working in Continuous Conduction Mode (CCM). The steady-state average values for all the components is given by,

$$V_o = V_{o1} + V_{o2} \tag{3.1}$$

V_{o1} and V_{o2} are the terminal voltage of the individual modules, V_o is the output voltage

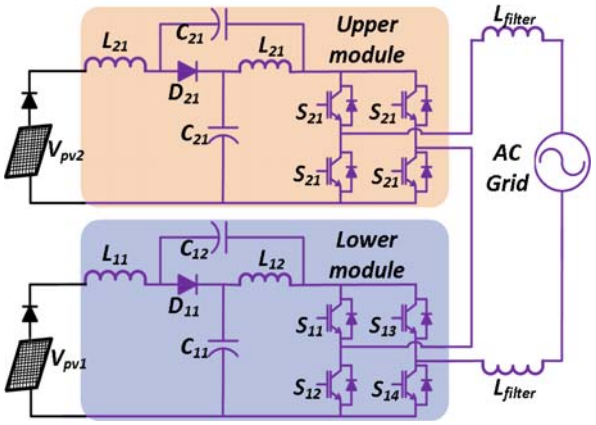
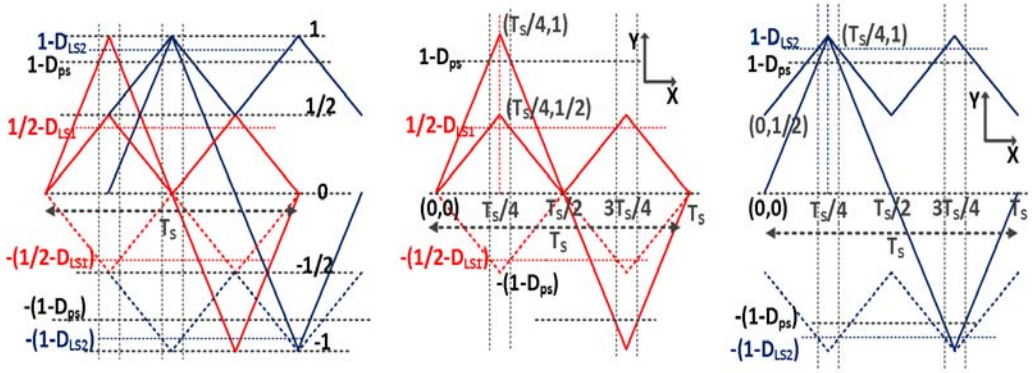


Figure 3.2. Single-phase qZS-CMI PV power system

of the qZS-CMI.

3.2.2. The relation between PS-PWM & APOD-PWM for qZS-CMI

Figure 3.3(a) represents the PS-PWM and APOD-PWM along with their STS duty references. The carriers "0 to 1 to 0 and then 0 to -1 to 0" are for the PS-PWM technique. These carriers generate switching signals for the lower and upper modules, respectively.



(a) (b) (c)

Figure 3.3. (a) Geometrical analysis for the relation between the PS-PWM and PODPS-PWM, (b) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (0,1/2, 0) and (0, -1/2, 0) for PODPS-PWM, Represents the bottom modules in both, (c) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (1/2, 1,1/2) and (-1/2,-1, -1/2) for PODPS-PWM, Represents the top modules in both.

The carrier signal (denoted by red) “0 to 1/2 to 0” and “0 to -1/2 to 0” are for the APOD-PWM of the lower module. Similarly, the carrier signal from (denoted by blue) “1/2 to 1 to 1/2” and “-1/2 to -1 to -1/2” are for the APOD-PWM of the upper module. In a simple boost control scheme in PS-PWM, STS references ($1–D_{ps}$) and $–(1–D_{ps})$ create the identical STS pulse during the whole modulation cycle. These intersecting points are then projected to the APOD-PWM with the carrier signal at the same height from the zero. The raising slopes for the two carriers of the lower/upper modules are different. The geometrical investigation of the two-dimensional *(X, Y)* plane is carried out as given below.

In Figure 3.3(b), (0, 0) and (T_s/4, 1) are the two points on the straight line for the PSPWM carrier denoted by Y_1. Similarly, (0, 0) and (T_s/4, 1/2) are the two points on the straight line for the APOD-PWM carrier denoted as Y_2. Equation of Y_1 and Y_2 defined as,

$$Y_1 = \frac{4}{T_S} X_1 \tag{3.2}$$

$$Y_2 = \frac{2}{T_S} X_2 \tag{3.3}$$

For PSPWM, the STS duty is considered as $1–D_{ps,}$ in (3.2). The following relation is obtained as,

$$X_1 = \frac{(1–D_{ps})T_S}{4} \tag{3.4}$$

It is observed from Figure 3.4(b) that $X_1=X_2$, then substituting (3.2) in (3.3),

$$Y_2 = \frac{2}{T_S} * \frac{(1–D_{ps})T_S}{4} = \frac{(1–D_{ps})}{2} \tag{3.5}$$

Y_2 is reflected as $(1/2\text{-}D_{Ls1})$ for the APOD-PWM, so the resultant STS duty for the lower module is,

$$\frac{1}{2} - D_{Ls1} = \frac{(1-D_{ps})}{2} \tag{3.6}$$

D_{Ls1} is the STS duty ratio of the lower module. A similar two-point straight-line geometrical equation concept is applied to Figure 3.3(c) STS duty for the upper module can be realized as,

$$1 - D_{Ls2} = \frac{(1-D_{ps})}{2} + \frac{1}{2} \tag{3.7}$$

D_{Ls2} is the STS duty ratio of the upper modules. From (3.4)-(3.6), it can be concluded that both the modules having the same amount of STS duty can be given as,

$$D_{Ls1} = D_{Ls2} = \frac{D_{ps}}{2} = D_{Ls} \tag{3.8}$$

In two module systems, to overcome the problem of overlap of STS duty in PS-PWM following equation has to be satisfied,

$$M + D_{ps} \leq 1 \tag{3.9}$$

M is the modulation index. The new safe operating limit for the APOD-PWM can be achieved as,

$$\begin{aligned} M + D_{Ls2} &\leq 1 \\ M + \frac{D_{ps}}{2} &\leq 1 \end{aligned} \tag{3.10}$$

3.3. Proposed APOD-PWM for qZS-CMI

3.3.1. Proposed APOD-PWM for Unequal Power-sharing

The operation of the proposed APOD-PWM is illustrated in Figure 3.4 for five-level qZS-CMI. This can be achieved by cascading two qZSI modules whose carriers are level-shifted as C_{1S} and C_{2S} for the lower (bottom) module while the C_{3S} and C_{4S} for the

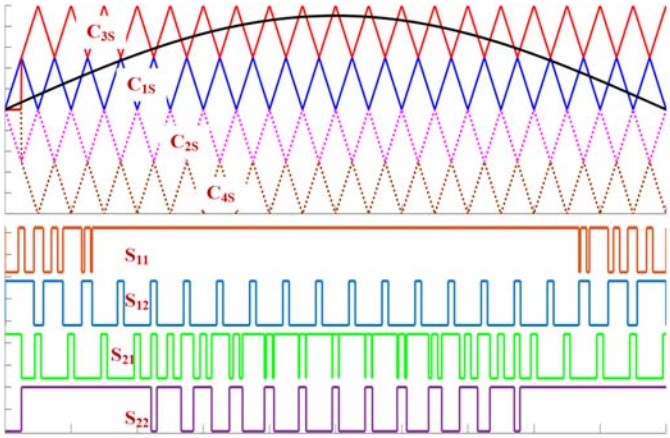


Figure 3.4. Proposed APOD-PWM for unequal power distribution between the qZS-CMI modules.

upper (top) module. The sinusoidal modulator (M) for the half-cycle is represented in Figure 3.4. In total four carriers and 2 STS duty references are required for the five-level qZS-CMI. These carriers are compared with the simple logic gates. As the modulating signal is compared with C_{1S} carrier, the respective switching pulses are generated while C_{3S} is well above M and produces only STS pulses. Once the modulation signal crosses the C_{1S} carrier, the switching pulse becomes high until it reaches the C_{1S} carrier. In this state, only C_{3S} carrier produces the switching pulses for the active states, the STS and AS can be generated by the lower module to maintain the DC-link.

The power-sharing by the lower module is higher than the upper module. Because the upper module is in ZS until it reaches the comparison zone for the C_{3s} carrier. This avoids the input harmonic current cancellation and generates the distortions. In order to eliminate these distortions and making the power balanced between the operating modules, the carrier rotation technique is proposed.

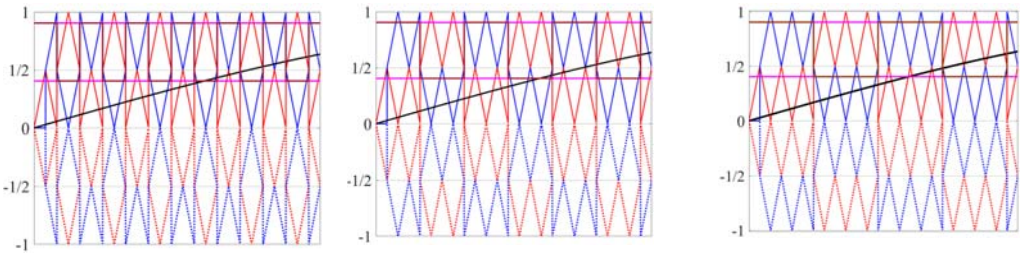
3.3.2. Proposed APOD-PWM for Equal Power-sharing

The bridge output voltage (RMS value) among the operating modules is inherently

unequal as seen from Figure 3.5. To achieve the equal RMS voltage across the modules (as observed in PS-PWM), the carriers must be rotated between the two operating modules (i.e., from one level to the other). This carrier rotation must be kept in such a way that the average power in both the modules is equal. The fundamental understanding of the carrier rotation is (i) reduced average power flow is obtained by shifting the carrier signal of the module to the upper levels and (ii) increased power flow is achieved by shifting the carrier signal of the module to the lower levels. Hence there can be several methods of rotating the carrier proposed as; i) single-cycle carrier rotation, ii) double-cycle carrier rotation and, iii) three-cycle carrier rotations. These methods are elaborated further in the following subsection.

a) Method 1, One-Cycle Carrier Rotation

Figure 3.5(a) denotes the proposed method 1 for the single-cycle carrier rotation technique. Red and green carrier signals are assigned for the lower and upper modules. According to APOD-PWM, these carriers are phase-shifted by 180^0. At the end of every switching cycle, carriers change their position from one level to the other. The lower module (red) carrier signal is present between 0 and 1/2 level. For the next switching



(a) Single-cycle (b) Two-cycle (c) Three-cycle

Figure 3.5. Proposed carrier rotation techniques of the APOD-PWM for Equal power distribution between the qZS-CMI modules different carrier rotation. Carrier Signals – Lower and Upper Modules, Modulation Signal, Shoot-through duty reference – Lower, Upper

cycle, the carrier is shifted between the ½ and 1 level. Again, For the next cycle, it comes back to the lower level. This completes one rotating cycle for the lower module carrier for the positive half cycle modulation. In the negative cycle, modulation is phase opposed with positive cycle to get in-phase STS duty for the respective module, as shown in Figure 3.5(a). Similarly, the upper carrier starts from the upper level and comes to the lower- level during rotation.

b) Method 2,Two-Cycle Carrier Rotation

Figure 3.5(b) denotes the proposed method 2 for the two-cycle carrier rotation technique. Red and green carriers are assigned for the lower and upper modules. According to APOD-PWM, these carriers are phase-shifted by 180^0. For the lower module, carrier signal red is present between the 0 and 1/2 levels for the first two switching cycles. For the next set of two cycles, the carrier is shifted between the ½ and 1 level. Again, at the second cycle, this set of two carriers comes back to the lower level. This completes one rotating cycle for the lower module carrier for the positive half cycle modulation. In the negative cycle, the modulation signal must be phase opposed with positive cycle to get the in-phase STS duty for the respective module, as shown in Figure 3.5(b). Like the positive side, two-cycle carrier rotation is done on the negative side.

c) Method 3,Three-Cycle Carrier Rotation

Figure 3.5(c) denotes the proposed method 3 for the three-cycle carrier rotation technique. Similarly, as a single carrier and two carriers rotation, the three carriers together will shift from one level to the other. However, unlike the single and two carriers rotation, the overlap zone and no carrier zones are much reduced. This method reduces much of the overlap and no carrier zones. So, the THD, in this case, is far superior to Method 1 and 2. Finally, with this method, the IEEE-512 standard grid code

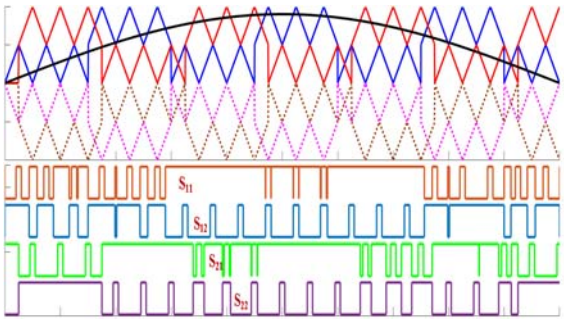


Figure 3.6. Detailed switching gate pulse of the proposed three carrier rotation techniques of the APOD-PWM for Equal power distribution between the qZS-CMI modules

can be satisfied for both the voltage and current.

Figure 3.6 depicts the detailed switching gate pulse for the lower (S_{11} and S_{12}) and upper (S_{21} and S_{22}) modules MOSFETS for the equal power distribution between them. STS duties are inserted in regular intervals within the switching cycle (f_s). The lower module (C_{1S}) carrier is compared with the sinusoidal modulator (Black) to get the first leg gate pulses as S_{11} and S_{12}. Similarly, the upper modules carrier (C_{3S}) is compared with the sinusoidal modulator (M) to get the first leg gate pulses as S_{21} and S_{22}.

3.4. Switching Loss Analysis of Proposed PWM Methods

The number of cycles in each output voltage level in a particular modulation region is given by,

$$No.of\ cycles = \frac{f_S}{f_m * 2\pi} * \left\{\sin^{-1}\left(\frac{m+1}{N}\right) - \sin^{-1}\left(\frac{m}{N}\right)\right\} \quad (3.11)$$

Where, f_s is the switching frequency; f_m is the modulation frequency; N represents the number of qZSI modules; m = 0, 1represents modulation range from 0 to 1/2, 1/2 to 1 respectively.

3.4.1. Switching loss analysis for PODPSPWM with carrier rotation (PODPS – I)

To analyze the switching loss occurring in the qZSI module, a detailed understanding

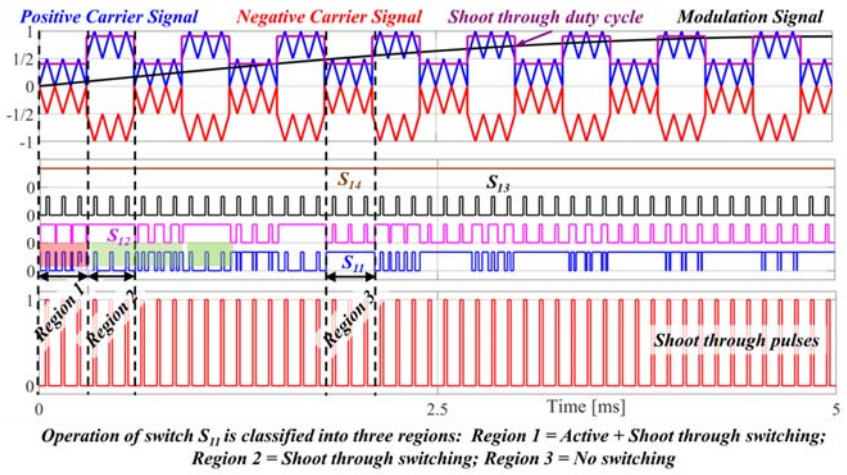


Figure 3.7. Identification of different regions of switching during carrier rotation for bottom module

of the carrier rotation concept and its effect on switching pulses must be done. Figure 3.7 shows a detailed pulse generation process for a quarter fundamental cycle (o to 90^0). Figure 3.7, shows bottom module carrier signals rotated for three cycles in each modulation level. To achieve the desired performance of output voltage RMS value as well as voltage boost, both active and shoot-through pulses must be generated. Logical OR operation is performed between these two pulses to generate resultant pulses as shown in Figure 3.7. When the carrier signal is rotated between the two available modules, three regions are identified for switch S_{11} as observed in Figure 3.7. Characteristics of these regions are defined below,

Region – 1, In this region, switching pulses consists of PWM-generated active pulses and equidistant shoot-through pulses. When the carrier signal is in this region, both active and shoot-through pulses are observed. Performance in this region is the same as the conventional PS-PWM region and there is no saving in switching losses.

Region – 2, In this region, the carrier signal goes above the modulation signal. Due to this, no active pulses are generated in this region. As a result, only switching pulses are

generated in this region. When compared to conventional PS-PWM switching, no active switching occurs in this region and

Region – 3, In this region, the carrier signal lies below the modulation signal. Due to this, the generated active pulses are continuous pulses thereby avoiding any active or shoot-through switching in this region. When compared to conventional PS-PWM switching, no active or shoot-through switching occur in this region.

For five-level qZSI operation consisting of two qZSI modules, the performance of each qZSI switch of the bottom module for the entire fundamental cycle is shown in Table 3.1. For two modules, the modulation signal is categorized into two modulation levels. Here for range m = 0 to 1/2, output voltage level consists of voltage transitions from 0 to V_{dc}. Similarly, for m = 1/2 to 1, output voltage consists of transitions between V_{dc} to $2V_{dc}$. Similar behavior is observed in the negative half cycle. Based on this operating principle, the fundamental cycle is classified into eight regions and the performance of each switch is determined in the given region. In Table 3.1, *'A/2'* indicates active

Table 3.1. Active and shoot – through switching over a fundamental cycle

	Active State				Shoot-through			
Region	S_{11}	S_{12}	S_{13}	S_{14}	S_{11}	S_{12}	S_{13}	S_{14}
$0 - \frac{\pi}{6}$	A/2	A/2	0	0	ST	ST/2	*ST*	0
$\frac{\pi}{6} - \frac{\pi}{2}$	A/2	A/2	0	0	ST/2	*ST*	*ST*	0
$\frac{\pi}{2} - \frac{5\pi}{6}$	A/2	A/2	0	0	ST/2	*ST*	*ST*	0
$\frac{5\pi}{6} - \pi$	A/2	A/2	0	0	*ST*	ST/2	*ST*	0
$\pi - \frac{7\pi}{6}$	0	0	A/2	A/2	*ST*	0	*ST*	ST/2
$\frac{7\pi}{6} - \frac{3\pi}{2}$	0	0	A/2	A/2	*ST*	0	ST/2	*ST*
$\frac{3\pi}{2} - \frac{11\pi}{6}$	0	0	A/2	A/2	*ST*	0	ST/2	*ST*
$\frac{11\pi}{6} - 2\pi$	0	0	A/2	A/2	*ST*	0	*ST*	ST/2

switching losses only in one of the modulation levels (out of two) identified as Region 1 for switch S_{11} in Figure8. *'ST*k/N'* (where k = 1, 2 and N = 2 for seven-level qZSI) indicates shoot-through switching losses in 'k' modulation levels out of N modulation levels.

Since unipolar switching is used in qZSI, four switches of the qZSI can be categorized into two types. Type – 1 switch consists of S_{11} and S_{13} switches which give the same average loss for the fundamental cycle – performance of S_{11} from 0 to π is identical to S_{13} switching from π to 2π. Similarly, Type – 2 switch consisting of S_{12} and S_{14} gives identical switching loss when averaged over a fundamental cycle. Switching loss for Type – 1 and Type – 2 switches are given below,

3.4.1.1. Switching losses in the active state

Switching losses for semiconductor switch during the active state are given by,

$$P = \frac{1}{2\pi}\int_0^{\pi} \frac{f_s(E_{ON}+E_{OFF}+E_{REC})\,V_{dc}i_{ac}}{V_{ref}I_{ref}}\,d\omega t \qquad (3.12)$$

f_s is the switching frequency

E_{ON} and E_{OFF} are the turn-on and turn-off energy losses per pulse of the IGBT

E_{REC} is the reverse recovery loss of the antiparallel diode

V_{ref} and I_{ref} are the switched voltage and current references

V_{dc} is the dc-link peak voltage of each module and

i_{ac} is the ac load current.

For type – 1 switch (S_{11} and S_{13}), in the modulation region 0 to $\frac{\pi}{6}$, active switching losses occur for half of the duration i.e., the switching losses occur from 0 to $\frac{\pi}{12}$. A similar analogy can be drawn for other modulation regions from Table – A (given in Appendix). Conclusively, active switching losses when averaged over a fundamental cycle are given by,

$$P_{POD-A} = \frac{P_{F\,AC} I_m}{2\pi}\left[\int_0^{\frac{\pi}{12}} Sin\omega t d\omega t + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} Sin\omega t d\omega t + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} Sin\omega t d\omega t + \right.$$

$$\left. \int_{\frac{5\pi}{6}}^{\frac{5\pi}{6}+\frac{\pi}{12}} Sin\omega t d\omega t + \int_{\pi}^{2\pi} 0 * Sin\omega t d\omega t\right] \quad (3.13)$$

Where, $\frac{2P_{F\,AC}\,I_m}{\pi}$ is defined as the active state switching losses in PS-PWM and I_m is the peak of ac load current. Simplifying the above equation,

$$P_{POD-A} = \frac{P_{F\,AC} I_m}{2\pi}[1.0] \quad (3.14)$$

$P_{POD-A} = 25\%$ of active state switching loss in PS-PWM.

3.4.1.2. Switching losses in shoot-through states

For Type – 1 switch, shoot – through state switching losses occurs throughout the fundamental cycle. Switching losses in this switch type is given by,

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[\int_0^{\frac{\pi}{6}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \right.$$

$$\left. \int_{\frac{5\pi}{6}}^{\pi}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\pi}^{2\pi}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t\right] \quad (3.15)$$

where $P_{F\,ST}$ is defined as the shoot-through state switching losses in PS-PWM and I_L is the average inductor current.

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[\frac{5\pi}{3} I_L + \frac{I_m}{2}\left(\frac{2-\sqrt{3}}{2}\right)\right] \quad (3.16)$$

$$P_{POD-SI} = P_{F\,ST}\left[\frac{5}{6} I_L - \frac{0.067 I_m}{2\pi}\right] \quad (3.17)$$

For Type – 2 switch (S_{12} and S_{14}), shoot – through state switching losses occurs throughout the fundamental cycle. Switching losses in this switch type is given by,

$$P_{POD-SII} = \frac{P_{F\,ST}}{2\pi}\left[\int_0^{\frac{\pi}{12}}\left(i_L - \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{6}}^{\frac{\pi}{2}}\left(i_L - \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{2}}^{\frac{5\pi}{6}}\left(i_L - \frac{i_{ac}}{2}\right) d\omega t + \right.$$

$$\left. \int_{\frac{5\pi}{6}}^{\frac{11\pi}{12}}\left(i_L - \frac{i_{ac}}{2}\right) d\omega t + \int_{\pi}^{2\pi} 0 * \left(i_L - \frac{i_{ac}}{2}\right) d\omega t\right] \quad (3.18)$$

$$P_{POD-SII} = \frac{P_{F\,ST}}{2\pi}\left[\frac{5\pi}{6}I_L - \frac{(2+\sqrt{3})I_m}{4}\right] \quad (3.19)$$

$$P_{POD-SII} = P_{F\,ST}\left[\frac{5}{12}I_L - \frac{0.933}{2\pi}I_m\right] \quad (3.20)$$

3.4.2. Switching loss analysis for PODPS-PWM without carrier rotation (PODPS – II)

Figure 3.8 shows bottom module carrier signals rotated for three cycles in each modulation level. To achieve the desired performance of output voltage RMS value as well as voltage boost, both active and shoot-through pulses must be generated. Logical OR operation is performed between these two pulses to generate resultant pulses as shown in Figure 3.8. With the proposed PWM method (no carrier rotation), here also three regions are identified for operating switches as observed in Figure 3.8. Characteristics of these regions are defined as,

Region – 1, For switch S_{11}, in this region, both active and shoot – through switching losses occurs.

Region – 2, For switch S_{12}, in this region, only shoot-through switching loss occurs.

Region – 3, For switch S_{11}, in this region, neither active nor shoot-through switching loss occur.

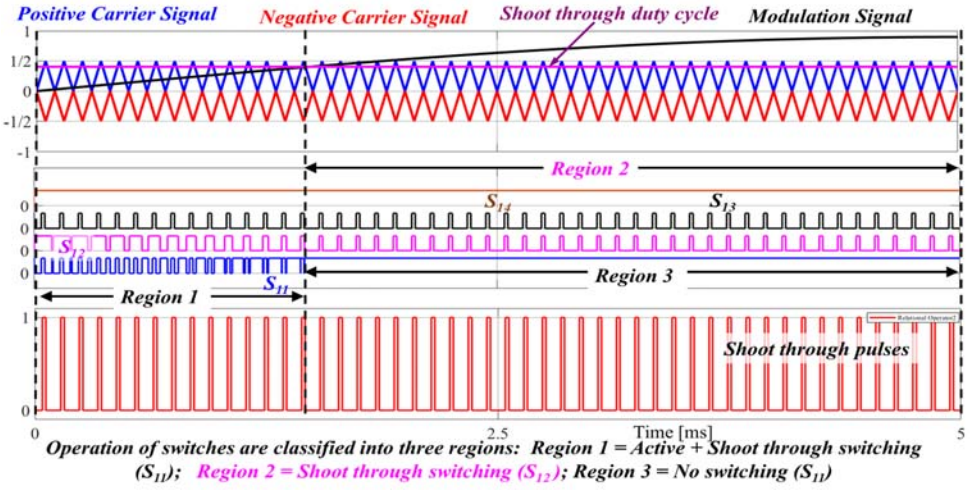


Figure 3.8. Identification of different regions of switching for bottom module switches

Based on Figure 3.8, for the proposed modulation method, the switching states of bottom module switches are given in Table 3.2. Based on these switching angles, switching losses for these two switches are calculated as below.

3.4.2.1. Switching losses in active state

For qZSI switches, switching losses for semiconductor switch during the active state are given by,

$$P_{POD-AI} = \frac{P_{F\,AC} I_m}{2\pi}\left[\int_0^{\frac{\pi}{6}} Sin\omega t d\omega t + \int_{\pi-\frac{\pi}{6}}^{\pi} Sin\omega t d\omega t\right] \quad (3.21)$$

$$P_{POD-AI} = \frac{P_{F\,AC} I_m}{2\pi}[0.2679] \quad (3.22)$$

$P_{POD-AI} = 6.7\%$ of active state switching loss in PS-PWM.

3.4.2.2. Switching losses in shoot-through states

For type – I switch, shoot – through state switching losses in the time intervals – 0 to $\frac{\pi}{6}$, $\frac{5\pi}{6}$ to π and π to 2π. Switching losses are given by,

Table 3.2. Active and shoot – through switching over a fundamental cycle for PODPS – II

	Active State				*Shoot-through*			
Region	S_{11}	S_{12}	S_{13}	S_{14}	S_{11}	S_{12}	S_{13}	S_{14}
$0 - \frac{\pi}{6}$	A	A	0	0	ST	ST	ST	0
$\frac{\pi}{6} - \frac{\pi}{2}$	0	0	0	0	0	ST	ST	0
$\frac{\pi}{2} - \frac{5\pi}{6}$	0	0	0	0	0	ST	ST	0
$\frac{5\pi}{6} - \pi$	A	A	0	0	ST	ST	ST	0
$\pi - \frac{7\pi}{6}$	0	0	A	A	ST	0	ST	ST
$\frac{7\pi}{6} - \frac{3\pi}{2}$	0	0	0	0	ST	0	0	ST
$\frac{3\pi}{2} - \frac{11\pi}{6}$	0	0	0	0	ST	0	0	ST
$\frac{11\pi}{6} - 2\pi$	0	0	A	A	ST	0	ST	ST

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[\int_0^{\frac{\pi}{6}}\left(i_L + \frac{i_{ac}}{2}\right)d\omega t + \int_{\frac{5\pi}{6}}^{\pi}\left(i_L + \frac{i_{ac}}{2}\right)d\omega t + \int_{\pi}^{2\pi}\left(i_L + \frac{i_{ac}}{2}\right)d\omega t\right] \quad (3.23)$$

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[I_L\left(\frac{4\pi}{3}\right) - \frac{\sqrt{3}}{2}I_m\right] \quad (3.24)$$

$$P_{POD-SI} = P_{F\,ST}\left[\frac{4}{6}I_L - \frac{\sqrt{3}}{4\pi}I_m\right] \quad (3.25)$$

For Type – 2 switch, shoot – through state switching losses in the time interval of 0 to π. Switching losses are given by,

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[\int_0^{\pi}\left(i_L - \frac{i_{ac}}{2}\right)d\omega t\right] \quad (3.26)$$

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}[I_L(\pi) - 2I_m] \quad (3.27)$$

$$P_{POD-SI} = P_{F\,ST}\left[\frac{1}{2}I_L - \frac{1}{\pi}I_m\right] \quad (3.28)$$

Comparison of PSPWM with proposed two methods in terms of switching losses, voltage utilization, and THD comparison is given in Table 3.3. In the proposed APOD-I, the losses in the active states is only 25% while in APOD-II is 6.7%, which are better

Table 3.3 Comparison of proposed PWM methods with PSPWM

Modulation	Type – 1 Switch	Type – 2 Switch
Active state		
PS-PWM	100%	100%
PWAM	13.4%	50%
PODPS - I	25%	25%
PODPS – II	6.7%	6.7%
Shoot – through state		
PS-PWM	$P_{F,ST}I_L$	$P_{F,ST}I_L$
PWAM	$P_{F,ST}\left[\frac{5}{6}I_L - \frac{1}{4\pi}I_m\right]$(≥ 16% saving)	$P_{F,ST}\left[\frac{2}{3}I_L - \frac{\sqrt{3}}{4\pi}I_m\right]$(≥ 33% saving)
APOD-PWM – I	$P_{F\,ST}\left[\frac{5}{6}I_L - \frac{0.067}{2\pi}I_m\right]$(≥ 16% saving)	$P_{F\,ST}\left[\frac{5I_L}{12} - 0.933\frac{I_m}{2\pi}\right]$(≥ 58% saving)
APOD-PWM – II	$P_{F\,ST}\left[\frac{4}{6}I_L - \frac{\sqrt{3}}{4\pi}I_m\right]$(≥ 33% saving)	$P_{F\,ST}\left[\frac{1}{2}I_L - \frac{1}{\pi}I_m\right]$(≥ 50% saving)

way lesser than the any other modulation in the literature. Similarly during the shoot-through state it is 16% for type-1 and 58% for the type-2 for the APOD-PWM-I, while 33% (type-1) and 50% (type-2) for the APOD-PWM-II. So in overall the proposed PWM schemes have better performance and efficiency than the standard PWM schemes.

3.5. Simulation Results and Discussions

Proposed modulation techniques for equal and unequal power-sharing between the qZS-CMIs are simulated in the MATLAB/Simulink. The parameters used are presented in Table 3.4. The operating frequency is 10 kHz and the input PV voltage for each module is considered as 95V. The STS duty for both the modules is 10% each. Figure 3.9 illustrates the comparison of the APOD-PWM with the proposed different schemes. Figure 3.10(a), denotes the output voltage levels and output current for the APOD-PWM, which indicates THD of the output voltage is 38% at 240V RMS and 1.76% THD at 7.6A load current. The output switching harmonics is at 10 kHz instead of 40 kHz for the PS-PWM technique. The power-sharing is unequal as the RMS output voltage of the individual qZSI modules is 150V (for the lower module) and 120V (for the upper module).

Table 3.4. Component specifications for qZSI-CMI

Components	Simulation	Experimental
$L_{n1} = L_{n2}$	Series RLC branch	1.6mH, 15A
$C_{n1} = C_{n2}$	Series RLC branch	2mF, 400V
Diode D_{n1}	Simscape block	STTH30R04, 400V, 15A
SiC-MOSFET	Simscape block	FDP19N40, 1200V, 40 A
frequency	10KHz	10KHz
RL-load	1.5KW	1.5KW
Modulation Index	0.933	0.933
Control Board	Computer PC	Virtex-5 FPGA

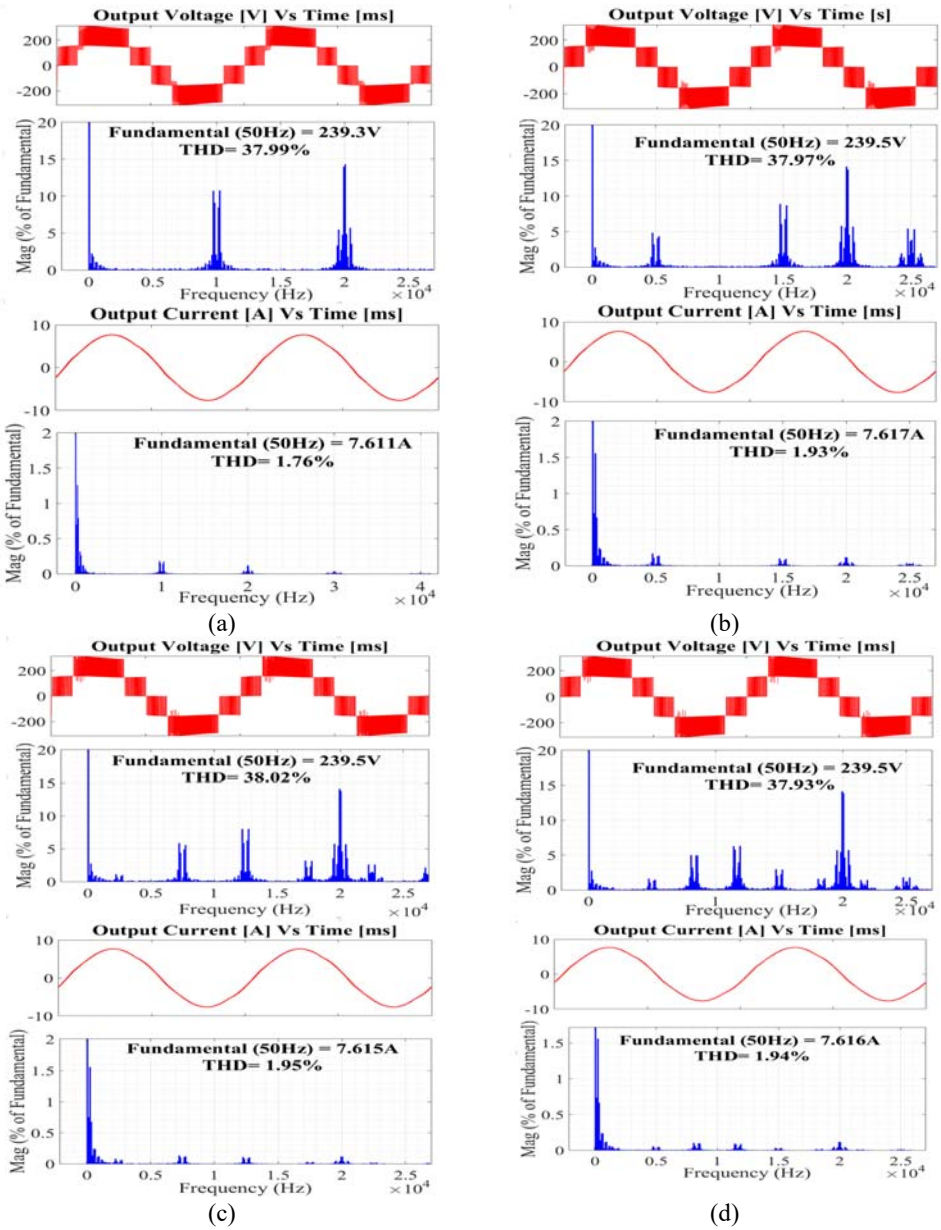


Figure 3.9. Harmonic spectra of load voltage and load current with different proposed APOD-PWM techniques (a) Output voltage/current and THD for unequal power-sharing (b) Output voltage/current and THD for equal power-sharing for single-cycle carrier rotation (c) Output voltage/current and THD for equal power-sharing for two-cycle carrier rotation (d) Output voltage/current and THD for equal power-sharing for three cycle carrier rotation.

Figure 3.9(b), denotes the output voltage levels and output current for the APOD-PWM modified with a single carrier rotation technique to achieve equal power-sharing. Here, voltage THD of 46.38% for output voltage (at 240V RMS) and current THD of 2.07%

for load current (at 7.6A). The dominant harmonic component is at 5 kHz instead of 40 kHz for the PS-PWM technique and 10 kHz for the unequal power-sharing technique. The power-sharing is equal as the RMS output voltage of both qZSI modules is 130V. No-carrier and overlap zones of the carrier are the insignificant amount and thus level jumps can be observed in Figure 3.9(b), but they are much smaller which is not significant.

Figure 3.9(c), denotes the output voltage levels and output current for the APOD-PWM for the two-cycle carrier rotation technique for equal power-sharing. Here voltage THD of 42.57% at 240V output voltage RMS and current THD of 2.13% at 7.6A load current are obtained. The dominant harmonic component is at 2.5 kHz instead of 40 kHz for the PS-PWM technique. The power-sharing is equal as the output voltage of both qZSI modules is 135V. No-carrier and overlap zones of the carrier are lesser than that of single carrier rotation, so the observed level jumps are lesser. Because of a shift in the fundamental frequency at 2.5 kHz, the filter design must be improved. The THD of the output current is lesser and voltage THD is better than the single cycle rotation.

Figure 3.9(d), denotes the output voltage levels and output current for the APOD-PWM for three-cycle carrier rotation. Here, THD of 41.03% at 240V RMS and 2.17% at 7.6A load current are obtained. The dominant harmonic component is at 1.6 kHz instead of 40 kHz for the PS-PWM technique. The power-sharing is equal as the RMS output voltage of the individual qZSI modules is 135V. No-carrier and overlap zones of the carrier are lesser than the above two techniques, so the observed level jumps are less. The THD of the output current is lesser and voltage THD is better than the two-cycle rotation technique. Hence, it can be concluded from Figure 3.9 that as the number of cycles for each rotation increases, the THD of output voltage and current improves. So,

based on the application (grid integration or motor drive) the number of carrier cycles rotation must be selected. All the proposed techniques are well suited for the grid integration as the current and voltage THDs are within the IEEE-512 standards.

3.6. Experimental Verification of the proposed Modulation Scheme

A 1.5kW experimental prototype is developed in the laboratory to validate the proposed APOD-PWM modulation techniques for the single-phase five-level qZS-CMI. Figure 3.10 shows the hardware prototype consisting of power circuit components mounted on PCB, gate drivers of the upper and lower modules, and the control board Virtex-5 FPGA. All the components used are listed in Table 3.4. qZS network is designed considering 10 kHz operating frequency. For comparison, an input voltage of 120V is applied from the DC power supply and 17.2% STS is applied to achieve 240V RMS and 380V peak voltage. A load current of 7.7A is obtained in all the cases.

Figure 3.11 shows the experimental results for APOD-PWM for unequal power-sharing between the qZSI modules. Figure 3.11(a), shows the five-level qZS-CMI (240Vrms and 7.7A load current). In Figure 3.11(a), harmonic spectra of these signals are also7.7A RMS at 0.95 power factor. FFT spectrum of output voltage and current indicates that the first maxima occur at 10 kHz (same as switching frequency). In Figure

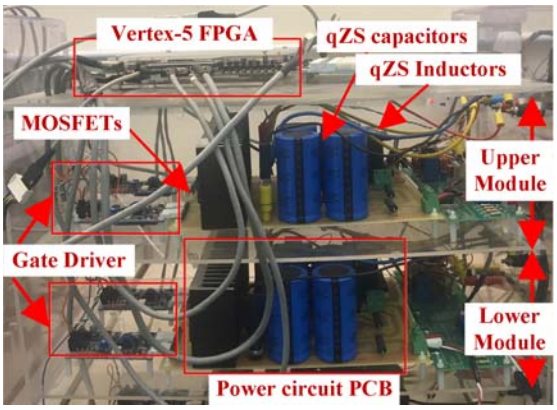
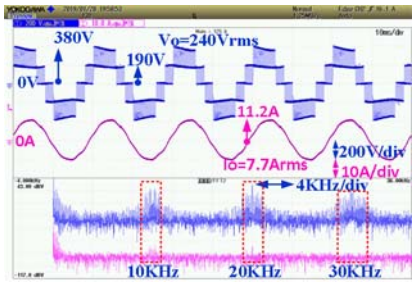
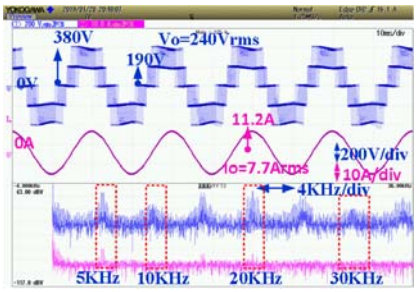


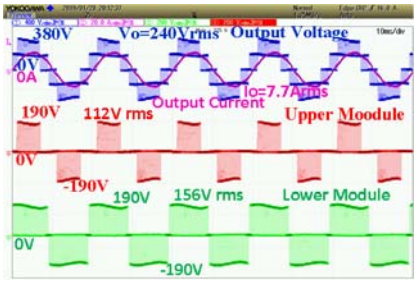
Figure 3.10. Shows the photograph of the experimental setup



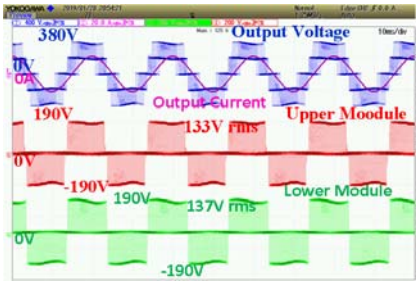
(a) output voltage 240V and output current 7.7A with FFT spectrum



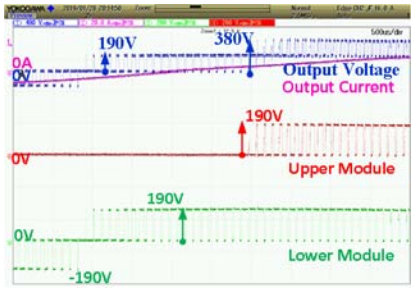
(a) output voltage 240V and output current 7.7A with FFT spectrum



(b) Output voltage, output current, lower 156V and upper 112V module voltages

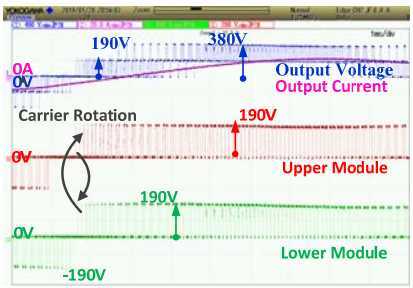


(b) Output voltage, output current, lower 137V and upper 133V module voltages



(c) zoomed part of the positive cycle.

Figure 3.11. APOD-PWM for unequal power-sharing between modules



(c) zoomed part of the positive cycle

Figure 3.12. APOD-PWM for equal power-sharing between modules for single-cycle carrier rotation

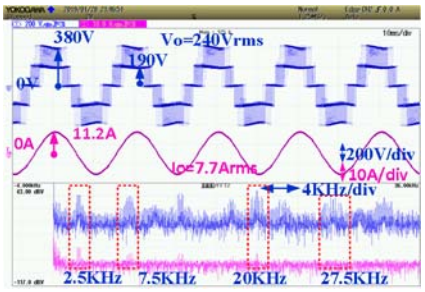
3.11(b), the RMS values of the output voltage of the upper and lower module are shown as 112V and 156V, respectively. The output voltage is 240V RMS and the load current of conduction time for the upper module is lesser than the lower module (whole fundamental period conduction). In Figure 3.11(c), boosting operation is shown as

120V input is boosted to 190V peak for each module and zoomed portion of positive cycle zoom of Figure 3.11(b) is also shown.

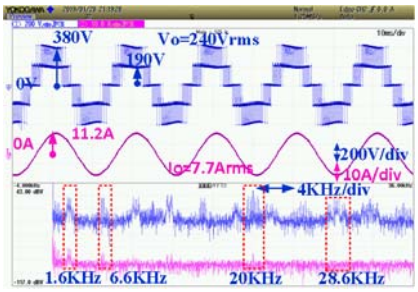
Figure 3.12 represents the APOD-PWM for single-cycle carrier rotation to achieve equal power-sharing. In Figure 3.12(a), output voltage and output current are shown along with the harmonic spectrum. As the carriers are rotating, the transition carrier overlap with the modulation signal is for every 5 kHz. The FFT spectrum indicates the peak at the fundamental frequency and dominant harmonic at 10 kHz. As the overlapping carriers are in a significant amount, the output voltage with unwanted levels can be seen in Figure 3.12(b). Also, an equal RMS output voltage of 133V and 136V for the upper and lower modules is achieved. The single-cycle carrier rotation is validated in Figure 3.12(c), which is a zoomed portion for the positive cycle of Figure 3.12(b).

Figure 3.13 represents the APOD-PWM for two-cycle carrier rotation for equal power-sharing. Figure 3.12(a), shows the output voltage and output current along with their harmonic spectra. Two-cycle carrier rotation increases the time of carrier transition, so the dominant harmonic component is observed at 2.5 kHz. As the overlapping carriers are lesser than single carrier rotation, the output voltage now contains fewer unwanted levels as observed in Figure 3.13(b). Here, the RMS output voltage of the two modules is 136V and 142V respectively. The zoomed view of Figure 3.13(b) is shown in Figure 3.13(c), validating the two-cycle carrier rotation for the positive cycle.

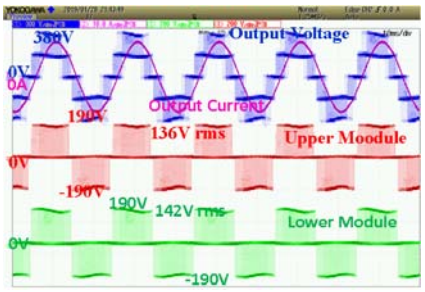
Figure 3.14 represents the APOD-PWM for three-cycle carrier rotation for equal power-sharing. In Figure 3.14(a), output voltage and output current obtained with 120V input are shown. In three carrier rotation transition time is thrice, so the first dominant harmonic peak is observed at 1.66 kHz. Here, lesser unwanted voltage levels are observed in the output voltage waveform as shown in Figure 3.14(b). Here RMS output



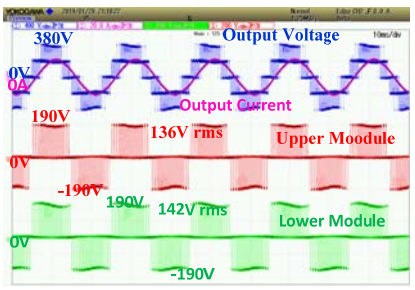
(a) output voltage 240V and output current 7.7A with FFT spectrum



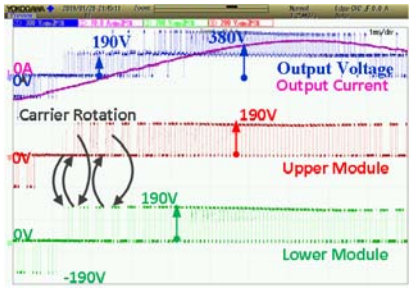
(a) output voltage 240V and output current 7.7A with FFT spectrum



(b) Output voltage, output current, lower 142V and upper 136V module voltages

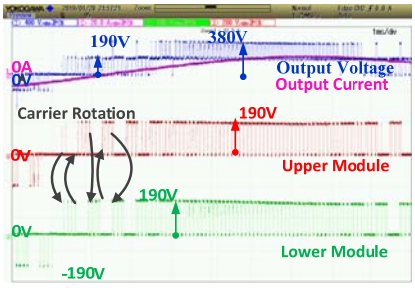


(b) Output voltage, output current, lower 142V and upper 136V module voltages



(c) zoomed part of the positive cycle.

Figure 3.13. APOD-PWM for equal power-sharing between modules for two-cycle carrier rotation



(c) zoomed part of the positive cycle.

Figure 3.14. APOD-PWM for equal power-sharing between modules for three-cycle carrier rotation

voltages of 136V and 142V are observed at the two modules. The zoomed view of Figure 3.14(b) is shown in Figure 3.14(c).

It can be concluded from Figure 3.12-Figure 3.14, that as the number of carriers cycle rotations increases the output voltage THD improves, but the current THD reduces. So,

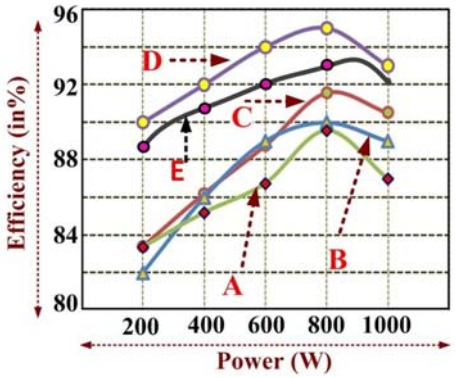


Figure 3.15. Per module Efficiency comparison A, Conventional qZSI [12], B, standard two-stage conversion [1], C, Modified qZSI [15], D, Proposed APOD PWM – II, E, Proposed APOD PWM – I

based on the application the number of carrier cycles must be selected. All the proposed techniques are well suited for the grid integration as the current and voltage THDs are within the IEEE-512 standards.

The detailed efficiency comparison for per module power is carried out, as shown in Figure 3.15. The switching losses and the conduction losses are significantly reduced in the proposed systems. The detailed loss analysis has been presented in section IV. Even though the efficiency is improved in [15], but the feasibility of applying the converter in a cascaded manner will consume a higher size. The proposed APOD PWM - II for the qZSI system achieves the highest per module efficiency. Furthermore, the proposed APOD PWM - II can create extra room for operating the converters to address the partial shading problem.

3.7. Summary

A novel APOD-PWM technique (equal and unequal power-sharing) for the qZS-CMI has been reported in this chapter. This chapter presents the relation between shoot-through duty and modulation indices of PS-PWM and APOD-PWM. The proposed modulation technique (for qZS-CMI) combines the advantages of APOD-PWM (a

subsidiary of LS-PWM) and PS-PWM, resulting in high-quality output voltages and ripple free input currents drawn from the PV panels. The equal and unequal power-sharing together overcomes the drawbacks of conventional techniques. These APOD-PWM for qZS-CMI can be applied to the PV systems to address the real-time problems of partial shading, dust accumulation, temperature variation and power distribution among the operating modules. To verify the advantages with proposed PWM techniques, detailed switching loss analysis, simulation and experimental results are presented. With carrier rotation in the proposed PWM, equal utilization is observed whereas, without carrier rotation, the highest efficiency is observed. The proposed APOD-PWM techniques have nearly the same THD as conventional schemes and higher voltage gain and power yielding capability with higher efficiency than PS-PWM thereby validating its feasibility for qZSI related applications. The developed PWM scheme is suited to only two module structure. The next chapter elaborate the novel PWM schemes for higher number of cascaded modules.

CHAPTER 4: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR CASCADED MULTILEVEL QUASI IMPEDANCE SOURCE INVERTER

4.1. Introduction

In the previous chapter, the LS-PWM for the qZS cascaded converters is implemented. However, the validation has been done for two cascaded modules. The developed APOD-PWM of Chapter 3 cannot be applied to the 3-modules and higher number of modules connected in the cascaded structure. As the shoot-through pulses for the even numbered modules will be overlapping with one another, similar overlapping will also happens for the odd numbered modules. This prevents the number of level formation in the output of the complete cascaded system. This encourages to work on the 3 modules cascaded qZSI system for the LS-PWM operation.

Cascaded multilevel qZSI topology to realize a higher power rating has also been proposed, which makes them suitable for solar PV applications [56, 57]. Different MPPT algorithm for solar-powered grid-connected qZSI is also discussed in the literature [58-60]. In [53, 61], multilevel qZSI for the integration of solar power to the utility grid are discussed.

The PWAM method controls the qZSI with reduced switching losses and higher voltage utilization [62-64].Grid current control realization using traditional PI controller and advanced control techniques is reported in the literature [65, 66]. On similar lines, the employment of PS-PWM to solar-connected qZSI based multilevel operation suffers from the same drawback of decreased power extraction from healthy modules during partial shading conditions [65]. For multilevel qZSI, the employment of LS-PWM would help in improved power extraction in a solar-powered grid-connected qZSI system. A modified LSPWM switching technique has been proposed for five-level qZSI [67]. Here, phase–shifting of 90^0 among the carrier signals (with Alternate Phase

Opposed Disposed of PWM) is targeted to avoid simultaneous shoot–through. However, this technique is not extendable or more than a five-level qZSI operation. Direct implementation of the PWM method would result in low voltage gain, poor THD, and high *dV/dt*. Thus, there is a need for a novel PWM method to address this issue at lower switching losses in the grid-connected qZSI system.

4.2. System Description

Seven – level qZSI system connected to RL load is shown in Figure 4.1. Three qZSI modules are connected in cascade to achieve seven–level output voltage. Each qZSI module comprises of passive components–based impedance network termed as quasi network followed by H – Bridge.

In Figure 4.1, input voltages to qZSI are marked as V_{in1}, V_{in2}, and V_{in3} representing input voltages for the bottom, middle and top modules, respectively. L_{filter} represents the filter inductance (if any) for connecting the cascaded qZSI system to RL load.

When LS-PWM is applied to achieve multilevel qZSI operation, the following concerns are observed

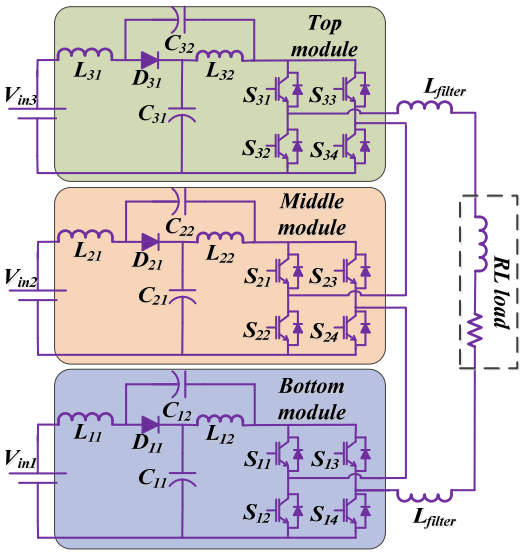


Figure 4.1. Three – phase seven-level qZSI connected to RL load

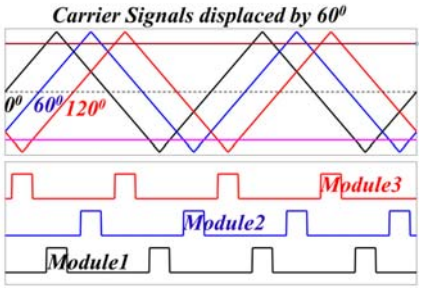
Low voltage magnitude and poor THD performance, Due to simultaneous application of shoot-through pulses, resultant output voltage consists of transitions from any given level to zero voltage. This results in low output voltage magnitude, high *dV/dt,* and higher output voltage *THD.* Thus, no advantage of a multilevel system is achieved.

DC-link voltage control, LS-PWM method exhibits uneven power distribution due to an unequal number of switchings in different modules. For example, module 3 generates active switching pulses in the range of *2/3* to *M* on the positive side and *–2/3* to *–M* on the negative side. As a result, current or power drawn from module 3 is heavily dependent upon modulation index *M*. If the value of *M* is close to unity, then the average current drawn by this module will be more. If the value of *M* is close to *2/3*, then the average current drawn by the module will be less. This variability in power due to the modulation index reflects in the stability of this qZSI module (lightly loaded qZSI tends to unstable due to the presence of energy storage elements). Conclusively, it can be said that the top module must be sufficiently loaded (*M* close to unity) to ensure stability.

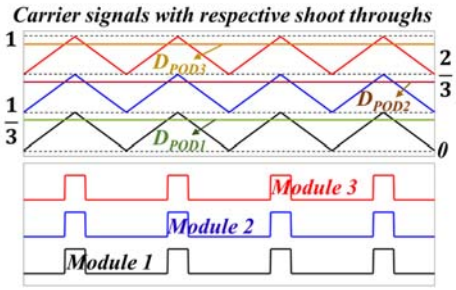
4.3. Proposed PODPS-PWM for Multilevel qZSI

4.3.1. PODPS-PWM Modulation

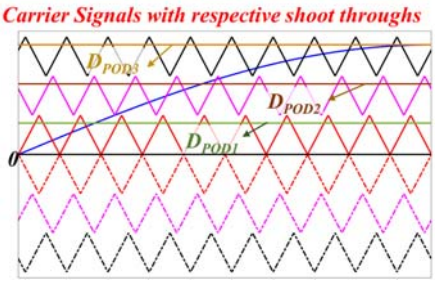
Incorporating the above-said recommendations, a new PODPS-PWM technique is proposed in this dissertation. Simply, it can be described as an optimum combination of PSPWM and LS-PWM techniques. The proposed PODPS-PWM technique consists of '*2n'* carrier signals (uniformly distributed vertically from – 1 to + 1) time-displaced by $180^0/n$ as shown in Figure 4.2(c). Uniform vertical displacement of the carrier signals results in unequal switching's in the respective modules, thereby leading to unequal power distribution among the operating modules. On the other hand, due to the time displacement of carrier signals, the shoot–through pulses are not generated



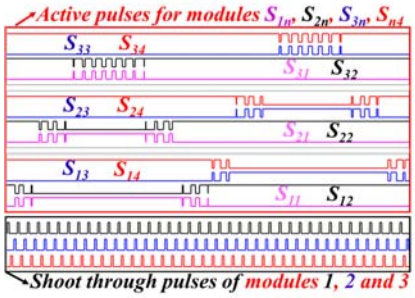
(a) Conventional PS-PWM shoot-through generation



(b) Conventional LS-PWM shoot-through generation



(c) PODPS-PWM switching technique consisting of six carrier signals uniformly displaced vertically and phase-shifted by 60^0



(d) Active pulses and shoot-through pulses of the three modules.

Figure 4.2. PSPWM and LS PWM

simultaneously (and thus shorting of all operating modules is avoided) thereby avoiding any unwanted transitions from V_{dc} to zero.

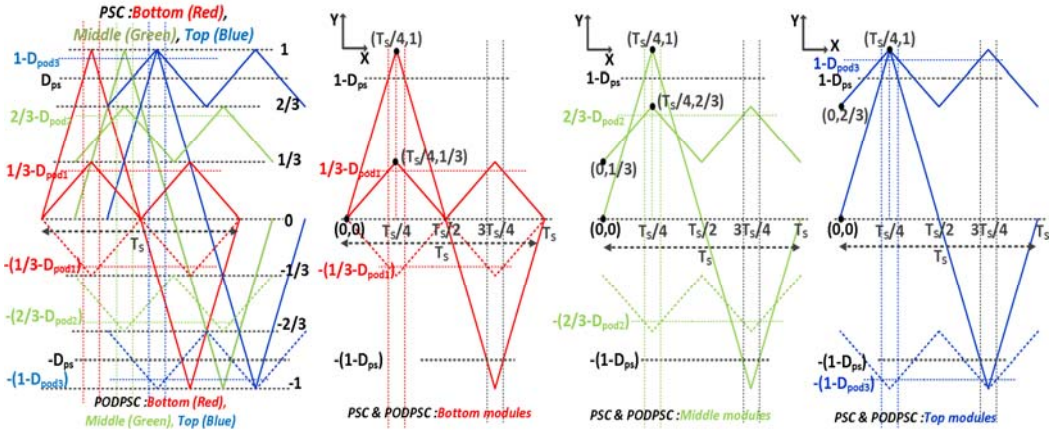
The generated active and shoot-through pulses for a cycle of modulation signal by controlling multilevel qZSI with the proposed PODPS-PWM are shown in Figure 4.2(d). For better understanding, a low switching frequency of carrier signal (1kHz) is considered here. As indicated in Figure 4.2(c), the bottom most carrier signal generates active PWM pulses for S_{11} and S_{14} during the positive half cycle. Similarly, for S_{12} and S_{13} active PWM pulses are generated during the negative half cycle. The bottom module is switched continuously throughout the modulation cycle. Voltage transitions from 0

to V_{dc} and -V_{dc} to 0 are contributed by the bottom module. When the modulation signal is in the 1/3 to 2/3 range, the middle carrier signal generates PWM switching for S_{21} and S_{24} during the positive half cycle and for S_{22} and S_{23} during the negative half cycle and voltage levels transition from V_{dc} to $2V_{dc}$ or $-V_{dc}$ to $-2V_{dc}$ are obtained. The middle module generates zero output voltage during modulation range of $0 - 1/3$ or $-1/3$ to 0 as shown in Figure 4.2(d) [freewheeling through bottom switches S_{22} and S_{24} during the positive half cycle and through S_{21} and S_{23} during negative half cycle]. Similarly, when the modulation signal is in the range of $2/3$ to M or $-2/3$ to $-M$, the top carrier signal generates active PWM pulses for S_{31} and S_{34} during the positive half cycle and S_{32} and S_{33} during a negative half cycle and voltage transitions from $3V_{dc}$ to $2V_{dc}$ or $-3V_{dc}$ to $-2V_{dc}$ are obtained. When the modulating signal is in the range of $0 - 2/3$ or $-2/3 - 0$, like a middle module, a zero switching state is generated by the top module.

4.3.2. The relation between PS-PWM & PODPS-PWM

Figure 4.3(a) shows the carrier signals of PS-PWM and PODPS-PWM along with their *ST* reference. The red-colored carrier signals (continuous and dashed) are for the bottom modules, with higher amplitude belongs to PSPWM and the other carrier with lesser amplitude is of PODPS-PWM. In a simple boost control technique, *ST* references $(1-D_{ps})$ and $-(1-D_{ps})$ creates the same *ST* pulse during the entire modulation cycle, which intersects with the carrier at the same height from zero. Because of the half-wave symmetry of the carriers, only the positive slopes are considered. The simple geometrical analysis of the two-dimensional (X, Y) plane is carried out here.

From Figure 4.3(b), (0, 0) and $(1, T_s/4)$ are the two points on the straight line for PSPWM carrier (Y_1). Similarly, (0,0) and $(1/3, T_s/4)$ are the two points on the straight line for the PODPS PWM carrier (Y_2). Equation of Y_1 and Y_2 are defined as,



(a) (b) (c) (d)

Figure 4.3. (a)Graphical analysis for the relation between the PS-PWM and PODPS-PWM, (b) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (0,1/3, 0) and (0, -1/3, 0) for PODPS-PWM, Represents the bottom modules in both, (c) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (1/3, 2/3,1/3) and (-1/3,-2/3, -1/3) for PODPS-PWM, Represents the middle modules in both, (d) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (2/3, 1, 2/3) and (-2/3,-1, -2/3) for PODPS-PWM, Represents the middle modules in both.

$$Y_1 = \frac{4}{T_S} X_1 \;;\; Y_2 = \frac{4}{3T_S} X_2 \tag{4.1}$$

Substituting $Y_1=(1-D_{ps})$ gives

$$X_1 = \frac{(1-D_{ps})T_S}{4} \tag{4.2}$$

As seen from Figure 4.3(b), $X_1=X_2$, then substituting (4.2) in Y_2(4.1),

$$Y_2 = \frac{4}{3T_S} * \frac{(1-D_{ps})T_S}{4} = \frac{(1-D_{ps})}{3} \tag{4.3}$$

Y_2 is considered as $(1/3-D_{pod1})$ for PODPS-PWM, so the resultant *ST* for the bottom module is

$$\frac{1}{3} - D_{pod1} = \frac{(1-D_{ps})}{3} \tag{4.4}$$

Here, D_{pod1} is the *ST* duty ratio of the bottom module.

A similar straight-line equation concept is applied to Figure 4.3(c) and Figure 3(d) and the respective ST duties for the middle and top modules can be achieved as follows,

$$\frac{2}{3} - D_{pod2} = \frac{(1-D_{ps})}{3} + \frac{1}{3}; 1 - D_{pod3} = \frac{(1-D_{ps})}{3} + \frac{2}{3} \tag{4.5}$$

D_{pod2} and D_{pod3} are the ST duty ratio of the middle and top modules, respectively.

In the n-module qZS-CMI system, the ST duty for the k^{th} module (for bottom module $k = 1$ and for the top module $k = n$) is,

$$\frac{k}{n} - D_{podk} = \frac{(1-D_{ps})}{n} + \frac{k-1}{n} \tag{4.6}$$

From (4.5) - (4.7), it can be concluded that all the modules have the same amount of ST duty which is

$$D_{podn} = \frac{D_{ps}}{3} \tag{4.7}$$

In *n*-modules cascaded system, the following relation (in PS-PWM) is respected to avoid overlapping of AS and ST pulses,

$$M + D_{ps} \leq 1 \tag{4.8}$$

Here, M is the modulation index. The new safe operating limit for the PODPS-PWM can now be defined as

$$M + \frac{D_{ps}}{n} \leq 1 \tag{4.9}$$

4.4. Comparison of Switching losses

Switching pulses for the bottom module (with PODPS-PWM) can be characterized into six regions as shown in Table 4.1. Here, 'A' refers to active state switching; 'ST' refers to shoot – through switching; 'A + ST' refers to both active state and ST state switching during the defined period.

Table 4.1. Active and shoot-through pulses for a modulating cycle

Modulation Signal Region	S_{11}	S_{12}	S_{13}	S_{14}
0 to $\pi/9$	A+ST	A+ST	ST	0
$\pi/9$ to $\pi-\pi/9$	0	ST	ST	0
$\pi-\pi/9$ to π	A+ST	A+ST	ST	0
π to $\pi+\pi/9$	ST	0	A+ST	A+ST
$\pi+\pi/9$ to $2\pi-\pi/9$	ST	0	0	ST
$2\pi-\pi/9$ to 2π	ST	0	A+ST	A+ST

From Table 4.1, it can be inferred that switching losses in switches S_{11} and S_{13} are the same when time-averaged for a modulating cycle. Similarly, switching losses in switches S_{12} and S_{14} are the same when time averages for a modulating cycle. This is due to the nature of LS-PWM switching. Thus, these four switches can be categorized as type – 1 and type – 2 switches.

4.4.1. *Switching losses in the active state*

Switching losses for switches during the active state are given by,

$$P = \frac{1}{\pi}\int_{0}^{\pi} \frac{f_s(E_{ON} + E_{OFF} + E_{REC})V_{dc}i_{ac}}{V_{ref}I_{ref}}\, d\omega t \tag{4.10}$$

where f_s is the switching frequency; E_{ON} and E_{OFF} are the turn-on and turn-off energy losses per pulse of the MOSFET; E_{REC} is the reverse recovery loss of the antiparallel diode; V_{ref} and I_{ref} are the switched voltage and current references; V_{dc} is the dc-link peak voltage of each module and i_{ac} is the ac load current. For further simplification, P_{FAC} is defined as

$$P_{FAC} = \frac{f_s(E_{ON} + E_{OFF} + E_{REC})V_{dc}}{V_{ref}I_{ref}} \tag{4.11}$$

For type – I switch (S_{11} and S_{13}), active switching losses occur from 0 to $\frac{\pi}{9}$ and $\frac{8\pi}{9}$ to π. For type – I switch, active state switching losses are given by,

$$P_{POD-AI} = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\int_{0}^{\pi/9} \mathrm{Sin}\,\omega t d\omega t + \int_{8\pi/9}^{\pi} \mathrm{Sin}\,\omega t d\omega t\right] \tag{4.12}$$

$$P_{POD-AI} = \frac{2P_{FAC}\,\mathrm{Im}}{\pi}\left[0.0603\right] \tag{4.13}$$

where $\frac{2P_{F\,AC}\,I_m}{\pi}$ is defined as the active state switching losses in PS-PWM and I_m is the peak of ac load current. $P_{LSPWM} = 6\%$ of switching losses in PS-PWM. For type – II switches (S_{12} and S_{14}), active state switching losses occur from π to $\pi + \frac{\pi}{9}$ and $\pi + \frac{8\pi}{9}$ to 2π. Losses are given by,

$$P_{POD-AI} = \frac{P_{FAC}}{\pi}\left[\int_{0}^{\pi+\pi/9} \mathrm{Sin}\,\omega t d\omega t + \int_{\pi+8\pi/9}^{\pi} \mathrm{Sin}\,\omega t d\omega t\right] \tag{4.14}$$

$$P_{POD-AI} = \frac{2P_{FAC}\,\mathrm{Im}}{\pi}\left[0.0603\right] \tag{4.15}$$

$P_{POD-AII} = 6\%$ of switching losses in PS-PWM.

During a fundamental frequency cycle, active state losses in all the switches remain the same.

4.4.2. *Switching losses in shoot-through state*

Switching losses in this state are given by,

$$P_{sw,ST} = \frac{1}{2\pi}\int_{0}^{2\pi} f_s\left(E_{ON} + E_{OFF}\right)\left(\frac{V_{dc}}{V_{ref}I_{ref}}\right)\left(i_L + \frac{i_{ac}}{2}\right)d\omega t \tag{4.16}$$

For simplification of further analysis, P_{FST} is defined as equal to $P_{FST} = f_s\left(E_{ON} + E_{OFF}\right)\left(\frac{V_{dc}}{V_{ref}I_{ref}}\right)$.

For type – I switch, shoot – through state switching losses occur from 0 to $\frac{\pi}{9}$ and $\pi - \frac{\pi}{9}$ to 2π. For these switches, shoot – through state switching losses are given by,

Table 4.2. Switching losses comparison for different modulations

Modulation	S_1	S_2	S_3	S_4
Active state				
PS-PWM	100%	100%	100%	100%
PWAM [15]	13.4%	13.4%	50%	50%
PODPS	6%	6%	6%	6%
Shoot – through state				
PS-PWM	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$
PWAM [15]	$P_{FST}\left[\frac{5I_L}{6}-\frac{\mathrm{Im}\,ss}{4\pi}\right]$(>16% saving)		$P_{FST}\left[\frac{2I_L}{3}-\frac{\sqrt{3}\,\mathrm{Im}\,ss}{4\pi}\right]$(> 33% saving)	
PODPS	$P_{FST}\left[\frac{11I_L}{18}-\frac{0.94\,\mathrm{Im}\,ss}{4\pi}\right]$(> 39% saving)		$P_{FST}\left[\frac{I_L}{2}-\frac{\mathrm{Im}\,ss}{2\pi}\right]$(>50% saving)	

$$P_{POD-SI}=\frac{P_{FST}}{2\pi}\left[\int_0^{\pi/9}\left(i_L+\frac{i_{ac}}{2}\right)d\omega t+\int_{8\pi/9}^{2\pi}\left(i_L+\frac{i_{ac}}{2}\right)d\omega t\right] \tag{4.17}$$

$$P_{POD-SI}=P_{FST}\left[\left(\frac{11}{18}\right)I_L-\left(\frac{0.9397}{4\pi}\right)\mathrm{Im}\,ss\right] \tag{4.18}$$

where $P_{F\,ST}\,I_L$ is defined as the shoot-through state switching losses in PS-PWM, I_{mss} is the steady-state peak load current and I_L is the average inductor current.

For type – II switch, shoot – through state switching losses occur from 0 to π. For these switches,

$$P_{POD-SII}=\frac{P_{FST}}{2\pi}\left[\int_0^{\pi}\left(i_L-\frac{i_{ac}}{2}\right)d\omega t\right] \tag{4.19}$$

$$P_{POD-SII}=P_{FST}\left[\frac{I_L}{2}-\frac{\mathrm{Im}\,ss}{2\pi}\right] \tag{4.20}$$

A comparison of switching losses with the proposed PWM method is given in table 4.2.

4.5. Experimental Results and Discussion

A 1.5kW, 230V experimental prototype is built to validate the proposed PODPS-PWM switching strategy in a cascaded multilevel qZS converter. Three qZSI modules are

connected in cascade to achieve seven–level output voltage across the RL load. The components specification for the experimental prototype is given in Table 4.3. The Virtex-5 FPGA control board is used for the control of seven-level qZSI at 5 kHz switching frequency. Each module is supplied with an input voltage of 95V. Input voltage is boosted to 140V at 16% shoot-through duty.

4.5.1. THD Performance of proposed PWM switching

Figure 4.4 shows the seven–level output voltage and load current waveform along with their respective *THD* spectrum. Each voltage level is 140V obtained by boosting the respective input voltage of 95V. the resultant seven – level voltage peak is obtained at 420V and RMS value is 240V with a modulation index of 0.8. From the *THD*

Table 4.3 Quasi Impedance Source Inverter parameters

Component	Specification	Component	Specification
$L_1 = L_2$	1 mH, 15A	Quasi Diode	160V, 15A
C_1	500 uF, 125 V	MOSFET	200V, 20 A
C_2	500 uF, 35 V	V_{dc}	140V

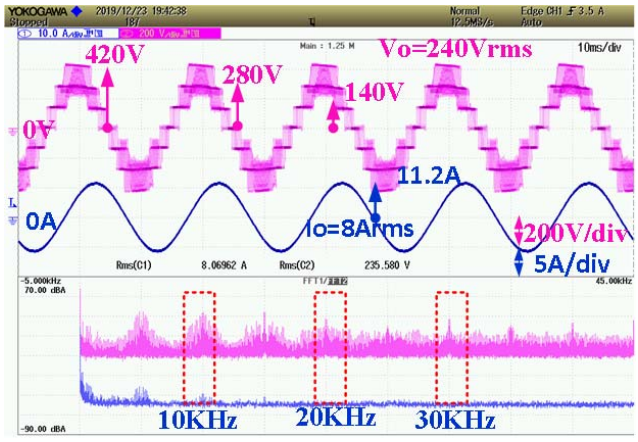
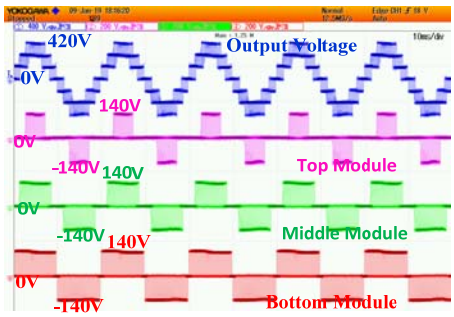


Figure 4.4. Output voltage levels and the output current with FFTs

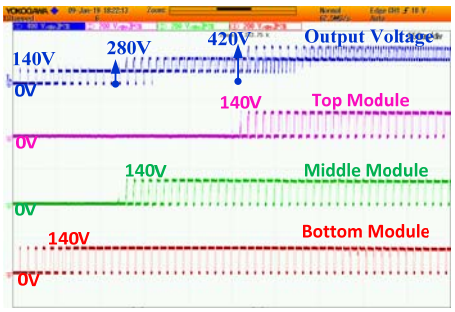
spectrum of both signals, it should be observed that dominating frequency component is 10kHz (2 times the switching frequency). Benefits of using multilevel qZSI (like low *dV/dt* and *THD*) are obtained with the proposed method.

4.5.2. Multilevel Operation with PODPS-PWM,

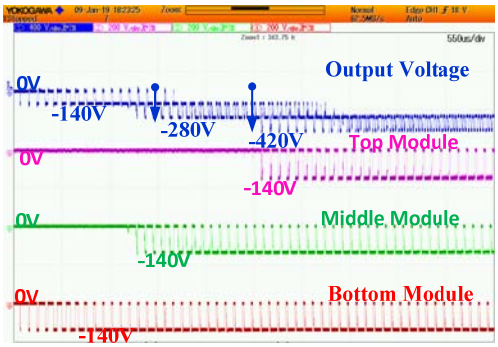
From Figure 4.5(a), it can be observed that the output voltage waveform consists of the transition between only two levels i.e., between nV_{dc} *to* $(n-1)*V_{dc}$ where $n \in [0, 3]$ on the positive side and $n \in [0, -2]$ on the negative side. Also Figure 4.5(a) clearly shows the contribution of the respective module according to their placement and control in the multilevel structure i.e., the bottom module generates output voltage throughout the



(a) Steady state waveform



(b) zoomed portion for the positive half cycle



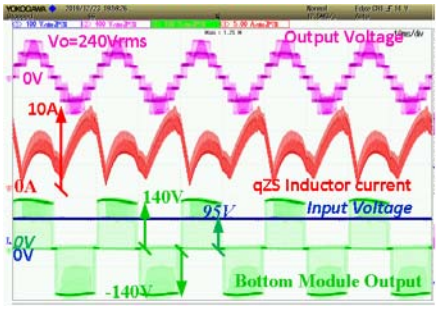
(c) zoomed portion for the negative half cycle.

Figure 4.5. Voltage waveforms for line voltage (blue), module output voltages, top (pink), middle (green) and bottom (red).

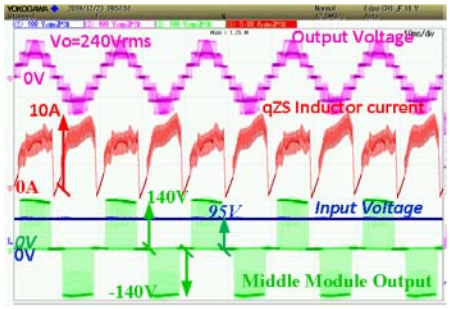
entire modulation cycle whereas middle and top modules generate output voltage once the modulation index exceeds *1/3* and *2/3* respectively on the positive side. Zoomed waveform of the positive half cycle shows in Figure 4.5(b) clearly validates this fact. Similar behavior can be observed in the negative half cycle as shown in Figure 4.5(c). These results clearly indicate level-shifted operation with the proposed PODPS-PWM technique achieving low *dV/dt,* stable dc bus output voltage, and multilevel operation.

4.5.3. Unequal Power-sharing with PODPS-PWM

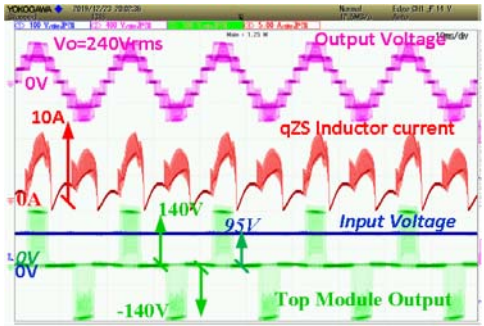
Figure 4.6 shows phase output voltage, DC-link voltage, input voltage, and inductor current of the bottom, middle, and top modules respectively. Input voltage of 95V is applied to each qZSI module and each dc bus voltage of 140V is obtained at the output of quasi network *(V_{dc})*. For the bottom module (shown in Figure 4.6(a)), a continuous



(a) Bottom module



(b) Middle module



(c) Top module

Figure 4.6. Module level waveforms of CMLI output voltage (pink), inductor current (red), input voltage (blue) and bridge output voltage (green).

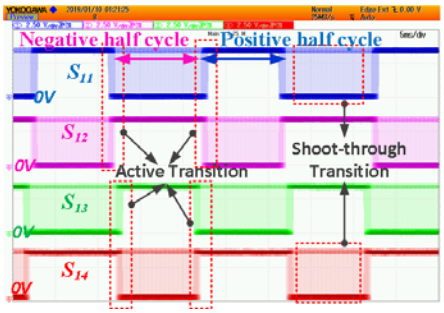
input current of 7.3A mean (11A peak) is drawn. For the middle module (shown in Figure 4.6(b)), an input current of 6.3A is drawn (peak current 10A). For the top module, the input current of 3.5A (as shown in Figure 4.6(c)) with the same peak current of 10A is drawn from the power supply. It can be observed here, that although the three currents have the same peak value, the mean value of input current is different suggesting operation at uneven power distribution among operating modules.

4.5.4. Validation of switching losses with switching pulses

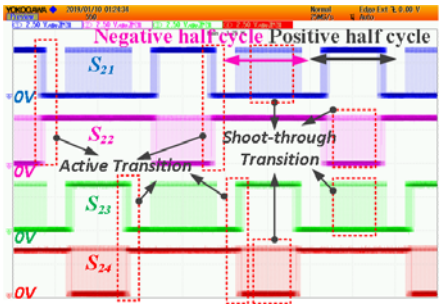
In section 4.5.4, switching losses with PODPS-PWM are discussed. From there, it should be observed that when the switch conducts continuously no shoot-through state and no active state switching losses occur. However, when PWM switching (instead of continuously pulse) is obtained, then both shoot-through and active losses occur in the switch.

Figure 4.7(a) shows switching pulses for the bottom qZSI module switches (S_{11}, S_{12}, S_{13} *and* S_{14}). During the positive half cycle, S_{11} is switched initially according to PWM and S_{14} is continuously ON. For the remaining entire period, both S_{11} and S_{14} are continuously ON. During the positive half cycle, S_{12} and S_{13} switches are turned ON only during the shoot-through period. Similarly, during the negative half cycle, S_{13} and S_{12} are switched according to PWM initially. For the remaining negative cycle period, S_{13} and S_{12} are continuously ON whereas S_{11} and S_{14} are ON only during the shoot-through period in the negative cycle.

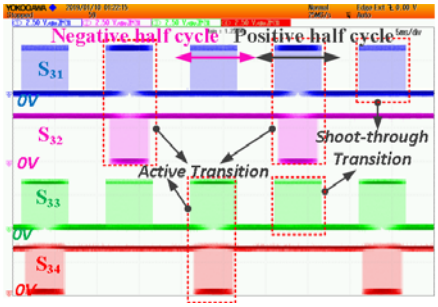
Switching gate signals (S_{21}, S_{22}, S_{23}, *and* S_{24}) of the middle modules are given in Figure 4.7(b). At the beginning of the positive cycle, S_{21} and S_{23} are OFF and S_{22} and S_{24} are continuously ON to create zero output voltage of the middle module (during *0 to 1/3* range of modulating signal). Active transition happens with the help of S_{21} and S_{24} to



(a) bottom module



(b) middle module



(c)) top module

Figure 4.7. Switching pulses waveforms for the four switches showing S_{n1} (blue), S_{n2} (pink), S_{n3} (green), S_{n4} (red) where $n = 1$ (bottom), 2 (middle) and 3(top).

create 140V and 280Voutput voltage levels. For the rest of the positive half cycle, S_{21} and S_{24} remain ON. S_{22} and S_{23} are turned ON only for the shoot-through state. For the negative half cycle, S_{22} and S_{23} will be turned ON according to PWM and for the rest of the negative cycle, S_{22} and S_{23} are continuously ON. Due to this switching, transition from -140V to -280V occurs. S_{21} and S_{24} are turned ON only to achieve the shoot-through state.

Switching gate signals (S_{31}, S_{32}, S_{33}, *and* S_{34}) of the top module are given in Figure 4.7(c). Similar, to the middle module, the top module also operates at zero output voltage for modulation signal duration of 0 to *2/3* on the positive side and 0 to *-2/3* on the negative side. During the positive half cycle, S_{31} and S_{34} are mostly ON and S_{32} and S_{33} are turned ON only to achieve the shoot-through state. On the negative half cycle,

S_{32} and S_{33} are mostly ON and S_{31} and S_{34} are only turned ON only to achieve the shoot-through state.

4.6. Summary

In this chapter, a novel PODPS-PWM switching technique is proposed for multilevel qZSI to achieve unequal power-sharing among the operating modules. Firstly, conventional LS-PWM is implemented to multilevel qZSI. Here, poor THD performance, low voltage magnitude and unstable qZSI operation are obtained. The proposed modulation method and switching loss analysis are presented in detail to highlight the benefits. Detailed experimental results for 1.5kW, 7-level qZSI connected to RL load are presented with the proposed PODPS-PWM. Conclusively, the results presented validate the unequal power-sharing nature, low switching losses, improved PV power extraction, and stable operation of the proposed PWM. The major drawback of this proposed PWM is the unequal power sharing between the modules. Which can be clearly observed in the input current and the grid current. So in the next chapter the modification to this PWM has been carried.

CHAPTER 5: NOVEL LEVEL-SHIFTED PWM TECHNIQUE FOR EQUAL POWER-SHARING AMONG QUASI Z SOURCE MODULES IN CASCADED MULTILEVEL INVERTER

5.1. Introduction,

In the previous chapter it is observed that in the Cascaded qZS MLI the unequal power distribution is hindering its application to the PV systems. To address this issue further control and different PWM have been investigated and developed. Multidimensional pulse width modulation (MD-PWM) [19], was proposed to improve the voltage control of the modules at a higher speed and accuracy by using the hysteresis controller. This results in unequal switching frequency which H–Bridge-based CMIs are also controlled with *'2n'* carrier signals, which are uniformly displaced vertically between *'-1'* to *'+1'* where 'n' represents number of HB modules. This method is known as LS-PWM [20]. Mainly, LS-PWM includes PD-PWM, POD-PWM, and APOD-PWM methods. These different LS-PWM methods are shown in Figure 5.1. In [21], an attempt has been made to apply these LS-PWM techniques to five-level qZS-CMIs. The rotating carrier PWM technique applied to the CML-HB is reported in [22, 23]. Therefore, it can be observed from [21], that power distribution among the operating modules is uneven and the switching sequence is different for different modules resulting in increased input

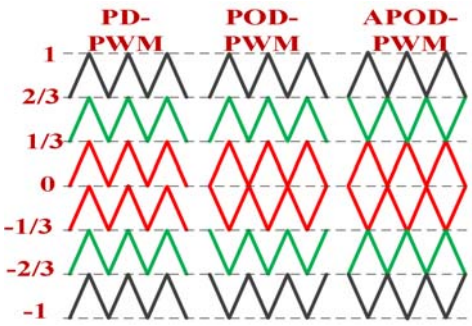


Figure 5.1. Different LS-PWM schemes

current distortion and higher THD. In [22], as a standard two-stage converter is connected in the Single Delta bridge cell format, which balances the power by injection of 3rd harmonic component between the cascaded modules. For high power applications, these harmonics consume a significant amount of power thereby limiting the practical applications. To address this power imbalance problem, authors in [24-27] have proposed novel technique by rotating the carriers for CML-HBI.

This chapter proposes a new modulation technique that combines the advantages of PS-PWM-based qZS-CMI and LS-PWM-based CML-HBI. This includes features like only one module switching at a time (like LS-PWM) and equal power-sharing among operating modules (like PS-PWM). The proposed method uses POD-PWM (a method of LS-PWM) and PS-PWM so it is named as PODPS-PWM for the qZS-CMI. The feasibility of the proposed method is validated using simulation and experimental results.

5.2. Single Phase qZS-CMI, Characteristics of qZSI

Single-phase qZS-CMI based solar PV power system is represented in Figure 5.2. There are three qZSI modules connected in cascade. Each qZSI module consists of PV panels, two inductors L_{n1} and L_{n2}, two capacitors C_{n1} and C_{n2}, one diode and four MOSFETs based HB module, where $n \in [3]$. Each module works in three different states, Active state (AS), shoot-through state (ST) and zero state (ZS). qZSI is assumed to be operating in Continuous Conduction Mode (CCM). The boosted DC voltage (output of qZS network) is the sum of the two capacitor voltages C_{n1} and C_{n2}.

The resultant output voltage of the qZS-CMI for Figure 5.2 is,

$$V_o = V_{o1} + V_{o2} + V_{o3} \tag{5.2}$$

V_{o1}, V_{o2}, *and* V_{o3} are the output voltage of the individual modules, Vo is the output

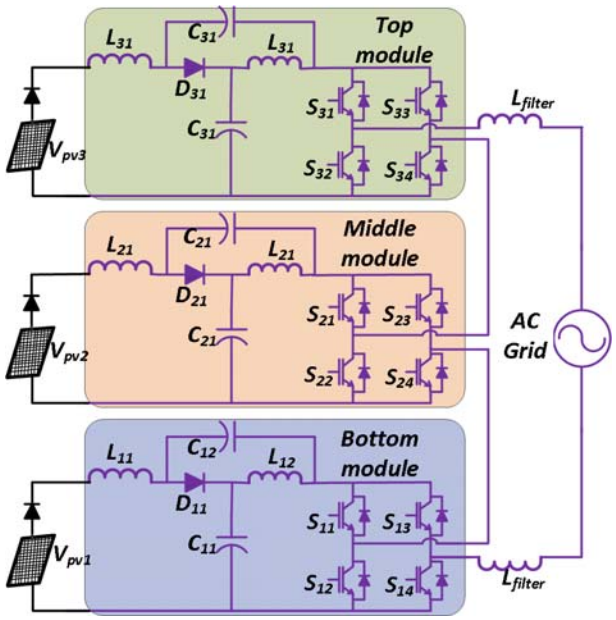


Figure 5.2. Single phase qZS-CMI PV power system

voltage of the CMLI. The grid voltage magnitude, phase and frequency should be the same as that of the qZS-CMI output.

5.3. PODPS-PWM for Single Phase QZS-CMI

5.3.1. PODPS-PWM for qZS-CMI

The working principle of PODPS-PWM is illustrated in Figure 5.3 for the seven-level qZSI. The conventional rule is to use six carriers for a seven-level inverter. All the upper carriers are level-shifted by an amplitude 1/3 and phase-shifted by 120^0 with respect to one another. All the lower carriers are exactly phase opposed with their respective upper carriers (color coding is represented). The outer carriers are used to generate the PWM signals for the top module (black color in Figure 5.3), middle carriers are used to generate the PWM signals for the middle module, similarly innermost carriers are used for bottom modules. Due to this phase shift, the ST interferences are avoided as seen in Figure 5.3, thereby avoiding unwanted high *dV/dt*, low rms voltage and high THD content. It can be observed that the module output

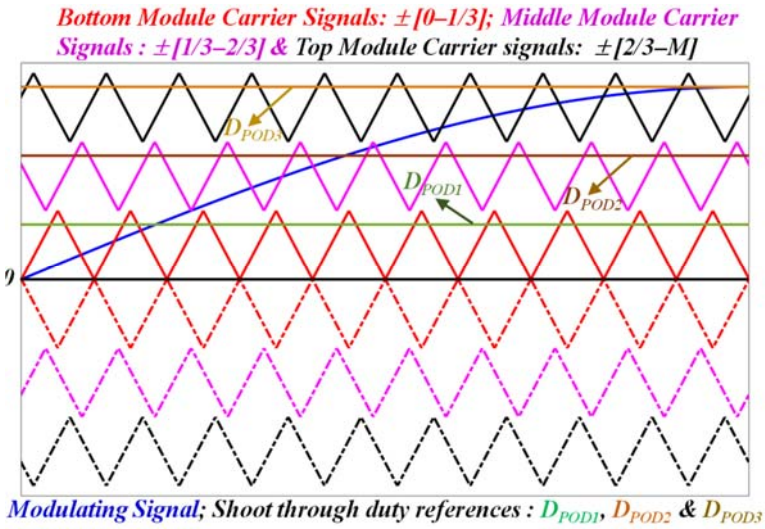
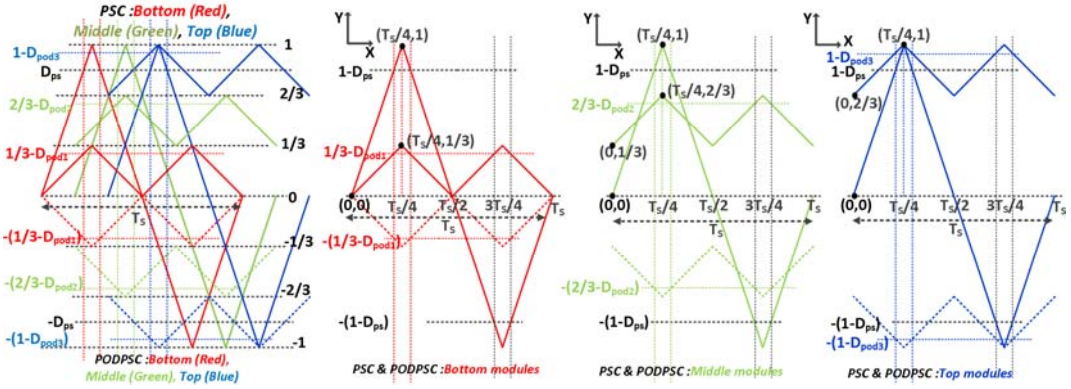


Figure 5.3. PODPS-PWM for qZS-CMI

voltages for all the three modules are different. The bottom module and the middle module are operated in over modulation mode. Furthermore, top module is operated in under modulation mode. Depending upon the required voltage reference, the middle module may also operate in under modulation mode. These PWM switching patterns ensure proper voltage levels but create uneven distribution of the power between the modules in normal operation (when equal input voltage is applied to all the qZSI modules). This also generates higher input current harmonics. In order to eliminate the drawbacks of PODPS-PWM, a simple and effective modification is introduced in PODPS-PWM to balance the power among the operating modules in normal full load operation. In this chapter, normal operation considered as balanced equal power condition.

5.3.2. Relation between PS-PWM & PODPS-PWM for qZS-CMI

Figure 5.4(a) shows the carrier signals of PS-PWM and PODPS- PWM along with their shoot-through (ST) reference. The red-colored carrier signals (continuous and dashed) are for the bottom modules, with higher amplitude belongs to PSPWM and the



(a) (b) (c) (d)

Figure 5.4. (a)Graphical analysis for the relation between the PS-PWM and PODPS-PWM, (b) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (0,1/3, 0) and (0, -1/3, 0) for PODPS-PWM, Represents the bottom modules in both, (c) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (1/3, 2/3,1/3) and (-1/3,-2/3, -1/3) for PODPS-PWM, Represents the middle modules in both, (d) carrier (0, 1, 0, -1,0) for PS-PWM, carrier (2/3, 1, 2/3) and (-2/3,-1, -2/3) for PODPS-PWM, Represents the middle modules in both.

other carrier with lesser amplitude is of PODPS-PWM. In simple boost control technique, ST references ($1-D_{ps}$) and $-(1-D_{ps})$ creates the same ST pulse during the entire modulation cycle, which intersects with the carrier at the same height from zero. Because of the half-wave symmetry of the carriers, only the positive slopes are considered. The simple geometrical analysis of the two-dimensional (X, Y) plane is carried out here.

From Figure 5.4(b), (0, 0) and (1, $T_s/4$) are the two points on the straight line for the PSPWM carrier represented by Y_1. Similarly, (0, 0) and (1/3, $T_s/4$) are the two points on the straight line for PODPS-PWM carrier represented asY_2. Equation of Y_1 and Y_2 are defined as,

$$Y_1 = \frac{4}{T_S} X_1 \tag{5.2}$$

$$Y_2 = \frac{4}{3T_S} X_2 \tag{5.3}$$

Substituting the known ST duty of 1-D_{ps} in (4) we get,

$$X_1 = \frac{(1-D_{ps})T_S}{4} \tag{5.4}$$

As seen from Figure 5.5(b), X_1=X_2, then substituting (5.3) in (5.4),

$$Y_2 = \frac{4}{3T_S} * \frac{(1-D_{ps})T_S}{4} = \frac{(1-D_{ps})}{3} \tag{5.5}$$

Y_2 is considered as (1/3-D_{pod1}) for the PODPS-PWM, so the resultant ST for the bottom module is,

$$\frac{1}{3} - D_{pod1} = \frac{(1-D_{ps})}{3} \tag{5.6}$$

Here, D_{pod1} is the ST duty ratio of the bottom module.

A similar straight-line equation concept is applied to Figure 5.4(c) and Figure 5.4(d) and the respective ST duties for the middle and top modules can be achieved as follows,

$$\frac{2}{3} - D_{pod2} = \frac{(1-D_{ps})}{3} + \frac{1}{3} \tag{5.7}$$

$$1 - D_{pod3} = \frac{(1-D_{ps})}{3} + \frac{2}{3} \tag{5.8}$$

D_{pod2} and D_{pod3} are the ST duty ratio of the middle and top modules respectively.

In n-module qZS-CMI system, the ST duty for the kth module (for bottom module k = 1 and for the top module k = n) is given by,

$$\frac{k}{n} - D_{podk} = \frac{(1-D_{ps})}{n} + \frac{k-1}{n} \tag{5.9}$$

From (5.8) - (5.10), it can be concluded that all the modules having the same amount of ST duty can be given as,

$$D_{pod1} = D_{pod2} = D_{pod3} = \frac{D_{ps}}{3} = D_{podn} \tag{5.10}$$

In n-modules cascaded system, to overcome the problem of overlap between the AS and ST in PS-PWM following equation has to be satisfied,

$$M + D_{ps} \leq 1 \tag{5.11}$$

M is the modulation index. The new safe operating limit for the PODPS-PWM can be achieved as,

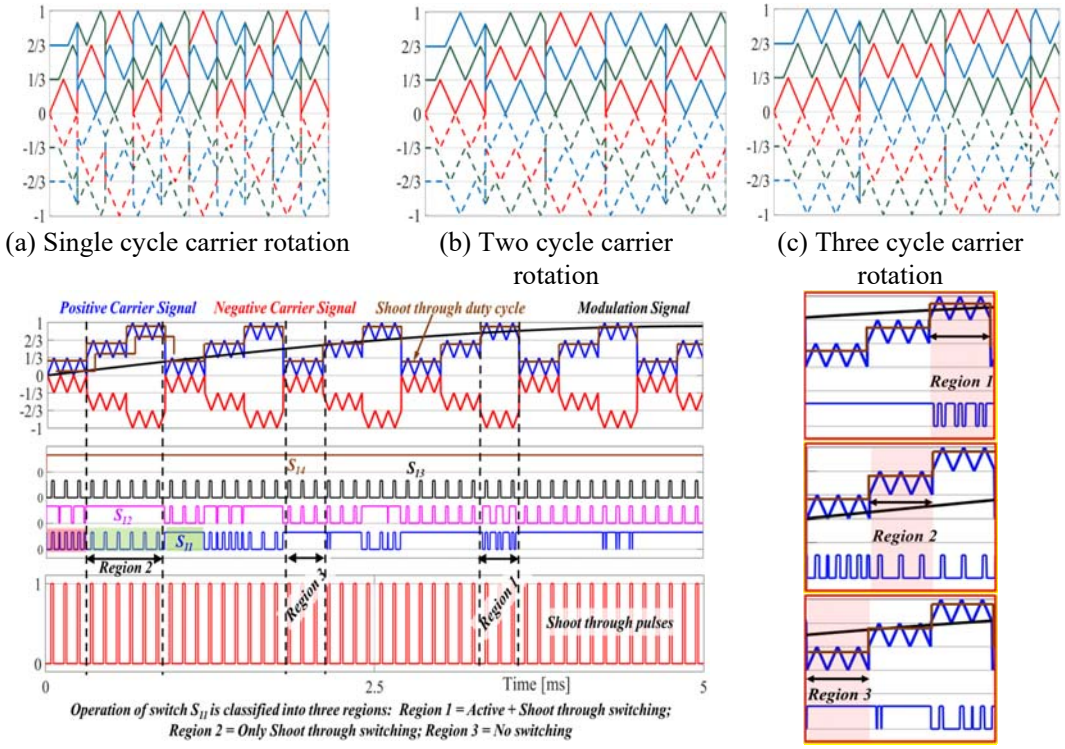
$$\begin{aligned} M + D_{podn} &\leq 1 \\ M + \frac{D_{ps}}{n} &\leq 1 \end{aligned} \tag{5.12}$$

5.4. Proposed Modified PODPS-PWM for QZS-CMI

From Figure 5.3 it can be observed that the number of switching in all the modules will be unequal due to level – shifted modulation approach. To make the switching's across the modules to be equal, carrier signals must be rotated between the levels, which will make the power distribution between the modules vary according to the rotation of the carriers. The rotation must be maintained in such a way that the average power in each module is equal. There are several chapters that propose cyclic carrier rotation for fixed [24] and variable [26] time intervals. In [27], the authors proposed an unrestricted carrier rotation scheme, as the rotation is not fixed and not variable time. Here, two or more carriers are interchanged during the rotation process. There are several methods for the carrier rotation scheme to control input power and the DC-link capacitor voltage level. At unity power factor, shifting carrier to upper levels reduces the average power output of the module, whereas shifting to lower levels will increase the average power output of the modules.

5.4.1. Method 1, Single Cycle Carrier Rotation

Figure 5.5(a) represents proposed method 1 i.e., single cycle carrier rotation technique. Red, green and blue carriers are assigned for the bottom, middle and top modules. These carriers are phase-shifted by 120^0 to include the benefits of PS-PWM to form the PODPS-PWM. In every switching cycle, these carriers will change their position from one level to the other. The bottom module carrier (red) presents its first carrier (first switching cycle) in between *0 - 1/3* level but in the next cycle, the carrier is shifted to *1/3 - 2/3* level, then in its third cycle, the carrier is shifted to *2/3 - 1* level. After the third cycle, it comes back to the initial position i.e., *0 - 1/3* level to start a new cycle. This forms one complete rotation of the bottom carrier for the positive half cycle modulation. For achieving the negative half cycle modulation, phase opposition is applied to the positive carrier. This means it must be multiplied with *"-1"* to change from the positive side to the negative side and will exactly be in phase to avoid the ST



(a) Single cycle carrier rotation (b) Two cycle carrier rotation (c) Three cycle carrier rotation

(d) Detailed switching of the uniform rotation of the proposed modulation scheme

Figure 5.5. Different carrier rotation techniques of the PODPS-PWM for the qZS-CMI

duty overlap and higher *dV/dt* problems. A similar process applied to the middle and the top modules starts its first cycle of rotation from *1/3 – 2/3* and *2/3 – 1* levels respectively.

5.4.2. Method 2, Two Cycle Carrier Rotation

Figure 5.5(b) represents the proposed method 2 for the two-cycle carrier rotation technique. Similar to single carrier rotation, instead of one carrier, two carriers will be rotated here. For every two switching cycle, these carriers will change their position from one level to the other level. In case of the red (bottom module carrier), it presents its first two carrier cycles in *0 – 1/3* level but the next set of two carrier cycles is shifted to *1/3 – 2/3* level, then its third set of carrier cycles are shifted to *2/3 – 1* level. After the third set of shifting, carriers come back to the initial position of *0 – 1/3* level to start its new cycle. This forms one complete rotation of the bottom carrier for the positive half cycle modulation. For achieving the negative half cycle modulation, phase opposition is applied to positive carrier by multiply it with *"-1"*. Similar process is applied to the middle and the top modules starting the first two cycles from *1/3 – 2/3* and *2/3 – 1* levels, respectively.

5.4.3. Method 3, Three Cycle Carrier Rotation

Figure 5.5(c) represents the proposed method 3 for three cycle carrier rotation technique. Like above two methods, carrier signal position is changed after every three switching cycles as illustrated for the three module carrier signals in Figure 5.5(c). For carrier signals on the negative side, carrier signal is multiplied with '-1' to achieve the other three carrier signals.

The detailed PWM generation logic for bottom module carrier signals and first module switching signal is given in Figure 5.5(d).

5.5. Switching Loss Analysis

The number of cycles in each output voltage level in a particular modulation region are given by,

$$No.of\ cycles = \frac{f_S}{f_m * 2\pi} * \left\{\sin^{-1}\left(\frac{m+1}{N}\right) - \sin^{-1}\left(\frac{m}{N}\right)\right\} \quad (5.13)$$

where f_s is the switching frequency; f_m is the modulation frequency; N represents the number of qZSI modules; m = 0,1,2 represents modulation range from 0 - 1/3, 1/3 - 2/3 and 2/3 – 1, respectively. This equation shows an unequal number of voltage pulses in each voltage level, due to non – linear nature of the sinusoidal modulation signal.

To analyze the switching loss occurring in qZSI module, a detailed understanding of the carrier rotation concept and its effect on switching pulses must be done. Figure 5.5(d) shows a detailed pulse generation process for the quarter fundamental cycle.

Figure 5.5(d) shows bottom module carrier signals rotated for three cycles in each modulation level. When the carrier signal is rotated between the three available modules, the following three regions are identified for switch S_{11} as observed in Figure 5.5(d).

a) Region – 1, In this region, switching pulses consists of PWM-generated active pulses and equidistant shoot – through pulses. When the carrier signal is in this region, both active and shoot – through pulses are observed.
b) Region – 2, In this region, the carrier signal goes above the modulation signal. Due to this, no active switching occurs here, however, shoot-through pulses are generated in this region.
c) Region – 3, In this region, the carrier signal lies below the modulation signal. Due to this, the generated active pulses are continuous pulses thereby avoiding any active switching in this region.

For switching loss analysis, the fundamental cycle is classified into twelve regions

and the performance of each switch is determined in the given region. Characterization of switches and conduction angle in a given modulation range (i.e., *0 - 1/3, 1/3 - 2/3, 2/3 - 1* for seven-level qZSI) are given in Table – A in the appendix section. From Table – A (in appendix), it can be observed that when averaged over a fundamental cycle, switches S_{11} and S_{13} would incur the same average loss (although shifted by half fundamental cycle). On the other hand, the same is true for switches S_{12} and S_{14}. Based on this observation, these four switches can be classified as Type – 1 and Type – 2 switches.

Type – 1 switch consists of S_{11} and S_{13} switches which give the same average loss for the fundamental cycle. Similarly, Type – 2 switch consisting of S_{12} and S_{14} gives identical switching loss when averaged over a fundamental cycle. Switching loss for Type – 1 and Type – 2 switches are given below,

5.5.1. Power loss in Equal power distribution

5.5.1.1. Switching losses in active state

Switching losses for semiconductor switch during active state are given by [6] &[68]

$$P = \frac{1}{2\pi}\int_0^{\pi} \frac{f_s(E_{ON}+E_{OFF}+E_{REC})\, V_{dc} i_{ac}}{V_{ref} I_{ref}}\, d\omega t \tag{5.14}$$

where fs is the switching frequency; E_{ON} *and* E_{OFF} are the turn-on and turn-off energy losses per pulse of the MOSFET; E_{REC} is the reverse recovery loss of the antiparallel diode; V_{ref} and I_{ref} are the switched voltage and current references; V_{dc} is the dc-link peak voltage of each module and i_{ac} is the ac load current.

For type – 1 switch (S_{11} and S_{13}), in the modulation region 0 to $\frac{\pi}{9}$, active switching losses occur for one-third of duration i.e., the switching losses occur from 0 to $\frac{\pi}{27}$. 3Conclusively, active switching losses when averaged over a fundamental cycle are given by (17).

$$P_{POD-A} = \frac{P_{F\,AC} I_m}{2\pi}\left[\int_0^{\frac{\pi}{27}} Sin\omega t d\omega t + \int_{\frac{\pi}{9}}^{\frac{\pi}{9}+\frac{5\pi}{36}*\frac{1}{3}} Sin\omega t d\omega t + \int_{\frac{\pi}{4}}^{\frac{\pi}{4}+\frac{\pi}{12}} Sin\omega t d\omega t + \right.$$

$$\left.\int_{\frac{\pi}{2}}^{\frac{\pi}{2}+\frac{\pi}{12}} Sin\omega t d\omega t + \int_{\frac{\pi}{2}+\frac{\pi}{4}}^{\frac{\pi}{2}+\frac{\pi}{4}+\frac{5\pi}{36}*\frac{1}{3}} Sin\omega t d\omega t + \int_{\pi-\frac{\pi}{9}}^{\pi-\frac{\pi}{9}+\frac{\pi}{27}} Sin\omega t d\omega t + \int_{\pi}^{2\pi} 0 * Sin\omega t d\omega t\right] \quad (5.15)$$

Substituting the limits and simplifying,

$$P_{POD-A} = \frac{P_{F\,AC} I_m}{2\pi}[0.6605] \quad (5.16)$$

$P_{POD-A} = 33\%$ of active state switching loss in PS-PWM.

For type – II switch also the active state switching losses will be same when averaged over a fundamental cycle.

5.5.1.2. Switching losses in shoot-through states

In conventional PS-PWM switching technique, shoot – through state loss is given by [68],

$$P_{sw,\,ST} = \frac{1}{2\pi}\int_0^{\pi} f_s(E_{ON} + E_{OFF})\frac{V_{dc}}{V_{ref} I_{ref}}\left(\frac{i_L + i_{ac}}{2}\right) d\,\omega t \quad (5.17)$$

For type – I switch, shoot – through state switching losses occurs throughout the fundamental cycle. Switching losses in this switch type is given by (5.20).

$$P_{POD-SI} = \frac{P_{F\,ST}}{2\pi}\left[\int_0^{\frac{\pi}{9}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{9}}^{\frac{22\pi}{108}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{\pi}{4}}^{\frac{\pi}{3}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \right.$$

$$\left.\int_{\frac{\pi}{2}}^{\frac{7\pi}{12}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{3\pi}{4}}^{\frac{91\pi}{108}}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\frac{8\pi}{9}}^{\pi}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t + \int_{\pi}^{2\pi}\left(i_L + \frac{i_{ac}}{2}\right) d\omega t\right] \quad ...(5.18)$$

Here P_{FST} &I_L is defined as the shoot-through state switching losses in PS-PWM and the average inductor current.

Simplifying this equation gives,

$$P_{POD-SI} = P_{F\,ST}\left[\frac{85}{108} I_L - \frac{0.5514 I_m}{2\pi}\right] \quad (5.19)$$

For type – II switch, shoot – through state switching losses occurs 0 to 2π. Switching losses in this switch type is given by (5.22). Simplifying this equation gives,

Table 5.1. Comparison of switching losses in different modulation methods

Method	S_1	S_2	S_3	S_4
Active state				
PS-PWM	100%	100%	100%	100%
PWAM	13.4%	13.4%	50%	50%
Proposed	33%	33%	33%	33%
Shoot – through state				
PS-PWM	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$
PWAM	$P_{F,ST}\left[\frac{5}{6}I_L - \frac{1}{4\pi}I_{m\,ss}\right]$(>16% Saving)		$P_{F,ST}\left[\frac{2}{3}I_L - \frac{\sqrt{3}}{4\pi}I_{m\,ss}\right]$(> 33% saving)	
Proposed	$P_{F\,ST}\left[\frac{85}{108}I_L - \frac{0.55}{2\pi}I_m\right]$(> 24% saving)		$P_{F\,ST}\left[\frac{41I_L}{108} - \frac{0.88I_m}{2\pi}\right]$ (>62% saving)	

$$P_{POD-SII} = P_{F\,ST}\left[\frac{41}{108}I_L - \frac{0.8825}{2\pi}I_m\right] \tag{5.20}$$

For the purpose of comparison, the switching losses obtained with this PWM are compared with other modulation methods are shown in Table 5.1.

5.5.2. Power loss in Un-Equal power distribution

5.5.2.1. Switching losses in active state

For type – I switch, active switching losses occur from 0 to $\frac{\pi}{9}$ and $\frac{8\pi}{9}$ to π whereas for type – II switch, active switching losses occur from π to $\pi + \frac{\pi}{9}$ and $\pi + \frac{8\pi}{9}$ to 2π.

For type – I switch, active state switching losses are given by,

$$P_{POD-AI} = \frac{P_{FAC}\,\mathrm{I_m}}{\pi}\left[\int_0^{\pi/9} \mathrm{Sin}\,\omega t d\omega t + \int_{8\pi/9}^{\pi} \mathrm{Sin}\,\omega t d\omega t\right] \tag{5.21}$$

$$P_{POD-AI} = \frac{P_{FAC}\,\mathrm{I_m}}{\pi}[0.1206] \tag{5.22}$$

Where $\frac{P_{F\,AC}\,I_m}{2\pi}$ is defined as the active state switching losses in PS-PWM and Im is peak of ac load current. $P_{LSPWM} = 12.06\%$ of switching losses in PS-PWM. For type – II

switch also, active state switching losses are given by,

$$P_{POD-AII} = \frac{P_{FAC}}{\pi}\left[\int_{0}^{\pi+\frac{\pi}{9}} \text{Sin}\,\omega t d\omega t + \int_{\pi+\frac{8\pi}{9}}^{\pi} \text{Sin}\,\omega t d\omega t\right] \tag{5.23}$$

$$P_{POD-AII} = \frac{P_{FAC}\,\text{I}_m}{\pi}[0.1206] \tag{5.24}$$

$P_{POD-AII} = 12.06\%$ of switching losses in PS-PWM.

During a fundamental frequency cycle, active state losses in all the switches remains the same.

5.5.2.2. Switching losses in shoot – through state

Switching losses for semiconductor switch during shoot – through state are given in Equation (5.19). For type – I switch, shoot – through state switching losses occur from 0 to $\frac{\pi}{9}$ and $\pi - \frac{\pi}{9}$ to 2π. For these switches, shoot – through state switching losses are given by,

$$P_{sw,\,ST} = \frac{1}{2\pi}\int_{0}^{2\pi} f_s\left(E_{ON} + E_{OFF}\right)\left(\frac{V_{dc}}{V_{ref}I_{ref}}\right)\left(i_L + \frac{i_{ac}}{2}\right)d\omega t \tag{5.25}$$

$$P_{POD-SI} = \frac{P_{FST}}{2\pi}\left[\left(\frac{11\pi}{9}\right)I_L - \left(\frac{0.9397}{2}\right)\text{I}_{m\,ss}\right] \tag{5.26}$$

Where $P_{F\,ST}$ is defined as the shoot-through state switching losses in PS-PWM and I_L is the average inductor current. For type – II switch, shoot – through state switching losses occur from 0 to π. For these switches, shoot – through state switching losses are given by,

$$P_{POD-SII} = \frac{P_{FST}}{2\pi}\left[\int_{0}^{\pi}\left(i_L - \frac{i_{ac}}{2}\right)d\omega t\right] \tag{5.27}$$

$$P_{POD-SII} = P_{FST}\left[\frac{I_L}{2} - \frac{\text{I}_{m\,ss}}{2\pi}\right] \tag{5.28}$$

Table 5.2. Comparison of switching losses in different modulations

Modulation	S_1	S_2	S_3	S_4
		Active state		
PS-PWM	100%	100%	100%	100%
PWAM	13.4%	13.4%	50%	50%
PODPS	12.06%	12.06%	12.06%	12.06%
		Shoot – through state		
PS-PWM	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$	$P_{F,ST}I_L$
PWAM	$P_{F,ST}\left[\frac{5}{6}I_L - \frac{1}{4\pi}I_{m\,ss}\right]$ (>16%)		$P_{F,ST}\left[\frac{2}{3}I_L - \frac{\sqrt{3}}{4\pi}I_{m\,ss}\right]$(> 33%)	
PODPS	$P_{F\,ST}\left[\frac{11}{18}I_L - \frac{0.94}{2\pi}I_m\right]$ (> 39%)		$P_{F\,ST}\left[\frac{I_L}{2} - \frac{I_{m\,ss}}{2\pi}\right]$(>50%)	

Table 5.2 summarizes the switching losses obtained and compares it with other modulation methods.

5.6. Detailed Simulation Results and Discussions

Parameters used for MATLAB/Simulink® simulation of the proposed modified carrier rotation scheme for qZS-CMI are given in the Table 5.3. Figure 5.6 shows the comparison of PODPS-PWM (unequal power) with the proposed three different carrier rotation schemes (to achieve equal power POSPS-PWM). Figure 5.6(a)–(d), represents the output voltage levels for the PODPS-PWM (unequal power), Method 1 (single carrier rotation), Method 2(double carrier rotation) and Method 3 for the three carrier

Table 5.3. Component specifications for qZSI-CMI

Component name	Experimental qZS-CMI	MATLAB R18a Simulink
Inductors $L_{n1} = L_{n2}$	Ferrite core 0.5 mH, 15A	Series RLC; branch type
Capacitors $C_{n1} = C_{n2}$	Electrolytic, 100uF, 400V	Series RLC; branch type
Diode D_{n1}	C3D10060G; 600V, 14A	Simscape, power electronic library
SIC-MOSFET S_{n1}-S_{n4}	FDP19N40; 1200V, 40 A	Simscape, power electronic library
frequency	50KHz	50KHz
RL-load	240V	1.5KW
Modulation Index	0.933	0.933
Control Board	Virtex-5 FPGA	Computer PC

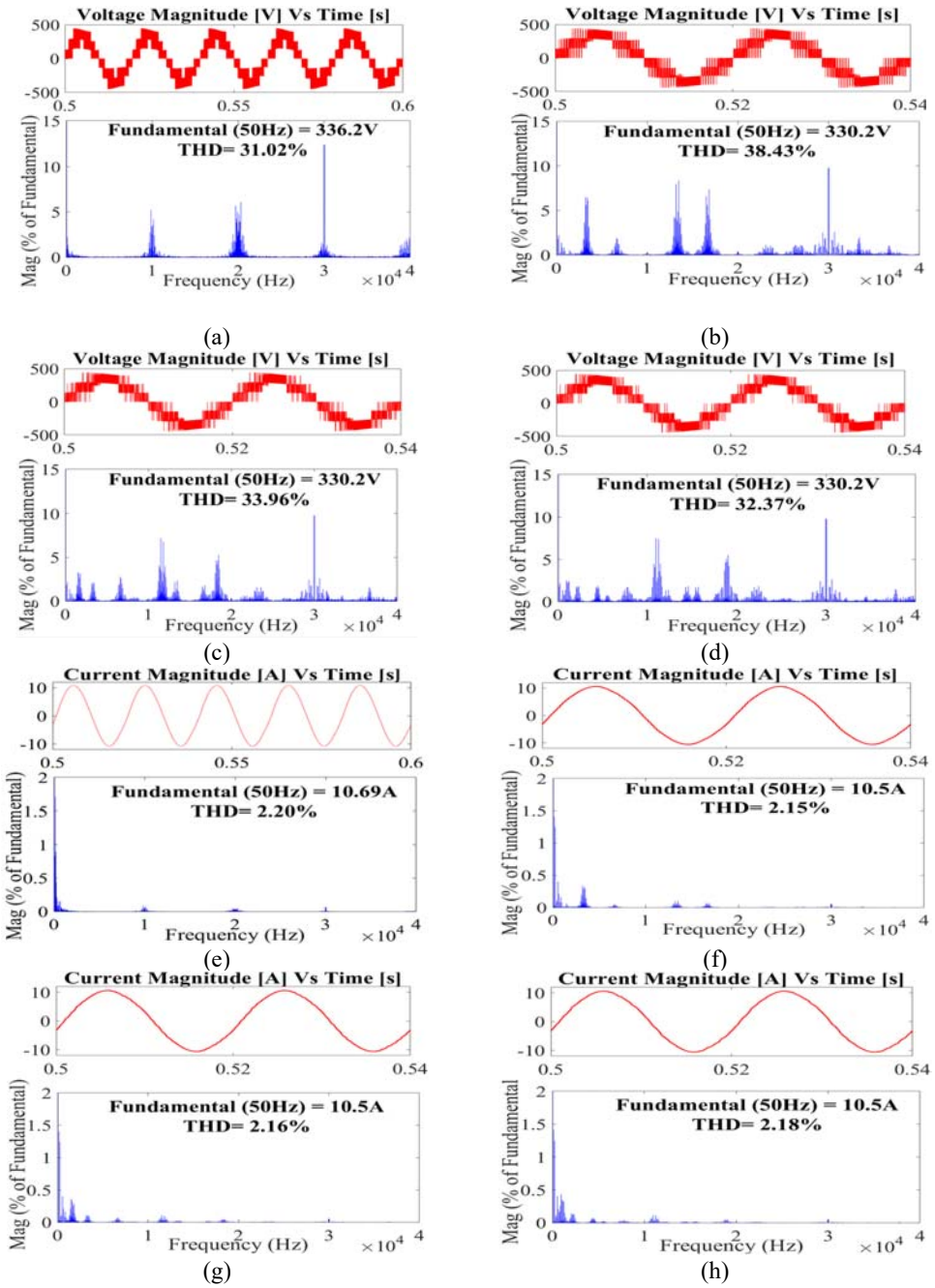


Figure 5.6. Harmonic spectra of load voltage with (a) PODPS-PWM , proposed method for (b) Single cycle (c) Double cycle and (d) Three cycle carrier rotations. Harmonic spectra of load current with (e) PODPS-PWM , proposed method for (f) Single cycle (g) Double cycle and (h) Three cycle carrier rotations.

rotation techniques respectively. It is observed that THD performance with method 3 is better than that of method 1 and method 2. The existence of lower frequency

components in the harmonic spectrum are eliminated by increasing the number of cycles used for rotation leading to better performance. As per the analysis, lower-order harmonics are formed due to the incomplete switching cycle observed during carrier rotation crossovers. Conclusively, the THD of method 3 is nearly the same as that of unequal power-based PODPS-PWM.

Figure 5.6(e)–(h) depicts the load current and its THD. The variation between the THD is very small for all the proposed methods and is very close to unequal power-based PODPS-PWM.

5.7. Experimental Verification of the proposed Modulation Scheme

For experimental validation of the modified PODPS-PWM, a 1.5kW prototype of seven-level qZS-CMI was developed. Figure 5.7 shows the photograph of the experimental setup. It consists of three qZSI modules (connected in cascaded structure), RL–load, DC-power supplies and Virtex-5 FPGA control board. Specifications of all the components are detailed in Table 5.3. A switching frequency of 50 kHz is selected and the qZS components are designed based on that. Each qZSI module is supplied with

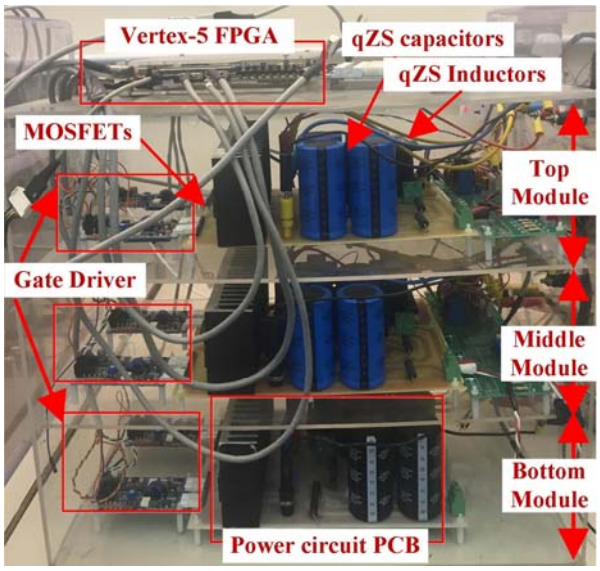


Figure 5.7. Shows the photograph of the experimental setup

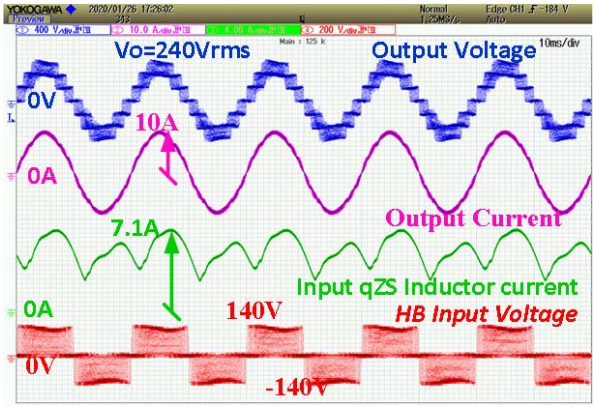
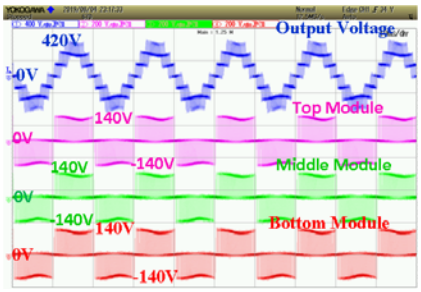


Figure 5.8. Seven-level qZS-CMI output voltage and output load current waveforms along input qZS inductor current and HB input voltage

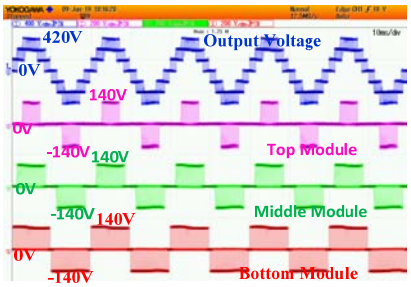
90V DC, which is boosted to 140V to form the DC-link for the H–Bridge MOSFETS at 20% shoot-through duty.

Figure 5.8, depicts the seven-level qZS-CMI output voltage and output load current waveforms along with input inductor current and the HB input voltage for the proposed three-cycle carrier rotation scheme. The output voltage is 240V RMS and the load current is 7.1A RMS at 0.95 power factor. It is observed that in the output voltage waveform, there are transitions between only two levels like 0V to 140V, 140V to 280V, and 280V to 420V for the positive half cycle. For the negative half cycle, the levels are 0V, -140V, -280V, and -420V. There is only one transition of voltage either from 0 to +140V or -140V. The current obtained is nearly sinusoidal thereby indicating low THD content.

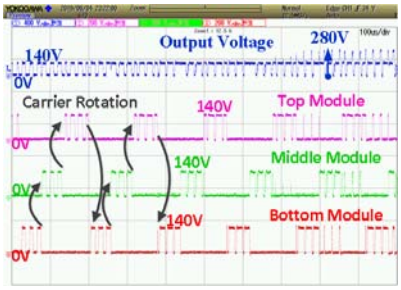
Figure 5.9(a) represents the seven-level qZS-CMI voltage for the equal power distribution case along with their individual qZSI modules' bridge output voltages. Figure 5.9(b) & Figure 5.9(c) represents zoomed waveforms of the output voltage for positive and negative cycles for a clear understanding of the switching patterns. All three modules are generating the same magnitude levels such as 140V-0V-(-140V) for



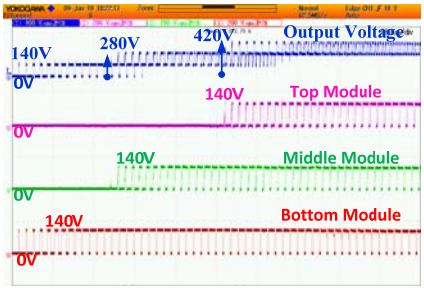
(a) Steady state waveforms



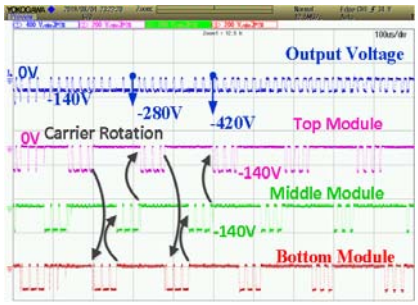
(a) Steady state waveforms



(b) zoomed portion for positive half cycle

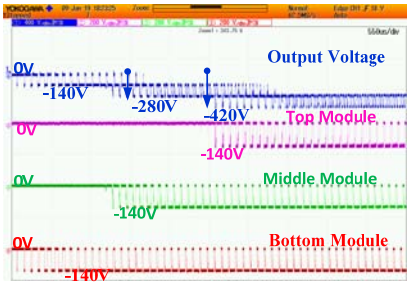


(b) zoomed portion for positive half cycle



(c) Zoomed portion for negative half cycle.

Figure 5.9. Equal Power distribution, The bottom, middle and top modules three level output voltages along with their cascaded seven level output voltage.



(c) Zoomed portion for negative half cycle.

Figure 5.10. Unequal Power Distribution, Voltage waveforms for output voltage (blue), module output voltages, top (pink), middle (green) and bottom (red).

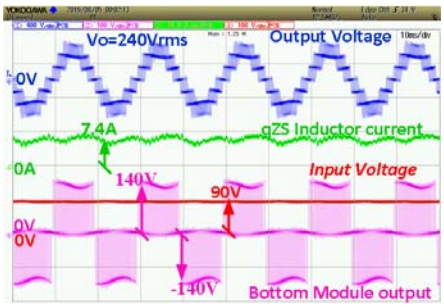
the entire modulation cycle. Thus, making the peak of the output voltage to be 420V. The average conduction time for all three modules are the same so the power-sharing among them is also the same. There are *2w* ripple in the passive components. These can be eliminated by advanced control algorithms which have been presented in the literature [69-72]. However, this chapter is trying to explore the application of the level-

shifted PWM technique into the qZS CMI

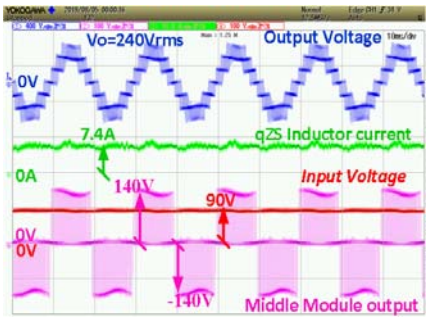
In Figure 5.9(b), the positive cycle is zoomed-in which the proposed carrier rotation is observed. The bottom module produces the first three output pulses of minimal width (after positive zero crossings) then the conduction is shifted to middle modules which produce the three pulses with increased width (in accordance to sinusoidal reference signal). Next, the conduction is shifted to top modules, which produce pulses of a further larger width. This rotation happens until the modulation reaches the peak of the first carrier. When the output voltage is in between the 140V and 280V, the conduction of the modules shifts after the sixth carrier cycles (due to two modules switching simultaneously). All three modules are switching for creating a 420V level of the output voltage. It can be observed that all three modules are generating 0V and 140V, but the ST states are phase-shifted by the 120^0 so there is no loss of active voltage levels. Similar rotation happens for the negative half cycle as shown in Figure 10(c). All the negative voltage levels can be observed along with three individual module voltages.

Figure 5.10(a) represents the seven-level qZS-CMI voltage for the unequal power distribution case along with their individual qZSI modules' bridge output voltages. In Figure 5.10(a)&(b) it is clear that the voltages are zero during a certain period of time during which the power delivered to load is also zero. This makes unequal power-sharing between the modules.

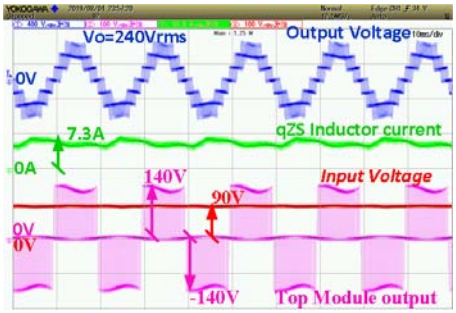
Figure 5.11 depicts the load voltage (seven-level), the output voltage of individual module, input voltage, and the input current drawn from theDC–power supply for the three modules. Figure 5.11(a) shows the bottom module output voltage of three levels of 140V, 0V and -140V. The average input current is 7.4A (for an applied input voltage of 90V from the DC – power supply. It is observed that the input current is continuous and never reaches zero value through its operation in all the operating modes. Even



(a) Bottom module



(b)Middle module

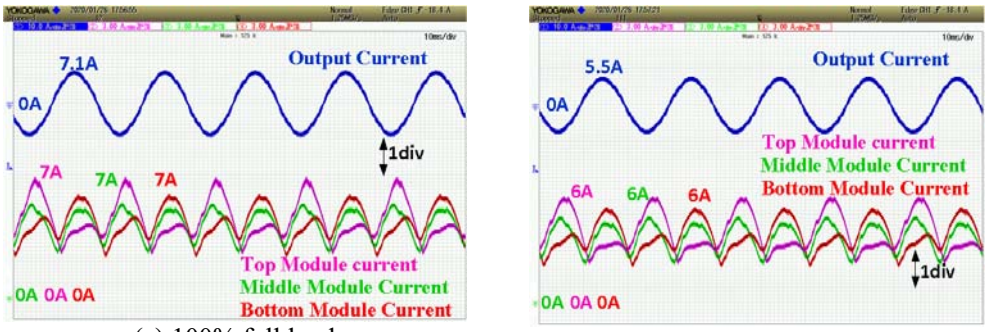


(c) Top module

Figure 5.11. Steady state operation of the individual modules while generating seven – level output voltage collectively.

though the level-shifted modulation technique is applied, the conduction of all the modules is continuous because of the carrier rotation.

Middle module output voltage levels are 140V, 0V, and -140V for an applied input voltage of 90V. Input average current of 7.4A is drawn from the power supply as shown in Figure 5.11(b). In all three modules, the current is never reaching zero and furthermore the current is almost constant having fewer ripples in it. It makes the size of the input capacitor to a small value. It should be noted that the switching frequency of 10 kHz is less compared to 50 kHz resulting in fewer switching's in the modules, at every zero crossings of the output voltage. This may lead to discontinuous current otherwise the capacitor size has to be increased. However, this can be eliminated by keeping the switching frequency 50kHz, and the current can be smoothened at higher switching frequency operation.



(a) 100% full load

(b)80% full load

(c)40% full load

Figure 5.12. Equal power-sharing between the modules during the different load currents.

Figure 5.11(c) shows the top module output voltage of three levels of 140V, 0V, and -140V for an input voltage of 90V. An average input current of 7.3A is drawn from the DC-power supply. It is observed that the input current is continuous.

The equal power-sharing between the modules has been presented in Figure 5.12. where the experiment is repeated for the different loading conditions. Input currents of all three modules are shown with respect to the load current are recorded. During 100% of the full load, all the module currents are equal and are equal to the rated output current of 7.5A as shown in Figure 5.12(a). In Figure 5.12(b), while operating at 80% of full load, the input currents are reducing linearly (5.7A to 6A) and giving an output current of 6A. Similarly, in Figure 5.12(c), during the 80% of full load, the inductor currents are almost identical (4.2A to 5A) to give a load current of 3.1A. Passive component discrepancies can lead to a small imbalance in current sharing during operating at small

load currents.

5.8. Summary

A novel modified PODPS-PWM technique for qZS-CMI is presented in this chapter. This chapter presents the relation between shoot-through duty and modulation indices of PS-PWM and PODPS-PWM. Shifting of shoot-through pulses by $180^0/n$ results in better *dV/dt* performance of qZS-CMI. The proposed modulation technique (for qZS-CMI) combines the advantages of LS-PWM and PS-PWM, resulting in high-quality output voltages and harmonic free input currents drawn from the PV panels. Simultaneously, it overcomes the drawbacks of uneven power distribution among the operating modules. The switching signals of MOSFETS of all modules represent equal utilization of them irrespective of their position in the system. To validate this concept, a detailed switching loss analysis and its comparison with other modulation methods are presented. From this analysis and results, it can be concluded that the proposed PODPS-PWM provides nearly the same higher power yielding capability as of PS-PWM with higher efficiency (due to lower switching losses). Detailed simulation and experimental results are presented which validates the benefits of the proposed PODPS-PWM.

CHAPTER 6: A 4-MW CASCADED MULTILEVEL INVERTER FOR SOLAR PV POWER CONVERSION SYSTEM

6.1. Introduction,

Over the years, a broad range of multilevel inverter (MLI) topologies have been established for medium-voltage applications, particularly in the last decade, to conform to the needs and follow the requirements of each niche. Using advanced medium-power semiconductor technologies, MLIs will cope with high voltage/current [82, 83]-[84]. The single-stage power converter topology that employs a capacitor-inductor network and has voltage-boost and voltage-buck capabilities [85-87]. In order to raise the input voltage and control the DC connection voltage for the inverter, the qZS-network uses shoot-though states. During the active states of the inverter, the peak DC connection voltage occurs around the load terminals. Then, between zero and peak DC connection voltage, the DC contact voltage is pulsating in nature. In addition, for grid-tie PV structures, a qZS-CHB topology was suggested in [65, 87-89]. This mixed topology is described by good-quality multilevel output voltage with lower THD, independent DC-link voltage compensation with a single-stage power conversion special voltage step-up/down feature, and independent power distribution control with high reliability. [89]. It should be remembered that the exact regulation of the peak voltage of the DC-link is very important for controlling the sum of total power supplied to the grid.

This chapter provides an effective control technique for integrating a qZS-CHB inverter PV device to the three-phase grid. Unity power factor and low THD current are delivered to the grid in the control structure. In addition, a dual-loop DC-link peak voltage regulation controls the volume of total power supplied to the grid [90] employed in every qZS-CHB module to balance the DC-link voltages (by controlling the shoot-

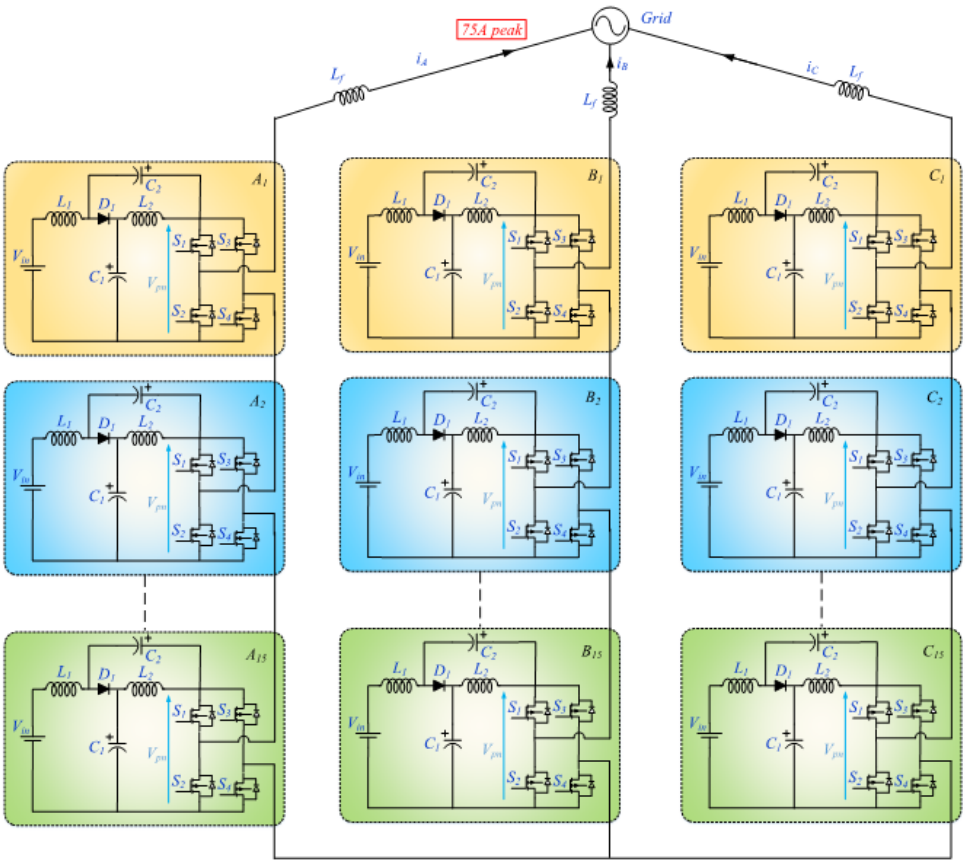


Figure 6.1. Proposed 4MW qZS-CMI, 16 modules per phase.

through ratio). Used to align the DC-link voltages in any qZS-CHB module (by controlling the shoot-through ratio). This chapter explains the full concept creation. In order to verify the proposed methods, simulation results focused on a 4 MW 3-phase 16-cell (48 cells in total) prototype is carried out.

6.2. Modulation and Mathematical Analysis

Figure 6.1 demonstrates the proposed qZS based PCS. By filtering inductors, the shown device consists of 48 grid-tie CHB inverters, where each cell is linked to a qZS network. Two inductors, two capacitors and one diode make up this network. To interface the PV output voltage with the inverter input with boost capabilities, this switchless network is used. The qZS-CHB inverter output voltage is a multilevel form (33-level

output voltage per phase) resulting from the sum of the output voltages of the sixteen modules.

6.3. Control strategy

DC-link peak voltage management for all qZS-CHB modules and power injection to the grid with unity power factor and low harmonic distortion are the control goals of the proposed PCS. To accomplish these aims, the full synoptic regulation seen in Figure 6.2 is suggested. For each qZS-CHB module, the DC-link peak voltage is controlled via the shoot-through duty ratio regulation. A dual loop principle is employed, as seen in Figure 6.2. To boost the dynamic response, a proportional (P) controller is used in the inductor current loop [86], For each qZS module, the transfer functions $G_{vpn}(s)$ (giving the DC-link peak voltage from the shoot-through duty ratio) and $G_{iL}(s)$ (giving the L1 inductor current from the shoot-through duty ratio) may be measured. Thus, the modified dual loop block diagram as seen in Figure 6.3. The output current is controlled to ensure power injection into the grid with a unit power factor and a low harmonic distortion. The block diagram of the planned existing output controller is seen in Figure 6.4. The grid-tie device has the following dynamics at the output of the qZS-CHB

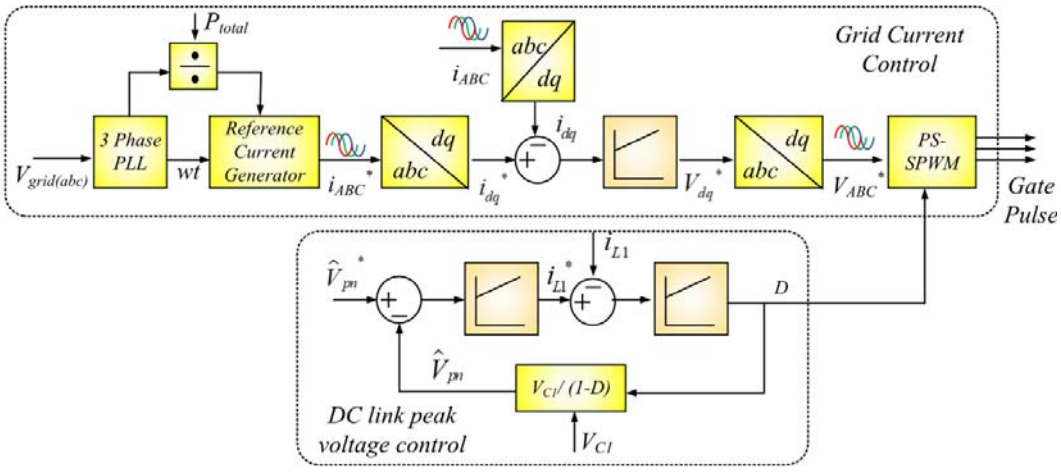


Figure 6.2. qZS CMI PV power control system algorithm

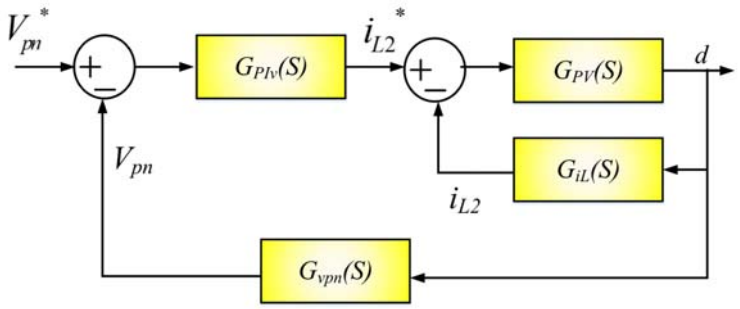


Figure 6.3. Control algorithm for the DC-link control

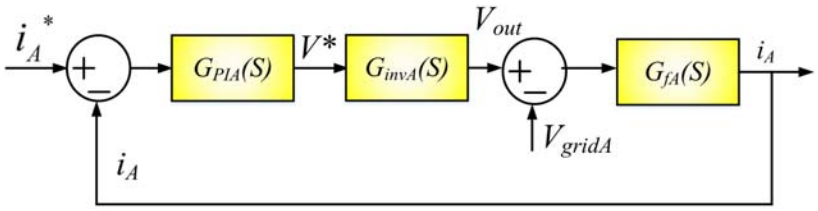


Figure 6.4. Block diagram for the grid current control.

inverter for phase A (imitation for phases B and C),

$$V_{AN}(t) = V_{gridA}(t) + L_f \frac{di_A(t)}{dt} + r_f i_A(t) \tag{6.1}$$

where V_{AN} is the phase output voltage, V_{gridA} is the phase grid voltage, i_A is the phase output current, L_f is the filter inductance, and r_f is its parasitic resistance. Thus, the output current transfer function $G_{fA}(s)$ can be given by,

$$G_{fA}(s) = \frac{I_A(s)}{V_{AN}(s) - V_{gridA}(s)} = \frac{1}{L_f s + r_f} \tag{6.2}$$

At the qZS network output, all the DC-link peak voltages are regulated around the same reference value. Thus, it is assumed that all qZS-CHB inverter modules have the same transfer function given by,

$$G_{invA}(s) = n * \widehat{V} pn \tag{6.3}$$

Then, the combined inverter-filter transfer function is obtained by,

$$G_{sysA}(s) = G_{invA}(s).G_{fA}(s) = \frac{n\hat{V}_{pn}}{L_f s + r_f} \tag{6.4}$$

Besides, a PI current controller is applied on the actual output current to guarantee a suitable tracking of the desired reference with unity power factor and low harmonic distortions. The PI transfer function is given by,

$$G_{PIA}(s) = k_{pA} + \frac{k_{iA}}{s} \tag{6.5}$$

Then, the compensated transfer function, after the application of the PI current controller, is calculated by,

$$G_{compA}(s) = G_{PIA}(s).G_{sysA}(s) = \frac{n(k_p s + k_i)\hat{V}_{pn}}{L_f s^2 + r_f s} \tag{6.6}$$

Therefore, the closed-loop transfer function of the output current regulation can be given by,

$$G_{closeA}(s) = \frac{G_{PIA}(s).G_{sysA}(s)}{1 + G_{PIA}(s).G_{sysA}(s)} = \frac{n(k_p s + k_i)\hat{V}_{pn}}{L_f s^2 + (r_f + nk_p\hat{V}_{pn})s + nk_i\hat{V}_{pn}} \tag{6.7}$$

6.4. Simulation Results

Simulations utilizing MATLAB/SIMULINK were carried out to test the proposed design, and findings are provided to demonstrate the efficacy of the system in achieving grid-tie current injection, low current THD, and balancing the DC-link voltage for all qZS-CHB inverter modules. In Table 6.1, the total device parameters are discussed.

In the case studied (4 MW output power system), the peak value of the qZS-CHB reference grid current is set to 210 A and the DC-link reference voltage V_{pn}* is set to 1530 V (B=1.7). In order to improve the conversion mode, the qZS network boosts the input voltage V_{in} (850 V) to the appropriate reference value V_{pn}* by varying the output

Table 6.1. Simulation Parameters

Parameters	Value
Total output power (P_{total})	4MW
AC grid RMS line-to-line voltage (V_{LLgrid})	11kV
qZS inductances (L_1, L_2)	2.5mH
qZS capacitances (C_1, C_2)	2mF
Filtering inductance (L)	1mH
AC load frequency (f)	50Hz
Switching frequency of each module	10kHz
No. of modules	16

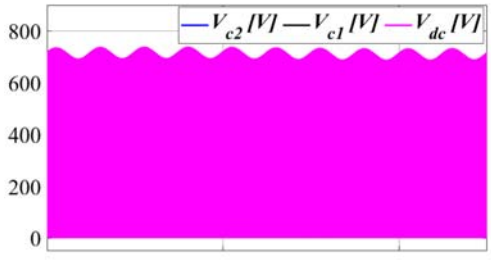


Figure 6.5. qZS DC-link voltages

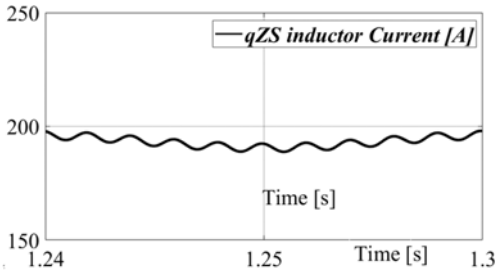


Figure 6.6. qZS inductor currents

by value D (regulating the output value as seen in Figure 6.3.

Figure 6.5 shows the simulation results of the regulated DC-link voltage and capacitor voltages. It can be noted that the DC-link voltage is properly regulated around the reference value (71530 V), Vc1 and Vc2 are controlled around the reference values (Vc1 *=1050 V, Vc2*=425 V) given by (6.11).

$$\begin{cases} V_{c1}^{*} = V_{in}\dfrac{1-D}{1-2D} \\ V_{c2}^{*} = v_{pn}^{*} - V_{c1}^{*} \end{cases} \tag{6.11}$$

Figure 6.5 demonstrates that the inductor currents of qZS are held in continuous mode to reduce the tightness of the input. Figure 6.6 also signifies a zoom of Figure 6.5 and Figure 6.5, displaying the shoot-through state progression of the qZS variables. The

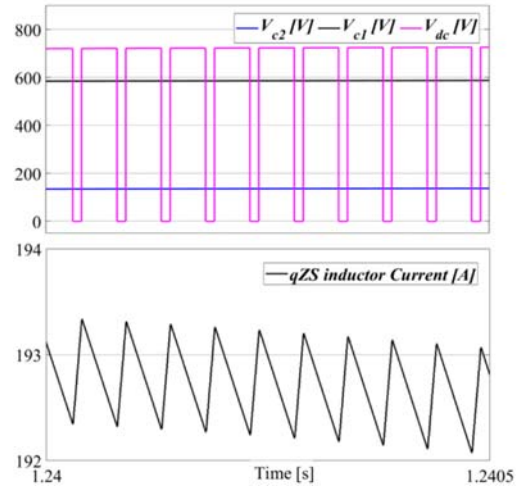


Figure 6.7. qZS inductor currents and DC-link voltages

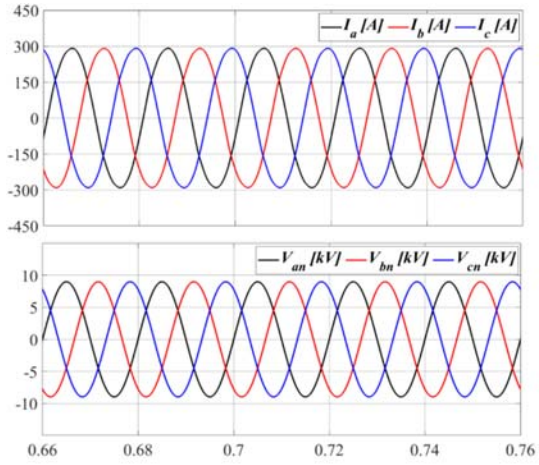


Figure 6.8. Three phase grid currents and voltages

upper part indicates that the DC-link voltage is correctly controlled around the reference value (1530 V), while the lower part shows that during the shoot-through and decrease during the non-shoot-through condition, the qZS inductor currents increase and decrease and are always retained in continuous mode.

In Figure 6.8, the three-phase grid currents are depicted with respect to their references with very suitable tracking quality. The current THD is given by Figure 6.9. The 3-phase 33-level output voltages are shown in Figure 6.10. Finally, Figure 6.11 shows the

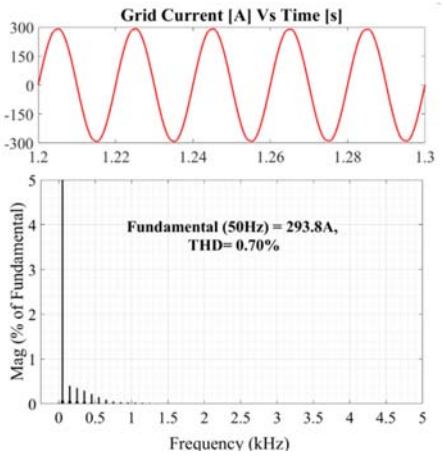


Figure 6.9. Grid current THD

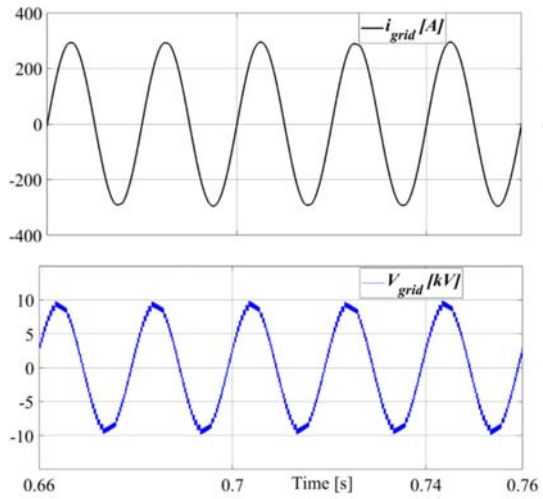


Figure 6.10. 33 level qZS CMI output voltage

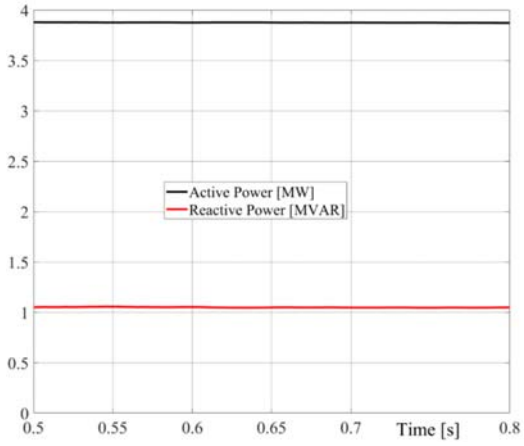


Figure 6.11. Total output active and reactive power

measured total output power as well as the grid currents and the line-to-line output voltages maintained in the continuous mode.

6.5. Summary

This chapter introduces a 4 MW grid-connected PV Power Conditioning Device by integrating qZS networks into CHB inverters. The proposed PCS consists of a 3-phase, 48-cell CHB inverter with a qZS network feeding each module. Using an improved

phase-shifted pulse width modulation technique, which inserts shoot-through states into the traditional zero states to regulate the qZS-CHB module, a multilevel output voltage waveform was developed. To achieve grid-tie current injection, low Total Harmonic Distortion (THD) current, unity power factor, and DC-link voltage balance for all qZS-CHB inverter modules, successful control schemes were suggested. The suggested multilevel PV energy conversion method and its control concepts were confirmed by simulation performance.

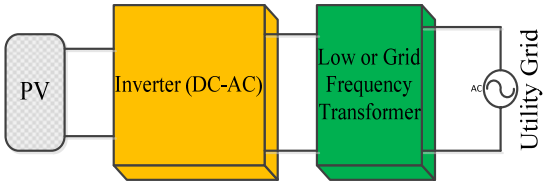
CHAPTER 7: NOVEL ISOLATED QUASI Z-SOURCE INVERTER FOR TRANSFORMERLESS GRID-CONNECTED SOLAR PV APPLICATIONS

7.1. Introduction,

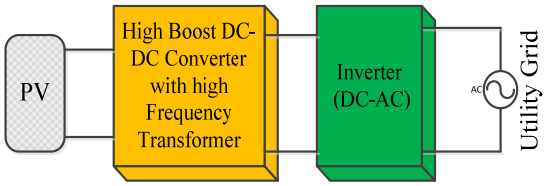
As the isolation is one of the major concerns of the grid connected systems. It is required because the of the low voltage and high voltage devices present in the PV system. Furthermore, PV panels has the insulation of only 1.5kV which are hindrance for the high voltage applications. For the low voltage application at higher frequencies the body capacitors formed between the panels and ground creates the common mode voltage which intern generates the ground current. So in the grid connected systems one has to tackle/address this issue.

In general grid-connected solar PV inverter topologies shown in Figure 7.1 (a)-(b), use some form of transformers to connect to the grid to provide galvanic isolation, eliminating dc current injection and eliminating or reducing common-mode leakage current [104]. As shown in Figure 7.1(a), the transformer used is of line frequency rating, then the size is bulky, cost of the overall system is high and the efficiency is reduced [105, 106]. Hence to reduce the volume and cost, the high-frequency transformer is used on the dc side.

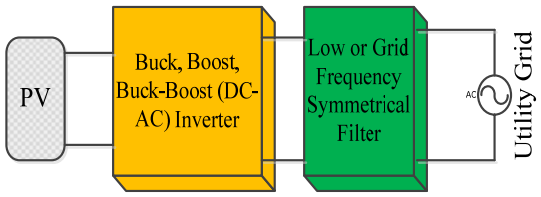
As shown in Figure 7.1(b) while eliminating the use of line frequency (50 Hz or 60 Hz) transformer. This solution offers the advantage of reduced common-mode leakage current. The use of a high-frequency transformer still lowers the overall efficiency of the system. Thus, it is important to develop a transformerless solution thereby



(a) Isolated topology using high-frequency transformer



(b) Isolated topology using low frequency transformer



(c) Transformerless topology

Figure 7.1. Connection topologies of PV systems

completely eliminating the use of a transformer [107], shown in Figure 7.1(c). This is a good solution from efficiency, cost, and overall size point of view, but still, safety is a concern in such cases due to high leakage current in isolated PV modules. Without a transformer, a direct leakage current path is established between the PV and the grid, this is also known as the non-existence of the galvanic isolation [108, 109].

Moreover, the varying common-mode voltage enlarges the leakage current that can increase injected current ripple, reduce overall efficiency, and enlarge electromagnetic interference. Several inverter topologies are available in the literature such as H5 [110], H6 [111], and HERIC [112] that eliminate the leakage current by clamping the common-mode voltages [108, 113]. In addition to the dc-ac stage, a dc-dc converter is also employed in a solar PV system. The role of the dc-dc converter is to operate the solar PV at their maximum power point continuously delivering maximum available

power. The other function of the dc-dc converter is to boost the available dc voltage. Thus, traditionally two dc-ac stages.

However, two-stage conversion leads to extra components and a double frequency component is formed at the capacitor of the HB. This increases the size of the capacitor and in overall the efficiency of the system reduces. The proposed solution is based on a single-stage conversion where boosting and conversion from dc to ac takes place simultaneously. This is achieved by quasi impedance source inverter that has LC in the form of letter Z, and a diode at the source side. Several variations of impedance source inverters are available in the literature [85, 114]. Here qZSI is considered since the source current in this topology is continuous when compared to standard Z-source where it is discontinuous [85, 115]. This chapter further proposes a modified PWM scheme to reduce the common-mode voltage and ground current in a single-phase qZSI topology that can be used as transformerless solution.

7.2. QZSI for Transformerless Grid Integration

The proposed non-isolated qZSI topology is shown in Figure 7.2. Two additional switches Q5 and Q6 are used along with diodes D5 and D6. For filtering purposes, two

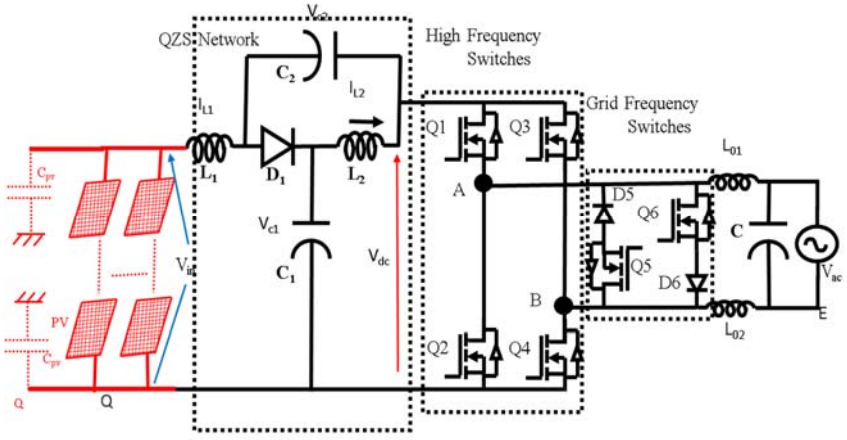
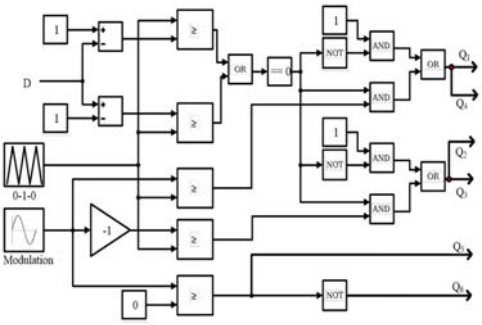


Figure 7.2 Proposed QZSI with additional switches.

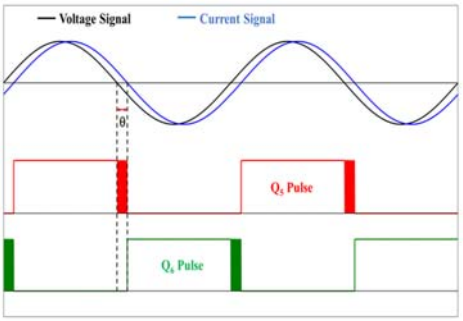
small inductors L_{01} and L_{02} are connected between the inverter and the grid. The additional switches Q5 and Q6 commutate at the grid frequency. The additional switches provide decoupling between the PV array and the grid and maintain the fixed potential of half of the boosted voltage at terminals A and B (Figure 7.2). It is further to be noted that the inclusion of the extra switches contributes to very low (negligible) switching losses since the switches operate at grid frequency. HB switches are operating at switching frequency but the additional switches are operating at the grid (50Hz) frequency. Furthermore, the conduction losses in the extra switches are extremely small because they conduct only in the freewheeling mode or during the shoot-through and zero states (non-active states). During the active states, one of the additional switches is ON but the diode blocks the conduction, hence no current flow in the branch. The detailed explanation is presented in sections 7-3 of the chapter.

7.3. PWM Generation and Operating Modes of QZSI

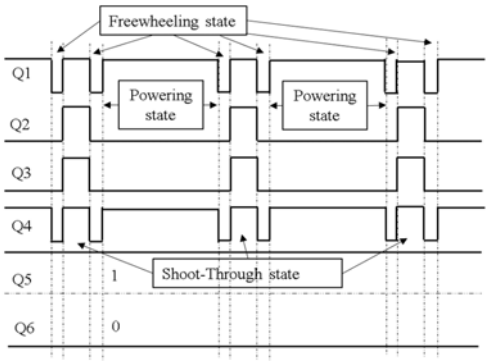
A novel PWM method is developed and a modified switching signal generation is proposed for the control of qZSI as illustrated in Figure 7.3. Three distinct switching states are formed namely; powering, freewheeling (FW) and shoot-through (ST). When the PV source is delivering power to the grid, it is in 'Powering' mode. When the inverter legs are shorted to boost the dc source voltage, such switching is called ST state. During the ST period, the inverter and grid are decoupled and circulating current flows through the additional switches at the grid side and the capacitors at the source site. After every ST state and powering state, an FW state is required [11, 116-119] for the charge balance of the impedance network inductors and grid-connected inductors.



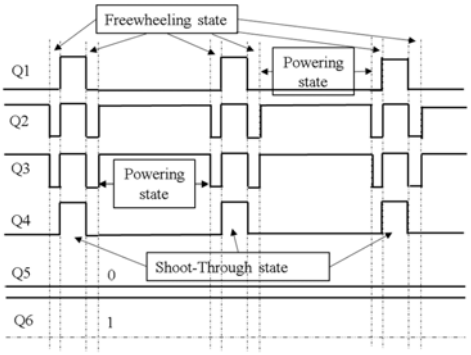
(a) Proposed modified modulation scheme for operation at unity power factor



(b) Proposed modified modulation scheme for operation at different power factors



(c) Positive half cycle of PWM logic



(d) Negative half cycle of PWM logic

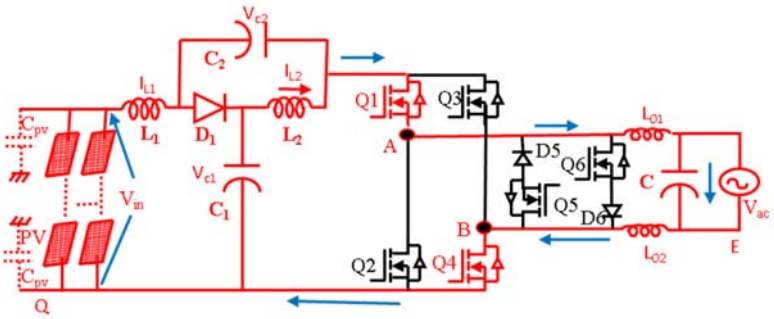
Figure 7.3. Proposed Modified PWM signals for the transformer-less grid-connected QZSI topology

To improve the system efficiency and reduce the common-mode voltage, it is important that the FW current of the grid should not flow through the antiparallel diodes of the power switches of the inverter legs. Hence the extra switches are connected in the grid side to provide the freewheeling path to the grid current in every switching cycle. The power diodes *(D5, D6)* used in the proposed topology have much better switching characteristics than the antiparallel diodes of the main power switches. The switch *Q5* conducts during the positive half grid cycle and off for the negative half grid cycle. The operation of *Q6* is complimentary of *Q5.* Hence the additional switches *Q5* and *Q6* are turned on and off once in a grid cycle and hence compared to the *Q1-Q4* the switching

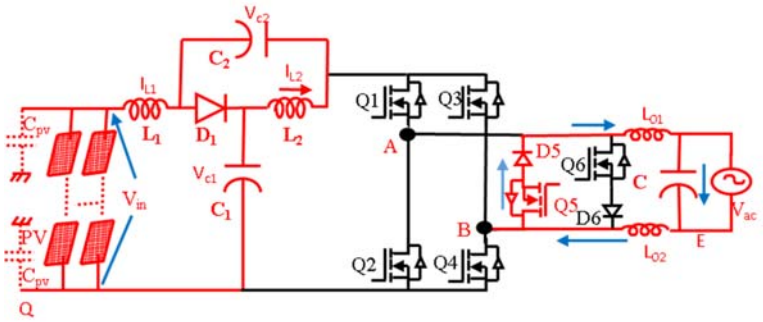
losses are negligible. The proposed modified modulation switching cycle pattern is given in Figure 7.3 (a). In Figure 3 (a), the *D* indicates the shoot-through duty generated from the quazi network controller. The main purpose of this modification in the switching pattern is to disconnect the PV panel from the grid during the non-powering (shoot-through and freewheel) period. Hence the potentials at inverter output terminals A and B will not vary and remain fixed at $V_{dc}/2$ (explained in section IV).

For operation at lagging or leading reactive power, there are four regions in the waveform depending upon the sign of the voltage and current signal. When the signs of both voltage and current are the same, a continuous switching pulse must be generated as shown in Figure 7.3(b). However, when the sign of voltage and current signal are not the same, application of continuous pulse leads to shorting of qZSI resulting in a dead short circuit of the utility grid. To overcome this, the switching pulse applied for *Q5* in the instance shown (when current is positive, and voltage is negative indicated by region θ), must be obtained by performing logical NOT operation on the *Q1* and *Q4* pulses (powering mode pulses). This results in non – conduction of *Q5* during powering mode and conduction during free–wheeling mode thereby preventing any shorting of qZSI. Similarly, pulses for *Q6* will be generated by negating *Q2* and *Q3* pulses (powering mode pulses) for positive voltage and the negative current region as shown in Figure 7.2(b).

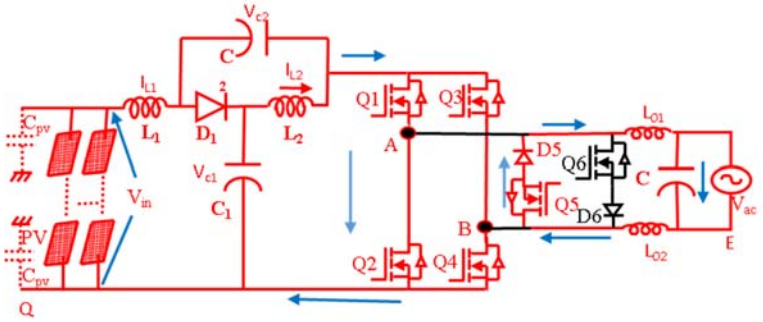
The operating modes of the qZSI are illustrated in Figure 7.4. As shown in Figure 7.4 (b), in the positive half grid cycle, the *Q5* remains on, and *Q1* and *Q4* switch synchronously at high-frequency. During powering mode *Q1*, *Q4* and *Q5* are on and *D5* is reverse biased. In Figure 7.4(c) (freewheeling period) *Q1 – Q4* is off and *Q5* is on and the freewheeling current will flow through D5 and Q5. During this period, the grid is isolated from the PV panel hence no reactive power flows. As shown in Figure



(a) Powering mode



(b) Freewheeling mode



(c) Shoot-through mode

Figure 7.4. All six operating modes of proposed Quasi Z-Source Inverter with additional switches.

7.4(c), when *Q1* and *Q2* or *Q3* and *Q4* are on (shoot-through state), the freewheeling current goes through *Q5* and *D5*. During shoot-through state the input side current charges the qZS network and boosts the voltage. Similarly, in the negative half cycle, *Q2 and Q3* are switched at high-frequency and *Q6* remains on. When *Q2, Q3, and Q6*

are on, negative grid current will be injected into the grid is called negative half cycle powering mode. When *Q2* and *Q3* are off and *Q6* is on, the freewheeling current will flow through D6 and Q6. Here the grid is isolated from the PV panel and therefore, no reactive power flows. When *Q1-Q2* or *Q3- Q4* are on (shoot-through state), the freewheeling current flows through *Q6* and *D6* during the negative half cycle.

7.4. Common-mode Voltage Analysis

In general stray capacitance (CPV) is formed between the PV panel and ground that provide electrical connection for the ground current, also known as common-mode current, as shown in Figure 7.5 [120-123]. Typically, the common-mode current is a function of the common-mode voltage. This current can be minimized or suppressed by lowering the frequency of the potential difference between the grid ground and the panel Negative terminal. Furthermore, the ground current depends on the stray capacitances of switches and the filter inductors. To investigate common-mode current flow in the proposed qZSI, a complete mathematical model is developed. The switching states of the proposed qZSI with a common-mode leakage loop are shown in Figure 7.6. The voltage V_{EQ} between the ground of grid (point E) and PV array frame (point N=Q) varies with inverter operating modes. So V_{EQ} is calcu lated according to six

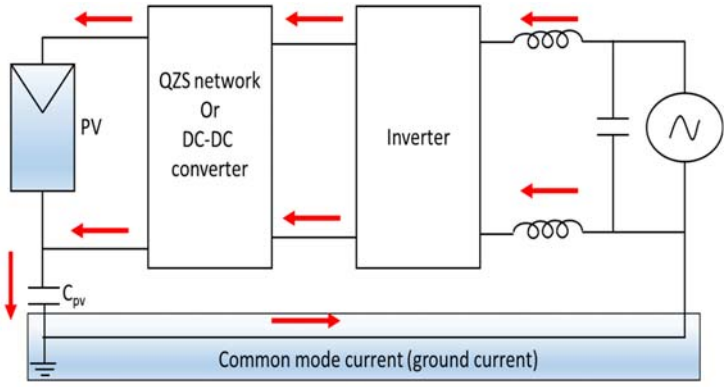


Figure 7.5. Common-mode current flow in PV system.

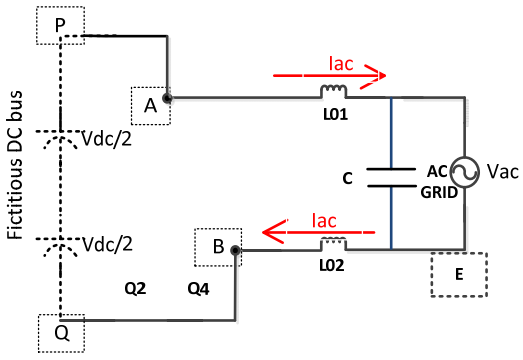
different operating modes, shown in Figure 7.6. Assuming, identical switches *Q1 to Q4* makes the output stray capacitance of the switches be the same. When freewheeling through *D5 and D6*, the voltage of the device will be clamped at half of the boosted DC bus voltage *(V_{dc})*. Hence as shown in Figure 7.6(a) in the positive half cycle, when *Q1* and *Q4* are on, V_{EQ} is,

$$V_E - V_Q = V_{dc} - V_{ac} - I_{ac} * j * \omega_{sw} * L_{01} \tag{7.1}$$

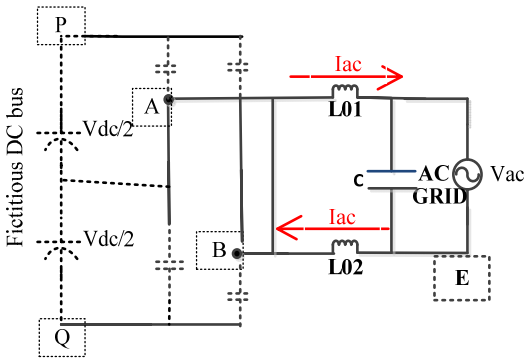
$$V_E - V_Q = I_{ac} * j * \omega_{sw} * L_{02} \tag{7.2a}$$

$$V_{EQ} = \frac{(V_{dc} - V_{ac}) * L_{02}}{L_{01} + L_{02}} \tag{7.2b}$$

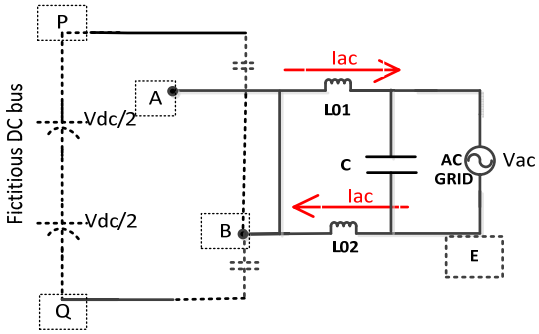
As shown in Figure 7.6(b), in the positive half grid cycle, when *Q1 - Q4* are off during freewheeling state, and freewheeling current goes through *Q5* and *D5, V_{EQ}* is,



(a) Powering mode in positive half cycle



(b) Freewheeling mode in positive half cycle



(c) Shoot-through state in positive half cycle

Figure 7.6. Common-mode current paths in positive half cycle.

$$V_E - V_Q = \frac{V_{dc}}{2} - V_{ac} - I_{ac} * j * \omega_{sw} * L_{01} \tag{7.3}$$

$$V_E - V_Q = \frac{V_{dc}}{2} + I_{ac} * j * \omega_{sw} * L_{02} \tag{7.4a}$$

$$V_{EQ} = \frac{V_{dc}}{2} + \frac{(-V_{ac}) * L_{02}}{L_{01} + L_{02}} \tag{7.4b}$$

As shown in Figure 7.6(c), in the positive half grid cycle, when *Q1* and *Q2* are on (shoot-through state) and freewheeling current flows through *Q5* and *D5,* V_{EQ} is,

$$V_E - V_Q = \frac{V_{dc}}{2} - V_{ac} - I_{ac} * j * \omega_{sw} * L_{02} \tag{7.5}$$

$$V_E - V_Q = \frac{V_{dc}}{2} + I_{ac} * j * \omega_{sw} * L_{01} \tag{7.6a}$$

$$V_{EQ} = \frac{V_{dc}}{2} + \frac{(-V_{ac}) * L_{01}}{L_{01} + L_{02}} \tag{7.6b}$$

In powering, shoot-through and freewheeling modes during the negative half grid cycle, common-mode voltage equations are, respectively,

$$V_{EQ} = \frac{(V_{dc} - V_{ac}) * L_{01}}{L_{01} + L_{02}} \tag{7.7}$$

$$V_{EQ} = \frac{V_{dc}}{2} + \frac{(-V_{ac}) * L_{02}}{L_{01} + L_{02}} \tag{7.8}$$

$$V_{EQ} = \frac{V_{dc}}{2} + \frac{(-V_{ac}) * L_{01}}{L_{01} + L_{02}} \tag{7.9}$$

In the proposed qZSI, L_{01} and L_{02} should be the same. Hence by substituting $L_{01} = L_{02}$ in all equations (7.2b), (7.4b), (7.6b), (7.7), (7.8) & (7.9) one gets the following,

$$V_{EQ} = \frac{(V_{dc} - V_{ac})}{2} \tag{7.10}$$

So V_{EQ} will be the same in all six different operating modes.

7.5. Losses in The Semiconductor Devices

The proposed converter has the traditional HB module losses, additional shoot-through

losses, freewheeling losses in the auxiliary switches, and the qZS diode loss.

7.5.1. HB module loss

It consists of the conduction and switching losses during both powering and shoot-through modes. The conduction losses during powering and shoot-through modes,

$$P_{con\_S(1-4)} = \frac{2}{\pi}\int_{0}^{\pi}\left[R_{DS(on)} * i_{ac}^2 * \frac{1+m}{2}\right] d\omega t + \left[R_{DS(on)} * i_{L1}^2 * D\right] * 4 \quad (7.11)$$

Where $R_{DS(on)}$ is the MOSFET's drain-source ON resistance. i_{ac} is load RMS current. The switching loss during powering mode (since there is no conduction of antiparallel diodes so no diode reverses recovery loss),

$$P_{sw\_S(1-4)} = \frac{2}{\pi}\int_{0}^{\pi}\left[V_{dc} * i_{ac} * \frac{tri + tfu}{2} * f_s\right] d\omega t \quad (7.12)$$

Where tri & tfi are the current rise and fall times respectively, tru & tfu are the voltage rise and fall times respectively, f_s is the switching frequency and V_{dc} the input of the HB module. The switching loss during shoot-through mode,

$$P_{sw\_S(1-4)} = 2 * V_{dc} * 2i_{L1} * \frac{tri + tfu}{2} * f_s \; + V_{dc} * \left(2i_{L1} * \frac{tru + tfi}{2} * f_s\right) .. (7.13)$$

7.5.2. Auxiliary switch loss

MOSFET's (Q5 and Q6) are switching at grid frequency, hence it has negligible switching losses and conduction loss during freewheeling and shoot-through states.

$$P_{con\_S(5-6)} = \frac{2}{\pi}\int_{0}^{\pi} u_d * i_{ac}\left(1 - \frac{1+m}{2}\right) d\omega t \quad (7.14)$$

Where u_d is ON state zero current voltage. However, the diodes (D5 and D6) will contribute to conduction and switching losses

$$P_{con+sw\_D(5-6)} = \frac{2}{\pi}\int_{0}^{\pi} R_D * i_a^2\left(1 - \frac{1+m}{2}\right) d\omega t + 4Q_{RR} * V_{dc} * f_{grid} \quad (7.15)$$

Table 7.1. Simulation parameters

Input DC voltage	100V
Output grid voltage	120Vac
Grid frequency	50Hz
Output power	500W
Switching frequency	10kHz
$L_1 = L_2$	2mH
$C_1 = C_2$	2000uF
$L_{01} = L_{02}$	2mH

Where Q_{RR} is reverse recovery charge and R_D ON-state resistance of the diode (D5 & D6). grid is grid fundamental frequency. Auxiliary switches conduction losses are only presented in the mathematical equations. The two switches S5 and S6 switching frequency is also mentioned in the mathematical formulae 8. 21 and 7.15, because it is also switching at grid frequency. If all the values are substituted in equation 7.15, the result will be very low and that can be neglected.

7.5.3. qZS network diode loss

It contains the conduction and reverses recovery loss. The conduction loss of the quasi network diode is

$$P_{con_{D1}} = \frac{2}{\pi}\int_0^{\pi}[u_{d1} * 2i_{L1} + R_{D1} * (2i_{L1})^2] * (1 - D - m)d\omega t \; + \frac{2}{\pi}\int_0^{\pi}[u_{d1} * (2i_{L1} - i_{ac}) + R_{D1} * (2i_{L1} - i_{ac})^2] * md\omega t \quad (7.16)$$

Where u_{d1} & R_{D1} ON state zero current voltage and the on-resistance of the qZS network diode.

7.6. Experimental Results

An experimental prototype of 500 Watts is built in the laboratory as shown in Figure 7.7. The H-bridge inverter is built using Semikron SKM100GB12T4. The qZS network is built using inductor $L_1 = L_2$ = 1mH, C=470uF. The control code is written in a system

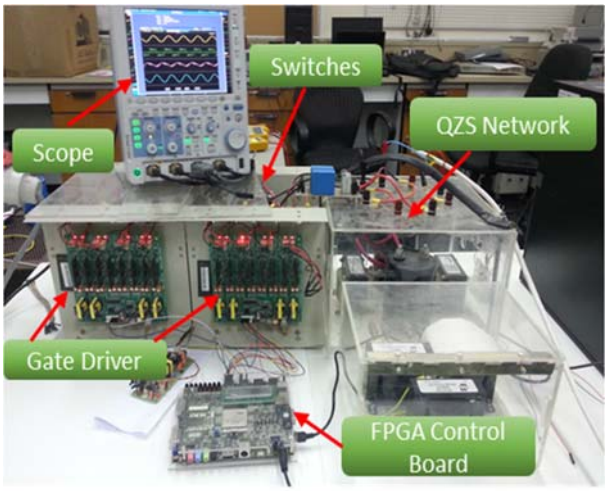


Figure 7.7. Hardware setup.

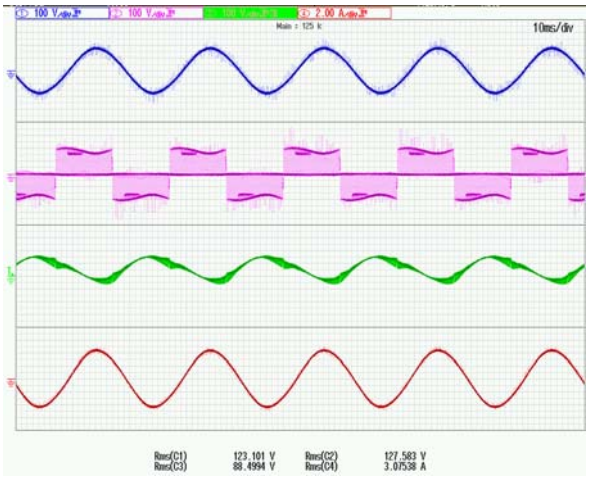


Figure 7.8. Experimental results of proposed qZSI, where input voltage=120, load voltage=123V (top-1), Load current=3.08A (bottem-4), common-mode voltage V_{EQ}=89V (middle-3) output power=380W; and inverter terminal voltage V_T=127V (middle-2)

generator and built using FPGA VIRTEX-5 XC5VLX50T. The switching frequency is kept at 10 kHz. The experimental waveforms of the ground potential V_{EQ} shown in Figure 7.8. The high ground leakage current is reduced because the high-frequency voltage of the ground potential is eliminated at every PWM switching commutation and at zero crossing instants. The experimental waveforms of the grid current, the inductor currents i_{Lo1}, and i_{Lo2} under the 120 V_{rms} grid voltage and half-load conditions are shown

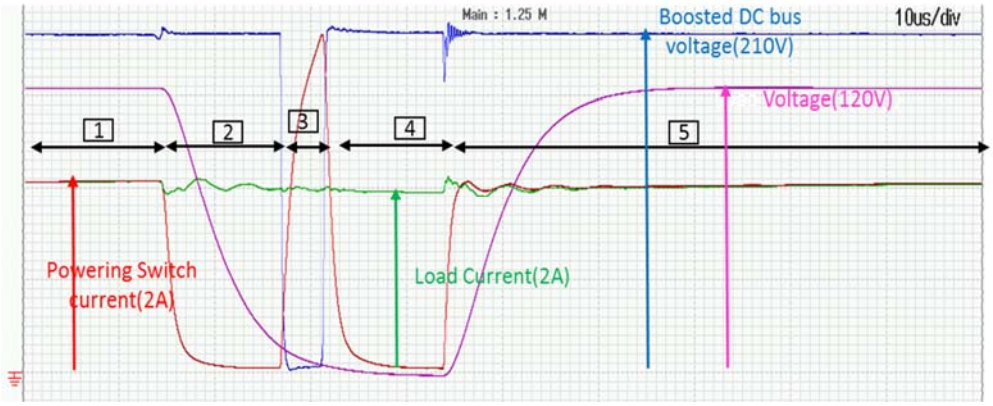


Figure 7.9. Switching cycle showing all operating states 1,powering 2,freewheeling 3,shoot-through 4,freewheeling 5,powering, with load current(green), inverter terminal voltage(pink), powering switch current(red), boosted DC bus voltage(blue)

in Figure 7.8.

One complete switching cycle operation of qZSI is illustrated in Figure 7.9. Different switching states are identified and discussed,

State – 1, Powering state, In this state, the load current is positive and Q1, Q4 are conducting. During this period, the auxiliary switches (Q5 and Q6) are not conducting any current as shown in Figure 7.9 & 7.3. After this state, the freewheeling state starts, where Q1-Q4 should not conduct and load current should flow through auxiliary switches.

State – 2, Freewheeling state, From Figure 7.9, one can notice that at the starting of this state, powering device currents (Q1 and Q4) is falling to zero whereas auxiliary switches is conducting to take up the load current. As expected, during freewheeling there is no anti-parallel diodes conduction of any of the switches Q1-Q4.

State – 3, Shoot-through state, In this state, all the four powering switches (Q1-Q4) are conducting to charge the qZS network inductors, which will consequently boost the dc bus voltage. Freewheeling switches will not be conducting here because nodes A and

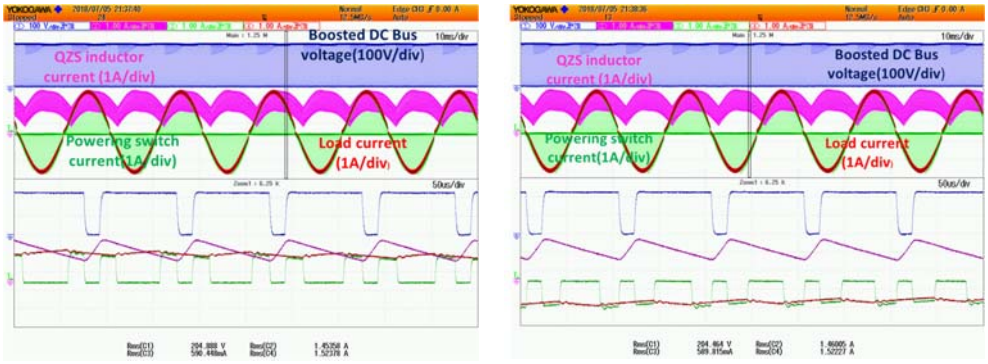
B are shorted, and the load current will flow through the powering switches.

State – 4, Freewheeling state, After the shoot-through state, the inductor will transfer the energy into the capacitors. The voltage of these capacitors will form the boosted auxiliary dc bus. On the load side, the freewheeling will be through the auxiliary switches and none of powering switches conducts.

State – 5, Powering state, During this state, the powering devices Q1, Q4 are on in positive half grid cycle.

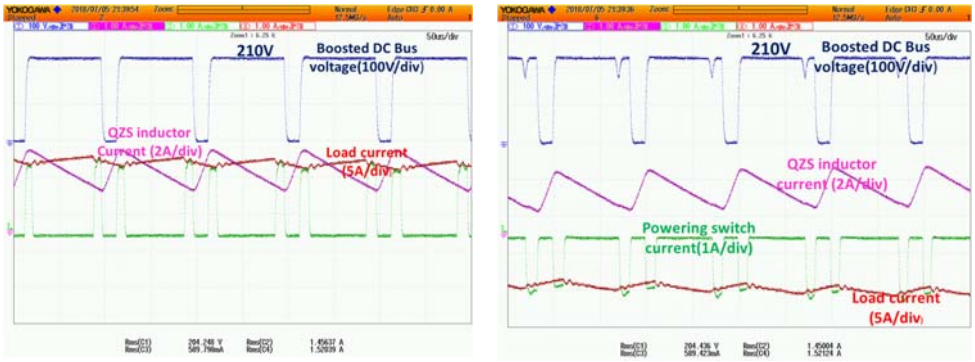
As seen in Figure 7.9, throughout the switching cycle in all the states there is no conduction of the body diodes of the power switches. In freewheeling state, there is no current flowing or voltage reflection between the AC load side and dc bus side. It shows AC decoupling is successfully achieving. The experimental results of all the switching currents is shown in Figure 7.10. Conduction of H – Bridge switches during shoot - through and powering mode is validated in Figure 7.10 (a) and (b) during positive and negative half-cycles respectively. For clarity, zoomed versions of the waveform are shown in Figure 7.11(a) and (b) for positive and negative half-cycles, respectively.

For validation of the proposed PWM control algorithm at different power factors, experimental results at unity power factor and lagging power factor are shown in Figure



(a) qZSI during positive half cycle (b) qZSI during negative half cycle

Figure 7.10. Switching currents validating the proposed PWM algorithm

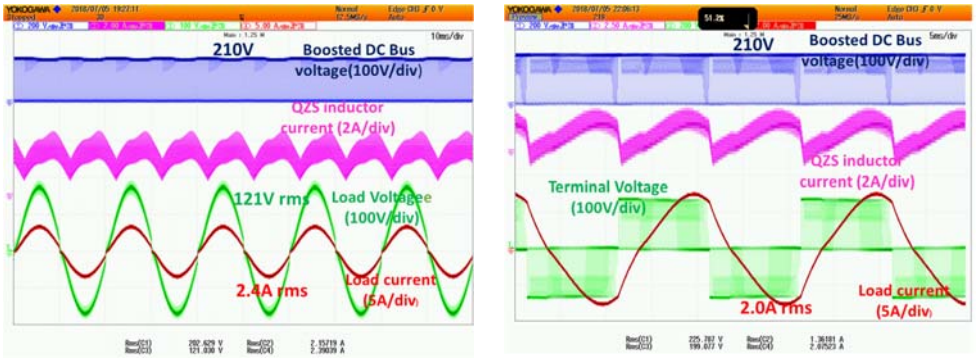


(a) Zoomed during positive half cycle (b) Zoomed during negative half cycle

Figure 7.11. Switching current in (a) positive half cycle (b) negative half cycle

7.12. During operation at unity power factor, the inductor current is always positive as the power transferred is always from the inverter to the utility grid as shown in Figure 7.12(a). However, during lagging power factor operation, negative inductor current suggests drawing of reactive power by the inverter from the utility grid as shown in Figure 7.12(b). Phase displacement between terminal voltage and load current also confirms lagging power factor operation.

THE proposed PWM control-based qZSI system is compared with the conventional qZSI system and conventional two-stage conversion for PV applications. Two-stage



(a) Operation at unity power factor (b) Operation at lagging power factor

Figure 7.12 qZSI performance (a) unity power factor (b) lagging power factor

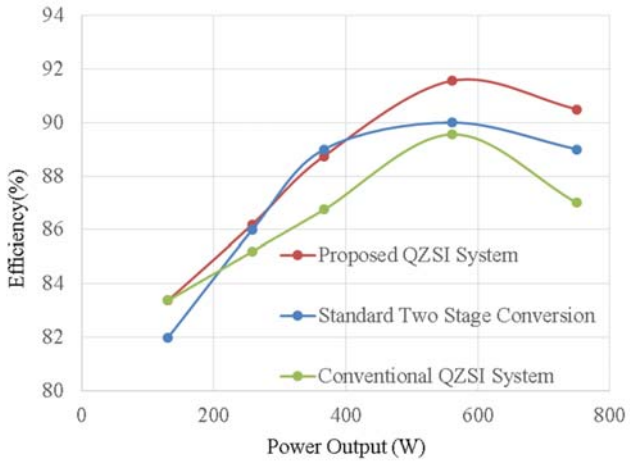


Figure 7.13. Efficiency of the proposed QZSI converter

conversion employs boost converter followed by H – Bridge inverter. Employment of shoot–through stage in qZSI leads to higher switching losses in the conventional qZSI system. With the proposed PWM algorithm, saving in switching losses is obtained by switching Q5, Q6 at grid frequency. qZSI H – Bridge switches are conducting only during powering and shoot – through modes whereas no conduction during free–wheeling mode. Thus, improved efficiency is obtained in the case of PWM control of the proposed qZSI system is compared with the standard methods in Figure 7.13.

7.7. Summary

A high boost transformerless single-phase qZSI for PV grid-connected applications is presented. Two additional switches are connected at the grid side to isolate the grid and the inverter. Modified PWM is presented to eliminate common-mode voltage and hence no common-mode current flows in the proposed topology. The major advantages of the proposed inverter topology are the boosting of the dc source voltage and elimination of common-mode leakage current between the grid and solar PV modules by using a novel and modified PWM method. Summary of the proposed qZSI characteristics,

- Body diodes of main switches (HB) are never activated throughout the fundamental

cycle and hence the overall efficiency of the system is enhanced.

- AC decoupling (unidirectional-current, D5 & Q5 and D6 & Q6 switches) occurs between PV array and AC grid during freewheeling and shoot-trough stages.
- Common-mode voltage shows isolation between grounds.

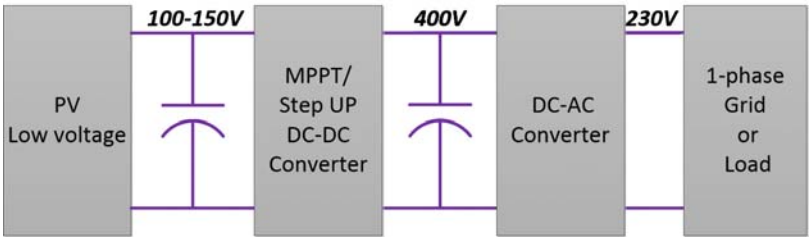
Simulations were carried out at different power factors. For validating its suitability for PV applications, simulation results with commercialized PV panels are also presented. THD performance of the proposed PWM-controlled qZSI system is better when compared to conventional PWM control. An experimental prototype of 500 Watts is developed in the laboratory and hardware results are presented. With the low leakage ground loop CM current, high efficiency, an excellent quality output current, and greatly enhanced reliability are obtained. The proposed inverter topology, controlled by the novel modified PWM technique, is suitable for transformerless PV inverter grid-connected and isolated applications. The overall efficiency of 91.4% is achieved with the proposed control algorithm.

CHAPTER 8: ISOLATED QUAZI Z-SOURCE NETWORK-BASED POWER CONVERTER

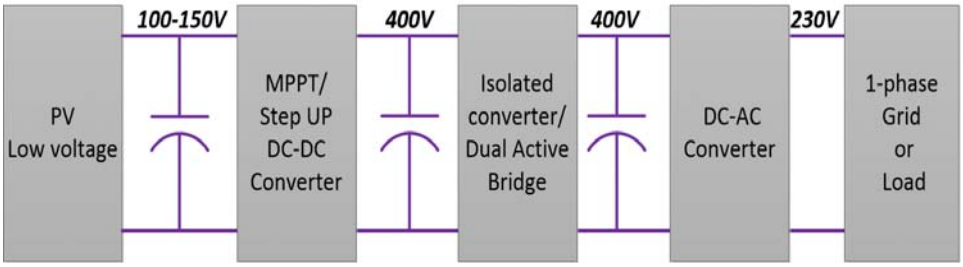
8.1. Introduction

A high gain DC-DC converter is generally used to convert the low voltage energy source to that of a higher voltage DC before connecting to the DC-AC inverter for grid-connected applications [124-128]. Solar Photovoltaics (PVs), Battery Energy Storage Systems (BESS), and Fuel Cells (FCs) are considered to be the low voltage energy sources used in power connection between the sources, loads, and the utility grid. To interlink the different sources to the utility grid, it needs two-stage power conversion like DC-DC and then DC-AC as shown in Figure 8.1(a). In this chapter, we are discussing the PV power integration with the utility grid. So the Low output PV voltage has to be boosted to the higher voltage, but simultaneously the maximum power point tracking (MPPT) has to be carried out.

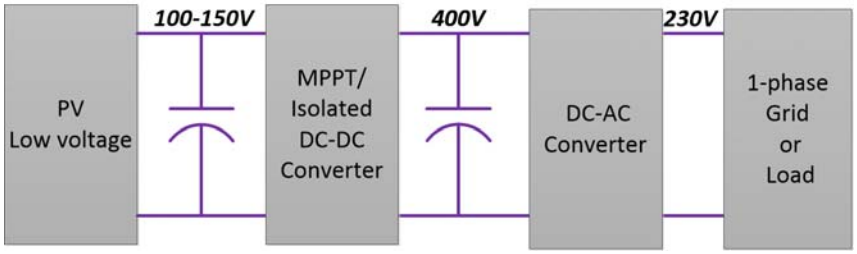
In recent years many high gain DC-DC converters have been proposed to obtain the high voltage gain in the isolated and the non-isolated converters. For the non-isolated converters, various topologies such as coupled inductor [125], cascaded converters [129], switched capacitor [126], switched inductor [127], and voltage multiplier converters [128] have been applied to the DC-DC to provide the high boost in the conversion process. However, the galvanic isolation provided in these converters is not suitable for/meets the safety standards. To address this issue number of isolated converters have been proposed. They are the boost type converters integrated with the high-frequency transformers [130, 131] and also the voltage lift techniques [132] to obtain the high voltage at the outputs. These isolated converters have two-stages DC-AC-DC power conversion. It is represented in Figure 8.1(b). It is observed that an



(a) Without Isolation



(b) With isolation



(c) Proposed isolated conversion system

Figure 8.1. PV output to the 1-phase AC conversion system

additional converter is required for the MPPT operation then this two-stage converter can isolate the grounds by providing the voltage gain through the transformer turns ratio. To improve the efficiency there are several soft-switching techniques have been reported in [60, 133, 134]. It is understood from this two-stage conversion, It is required 2 DC-link capacitors one in the PV side DC-DC converter output side and the second at the input of the DC-AC side. It reduces the reliability of the circuit topology. Furthermore, in increasing, the gain of the converter transformers are placed which leads to different voltages at the input and output side, so the different rating semiconductors will be required which increases the cost of the overall system. To address all the drawbacks of the above topologies impedance source (ZS & qZS) based power conversion system can be more appropriate for the PV applications it is shown

in Figure 8.1(c).

8.2. Isolated QZS based Conversion system

Compared to the ZS based conversion systems, QZS based system has the advantages such as the reduction of the passive component sizes and the continuous input current which leads to a lesser size of the filter capacitors. Figure 8.2 shows that the proposed Isolated QZS conversion system and in Figure 8.3. Switching logic of the proposed system. This proposed system utilizes the QZS network, HB MOSFETs at the input of the transformer, high-frequency transformer, voltage doubler rectifier (VDR), and the DC-AC converter with DC-link capacitor. In total it consists of two inductors, two capacitors in the QZS network, two capacitors in the DC-link, 8-MOSFETs, and one diode. As the source is directly connected to the inductor the input current is continuous.

8.2.1. Operating modes and circuit analysis

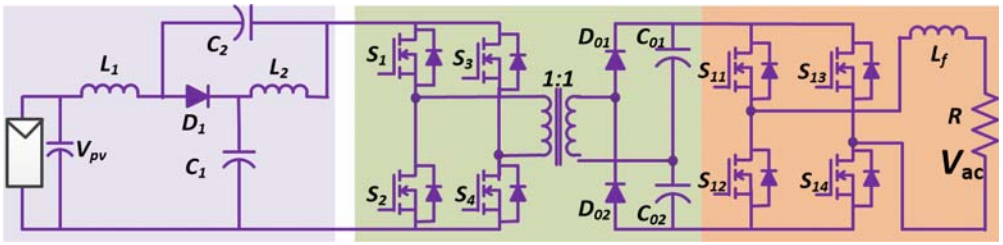


Figure 8.2. Proposed single-stage DC-AC conversion system

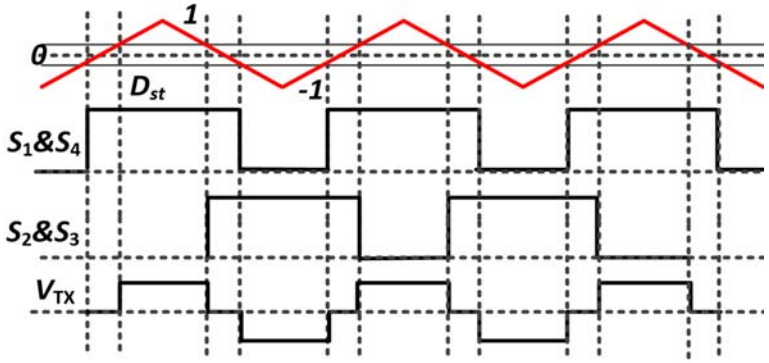
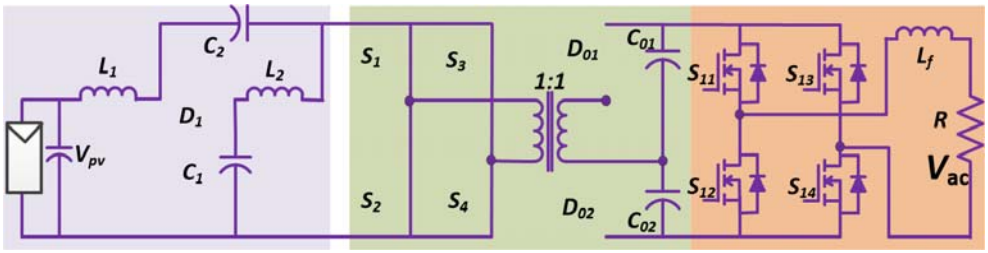
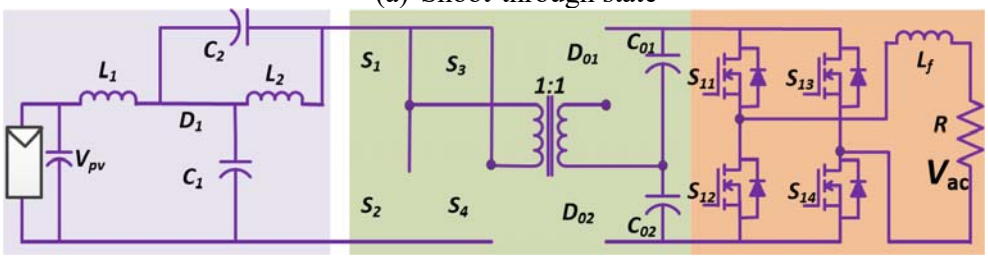


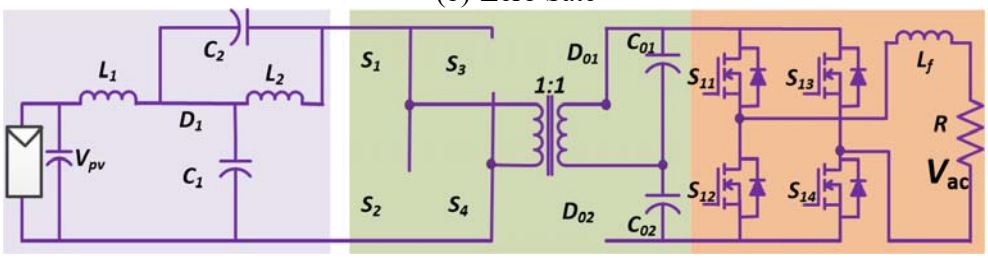
Figure 8.3. Switching logic of the proposed system



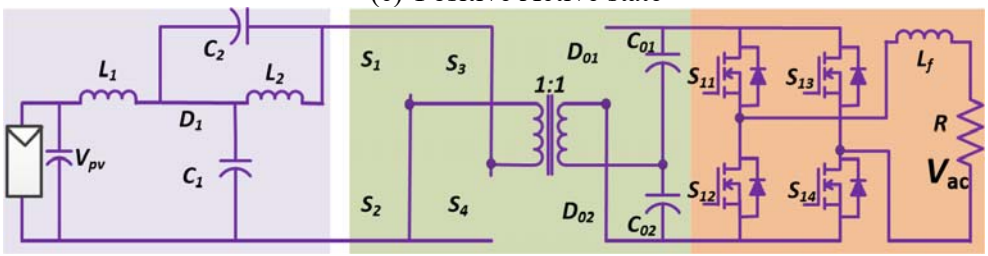
(a) Shoot-through state



(b) Zero Sate



(c) Positive Active state



(d) Negative Active state

Figure 8.4. All the operating modes of the proposed isolated converter

To simplify the operation following conditions are assumed, 1) the converter is operating under continuous conduction mode, 2) all the semiconductors are ideal, 3) capacitors are large enough to maintain the fixed voltages. Figure 8.4 shows the operating modes of the proposed isolated QSB conversion system.

In the shoot-through mode as shown in Figure 8.4(a), one of the HB legs becomes conducting (MOSFET switches *(S_1 & S_2 or S_3 & S_4)* are ON) which assumes the

transformer terminals as shorted and the VDR diodes become reverse biased. The diode D_1 in the QZS becomes reverse biased. During this mode inductor, L_1 is charged by the input and the capacitor C_2 and L_2 are charged from the capacitor C_1. The output voltage across the capacitors C_{01} and C_{02} are fixed and the DC-AC side gives the required output voltage and current from the DC-link capacitors formed by the C_{01} *and* C_{02}.

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = -i_{L2}(t) \\ C_2 \dfrac{dV_{C2}}{dt} = -i_{L1}(t) \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) + V_{C2}(t) \\ L_2 \dfrac{di_{L2}}{dt} = V_{C1}(t) \end{cases} \text{.....} \begin{cases} V_{p\_tx} = 0, i_{p\_tx} = 0 \\ V_{s\_tx} = 0, i_{s\_tx} = 0 \\ V_{out} = V_{c01} + V_{c01} \end{cases} \tag{8.1}$$

In the Zero state mode as shown in Figure 8.4(b), upper MOSFET switches *(S_1 and S_3)* or bottom MOSFET switches *(S_2 and S_4)* are ON which further assumes the transformer terminals as shorted and the VDR diodes become reverse biased. The diode D_1 in the QZS becomes forward biased. During this mode input source and inductor L_1 is discharged which energizes the capacitor C_1. L_2 is discharged and energizes the capacitor C_2. The output voltage across the capacitors C_{01} *and* C_{02} are fixed and the DC-AC side gives the required output voltage and current from the DC-link capacitors formed by the C_{01} *and* C_{02}.

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = i_{L1}(t) - i_{p\_tx} \\ C_2 \dfrac{dV_{C2}}{dt} = i_{L2}(t) - i_{p\_tx} \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) - V_{C1}(t) \\ L_2 \dfrac{di_{L2}}{dt} = -V_{C2}(t) \end{cases} \text{.....} \begin{cases} V_{p\_tx} = 0, i_{p\_tx} = 0 \\ V_{s\_tx} = 0, i_{s\_tx} = 0 \\ V_{out} = V_{c01} + V_{c01} \end{cases} \tag{8.2}$$

In the positive active mode as shown in Figure 8.4(c), S_1 & S_4 are ON. At this mode, the output voltage of the QZS network becomes the summation of the voltages of the

C_1 and C_2 which appear across the transformer primary terminals, at the secondary terminals the same polarity voltage will appear which forms the D_{01} forward biased and charges the capacitor C_{01}. C_{01} and C_{02} together form the DC-link voltage for the output AC power.

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = -i_{L2}(t) - i_{p\_tx} \\ C_2 \dfrac{dV_{C2}}{dt} = -i_{L1}(t) - i_{p\_tx} \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) + V_{C2}(t) \\ L_2 \dfrac{di_{L2}}{dt} = V_{C1}(t) \end{cases} \text{.....} \begin{cases} V_{p\_tx} = V_{C1} + V_{C2}, i_{p\_tx} \neq 0 \\ V_{s\_tx} = V_{C1} + V_{C2}, i_{s\_tx} \neq 0 \\ V_{c01} = V_{C1} + V_{C2} \\ V_{c02} = V_{C1} + V_{C2} \\ V_{out} = V_{c01} + V_{c02} \end{cases} \tag{8.3}$$

In the negative active mode as shown in Figure 8.4(d), S_3 & S_2 are ON. At this mode, the output voltage of the QZS network becomes the summation of the voltages of the C_1 and C_2, which appears across the transformer primary terminals in an inverted manner, at the secondary terminals the same polarity voltage will appear which forms the D_{02} forward biased and charges the capacitor C_{02}. C_{01} and C_{02} together form the DC-link voltage for the output AC power.

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = -i_{L2}(t) - i_{p\_tx} \\ C_2 \dfrac{dV_{C2}}{dt} = -i_{L1}(t) - i_{p\_tx} \\ L_1 \dfrac{di_{L1}}{dt} = V_{pv}(t) + V_{C2}(t) \\ L_2 \dfrac{di_{L2}}{dt} = V_{C1}(t) \end{cases} \text{.....} \begin{cases} V_{p\_tx} = V_{C1} + V_{C2}, i_{p\_tx} \neq 0 \\ V_{s\_tx} = V_{C1} + V_{C2}, i_{s\_tx} \neq 0 \\ V_{c01} = V_{C1} + V_{C2} \\ V_{c02} = V_{C1} + V_{C2} \\ V_{out} = V_{c01} + V_{c02} \end{cases} \tag{8.4}$$

The symmetricity in the application of the gate signals makes the transformer input voltage to be more square symmetric. So it can be observed that only there are two modes one as the shoot-through state $(D_{st}*T)$ and the other as the non-shoot-through state $((1- D_{st}) *T)$, by simplifying the above equations,

$$\begin{cases} V_{C1} = \dfrac{1-D_{st}}{1-2D_{st}} V_{pv} \\ V_{C2} = \dfrac{D_{st}}{1-2D_{st}} V_{pv} \\ V_{C1} + V_{C2} = \dfrac{1}{1-2D_{st}} V_{pv} = BV_{pv} \end{cases} \tag{8.5}$$

So the primary voltage of the transformer is having three voltage levels *+(V_{C1}+V_{C2}), 0,* and *-(V_{C1}+V_{C2}).* As we have selected the turn ratio of the transformer to be 1,1 the secondary voltage will remain the same. The output of the secondary can be obtained as follows,

$$\begin{cases} V_{c01} = V_{C1} + V_{C2} = \dfrac{1}{1-D_{st}} V_{pv} \\ V_{c02} = V_{C1} + V_{C2} = \dfrac{1}{1-D_{st}} V_{pv} \\ V_{out} = V_{c01} + V_{c02} = \dfrac{2}{1-D_{st}} V_{pv} \end{cases} \tag{8.6}$$

From the power balance equation, the below can be achieved,

$$\begin{cases} V_{p\_tx} I_{p\_tx} = I_{pv} V_{pv} \\ I_{pv} = I_{L1} = \dfrac{2}{(1-2D_{st})} I_{pv} \end{cases} \tag{8.7}$$

Where all the currents and the voltages are the average values.

8.3. Components Design

8.3.1. Inductor design and selection

The inductors in the proposed QZS based isolated converter are selected based on the peak-to-peak current ripple flowing through the inductors. The peak to peak inductor current ripple can be observed from the equations (7), and (1) are as below,

$$\begin{cases} \Delta I_L = \Delta I_{L1} = \Delta I_{L2} \\ \Delta I_L = \dfrac{(1-D_{st}) D_{st} T}{2(1-2D_{st}) L} V_{pv} \end{cases} \tag{8.8}$$

The ripple current passing through the inductor is at during the shoot-through state. If the inductor current ripple is chosen, so that $\Delta I_{L1} = \Delta I_{L2} < \%xI_L$, the required inductance should be,

$$\begin{cases} L = \dfrac{(1-D_{st})D_{st}T}{x\%(1-2D_{st})2P_{out}} V^2{}_{pv} \end{cases} \tag{8.9}$$

8.3.2. Capacitor design and selection

The capacitors are designed according to the capacitor voltage ripple. The current flowing through the capacitor during the shoot-through state in the proposed converter is calculated,

$$C_1 \frac{\Delta V_{C1}}{D_{st}T} = 2I_{s\_tx} + I_{L1} \tag{8.10}$$

Then final values can be achieved as follows,

$$\begin{cases} C_1 = \dfrac{(1-2D_{st})D_{st}T}{2y\%(1-D_{st})V^2{}_{pv}} P_{out} \\ C_2 = \dfrac{(1-2D_{st})T}{2y\%V^2{}_{pv}} P_{out} \end{cases} \tag{8.11}$$

Here the peak to peak capacitor voltage ripple is considered as y%.

The output capacitors *(C_{01} and C_{02})* of the VDR are selected as follows. The C_{01} and C_{02} capacitor currents are, the same as the and equal to the negative output current flowing when the converter in the zero states as in Figure 8.3 (b).to limit the ripple on the output voltage by *z%,* the capacitance should be,

$$C_{01} = C_{02} = \frac{(1-2D_{st})^2 D_o T}{4z\%V^2{}_{pv}} P_{out} \tag{8.12}$$

8.3.3. Transformer design

The design process for the transformer is dictated by the constraints imposed from

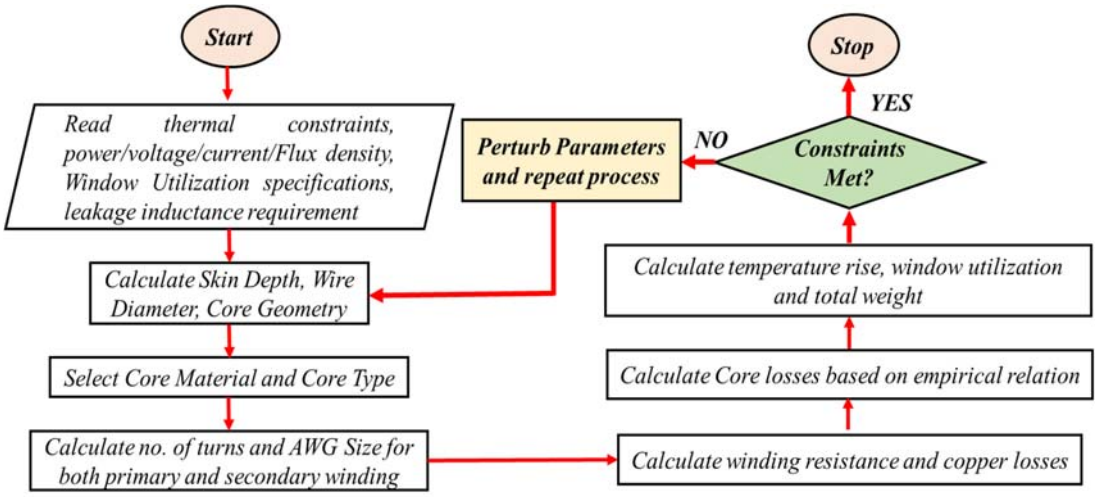


Figure 8.5. Flowchart showing design process of the high-frequency transformer

different domains. Majorly, thermal constraints dominate the design in addition to power requirements. The design process followed is shown in Figure 8.5. For operation at a high-frequency of 100kHz, skin depth must be estimated. Based on the skin depth, maximum wire diameter selection must be made.

Calculation of skin depth (ε) = $\frac{6.62}{\sqrt{f}}$ = 0.209cm

Wire diameter (D_{awg}) = 0.04186 cm

Bare Wire Area (A_w) = 0.0013768 cm^2

Following steps have been followed for the selection of core material, AWG wire size, and estimation of other operating performance parameters.

Step – 1, Total Apparent Power (P_t) = $KVA * \frac{1}{\eta}$ = 201.01kW

Step – 2, Electrical condition (K_e) = $0.145 * (K_f)^2 * (f)^2 * (B_m)^2 * 10^{-4} = 7.11 * 10^4$

Step – 3, Core geometry (K_g) = $\frac{P_t}{2K_e\alpha}$ = 0.1886

Step – 4, Based on these three parameters, the core must be selected. For this design, the selected core is U93-76-16 having the following specifications,

Iron weight (W_{tfe}) = 800gms; mean length of turn (MLT) = 15.2cm; iron area (A_c) = 4.48 cm^2; window area (W_a) = 34.752cm^2; area product (A_p)= 155.689cm^4; core geometry (K_g) = 18.3549cm^5; surface area (A_t) = 605.3cm^2.

Calculations for the primary side,

Step – 5, Number of primary turns (N_p) = $\frac{V_{in} * 10^4}{K_f B_{ac} f A_c}$ = 32 turns

Step – 6, Current density (J) = $\frac{P_t * 10^4}{K_f K_u B_{ac} f A_p}$ = 230.55 A/cm^2

Step – 7, Input current (I_{in}) = $\frac{P_o}{V_{in} * \eta}$ =101.01 A

Step – 8, Primary bare wire area (A_{wp}) = $\frac{I_{in}}{J}$ = 0.438cm^2

Step – 9, No. of primary strands (S_{np} for AWG25) = 319

Step – 10, Micrometer Ohms per centimeter = 4.1974 μΩ/cm

Step – 11, Primary Winding Resistance (R_p) = $MLT*N_p*Resistivity$ = 0.0011551Ω

Step – 12, Total primary copper loss (P_p) = I_p^2*R = 11.786 Watts

The calculation for the secondary side,

Step – 13, Secondary turns (N_s) = $\frac{N_p V_s}{V_{in}}\left(1+\frac{\alpha}{100}\right)$ = 34 turns

Step – 14, Secondary bare wire area (A_{ws}) = 0.36838 cm^2

Step – 15, No. of secondary strands (S_{np} for AWG25) = 268

Step – 16, Micrometer ohms per centimeter = 4.9963 μΩ/cm

Step – 17, Secondary winding resistance (R_s) = 0.0025821 Ω.

Step – 18, Total secondary copper loss (P_s) = 23.33 Watts

Step – 19, Transformer Regulation (α) = 0.0351%

Step – 20, mW/kg for core loss calculation = 93.98 mW/g

Step – 21, Core loss (P_{fe}) = $0.000557(f)^{1.68}(B_{ac})^{1.86} * W_{tfe} * 10^{-3}$ = 75.186 Watts

Step – 22, Total losses (P_{sigma}) = 19.31 Watts

Step – 23, Efficiency (η) = 98.88%

Step – 24, Watts per unit area (ϕ) = $\frac{P_{\Sigma}}{Surface\_Area}$ = 0.1822 W/cm^2

Step – 25, Temperature rise (T) = $450 * (\varphi)^{0.826}$ = 19.28^0 C

Step – 26, Total Window Utilization (K_u) = 0.7638 pu

Step – 27, Length with a total number of turns = 1003.2 cm

Step – 28, Weight of copper in the winding (W_{cu}) = 3534.5 grams

Step – 29, Steel to copper weight ratio (W_s, Wcu) = 0.226 unit less

Step – 30, Total weight (W_{tfe}+W_{cu}) = 4.334 kg

8.4. Simulation results and discussion

The parameters used for the simulation of the proposed converter are presented in Table 8.1. A 100KW high-frequency transformer is modeled in the Matlab Simulink to record the results obtained. Figure 8.6 shows that 450V input the capacitor voltages are 100V and 550V. The achieved DC-link voltage peak will be a summation of the qZS capacitors as 650V. In Figure 8.7, the inductor currents are equal and having a peak of 300A.

the HFT transformer's primary and secondary voltages are obtaining with 100kHz

Table 8.1 Simulation parameters for proposed isolated qZS inverter

Parameters	Value
Total output power (P_{total})	100kW
AC grid RMS voltage (V_{LLgrid})	1kV
qZS inductances (L_1, L_2)	1mH
qZS capacitances (C_1, C_2)	100uF
AC load frequency (f)	50Hz
Switching frequency of each module	100kHz

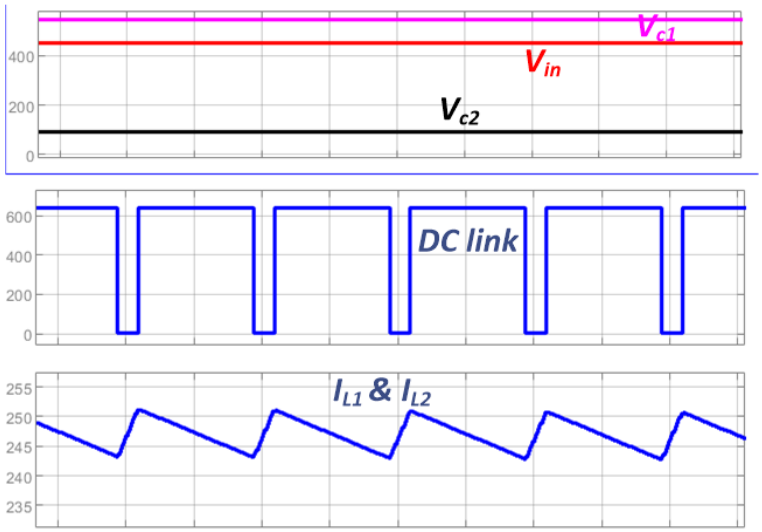


Figure 8.6. qZS network component voltages and currents.

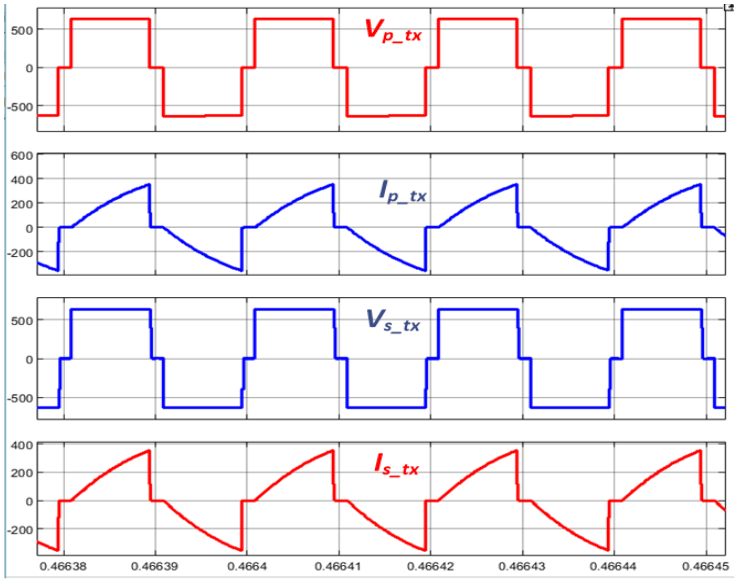


Figure 8.7. HFT primary and secondary side voltages and currents respectively

frequency as per the design.

Figure 8.8 shows the VDR diode voltages and capacitor voltages along with the DC-link voltage with the HB current. Where the DC-link capacitors voltage is double that of the transformer primary.

Figure 8.9. Output AC voltage and the load current of the proposed converter.

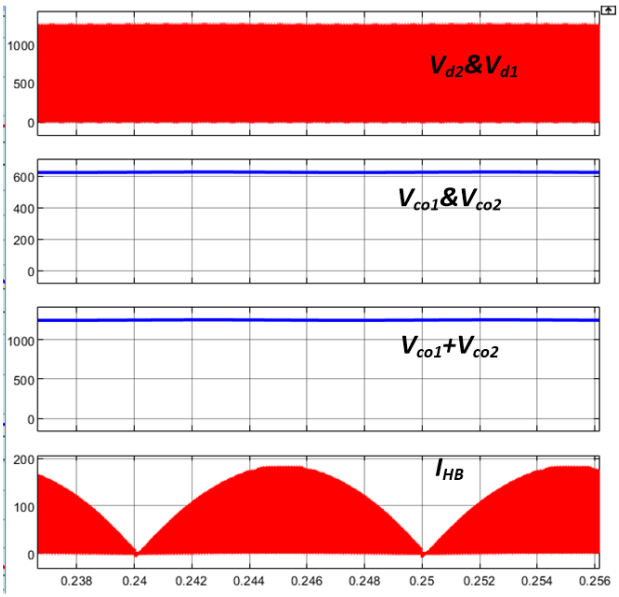


Figure 8.8. VDR diode voltages and capacitor voltages along with the DC-link voltage with the HB current.

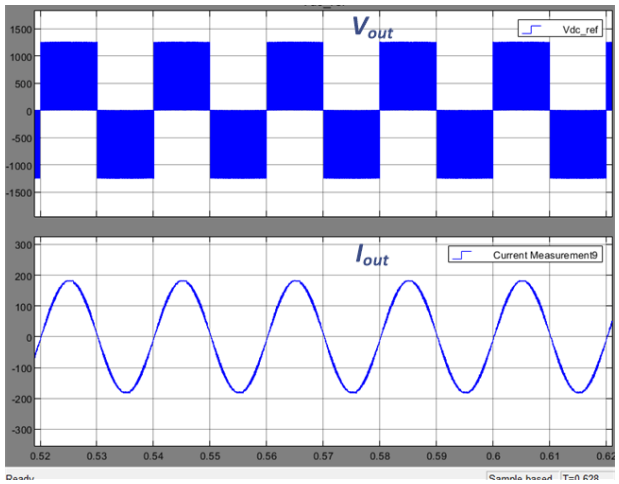


Figure 8.9. Output AC voltage and the load current of the proposed converter

8.5. Summary

In this chapter, an Isolated Quazi Z-Source converter system has proposed for the high-frequency operation, for the distributed power generation system. This system consists of a PV side qZS network, thus creates the continuous input current; High-frequency Transformer (HFT) for the isolation between the PV and AC side; Voltage Doubler

Rectifier (VDR) for boosting the input voltage; finally HB for the Dc-AC conversion. The high-frequency AC small-signal analysis for the qZS network has been presented and its passive components affect on the operation of the entire system. The HFT design details presented as the special type of techniques needed to reduce the impact of skin effect and proximity effect. In the end, the simulation and experimental results validated the proposed system.

CHAPTER 9: HIGH VOLTAGE HIGH POWER MULTILEVEL CONVERTER FOR SOLAR PV APPLICATIONS TO THE UTILITY GRID

9.1. Introduction

The sharp rise in the generating capacity of the huge PV power plants in the range of hundreds of kilowatts (KW) to tens and hundreds of megawatts (MW), has pushed the power electronic converter structures towards the multilevel converters research and development. These new MLI's have lower filter sizes, fast response time, onsite reactive power control feature, highest power density, etc. [135, 136]. PV applications employing qZS cascaded multilevel inverters (qZS-CMI) have recently gotten a lot of attention. In [137] author has presented the feasibility and application of the qZS-MLI for MW scale PV systems, in [88] design criterion for the module integrated PV converters when using a wide bandgap semiconductor, in [61, 65] control techniques and dispersed maximum power output has been detailed. The following aspects were shared by the qZS-CMI, 1) single-stage dc-ac power conversion with DC-link capacitor voltage balancing, 2) high efficiency of the power devices as the feasibility of the shoot-through sate, 3) direct connection of the medium voltage grid without the central stations bulky, costly, and uncontrolled line frequency transformer. The double line frequency (DLF) power oscillates at the DC-connection of every qZS-CMI module, instigating DLF ripples on the inductor currents and capacitor voltages of the qZS network [5]-[6]. To further minimize the undesired DLF ripple, suggestions were formulated in the following categories, 1) passive components of the qZS network are buffered the DLF voltage and current ripples within tolerant limits [138] but the wide range impedance values were selected despite using wide bandgap devices at the very high switching frequency, which confronted with the size, cost, power rating of the high power applications; 2) a hybrid PWM made the DC-link voltage envelop cope with the

AC voltage, thus not limiting the dc-link DLF voltage ripple and decreasing the qZS impedance [15], while a large capacitor is placed must be placed to at the PV terminals to prevent the propagation of the ripple power to the PV panels; 3) the ripples can be reduced by employing special control methods to decrease the impedance values [72, 139], while a bulky large capacitor has to place at the PV terminals to prevent ripple.

In light of the PVs natural dc and distributed characteristics modular multilevel converters (MMC) were designed for high power PV applications with the goal of reducing the power conversion steps, reducing the power losses in the lines, and increasing the efficiency [140, 141]. The PV panels in series forming the DC connection of the MMC's DC-AC portion have a dc-bus voltage which is far below the utility grid voltage [142] due to the PV panel insolation level is less than the 1.5KV. A DC-DC converter has to be placed along with the isolation transformer into each module of the qZS-CMI structure. Separate control methods and gating signals are required for the isolation and output stage converters, which would significantly increase controlling pressure, physical hardware, and costs as the dc-bus voltage level rises.

This chapter describes a modular cascaded multilevel converter (qZS-CMC) high power PV systems to resolve the above shortcomings. The proposed qZS-CMC is made up of a series of front end isolated qZS-HB DC-AC-DC converter submodules (SMs). The PV panel is safely grounded and isolated from the grid due to the front-end isolation. Because there is no DLF ripple power passing through DC-side PV panels, qZS impedance (inductors and capacitors) has lower impedance values than the qZS-CMI. The detailed operation of the single module is discussed in the previous chapter.

9.2. qZS-CMC based PV power system

9.2.1. System Configuration

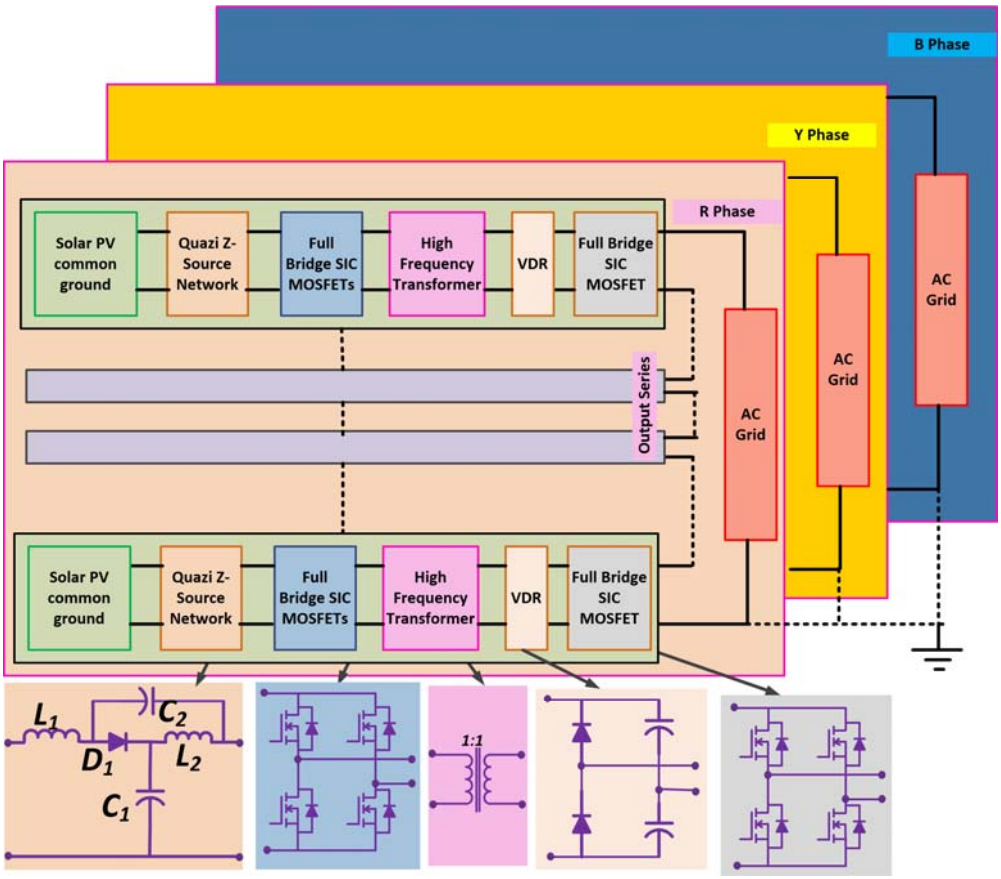


Figure 9.1. Configuration of the qZS-CMC PV power system

Figure 9.1 shows the proposed qZS-CMC for the high power high voltage PV system. Each submodule consists of PV panels, qZS network, primary HB for DC-DC-AC conversion, isolation transformer, Voltage doubler rectifier (VDR), and secondary HB for the DC-AC conversion. All these submodules are connected in series from the desired voltage at the AC utility grid. Here isolating transformer-isolated the PV array from the high voltage ac so that the insulation of 1.5KV can be maintained at the PV side. The primary HB converter acts for multiple purposes, such as the shoot-through stage can be used to extract the maximum power from the PV and the active state is used to transfer the power from the primary to secondary of the transformer. As the shoot-through duty is very minimal, during that mode current flowing through the

primary of the transformer is zero. As the secondary is connected between the diodes and the capacitor legs it will be considered as the equal voltage is distributed between the diodes, so the potential during the shoot-through state is also zero. Capacitors at the VDR are act as the dc-link for the DC-AC stage.

9.2.2. Operating Principle

Figure 9.2, presents the single submodule present in the proposed qZS-CMC. As the voltage, handling capability of the qZS concept is sufficient for one to two times the PV voltage, so a small duty ratio can be preferred to achieve this voltage margin. Furthermore, the VDR at the secondary of the transformer is increasing the voltage by a factor of two. So a 1,1turns ratio transformer is selected. This further simplifies the design and cost of the overall system. The qZS and primary HB operation and its gain formulae gain achieved as follows,

$$\begin{cases} V_{C1} = \dfrac{1-D_{st}}{1-2D_{st}} V_{pv} \\ V_{C2} = \dfrac{D_{st}}{1-2D_{st}} V_{pv} \\ V_{C1} + V_{C2} = \dfrac{1}{1-2D_{st}} V_{pv} = BV_{pv} \end{cases} \tag{9.1}$$

So the primary voltage of the transformer is having three voltage levels +(V_{C1}+V_{C2}), 0 and -(V_{C1}+V_{C2}). As we have selected the turn ratio of the transformer to be 1,1 the

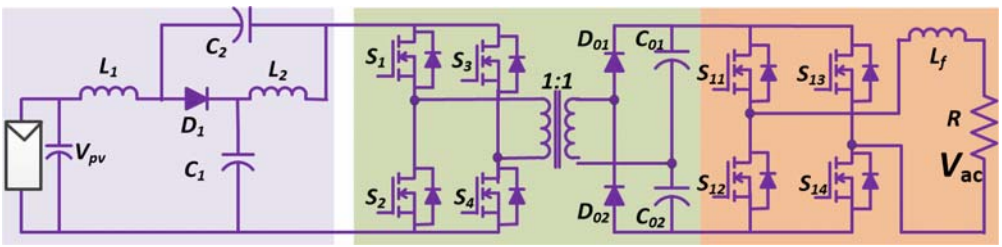


Figure 9.2. Submodule of the proposed qZS-CMC

secondary voltage will remain the same. The output of the secondary can be obtained as follows,

$$\begin{cases} V_{c01} = V_{C1} + V_{C2} = \dfrac{1}{1-2D_{st}} V_{pv} \\ V_{c02} = V_{C1} + V_{C2} = \dfrac{1}{1-2D_{st}} V_{pv} \\ V_{out} = V_{c01} + V_{c02} = \dfrac{2}{1-2D_{st}} V_{pv} \end{cases} \tag{9.2}$$

From the power balance equation, the below can be achieved,

$$\begin{cases} V_{p\_tx} I_{p\_tx} = I_{pv} V_{pv} \\ I_{pv} = I_{L1} = \dfrac{2}{(1-2D_{st})} V_{pv} \end{cases} \tag{9.3}$$

Where all the currents and the voltages are the average values.

9.3. 4 MW Isolated Quasi Powered Multilevel Converter, Control Algorithm,

The control algorithm for the proposed converter must satisfy the following control requirements,

(a) DQ axis control of grid current resulting in independent control of active and reactive current

(b) DC bus voltage of each module must be maintained at the desired value

(c) The possibility of operation at unity, lagging, and leading power factors must be demonstrated.

For developing this complex control algorithm, the conventional MASTER-SLAVE control strategy is used here. The three major control components are discussed in detail below,

9.3.1. Controller Unit

In vector control theory, a three-phase sinusoidal current is converted into two dc

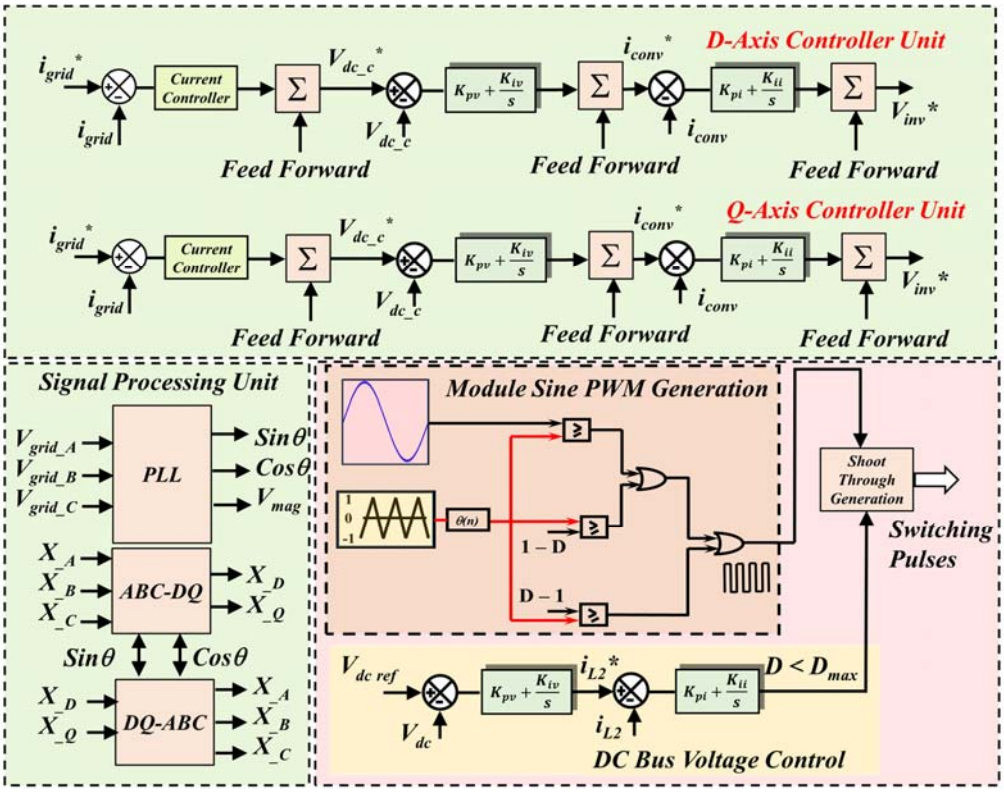


Figure 9.3 Control algorithm of proposed converter consisting of controller unit, signal processing unit and modular switching signal generation unit

current, which is independent of each other. These currents independently alter the torque and operating flux, thereby giving a highly dynamic and fast response. On similar lines, in this case, also, three-phase grid current can be segregated into d-q currents, which are responsible independently for active and reactive power flow. Thus, in the controller unit, two identical loops exist for d and q axis currents. As LCL filter is used at the grid side, three cascaded control loops are used as shown in Figure 9.3. Feedforward terms in the control algorithm represent the decoupling terms added to practically achieve completely isolated performance.

Following equations are used for d-axis control,

$$V_{id} = V_{cd} - \omega_s i_{Lq} + \left(L\frac{d}{dt}i_{Ld} + Ri_{Ld}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (9.4)$$

$$i_{Ld} = C\frac{dV_{cd}}{dt} + i_{1d} + \omega_s V_{cq} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9.5)$$

$$V_{cd} = V_{sd} - \omega_s i_{1q} + \left(L\frac{d}{dt}i_{1d} + Ri_{1d}\right) \ldots\ldots\ldots\ldots\ldots\ldots (9.6)$$

Following equations are used for q-axis control,

$$V_{iq} = V_{cq} + \omega_s i_{Ld} + \left(L\frac{d}{dt}i_{Lq} + Ri_{Lq}\right) \ldots\ldots\ldots\ldots\ldots\ldots (9.7)$$

$$i_{Lq} = C\frac{dV_{cq}}{dt} + \omega_s V_{cd} + i_{1q} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9.8)$$

$$V_{cq} = V_{sq} + \omega_s i_{1d} + \left(L\frac{d}{dt}i_{1q} + Ri_{1q}\right) \ldots\ldots\ldots\ldots\ldots\ldots (9.9)$$

In the above equations, X_{xd}, X_{xq} = suffix 'd', 'q' indicates quantities on d and q axes; V_{id}, V_{iq} = d, q axes components of inverter voltage; V_{cd}, V_{cq} = d, q axes components of filter capacitor voltage; V_{sd}, V_{sq} = d, q axes components of grid voltage; i_{Ld}, i_{Lq} = d, q axes components of inverter current; i_{cd}, i_{cq} = d, q axes components of filter capacitor current; i_{1d}, i_{1q} = d, q axes components of grid current; ω_s = grid frequency in rad/sec; L = filter inductance; C = filter capacitance; R = internal resistance of filter inductor.

In the control loop, firstly actual grid current is compared with the actual value and passed through the PI controller to generate voltage reference for the filter capacitance. This voltage is then compared with the actual value to give a reference for the converter current. This current is then compared with the actual value to generate an inverter voltage reference. All these controllers generated control signals are added with feedforward terms to compensate for the passive components drop as well as to achieve completely isolated performance. The final output of the controllers can also be limited using saturation limiters if deemed necessary.

9.3.2. Modular Sine PWM Generation

Table 9.1 Simulation setup parameters for multilevel qZS inverter connected to utility grid

Parameters	Value
Total output power (P_{total})	4MW
AC grid RMS line-to-line voltage (V_{LLgrid})	11kV
qZS inductances (L_1, L_2)	2.5mH
qZS capacitances (C_1, C_2)	2mF
AC load frequency (f)	50Hz
Switching frequency of each module	10kHz
No. of modules	16

Reference signals generated in the controller unit are transformed into three-phase voltages. These voltages are then divided by no. of modules (16 in this case). Further, the voltages are divided with the respective dc bus voltage to obtain a reference modulation signal for each module. As qZS inverter, also generates its shoot through duty cycle for boosting the voltage, the duty cycle must also be accommodated in the switching signal generation process as shown in Figure 9.3.

9.4. Simulation results and discussion

The proposed converter is simulated for a 4MW power rating. This converter can be operated at any desired power factor and the simulation results presented must validate this. Parameters used for simulation are shown in Table 9.1.

Following power, references are given in the control algorithm to validate the performance.

(a) At t = 0, the converter operates at unity power factor supplying 0.8pu active power (3.2MW)

(b) From t = 2-4 sec, the converter operates at 0.8 lagging power factor supplying 0.8pu active power and 0.6pu reactive power (i.e., 3.2MW and 2.4MVAR) and

(c) From t = 4 to 5sec, the converter operates at 0.8 leading power factor supplying 0.8pu active power and 0.6pu reactive power (i.e., 3.2MW and -2.4MVAR).

Figure 9.4 shows the simulation results for the system performance. Change in active power and reactive power are conveniently tracked with no performance deviations. However, transient performance can be further improved. The major drawback in this

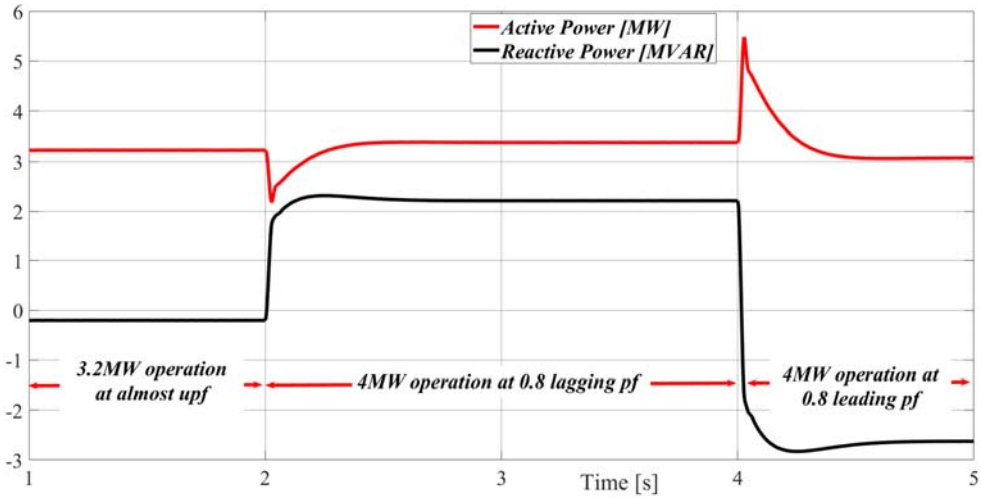


Figure 9.4. Transient response of system for change in active and reactive power references

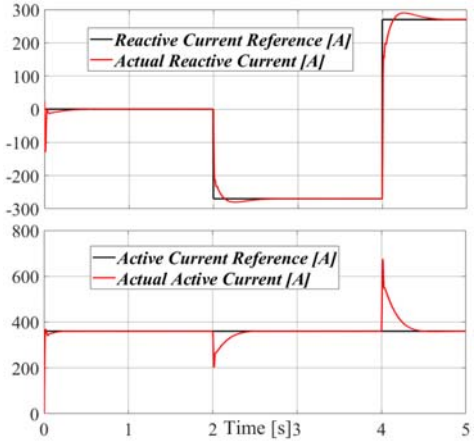


Figure 9.5 Tracking performance of active and reactive power producing d and q axes currents

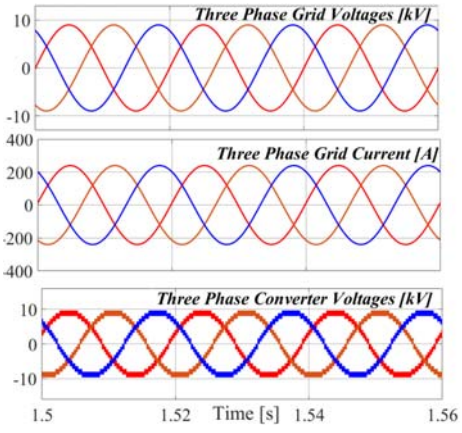


Figure 9.6. Grid voltage, current and converter voltage waveforms for unity pf operation

process is the densely populated passive component in the qZSI modules. For controlling active power, the d – axes current is controlled, whereas, reactive current only impacts the reactive power. For validation, Figure 9.5 shows the d and q axes' current tracking. Although the transient response is impacted by the change in reference, steady-state operations are completely independent of each other.

As the grid current obtained is a function of grid voltage and converter voltage, this current can be controlled by varying the converter voltage. To verify and demonstrate this principle, the zoomed results showing the grid voltage, converter voltage, and resulting grid current are also shown. Figure 9.6 shows the unity power factor operation of the system. It can be observed here that grid current is incomplete phase with the grid voltage. Also, the converter voltage is almost equal to grid voltage in magnitude, although the converter leads the grid voltage in phase.

Figure 9.7 shows the system operation at 0.8 lagging power factor. Here, the grid current lags behind the grid voltage. To achieve this, the converter voltage is higher than the grid voltage in magnitude and it also leads the grid voltage.

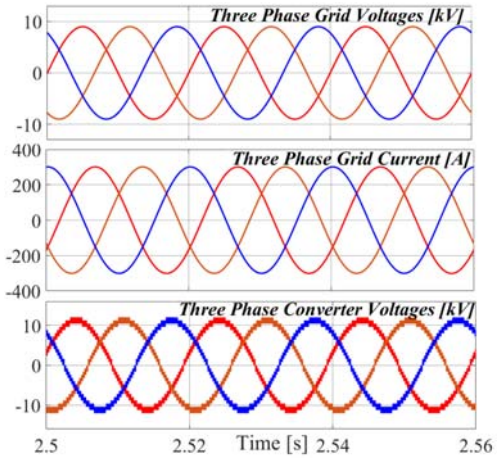


Figure 9.7 Grid voltage/current and converter voltage waveforms for lagging pf operation

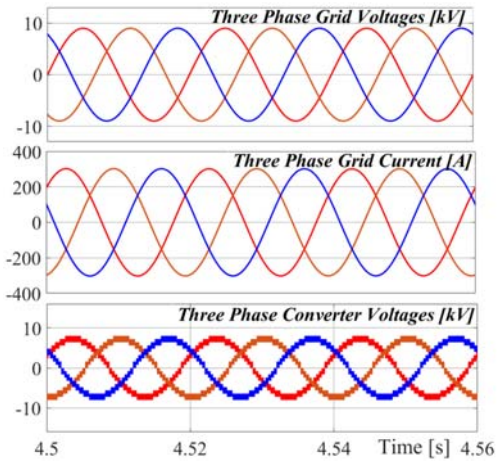


Figure 9.8. Grid voltage/current and converter voltage waveforms for leading pf operation

Figure 9.8 shows the system operation at 0.8 leading power factor. Here, the grid current leads to the grid voltage. To achieve this, converter voltage is lower than the grid voltage magnitude and as always leads the grid voltage in phase.

This converter can be conveniently operated at 1.0pu active power reference i.e., to its full capability supplying only active power. This operation is deemed ideal in current scenarios of a highly dynamic utility grid with the requirement of reactive power almost unavoidable.

9.5. Summary

In this chapter, by utilizing the above-developed (Chapter 9) topology a QZS based Cascaded Modular Converter was proposed for the high power and high voltage PV systems. The proposed systems operating principle, control mechanism, and modulation have been discussed in detail. The Matlab Simulink simulation results reported the suitability for the PV systems.

CHAPTER 10: CONCLUSION AND FUTURE WORK

10.1. Conclusion

A detailed review of the impedance source converters is elaborated and the necessity of the novel power converters for single-stage high gain power converters is identified and illustrated. Generally, Solar PV power conversion systems contain a basic DC-DC converter for the extraction of the maximum power from the solar panels, this is the first stage of the conversion. During the second stage, H-Bridge (HB) modules have to be placed to convert the regulated DC voltage to the required AC voltage. This makes the two-stage conversion less efficient. Furthermore, the operating switching frequency of the power converters is limited by semiconductor technology.

The power electronic converters for the PV applications are presented in this dissertation. This dissertation was divided into two parts, one is devoted to the multilevel converter for the non-isolated applications and the second discusses isolated conversion applications, for achieving the distributed generation integration with the utility grid. As the higher switching frequency semiconductors are more effective and their usage reduces the size, cost and increases the efficiency of the power converters. This prompted the PV converters to adopt this promising wide bandgap technology that facilitates higher switching frequency operations.

As discussed above the basic PV converters were operating in two-stages and also the size of the PV capacitor depends on the ripple current in the input PV capacitor. To address shortcomings of two-stage conversion, Z-source converters have been proposed in early 2003. However, they operate with discontinuous input current which leads to the use of higher capacitor size. To address this drawback of Z-source converters, a Quazi Z-source converter has been developed, that draws continuous input current. Furthermore, it has a single-stage conversion from DC to AC with boosting feature that

is facilitated by controlling the shoot-through state and it also integrates the MPPT operation of the PV array. At the higher switching frequency, the size of the impedance network becomes significantly smaller and thus offers a more efficient solution than the near competitor.

By using qZS as the front-end power converter many different power converters have been proposed and they are discussed in the introduction of this dissertation. However, all the reported topologies used phase-shifted pulse width modulation (PSPWM) scheme for their controlled desired operation. It means in the n-module MLI each module has to operate at switching frequency ($f_{sw,}$), then the resultant switching frequency at the output of the converter becomes n-times the f_{sw} (n*f_{sw}). The Electromagnetic interference (EMI) on the whole system becomes significant and also the losses in the whole system become substantial that reduces the overall efficiency of the converter. To address this issue, a novel level-shifted pulse width modulation (LS-PWM) is developed and reported in this dissertation.

To begin with the multilevel operation, two cascaded modules were selected and level-shifted techniques are applied. The detailed design, modulation, loss analysis, and control are developed successfully. This new modulation is quite similar to the standard Phase opposed disposed Pulse width modulation (PODPWM). However, as the number of modules per phase increases (more than 2), this proposed PWM technique cannot be applied. Because during the shoot-through state the output voltage becomes zero. Which further increases the size of the output filter. Hence to address this issue a unified combined hybrid PWM technique has been developed. Where the n-number of modules can be used for the MLI operation. The developed Phase opposed disposed and phase-shifted (PODPS-PWM) has unequal power distribution between the n-number of modules. This technique has been successfully implemented for addressing the partial

shading phenomenon in PV systems. Nevertheless, during the normal balanced operation, the power among the modules is different. Then further carrier rotation technique have been developed for operating in all the required modes to address the unequal power-sharing phenomenon. All the modulation procedures and their loss analysis has been validated by the simulation and also experimentally. By employing the PODPS-PWM technique, high power high voltage MLI has been controlled. The simulation results have been discussed. The presented technique offers better efficiency and performance than the available techniques in the literature.

The non-isolated converter configuration provides isolation of solar PV panels of up to 1.5 kV. For providing the isolation of higher voltage between the low voltage PV and the high voltage AC, converter configuration is modified by adding a pair of controlled switches that operate at grid frequency and special modulation is developed to create the isolation between the PV and AC grid. Two branches of the additional series-connected switch and diode are placed in parallel before the output filter (or after the HB output). Mathematical analysis and their loss analysis have been developed, to ensure efficiency improvement in the overall system. The simulation and experimental results have proved the superiority of the developed converter. However, this technique cannot be used in high power application as a large number of diodes and controlled switches will be needed. The control of the entire system becomes more complex. Even though, if it is implemented for cascaded converters, the isolation cannot be guaranteed because the developed algorithm is not suitable for the multilevel operation. An improved modulation was employed to address these issues.

In the conventional DAB-based PV systems there are two DC-link capacitors are present in the system along with a separate DC-DC converter that is placed to operate the PV at the MPPT and also maintain the continuous input current, to reduce the PV

capacitor sizes. Front-end qZS based single-stage DC-AC-DC converter was successfully developed for the AC output applications as an alternative to DAB. Where the component count is lesser than the standard converters and maintains the continuous input current. The high-frequency transformer (HFT) design is the center of this topology. The detailed small-signal model for the high-frequency operation of the qZS converter is presented in the dissertation, which also illustrates the stability analysis for the high-frequency operation, the impacts/effects of passive components are investigated and stability criterion has been obtained.

To achieve high power and high voltage the above HFT based topology is better suited. So on the primary side 1.5KV can be isolated from the high voltage secondary by using HFT. HFT primary side HB is operating in two modes one is shoot-through mode and the second is the non-shoot-through mode. These two modes help operate the PV side in MPPT condition and simultaneously generating the switching frequency voltage and currents in the transformer primary and the secondary sides. The distributed input series and output series converter is developed. To reduce the design problems and unifying the stresses on the semiconductors, 1,1 turns ratio HFT is selected. The detailed operation, modulation technique, simulation, and experimentation has been developed to show the superiority of the developed qZS-CMC converter.

The research presented in this dissertation was deliberately dedicated to improving techniques in PV power system applications. The results achieved hold promises in fostering a great deal faster commercialization of such power electronic converters.

10.2. Future Work

For future work, the following can be pursued by applying these improved modulation techniques,

- The developed PODPS-PWM techniques further can be applied for the

dispersed distributed maximum power point tracking application to address the partial shading phenomenon.

- The developed algorithm can also be effectively applied for the high power and high voltage motor drives.
- As the isolation between the high voltage and low voltage side is successfully implemented, it can be used for the Battery Energy storage systems (BESS) for the Input parallel and the output series applications.
- The application of the proposed converter for the development of fast-charging stations can be suitable candidate, Input Series (AC) and the output parallel (DC) applications.
- As the isolation between the high voltage and low voltage side is successfully implemented, it can be used for the AC and DC microgrid interconnections , Input parallel (DC) and the output series (AC) applications.
- The complete digital controllers have to be developed to operate autonomously.

CHAPTER 11: Appendix

11.1. Under equal power distribution condition

For a seven-level qZSI operation consisting of three qZSI modules, the performance of each qZSI switch of the bottom module for the entire fundamental cycle is shown in Table – A. For three modules, the modulation signal is categorized into three modulation levels. Here for range m = 0 to 1/3, output voltage level consists of voltage transitions from 0 to V_{dc}. Similarly, for m = 1/3 to 2/3, output voltage consists of transitions between V_{dc} to $2V_{dc}$ and for m = 2/3 to 1, voltage transition is from $2V_{dc}$ to

Table – A, Characteristics of different switches in different modulation region

	Active State				Shoot-through			
Modulation Region	S_{11}	S_{12}	S_{13}	S_{14}	S_{11}	S_{12}	S_{13}	S_{14}
0 to $\frac{\pi}{9}$	$\frac{A}{3}$	$\frac{A}{3}$	0	1	ST	$\frac{ST}{3}$	ST	0
$\frac{\pi}{9}$ to $\frac{\pi}{4}$	$\frac{A}{3}$	$\frac{A}{3}$	0	1	$\frac{2ST}{3}$	$\frac{2ST}{3}$	ST	0
$\frac{\pi}{4}$ to $\frac{\pi}{2}$	$\frac{A}{3}$	$\frac{A}{3}$	0	1	$\frac{ST}{3}$	ST	ST	0
$\frac{\pi}{2}$ to $\frac{3\pi}{4}$	$\frac{A}{3}$	$\frac{A}{3}$	0	1	$\frac{ST}{3}$	ST	ST	0
$\frac{3\pi}{4}$ to $\frac{8\pi}{9}$	$\frac{A}{3}$	$\frac{A}{3}$	0	1	$\frac{2ST}{3}$	$\frac{2ST}{3}$	ST	0
$\frac{8\pi}{9}$ to π	$\frac{A}{3}$	$\frac{A}{3}$	0	1	ST	$\frac{ST}{3}$	ST	0
π to $\frac{10\pi}{9}$	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	ST	$\frac{ST}{3}$
$\frac{10\pi}{9}$ to $\frac{5\pi}{4}$	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	$\frac{2ST}{3}$	$\frac{2ST}{3}$
$\frac{5\pi}{4}$ to $\frac{3\pi}{2}$	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	$\frac{ST}{3}$	ST
$\frac{3\pi}{2}$ to $\frac{7\pi}{4}$	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	$\frac{ST}{3}$	ST
$\frac{7\pi}{4}$ to $\frac{17\pi}{9}$	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	$\frac{2ST}{3}$	$\frac{2ST}{3}$
$\frac{17\pi}{9}$ to 2π	0	1	$\frac{A}{3}$	$\frac{A}{3}$	ST	0	ST	$\frac{ST}{3}$

Table B. Active and shoot-through pulses for a modulating cycle

Modulation Signal Region	S_{11}	S_{12}	S_{13}	S_{14}
0 to $\frac{\pi}{9}$	A+ST	A+ST	ST	0
$\frac{\pi}{9}$ to π - $\frac{\pi}{9}$	0	ST	ST	0
$\pi - \frac{\pi}{9}$ to π	A+ST	A+ST	ST	0
π to $\pi + \frac{\pi}{9}$	ST	0	A+ST	A+ST
$\pi + \frac{\pi}{9}$ to $2\pi - \frac{\pi}{9}$	ST	0	0	ST
$2\pi - \frac{\pi}{9}$ to 2π	ST	0	A+ST	A+ST

$3V_{dc}$. Similar behavior is observed in the negative half cycle. Based on this operating principle, the fundamental cycle is classified into twelve regions and the performance of each switch is determined in the given region. In Table – A, 'A/3' indicates active switching losses only in one of the modulation levels (out of three) identified as Region 1 for switch S11 in Figure 6(d). 'ST*k/N' (where k = 1,2,3 and N = 3 for seven – level qZSI) indicates shoot – through switching losses in 'k' modulation levels out of N modulation levels.

11.2. Under un-equal power distribution condition

Switching pulses for the bottom module (with PODPS-PWM) can be characterized into six regions as shown in Table B. Here, 'A' refers to active state switching; 'ST' refers to shoot – through switching; 'A + ST' refers to both active state and shoot – through state switching during the defined period.

11.3. Published Research Papers

1. **M. Meraj**, S. Rahman, A. Iqbal, and N. Al Emadi, "Novel level-shifted PWM technique for unequal and equal power-sharing in quasi z source cascaded multilevel inverter for PV systems," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.

2. **M. Meraj**, S. Rahman, A. Iqbal, and L. Ben-Brahim, "Common-mode voltage reduction in a single-phase quasi Z-source inverter for transformerless grid-connected solar PV applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 1352-1363, 2018.

3. **M. Meraj**, S. Rahman, A. Iqbal, L. Ben-Brahim and H. A. Abu-Rub, "Novel Level-Shifted PWM Technique for Equal Power-sharing Among Quasi-Z-Source Modules in Cascaded Multilevel Inverter," in IEEE Transactions on Power Electronics, vol. 36, no. 4, pp. 4766-4777, April 2021, doi, 9.1109/TPEL.2020.3018398.

4. **M. Meraj**, S. Rahman, A. Iqbal, L. Ben-Brahim, R. Alammari and H. Abu-Rub, "A hybrid active and reactive power control with Quasi Z-source inverter in single-phase grid-connected PV systems," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2994-2999.

5. **M. Meraj,** S. Rahman, A. Iqbal, L. Ben-Brahim, R. Alammari and H. Abu-Rub, Virtual Flux Oriented Sensorless Direct Power Control of QZS Inverter Connected to Grid for Solar PV Applications", IEEE Int. Conf. on Ind. Tech., ICIT, 13-15 Feb., Melbourne, Australia, pp. 1417-1423.

6. **M. Meraj,** etc., "A high efficiency and high reliability single-phase modified quasi Z-Source inverter for non-isolated grid-connected applications," IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 004305-004310.doi: 10.1109/IECON.2015.7392770.

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