ORIGINAL RESEARCH PAPER

Development of a three-phase interleaved converter based on SEPIC DC–DC converter operating in discontinuous conduction mode for ultra-fast electric vehicle charging stations

Bayan Hussein | **Nima Abdi** | **Ahmed Massoud**

Department of Electrical Engineering, Qatar University, Doha, Qatar

Correspondence
Bayan Hussein, Department of Electrical Engineering, Qatar University, Doha, Qatar.
Email: bh1602414@qu.edu.qa

Abstract

One of the main challenges that impact transportation systems electrification is their batteries' charging process. This work presents the development of a three-phase ultra-fast Electric Vehicle (EV) charger based on the SEPIC converter. Since SEPIC operating in Discontinuous Conduction Mode (DCM) is usually recommended for low-power applications, this work proposes a scheme for its employment in high-power EV chargers. This is achieved through three single-phase modules of interleaved SEPIC converters. The presented scheme ensures reducing the stresses on the semiconductor devices since the power is divided over the interleaved modules. The design addresses DCM operation in terms of both capacitor voltage and inductor current (DCVM and DICM, respectively). This paper examines the analysis of the proposed converter and the small-signal modelling. Also, the converter efficiency is assessed. A Constant Current (CC) charging approach is deployed for charging the EV battery. The validation of the designs is explored through simulation results using MATLAB/Simulink platform. A 4 kW experimental prototype for the interleaved SEPIC DC–DC converter is built to verify the claimed contributions with 92% efficiency.

1 | INTRODUCTION

A noteworthy growth in transportation systems electrification was witnessed in the last decade, particularly with their positive impact on the environment since they help reduce greenhouse emissions, pollution, and global warming [1]. Nonetheless, the electric transportation sector requires battery energy storage systems that meet the energy demands of the vehicles. Besides, the charging infrastructure plays a major role in controlling the charging speed and compensating for the driving range problem [2]. Generally, Electric Vehicle (EV) chargers can be categorized into several levels, namely, level 1, level 2, and level 3. Each level has its ratings that dictate the charger location, time, and power delivered [3].

A typical EV charger architecture rectifies the grid's power through an AC–DC conversion unit and regulates the output voltage or current through a Power Factor Correction (PFC) DC–DC conversion unit. Each stage of the charger has various Power Electronic Unit (PEU) configurations. Uncontrolled rectifiers, or diode-bridges, introduce highly-distorted input current, resulting in high Total Harmonic Distortion (THD) and low input Power Factor (PF). Several techniques were proposed to correct the PF, including the utilization of active and passive PFC. DC–DC converters with continuous input current are typically used as active PFC [4]. However, for a three-phase supply to provide fast or ultra-fast charging (i.e. Extreme-Fast Charging) (UFC) capability, a single-switch DC–DC converter is not suitable to be used since it is incapable of unfolding the three line-currents [5]. Hence, the employment of multiple modules is recommended.

The UFC concept requires advanced power electronics technologies and hence is being immensely studied and researched. UFC stations have been reported in the literature to indicate a collection of EV chargers, sharing the same upstream equipment, to charge many vehicles simultaneously [6]. However, if not well-controlled, this poses a heavy load on the grid and
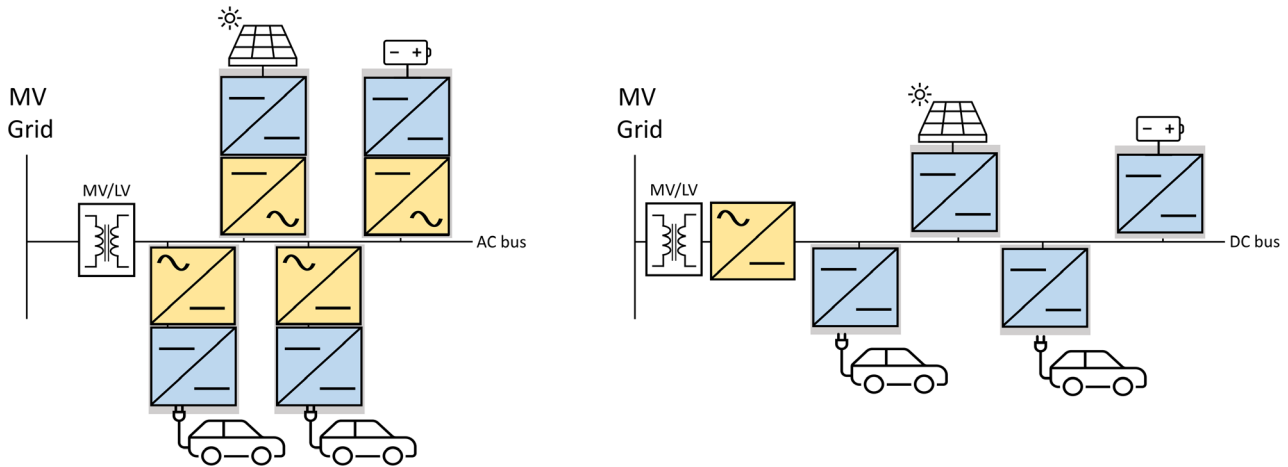
FIGURE 1 UFC Configurations: (a) AC connected systems, (b) DC connected systems

results in complications, like a transformer and feeder overloading, increasing power losses, and decreasing the power quality [7]. It also requires connecting to the Medium Voltage (MV) grid because of the UFC station's high power ratings. In [8], the inclusion of battery energy storage systems and renewable energy sources in UFC stations has been proposed to solve the aforementioned complications. In [9], coordinated planning for distribution networks and UFC stations with on-site storage has been discussed, and an optimized design for the UFC has been presented. In general. UFC stations can be AC-connected (with distributed AC–DC conversion stages) or DC-connected (with a centralized AC–DC stage between the grid and the DC bus). Typically, a step-down transformer is inserted as an interface between the MV grid and the AC or DC bus. In AC-connected systems, like Tesla supercharger station and ABB DC fast charging station, the AC bus feeds each charger separately, and each station has its AC–DC conversion unit, as shown in Figure 1(a). This approach increases the system's complexity and cost because of the increased number of conversion units. On the other hand, DC-connected systems, shown in Figure 1(b), employ one central AC–DC conversion unit following the step-down transformer. Chargers are then interfaced by connecting their DC–DC conversion units to the DC bus. DC-connected systems are advantageous in terms of straightforward control. However, their reliability is adversely affected, and they experience complications in the protection and metering systems. This becomes more complicated in bidirectional charging systems [6]. In [10] and [11], modular units of Dual-Active-Bridge (DAB) converter are utilized in the DC–DC conversion stage to achieve UFC and ensure equal power-sharing between the modules. In [12], partial power processing units are proposed for UFC. This scheme allows the realization of only a small portion of the total power, while the remaining power is fed directly to the load. Partial power processing reduces the power ratings. The size and cost of the charging units are thus reduced. However, it negatively affects the reliability and the fault ride-through capabilities of the system. Also, it does not provide isolation between EVs and the DC bus. In [13], a split storage stage is integrated within a modular scheme based on

cascaded H-bridge and isolated DC–DC converters. The proposed design has a large number of components. Since the energy storage is also integrated inside the design, the system requires large output capacitors or filters to reduce the second-order harmonic component. In [14], an AC-connected charger that feeds an ultra-capacitor bank of e-buses using a three-winding transformer between the MV grid and the converter units has been proposed.

Different power converter topologies for EV chargers have been reported in literature. Zeta, Cuk, and SEPIC, and buck-boost converters provide a single-stage single-switch topology with step-up/down capabilities [15] and behave as ideal PFC regulators when operating in Discontinuous Conduction Mode (DCM). The input current does not contain low-order harmonics; hence no bulky input filter is required [16]. Cuk-based PFC converters offer lower in-rush current, and continuous input and output currents [17]. Although Zeta-based converters provide good voltage regulation, low output ripple, and positive output voltage, they experience high voltage stresses in DCM. Soft switching is employed to reduce the stresses but at the cost of additional components [18]. In addition, Zeta and SEPIC converters offer smaller size capacitors and higher power densities than Cuk-based converters [19]. In [20], a three-phase rectifier employing a single Continuous Conduction Mode (CCM) SEPIC converter has been presented. Not only does the system employ a bulky input inductor in its design, but it also results in a THD of 26%. This is because of the single switch used for the three-phase system. Furthermore, the system lacks modularity which adversely impacts reliability. In [21], a three-phase PFC rectifier modular design has been proposed where one SEPIC module is employed in each phase, operating in CCM. The system is characterized by the need for two control loops to achieve an acceptable PFC. In [22], a CCM SEPIC converter with low reverse-recovery loss has been proposed. It employs an extra diode and uses coupled inductors to reduce the stresses on semiconductors.

DCM SEPIC converters provide straightforward control over the current ripple by the proper choice of the input inductor, in addition to the absence of a third harmonic in the input

TABLE 1 Possible DCM modes of operation of SEPIC DC–DC converter [33]

Operation mode	Features	
Discontinuous conduction mode (DCM)	• DCM-operated SEPIC has an inherent PFC property. • The inner control loop can be eliminated to simplify the control algorithm, leading to a robust and reliable system. • It can be classified based on inductor current (DICM) or capacitor voltage (DCVM).	
	Discontinuous Inductor Current Mode (DICM) • Discontinuity is defined by the non-positive current through the inductors. • Suitable for high-voltage-low-current applications. • High current peak causes high current stress on semiconductor devices, which results in high conduction losses [20]. • The control algorithm is simpler because the inner loop can be eliminated.	**Discontinuous Capacitor Voltage Mode (DCVM)** • Discontinuity is defined by the non-positive voltage across the intermediate capacitor [20]. • The intermediate capacitor value is small, and its voltage stays near zero during a switching period [24]. • Suitable for low-voltage-high-current applications. • The switch works with zero-voltage-turn-off • Low peak current, low stress on semiconductor devices, low conduction losses, and higher efficiency [25].
	DIICM – Defined by the current discontinuity in the input inductor. – Requires an additional filter at the input side to filter the harmonics at high-frequencies. – Input inductance size is significantly reduced, which results in a smaller converter size.	**DOICM** – Defined by the current discontinuity in the output inductor. – It does not require an additional filter at the input side since the large input inductance is sufficient to filter harmonics at high frequencies. – The switch works with zero-current-turn-off and zero-current-turn-on in the diode. This helps in reducing the switching losses.

current [23]. DCM operation can be categorized mainly into Discontinuous Inductor Current Mode (DICM) and Discontinuous Capacitor Voltage Mode (DCVM). The DICM operation is further classified based on the input or output inductors (DIICM or DOICM, respectively). Different modes and features are explained in Table 1. In [24], a modular three-phase PFC rectifier based on isolated DCM SEPIC is proposed. Because of the DCM operation, the design results in a reduced intermediate inductor size and a simpler control algorithm for output regulation. However, the system experiences a high peak current. It also employs large inductors on the input side for current filtering and lacks fault ride-through capabilities. In [25], the concept of interleaving is employed with the conventional DCM SEPIC converter in a single-phase design to allow coupling of input and output inductors. This design provides better system reliability but cannot handle high power due to the DCM operation. It also prevents the ride-through capabilities due to the coupling between the two interleaved levels. In [26], a unidirectional three-phase DCM SEPIC-based PFC rectifier has been proposed. The system reduces the voltage stresses on the components, but this comes at the expense of using a large number of components. Also, it does not provide isolation. The system requires an input filter that reduces harmonics at the switching frequency. In [27], a step-up DCM SEPIC-based converter has been presented with an extended number of components to create a resonant cell that allows zero-voltage-switching (ZVS). The addition of this stage increases the number of elements in the system and causes PWM control complications. In [28], a converter has been explored to enable the EV to charge from both the grid and the solar photovoltaic systems. The converter has a reduced number of components and operates in

the CCM mode, but it is designed for low powers (light EVs only). Although these converters experience a simpler control algorithm, they suffer from high current stresses [29]. In [30], a SEPIC-based PFC rectifier is used to feed a half-bridge LLC resonant filter for e-bike charging. This topology is suitable for low powers, and it employs a large number of components. In [31], bridge-less (BL) SEPIC PFC rectifiers have been proposed to reduce conduction losses, but no isolation is provided. Moreover, a bulky input inductor is required for filtering the input current harmonics, contributing to the system's size and copper losses. In Table 2, a comparative study between our proposed system and systems reported in the literature is shown.

Unlike the studies provided in [21–31], the concept of interleaving in phase-modular PFC rectifiers is not reported. In this regard, this paper presents a three-phase unidirectional EV UFC designed to operate in DCM. Since DCM operation is only suitable for low powers [32], a modular design is proposed, where isolated SEPIC DC–DC converter modules are interleaved per phase, allowing the employment of DCM operation in a high-power system. The system features can be summarized as follows:

1. Interleaving is employed, which allows the per-phase power division into several modules. It also reduces the current stresses on the semiconductor devices since the power is divided over the modules.
2. Interleaving allows the utilisation of lower-power rating semiconductor devices, which results in reducing the overall converter size.
3. Interleaving allows the SEPIC inductances of the interleaved modules to be significantly reduced, provided that they are

TABLE 2 Comparative study of the proposed converter with existing topologies

	Converter in [26]*	Converter in [28]	Converter in [31]	Proposed converter
Diode-bridge rectifier	2 diodes (BL)	4 diodes	0 dioes (BL)	4 diodes
Scheme	3-phase	1-phase	1-phase	3-phase
Static gain	$\dfrac{D}{2}\sqrt{\dfrac{3V_o^2(L_{ia}+L_{oa1})}{PL_{ia}L_{oa1}f_s}}$	–	$\dfrac{D}{\sqrt{\dfrac{2f_sP(L_1+L_2)}{V_o^2}}}$	$D\sqrt{\dfrac{3V_o^2(L_f+L_2)}{4Pf_sL_fL_2}}$
Voltage stress on switch	$\dfrac{V_o}{2}+V_s$	V_s+V_o	–	V_o+V_s
Voltage stress on diodes	$\dfrac{V_o}{2}+V_s$	V_s	–	V_o+V_s
Current stress on switch	$\dfrac{DV_s}{L_{ia}L_{oa1}f_s}\sqrt{\dfrac{D}{12}}$	–	–	$\dfrac{DV_s(L_f+L_{2N})}{NL_fL_{2N}f_s}$
Number of switches	6	3	2	3N
Number of didoes	6	2	2	3N
Number of transformers	0	1	2	3N
Number of inductors	9	1	1	6
Number of capacitors	8	3	3	3 (2N + 1)
Galvanic isolation	No	Yes	Yes	Yes
Current snsors/Voltage sensors	0/1	1/1	1/1	0/1
Efficiency	95.85%	91.7%	–	92%

*Converter in [26] is chosen as the 2S-bridgeless version.

magnetically coupled, yet affecting the fault ride-through capabilities.

4. In DCM, a single-loop control is sufficient for regulating the output current, whereas the inner loop is eliminated, and the input current is naturally in phase with the input voltage. In terms of conversion stages, the presented design is a single-switch single-stage converter per module.

5. The DCM operation allows eliminating the diodes reverse recovery loss and turn-on switching loss due to zero-current-switching.

6. The proposed isolated SEPIC-based converter is a phase-modular design where the output side is connected in parallel. Galvanic isolation is provided through a high-frequency transformer.

7. The cost of the semiconductor devices is reduced as relatively lower-rating switches, and diodes are employed. However, this reduction is offset by employing multiple interleaved modules, so the overall cost experiences insignificant change.

Consequently, the main contribution of this paper is to introduce the concept of interleaved converters in DCM operation for UFC EV chargers to achieve higher power ratings and higher efficiencies. Our work includes the small-signal modelling of the proposed interleaved isolated SEPIC-based converter, the control method, power loss analysis and fault-ride through capabilities testing, and a comparison between DICM and DCVM modes of SEPIC converter operation. This can be summarised as follows:

• Development of an interleaved phase-modular topology based on isolated SEPIC DC–DC converter for EV UFC

with its feedback control using Constant Current (CC) charging method.

• Enabling the elimination of diodes reverse recovery loss and MOSFETs' turn-on switching loss due to zero-current-switching. This further increases the converter's efficiency.

• Conducting a power loss analysis breakdown for efficiency evaluation of the proposed system.

• Enabling ultra-fast charging capabilities through interleaved modules.

2 | DESIGN AND ANALYSIS OF THE PROPOSED SYSTEM

2.1 | Proposed system

A unidirectional converter is employed in the proposed system using a full diode-bridge in the converter's first stage. As for the second stage, the basic SEPIC DC–DC converter is made into an isolated and interleaved version, as in Figure 2. DCM operation includes both DICM and DCVM. DICM is considered in the output inductance (the HFT's magnetizing inductance) while maintaining constant current on the battery side. DCVM operation is considered in SEPIC's intermediate capacitor. DCVM operation has been reported in [34] and [35], where a comparison between DCVM and DICM modes in the SEPIC-based converter has concluded that the DCVM operation is not recommended for high-power systems due to the higher voltage stress on the switch.

Interleaving is employed to allow DCM operation for low-power modules that can be aggregated and connected in parallel to handle higher power per phase. The proposed system has its
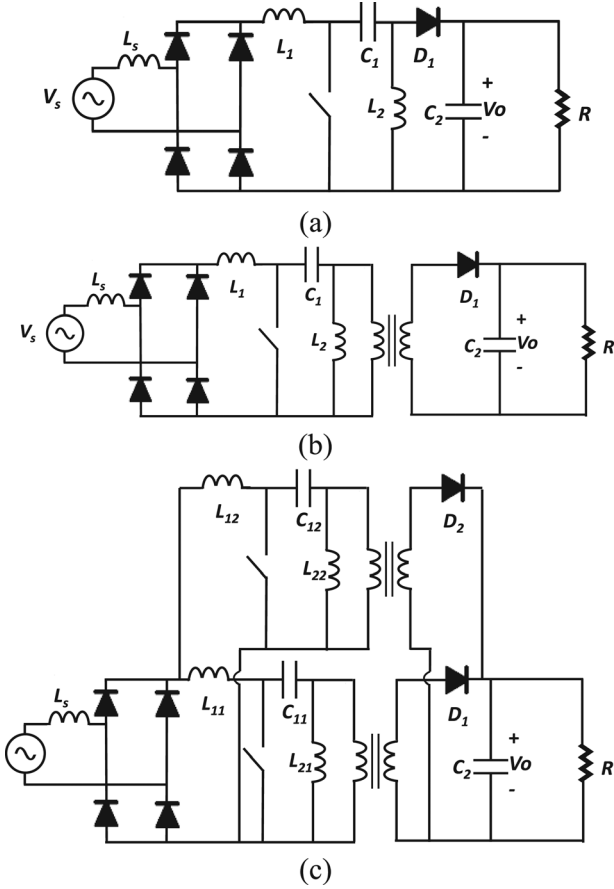
FIGURE 2 SEPIC DC–DC converter. (a) Basic SEPIC PFC converter, (b) isolated SEPIC PFC converter, (c) interleaved and isolated SEPIC PFC converter

FIGURE 3 Block diagram of phase-modular interleaved isolated SEPIC DC–DC converter

output from each phase connected in parallel, as shown in the system in Figure 3. The parallel connection at the output side requires isolation between the input and output sides, which can be achieved through HFTs.

2.2 | Closed-loop control

The block diagram of the closed-loop control of the overall converter using the Constant Current (CC) charging approach is shown in Figure 4, where a constant current is supplied to the EV battery. Only one control loop is sufficient for DCM operation, as shown in Figure 4, because SEPIC in DCM behaves as a resistive load, as will be mathematically proved based on the analysis in [23]. This concept still holds even when SEPIC modules are interleaved since they will act as parallel resistive loads.

2.3 | Mathematical analysis

This section presents the analysis of the interleaved phase-modular design shown in Figures 3 and 4. The analysis is for the DCM operation of the output inductor L_2 (DOICM). The
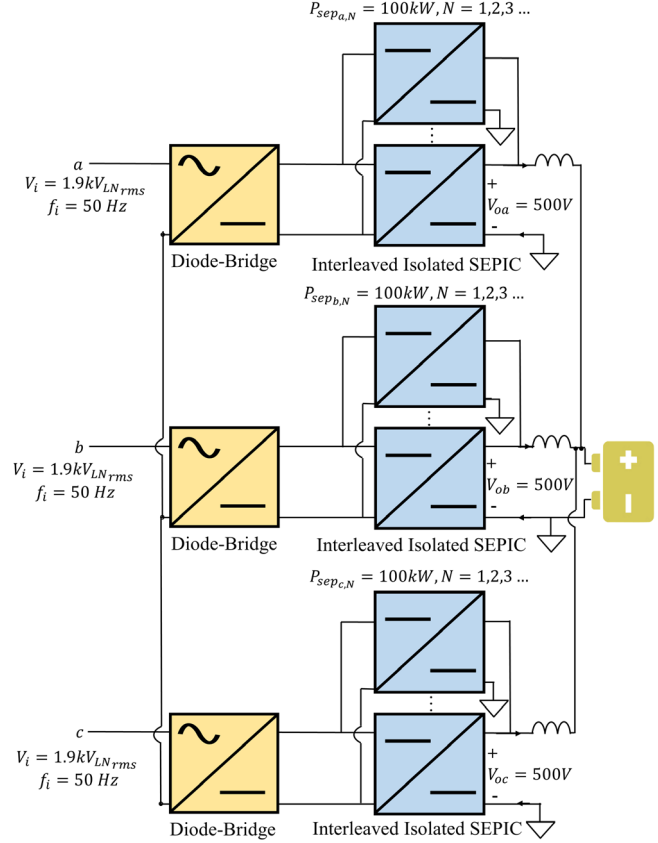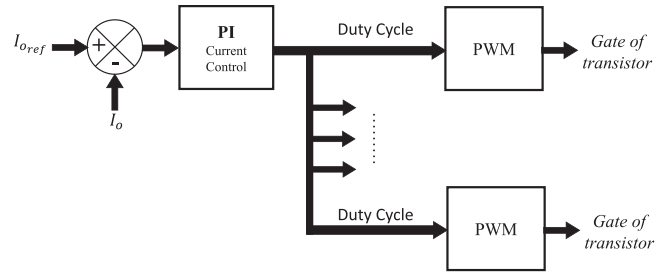

FIGURE 4 Block diagram of the closed-loop controller for DCM mode (employing CC charging approach)

following assumptions are made [23,33], where N refers to the number of modules in the interleaved converter within a single phase:

1. To maintain symmetry between all the modules in the three phases, all parameters are assumed equal.
2. To ensure operating in DOICM, the output inductance (magnetizing inductance of the HFT) should be smaller than the input inductance [33].
3. Theoretically, each intermediate capacitor's voltage is equal to the rectified phase-voltage, and it is constant during a switching cycle, whereas the output capacitor's voltage is
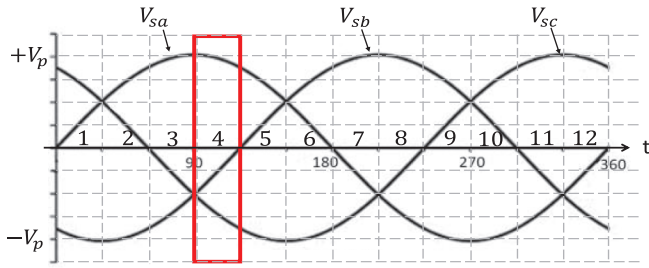
FIGURE 5 Three-phase input voltage

constant and equal to the output load voltage [33].

$$L_{1aN} = L_{1bN} = L_{1cN} = L_{1N} \text{ for } N = 1, 2, 3, ...$$

$$L_{2aN} = L_{2bN} = L_{2cN} = L_{2N} \text{ for } N = 1, 2, 3, ...$$

$$C_{1aN} = C_{1bN} = C_{1cN} = C_{1N} \text{ for } N = 1, 2, 3, ...$$

$$C_{2a} = C_{2b} = C_{2c} = C_2 \tag{1}$$

$$L_{1kN} \gg L_{2kN} \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{2}$$

$$v_{C_1kN} = |v_{sk}| \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{3}$$

$$v_{C_2k} = |V_{ok}| \text{ for } k = a, b, c \tag{4}$$

The analysis is carried out for one sector (sector 4) of the 12 sectors of the three-phase sinusoidal input voltages, shown in Figure 5. In this sector,

$$\begin{aligned} v_{sa} > 0, \ v_{sb} < 0, \ v_{sc} < 0 \\ |v_{sa}| > |v_{sc}| > |v_{sb}| \end{aligned} \tag{5}$$

Figure 6 illustrates the equivalent circuit referred to the primary side of the HFT by the transformer's turns ratio $n \, (= V_s/V_p)$. Using KCL, the output current is expressed as follows

$$i'_{oa} + i'_{ob} + i'_{oc} = i'_o = n i_o$$

$$\text{where } i'_{ok} = \sum_{i=1}^{N} i'_{oki}, k = a, b, c \tag{6}$$

The converter undergoes five modes periodically based on the pulse applied to the switch:

Mode 1: this mode is dictated by the ON time of the PWM signal applied to the semiconductor device. Before this stage, freewheeling input current stored in the input inductor circulates, and it is represented by i_{fwkN} for $k = a, b, c \ \& \ N = 1, 2, 3, ...$ The freewheeling current is positive in (7) because it is in the same direction as the current in L_f, and negative in (8) because it is opposite in direction to the current in L_2 [34]. In this mode, the inductors' currents can be mathematically expressed using KVL in Figure 7 as
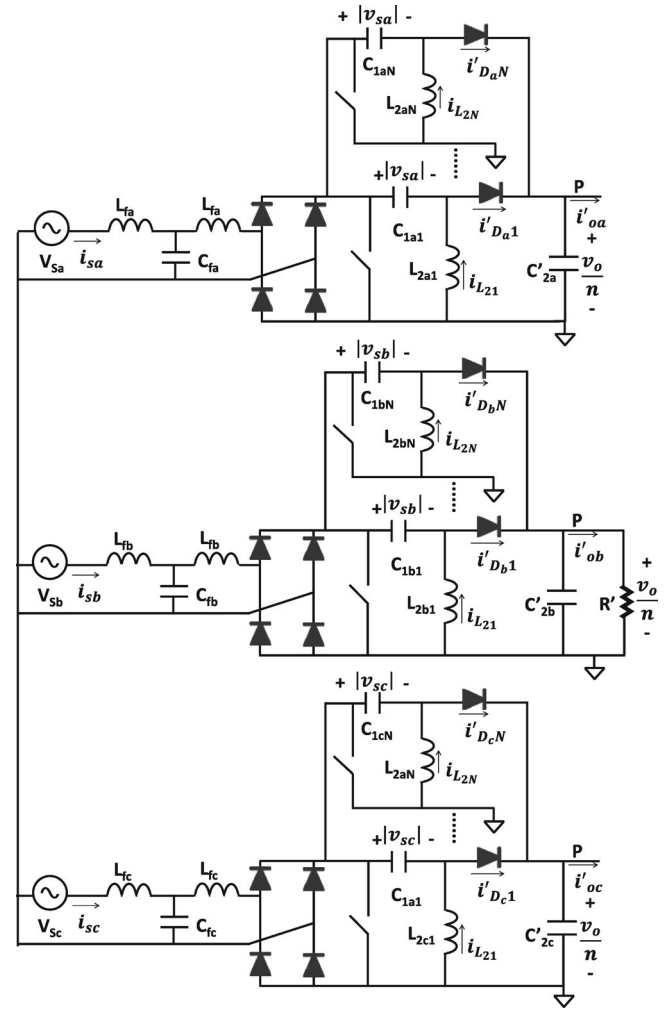

FIGURE 6 Circuit referred to primary

$$i_{s_k} = i_{fwkN} + \frac{v_{sk}}{L_f} t \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{7}$$

$$i_{L2N} = -i_{fwkN} + \frac{|v_{sk}|}{L_{2N}} t \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{8}$$

Mode 2: when gate signals become zero, the switches and diodes in all phases are OFF and ON, respectively. This signals the start of Mode 2. Using the equivalent circuit of this mode and applying KCL in Figure 8, the inductors' current can be expressed as

$$i_{s_k} = i_{fwkN} + \frac{v_{sk}}{L_f} dT_s - \frac{v_o}{nL_f} t$$

$$\text{for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{9}$$

$$i_{L2N} = -i_{fwkN} + \frac{|v_{sk}|}{L_2} dT_s - \frac{v_o}{nL_{2N}} t$$

$$\text{for } k = a, b, c \ \& \ N = 1, 2, 3, ... \tag{10}$$

The stored energy in L_{2N} is proportional to the current through L_{2N} and, accordingly, the phase voltage's magnitude,
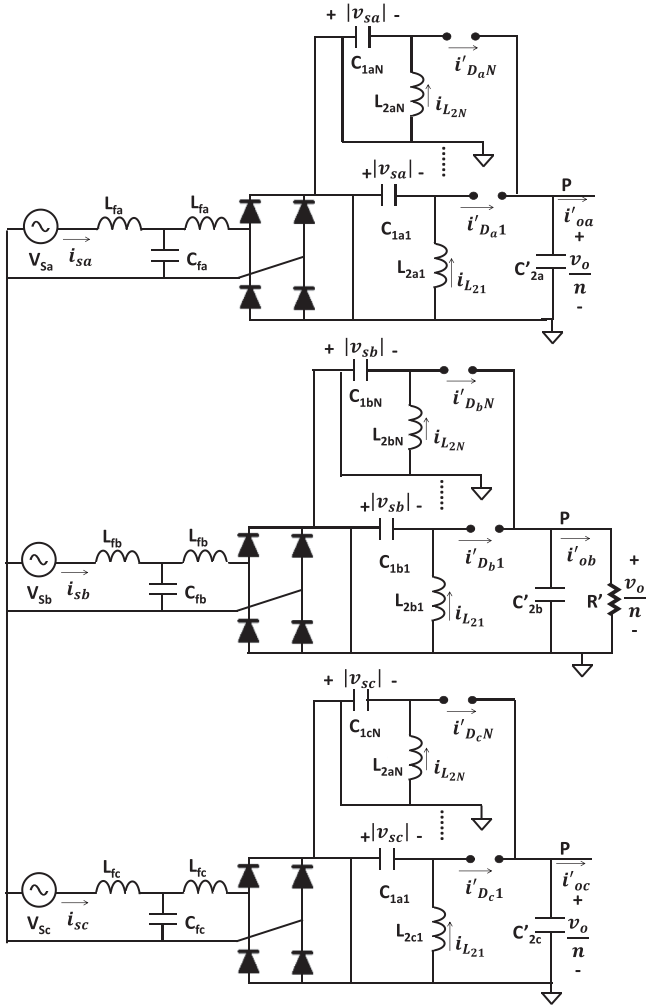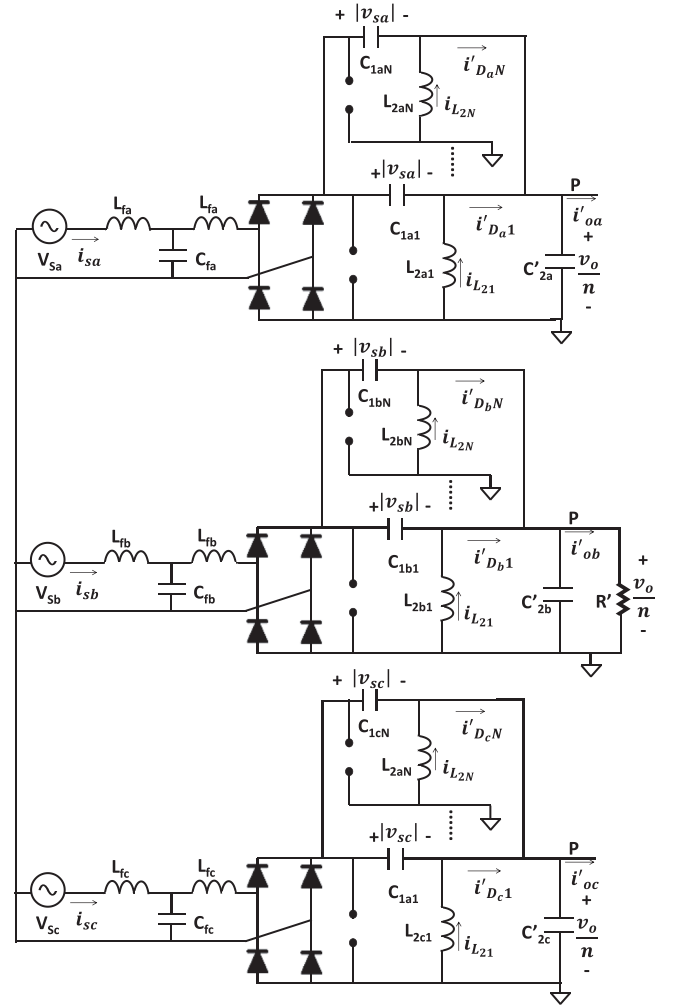
FIGURE 7 Mode 1

FIGURE 8 Mode 2

as given by (8). Hence, using (6) and (8), inductor L_{2N} in phase B has the least energy, and hence, the blocking of the diode in phase B ends this mode, which implies

$$i'_{Db} = 0 \rightarrow i_{L_fb} = -i_{L2bN} \text{ for } N = 1, 2, 3 \dots \quad (11)$$

Hence, the duration of Mode 2 is dictated by the diode ON time in phase B. To calculate the ON time of the diode by (9), (10), and (11):

$$t_{DbN_{ON}} = \frac{|v_{sb}|}{v_o} n d T_s = d_1 T_s \quad (12)$$

Mode 3: this mode starts when the diode is blocked in phase B and lasts till the diode in phase C is blocked, as in Figure 9. The duration of this mode is dictated by the ON time of the diode in phase C.

$$i'_{Dc} = 0 \rightarrow i_{L_fb} = -i_{L2cN} \text{ for } N = 1, 2, 3 \dots \quad (13)$$

Hence

$$t_{DcN_{ON}} = \frac{|v_{sc}|}{v_o} n d T_s = d_2 T_s \quad (14)$$

Mode 4: like Mode 3, this mode starts when the diode is blocked in phase C and remains until the diode in phase A is blocked. The equivalent circuit of this mode is shown in Figure 10. A general expression can be deduced using (12), (14), and (16), which shows that theoretically, the ON duration is the same for all modules in all phases and is given as

$$t_{DkN_{ON}} = \frac{|v_{sk}|}{v_o} n d T_s = d_i T_s \quad (15)$$

where $i = 1 \text{ for } k = b, i = 2 \text{ for } k = c, i = 3 \text{ for } k = a$.

Mode 5: all switches and diodes are OFF, as in Figure 11. Due to the large input inductances L_s, or L_{1N}, this mode is essentially the mode where the freewheeling currents circulate till the next switching period. The duration of this period can be calculated by

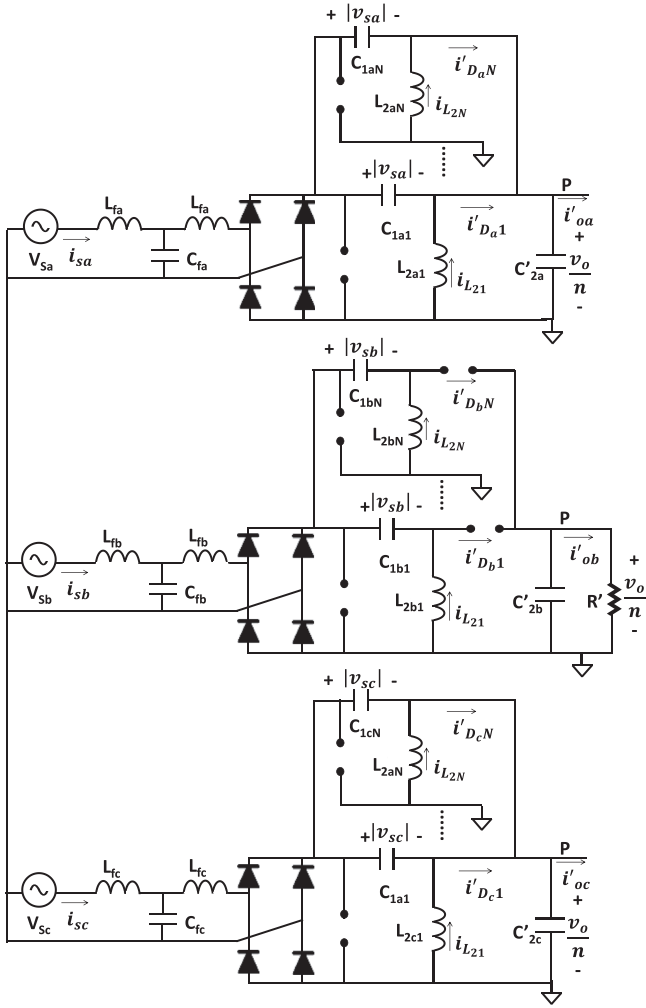$$d_4 T_s = \left(1 - d - \sum_{i=1}^{3} d_i\right) T_s \quad (16)$$
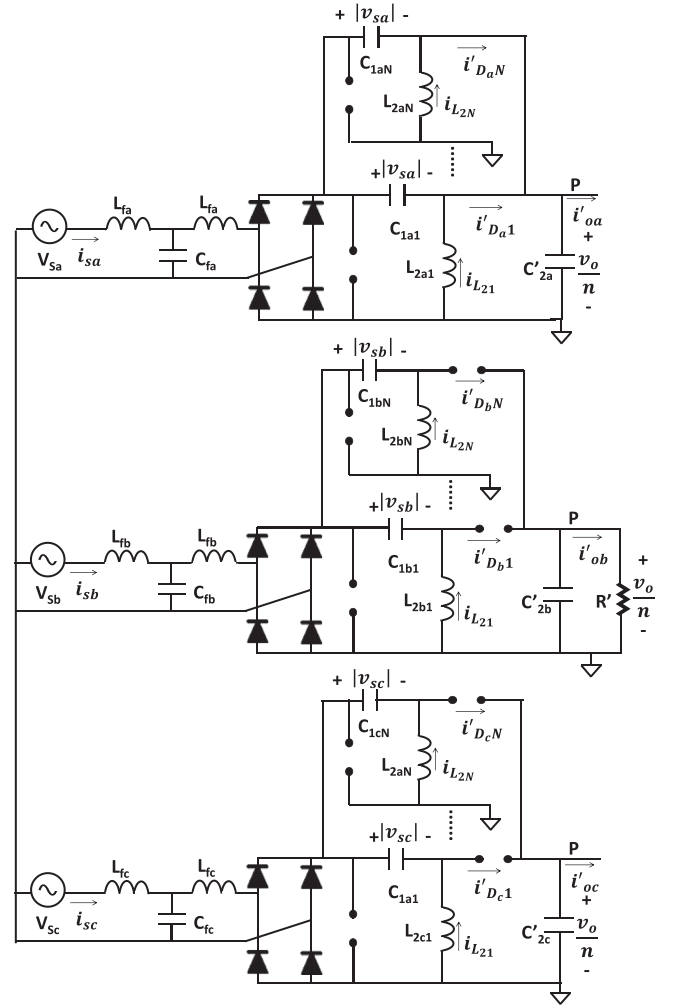
FIGURE 9 Mode 3

FIGURE 10 Mode 4

2.3.1 | Average output current

From the schematic of Figure 6 and using KCL, the average diode current in each module is equal to the average output current from the same module, that is

$$I'_{DkN} = I'_{okN} \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, \dots \quad (17)$$

Also, the peak diode current is equal to the peak output current of each module of the interleaved converter in each phase. The peak of the diode current happens at $t = dT_s$. By (7) and (17),

$$i'_{DkN_{pk}} = \frac{v_{sk}}{L_{eqN}} dT_s \text{ for } k = a, b, c \ \& \ N = 1, 2, 3, \dots \quad (18)$$

where L_{eqN} is the equivalent inductance in each module of the interleaved converter, and is given by

$$L_{eqN} = \frac{L_f L_{2N}}{L_f + L_{2N}} \quad \text{for } N = 1, 2, 3, \dots \quad (19)$$

Then, the average diode current is

$$I'_{DkN} = I'_{okN} = \frac{i'_{DkN_{pk}} t_{DkN_{ON}}}{2T_s} \text{ for } k = a, b, c \quad (20)$$

Using (15), (18), and (20)

$$I'_{DkN} = I'_{okN} = \frac{v_{sk}^2 d^2 T_s n}{2v_o L_{eqN}}$$

$$\text{for } k = a, b, c \ \& \ N = 1, 2, 3, \dots \quad (21)$$

Referring back to the secondary side of the transformer,

$$I_{okN} = \frac{v_{sk}^2 d^2 T_s}{2v_o L_{eqN}} \quad \text{for } k = a, b, c \ \& \ N = 1, 2, 3, \dots \quad (22)$$

The total output current through the load is the summation of all phase output currents by (6) and (22)

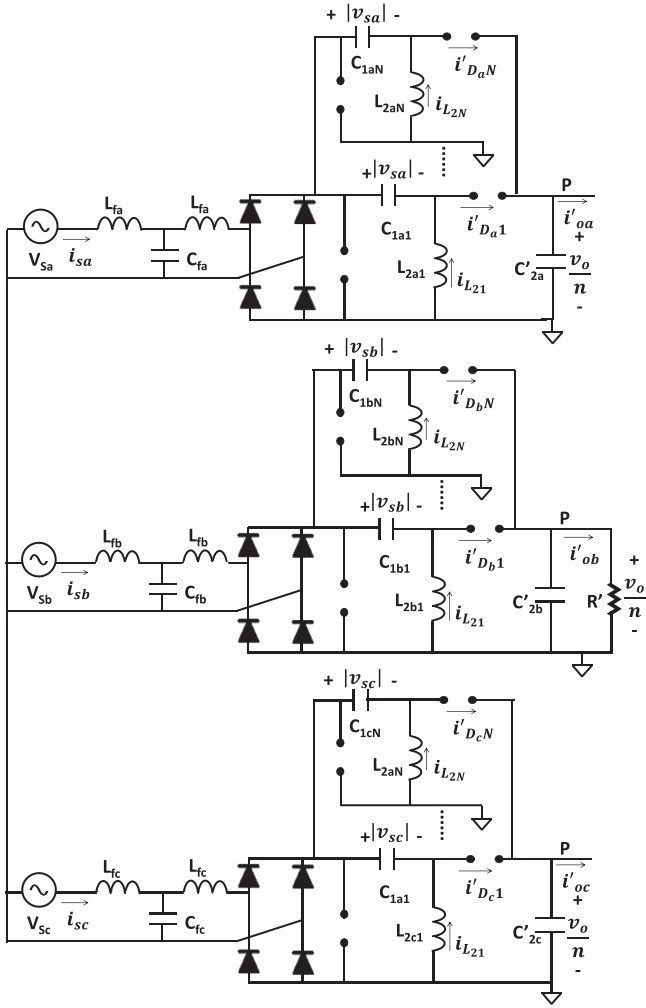$$I_o = \frac{N d^2 T_s}{2v_o L_{eqN}} \left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2 \right) \quad (23)$$

FIGURE 11 Mode 5

For $v_{sa} = V_p \sin(\omega t)$, $v_{sb} = V_p \sin(\omega t - \frac{2\pi}{3})$, $v_{sc} = V_p \sin(\omega t + \frac{2\pi}{3})$

$$\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right) = \frac{3}{2}V_p^2 \tag{24}$$

Using (22) and (24),

$$I_o = \frac{3NV_p^2 d^2 T_s}{4v_o L_{eqN}} \tag{25}$$

The average output current is then calculated over a line period by integrating the instantaneous average output current for sector 4, that is

$$I_o = \frac{\pi}{6} \int_{\pi/3}^{\pi/2} i_o(t) \, d(\omega t) = \frac{3NV_p^2 d^2 T_s}{4v_o L_{eqN}} \tag{26}$$

2.3.2 | Input current

For the proposed system, each single-phase module can be analysed separately for a balanced system. Assuming a lossless sys-

tem, the input power of one module in one phase is equal to the output power delivered by that module, that is

$$v_{sk} i_{skN} = v_o I_{okN} \tag{27}$$

By (22) and (27), and for $v_{sk} = V_p \sin(\omega t)$, the input current is given by

$$i_{skN} = \frac{v_{sk} d^2 T_s}{2 L_{eqN}} \tag{28}$$

$$i_{sk} = \frac{V_p d^2 T_s}{2 L_{eqN}} \sin(\omega t) = I_{Npk} \sin(\omega t) \tag{29}$$

where the peak of each module of each phase

$$I_{Npk} = \frac{V_p d^2 T_s}{2 L_{eqN}} \text{ for } N = 1, 2, 3 \dots \tag{30}$$

The peak of the total input current to phase k is then given by

$$I_{pk} = \sum_{i=1}^{N} I_{ipk} \tag{31}$$

By (29), the unity PF of SEPIC PFC is illustrated as the phase current, with a peak value I_{Npk}, is in-phase with the phase input voltage, for $k = a, b, c$. The input inductances filter the high-order harmonics, ensuring low THD.

2.3.3 | DCM operation

In sector 4, phases B and C essentially operate in DCM if phase A operates in DCM. To ensure DCM operation, the following conditions should hold

$$t_{N,ON} + t_{DaN\,ON} < T_s \tag{32}$$

By (16) and (32),

$$d\left(1 + \frac{V_p \sin(\omega t)}{v_o} n\right) < 1 \tag{33}$$

Let $M = \frac{v_o}{V_p}$ and for worst-case at $\omega t = 90^0$, Equation (33) is simplified to

$$d < \frac{M}{M + n} \tag{34}$$

The average output current is given by

$$I_o = \frac{v_o}{R} \tag{35}$$

From (26) and (35):
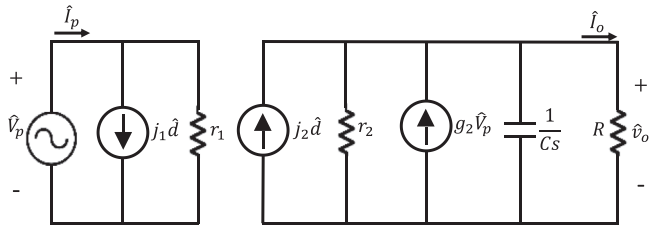
$$d = M\sqrt{\frac{2}{3}k_{aN}} \tag{36}$$

FIGURE 12   The small-signal model of one module of each phase of the overall system

where the conduction parameter k_a is given by

$$k_{aN} = \frac{2L_{eqN}}{RT_s} \tag{37}$$

Using (34) and (36), the critical value of phase A to ensure DCM

$$k_{a,Ncrt} = \frac{3}{2} \frac{1}{(M+n)^2} \tag{38}$$

2.3.4 | Inductors design

The value of inductors L_f is obtained depending on the anticipated ripple in the input current. The input current and its ripple are given by

$$\Delta i_{sN} = \frac{v_s}{L_f} dT_s \text{ where } i_{sN} = \frac{i_s}{N} \tag{39}$$

Using (39), the maximum ripple in the current happens when the voltage is at its maximum, and the inductor value can be calculated as

$$L_f = \frac{V_p dT_s}{\Delta i_{sN}} \tag{40}$$

The value of the inductance L_{2N} can then be calculated by (19) and (40) as

$$L_{2N} = \frac{L_f L_{eqN}}{L_f - L_{eqN}} \tag{41}$$

By (37),

$$L_{eqN} = \frac{RT_s k_{aN}}{2} \tag{42}$$

2.3.5 | Intermediate capacitor design

The value of the intermediate capacitor should satisfy two conditions: (1) should maintain a constant capacitor voltage in the switching period (2) should follow the input voltage in the line period. Also, the resonance frequency occurring due to C_{1N}, L_{1N}, L_{2N} should be considered to avoid oscillatory behaviour at every half cycle of the input current [33]. The resonant frequency should be between the line frequency and the switching frequency, that is

$$\omega_i < \omega_r < \omega_s \tag{43}$$

TABLE 3   Design parameters of simulation models

Stage	Parameter	DOICM	DCVM
Filtering	LCL	$L_f = 300uH, C_f = 10uF$	
	L_o (mH)	7	
	C_2 (mF)	4	
Input supply	V_{in} (kV$_{LN}$)	1.9	
	f (Hz)	50	
SEPIC	V_o (V)	500	
	f_{sw} (kHz)	40	
	L_2 (uH)	7.5	500
	C_1 (nF)	760	17.5
Load	I_o (A/phase)	400	

Hence, the capacitance value is

$$C_{1N} = \frac{1}{\omega_r^2 \left(L_f + L_{2N} \right)} \text{ for } N = 1, 2, 3, ... \tag{44}$$

2.3.6 | Small-signal modelling of the converter

Using the Current-Injected Equivalent Circuit Approach (CIECA) [36], the small-signal model is obtained. CIECA allows the linearization of the circuit by injecting the output current produced by the non-linear part. This is done by adding the small-signal perturbation to the input currents and voltages, output currents and voltages, and the duty cycle. Using (27), (28), (31), and small-signal approximation (perturbation is symbolized by ^), the small-signal model of one module in Figure 12 is given by

$$\hat{I}_o = j_2\hat{d} + g_2\hat{V}_p - \frac{1}{r_2}\hat{v}_o \tag{45}$$

$$\hat{I}_{pk} = j_1\hat{d} + \frac{1}{r_1}\hat{V}_p \tag{46}$$

where

$$j_2 = \frac{3V_p^2 dT_s}{2L_{eq}v_o}, \quad g_2 = \frac{3V_p d^2 T_s}{2L_{eq}v_o}, \quad r_2 = \frac{v_o}{I_o}, \quad j_1 = \frac{V_p dT_s}{L_{eq}}, \quad r_1 = \frac{2L_{eq}}{d^2 T_s}$$

Considering a CC charging approach, the output-to-control and the output-to-input transfer functions can be derived from (45) and (46) and expressed as

$$\frac{\hat{I}_o}{\hat{d}} = \frac{2K_1 V_p}{1 + \frac{RK_1 V_p d}{v_o} + sRC} \tag{47}$$

$$\frac{\hat{I}_o}{\hat{v}_p} = \frac{2K_1 d}{1 + \frac{RK_1 V_p d}{v_o} + sRC} \tag{48}$$
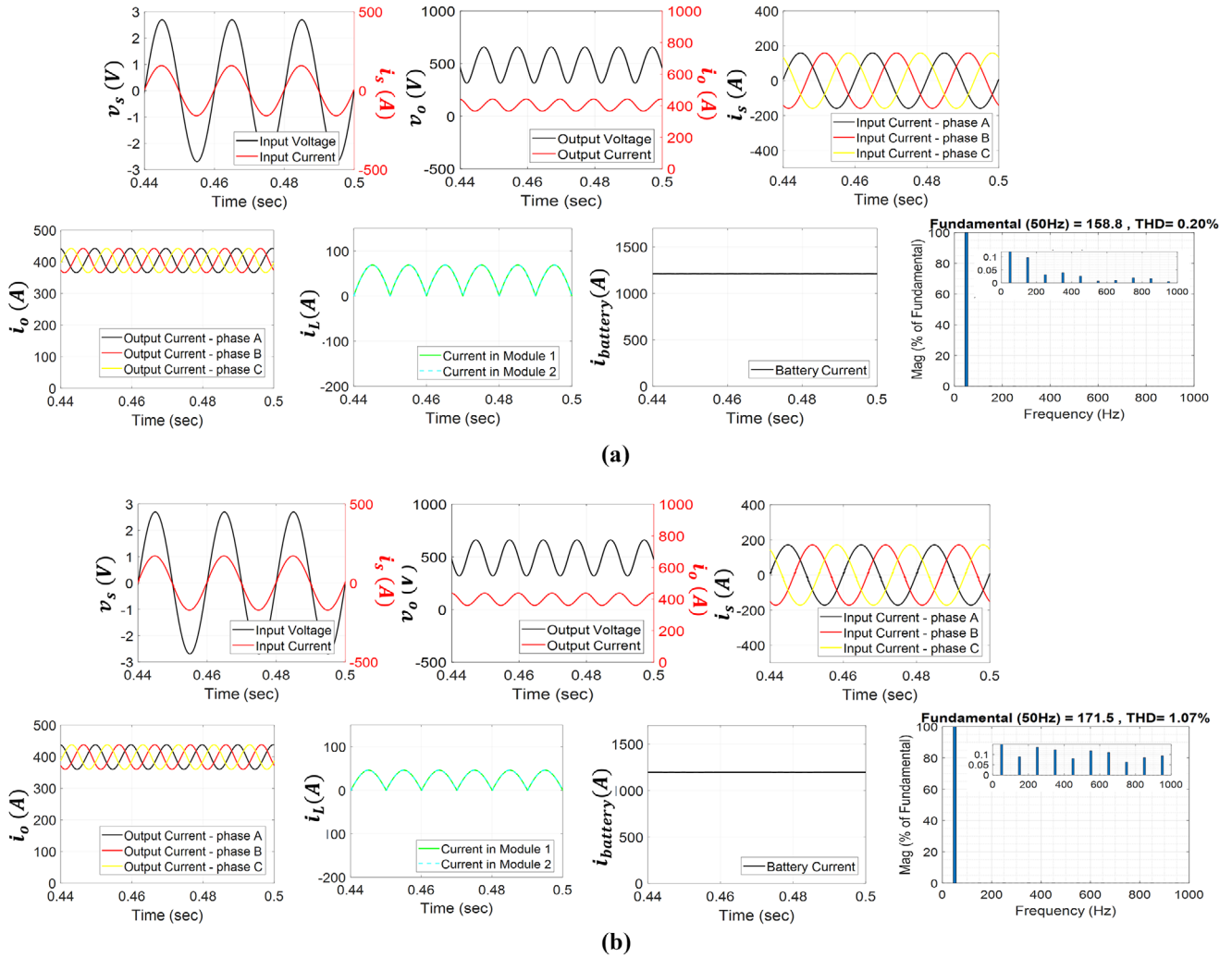
where

$$K_1 = \frac{3V_p dT_s}{4v_o L_{eq}} \tag{49}$$

FIGURE 13 Simulation results for battery load. (a) DOICM mode, (b) DCVM mode

TABLE 4 Component specification

Component	Specification
Diode-bridge rectifier	M50100SB1600 (1600V / 100A)
Power switches	SCT3030AL (1200V / 95A)
Intermediate inductor	120uH / 20A / 1.5 mm Cu / Air Core
SEPIC capacitors	1uF / 900V
SEPIC diode	3D050A120 (1200V / 50A)
Output capacitor	1mF / 450V
Input LCL filter	600uH / 20A / 1.5 mm Cu / Air Core
	C: 20uF / 420V
DSP	TI C2000 processor

TABLE 5 Parameters of experimental prototype

Stage	Parameter	1-module	2-module
Filtering	LCL	L_f = 600uH, C_f = 20uF	
	C_2 (mF)	1	
Input supply	V_{in} (V_{LN})	240	
	f (Hz)	50	
SEPIC	V_o (V)	234	240
	f_{sw} (kHz)	40	
	Duty cycle	0.3	
	Turns ratio	1	
	L_2 (uH)	120	
	C_1 (uF)	1	
Load	R (Ohms)	55	

3 | RESULTS AND DISCUSSION

The validation of the concept for fast charging at 10C was conducted by modelling the proposed system in MAT-LAB/Simulink using a 500 V battery with a 60 kWh capacity. The methodology followed was by first designing a 200 kW single-phase two-module interleaved SEPIC DC–DC converter, where each module carries a power of 100 kW. Then by using a three-phase supply, Y-connection on the input side, and parallel connection in the output side, the three-phase inter-
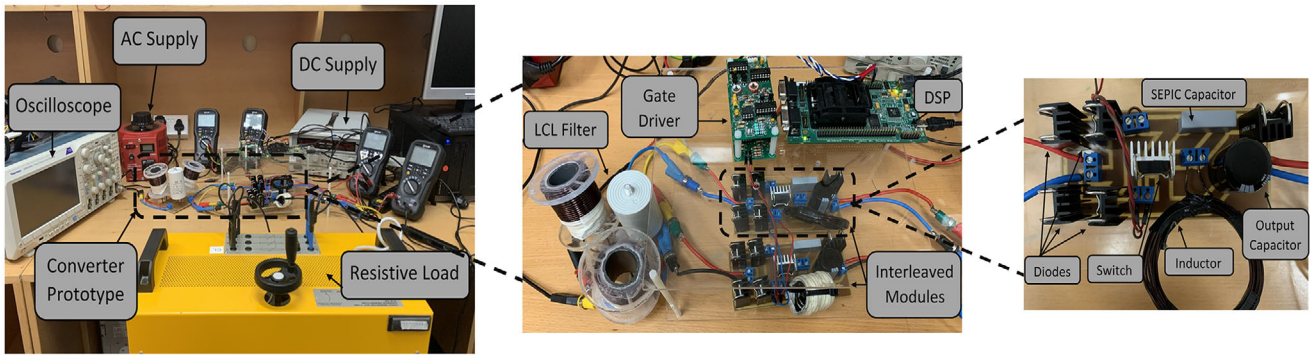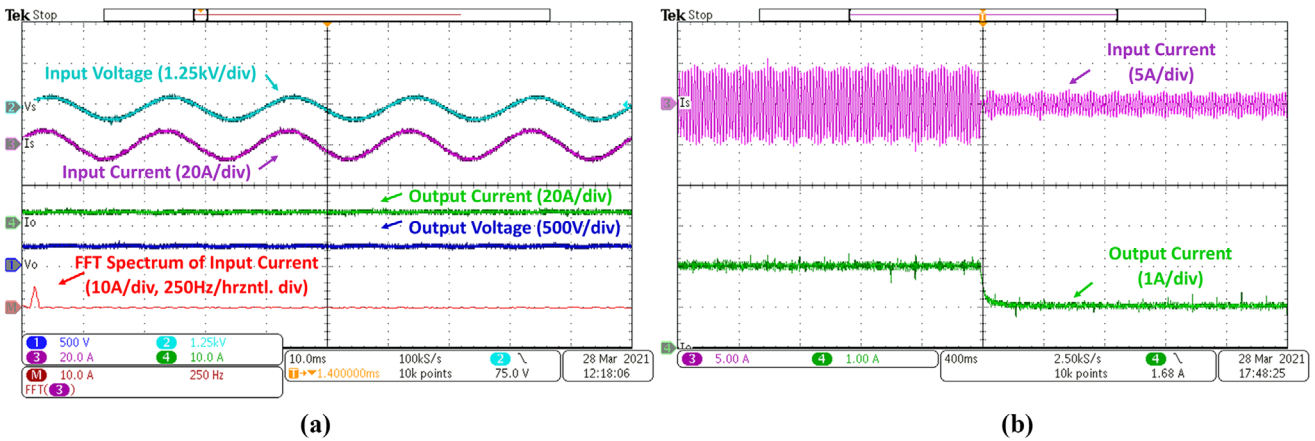
FIGURE 14 Experimental prototype setup

FIGURE 15 Experimental results of closed-loop operation: (a) I_o regulated 4 A, (b) step change from 2 to 1 A

leaved phase-modular isolated SEPIC-based off-board ultra-fast charger was simulated. Both DICM and DCVM modes of operation of the SEPIC converter were considered. The output inductance, L_o, was chosen based on a trade-off since it is inversely proportional to the ripple content of the output current and the THD of the input current and directly proportional to the converter's overall size. As for the value of C_2, it should be carefully chosen since with the reduction of C_2, the converter's

size is reduced, the lifetime is extended, and the high-ripple content tolerance increases.

3.1 | Simulation and experimental results

The simulation parameters are shown in Table 3 for DOICM and DCVM operations. The proposed interleaved phase-modular simulation results with a 500 V battery are shown in
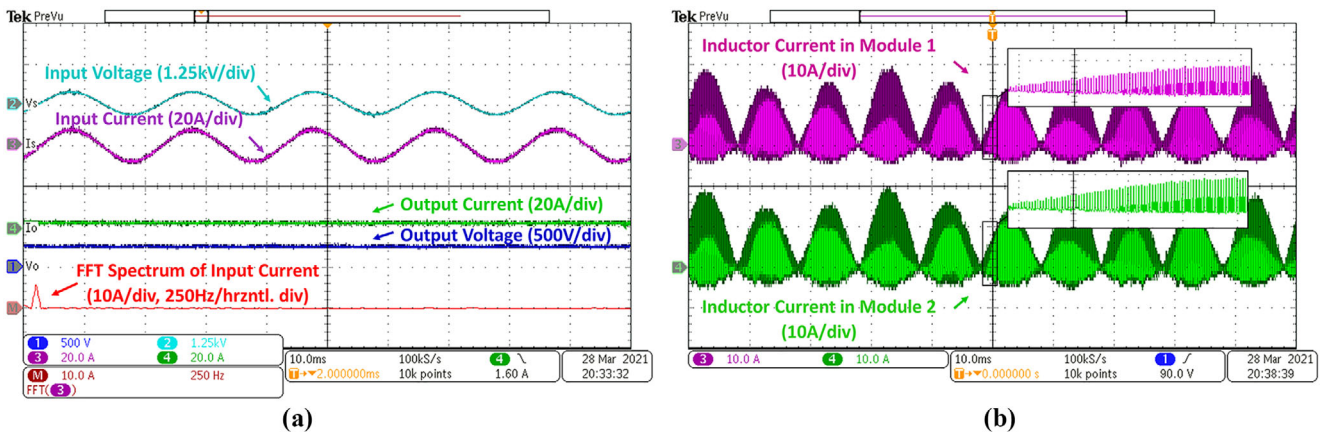

FIGURE 16 Experimental results of two interleaved modules: (a) input and output parameters, (b) inductor currents
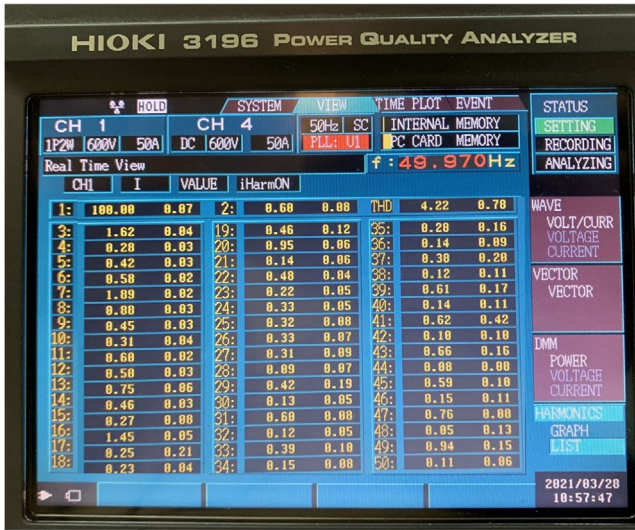
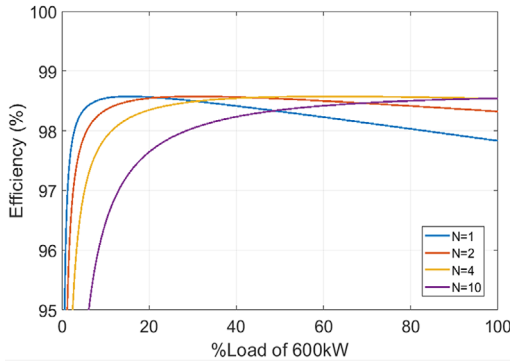**FIGURE 17** Harmonic profile on HIOKI 3196 PQ Analyzer

FIGURE 18 Performance assessment of the interleaved phase-modular system

Figure 13 for DOICM and DCVM operations, respectively. The steady-state results show that the charger absorbs a sinusoidal input current in phase with the input voltage, where the THD is 0.2% in DOICM and 1.07% in DCVM for the same system parameters. The modules experience power division between the phases and the inner modules, which reduces the current stresses in the MOSFET switches. From the DOCIM and DCVM simulation results in Figures 13(a) and 13(b), respectively, the input current is in phase with the input voltage in both operation modes. Moreover, the input current value for one phase is divided into the two modules of the SEPIC converter, and this is particularly clear by the current through modules waveforms. Moreover, the phase's output current is the summation of the output current from each module. The reference output current for each phase is set at 400 A, and the closed-loop control ensures high performance in tracking the reference. The output phase current has high ripple, which is the case in the SEPIC converter. This current ripple can be further reduced by increasing the size of the output filter inductor L_o. However, the ripple content is cancelled out in the total current feeding the battery, as plotted in Figure 13, with a total of

1200 A, that is

$$i_{oa}(t) = 400 + \sin(2\omega t) \tag{50}$$

$$i_{ob}(t) = 400 + \sin\left(2\omega t - \frac{2\pi}{3}\right) \tag{51}$$

$$i_{oc}(t) = 400 + \sin\left(2\omega t + \frac{2\pi}{3}\right) \tag{52}$$

Summing them all up by (6),

$$i_o(t) = 1200A \tag{53}$$

To validate the proposed system, a 4 kW single-phase two-module SEPIC-based prototype is developed with the specifications and parameters shown in Tables 4 and 5. The prototype is shown in Figure 14. A digital signal processor (DSP) is used to supply the 40 kHz gate signal to the Gate Driver Circuit, which amplifies the signal for the MOSFET in the power converter.

The results of one-module testing at a rated power of 1 kW are shown in Figure 15, where relevant voltages and currents, along with the FFT spectrum of the input current, are observed. The closed-loop operation is performed, and the results show regulated output current at 4A. To evaluate the robustness of the system, a step change is performed, where the reference of the output current is changed from 2A to 1A. Figure 15(b) shows that the PI controller successfully tracks the step change. Moreover, an interleaved two-module DCM SEPIC PFC rectifier is tested with design parameters shown in Table 5, and the results are shown in Figure 16, where the input power is split into the two modules, as evident by the inductor current waveforms. The achieved efficiency is 92%.

Furthermore, harmonic analysis is shown in Figure 17 using HIOKI PQ Analyzer, shows that the system meets the IEC61000-3-2.

3.2 | Efficiency assessment

To evaluate the system, the analysis of power loss is conducted to calculate its efficiency practically. In the proposed system, losses are mainly associated with semiconductor devices (diodes and transistors), and they mainly include switching and conduction losses [37]. In terms of the transistor, assuming Silicon Carbide (SiC) MOSFETs, the resistive element results in some power loss. In the diodes, the voltage drop across the device results in some more power loss. Considering both types of losses, the performance of the interleaved phase-modular system has been studied. A curve is obtained for different cases of interleaved modules per phase, N, in Figure 18. The efficiency has a flattened curve and high performance (more than 98% for all cases where SEPIC modules are interleaved) due to the employment of the SiC semiconductor devices characterized by their fastness and low switching losses. The reason why the interleaved design ($N > 1$) has higher efficiency than the case
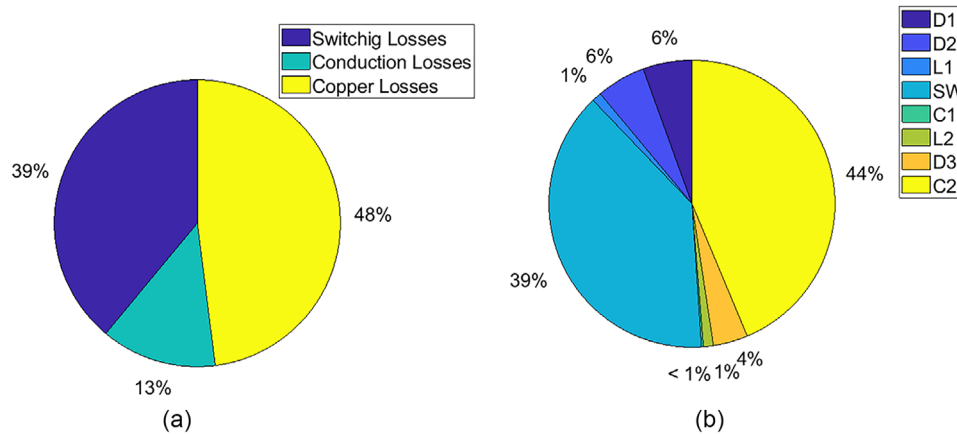
FIGURE 19 Power loss breakdown. (a) in terms of categories, (b) in terms of elements

where $N = 1$ is that the input current is divided into N modules, resulting in lower conduction and copper losses. Moreover, a more detailed analysis for power loss distribution was conducted for the proposed system to breakdown the losses into three categories that are: switching losses of MOSFET switches, conduction losses of both diodes and MOSFET switches, and copper losses, considering the parasitic elements of the passive components used in the converter. The power loss distribution in terms of the loss type is shown in Figure 19(a), whereas the power loss according to the elements in the circuit [38] was also conducted and is shown in Figure 19(b). The pie chart shows that switching and copper losses contribute more to the total power loss than conduction losses. This is also reflected in the second pie chart, where the losses in the switch SW contribute to 39% of the total power loss. In the practical work, an efficiency of 92% is achieved.

4 | CONCLUSION

This paper proposes an ultra-fast charger for EVs. The design consists of three single-phase two-module interleaved isolated SEPIC-based converters where their output is connected in parallel. The three main features of this design are modularity, fault ride-through capabilities, and redundancy, which all contribute to increasing the system's reliability. The simulation was carried out for a two-module interleaved system in MAT-LAB/Simulink, and the results show a unity PF in both DOICM and DCVM modes and an input current THD of 0.2% and 1.07%, respectively, for the same system parameters. Moreover, a single-phase 4 kW experimental lab prototype consisting of two interleaved SEPIC modules operating in DOICM was tested, and the results show an almost unity PF and a THD of 4.22%. Efficiency assessment and power loss analysis were conducted to evaluate the system, both theoretically and practically.

Improvements can be added to the design by further increasing the number of interleaved modules to reduce the converter's size by reducing the size of the employed devices. A bridge-

less design can also be adopted to significantly reduce the conduction losses, which are the major contributor to the system's power loss.

REFERENCES

1. Almutairi, A., Alyami, S.: Load profile modeling of plug-in electric vehicles: Realistic and ready-to-use benchmark test data. IEEE Access 9, 59637–59648 (2021)
2. Cano, Z.P., et al.: Batteries and fuel cells for emerging electric vehicle markets. Nat. Energy 3(4), 279–289 (2018)
3. Khaligh, A., Dantonio, M.: Global trends in high-power on-board chargers for electric vehicles. IEEE Trans. Veh. Technol. 68(4), 3306–3324 (2019)
4. Mohammed, S., Jung, J.: A Comprehensive state-of-the-art review of wired/wireless charging technologies for battery electric vehicles: Classification/common topologies/future research issues. IEEE Access 9, 19572–19585 (2021)
5. Kolar, J.W., Friedli, T.: The essence of three-phase PFC rectifier systems—Part I. IEEE Trans. Power Electron. 28(1), 176–198 (2013)
6. Tu, H., et al.: Extreme fast charging of electric vehicles: a technology overview. IEEE Trans. Transp. Electrif. 5(4), 861–878 (2019)
7. Wu, Q., et al.: Impact study of electric vehicle (EV) Integration on medium voltage (MV) grids. In: Proceedings of the 2nd IEEE PES International Conference and Exhibition on Innovative Smart Grid Technologies, Manchester (2011)
8. Meyer, D., Wang, J.: Integrating ultra-fast charging stations within the power grids of smart cities: A review. IET Smart Grid 1(1), 3–10 (2018)
9. Shao, C., Wang, Y., Wang, X.: Coordinated planning of extreme fast charging stations and power distribution networks considering on-site storage. IEEE Trans. Intell. Transp. Syst. 22(1), 493–504 (2021)
10. ElMenshawy, M., Massoud, A.: Modular Isolated DC—DC Converters for ultra-fast EV chargers: A generalized modeling and control approach. Energies 13(2540), (2020)
11. ElMenshawy, M., Massoud, A.: Hybrid multimodule DC–DC converters for ultrafast electric vehicle chargers. Energies 13(4949), (2020)
12. Iyer, V.M., et al.: An approach towards extreme fast charging station power delivery for electric vehicles with partial power processing. IEEE Trans. Ind. Electron. 67(10), 8076–8087 (2020)

13. Vasiladiotis, M., Rufer, A., Beguin, A.: Modular converter architecture for medium voltage ultra fast EV charging stations: global system considerations. In: Proceedings of IEEE International Electric Vehicle Conference, Greenville (2012)

14. Justino, J., Parreiras, T.M., Filho, B.C.: Hundreds kW charging stations for e-buses operating under regular ultra-fast charging. IEEE Trans. Ind. Appl. 52(2), 1766–1774 (2016)

15. Singh, B., et al.: Comprehensive study of single-phase AC–DC power factor corrected converters with high-frequency isolation. IEEE Trans. Ind. Inf. 7(4), 540–556 (2011)

16. Gangavarapu, S., Rathore, A.K.: A three-phase single-sensor-based Cuk-derived PFC converter with reduced number of components for more electric aircraft. IEEE Trans. Transp. Electrif. 6(4), 1767–1778 (2020)

17. Lin, X., et al.: A novel bridgeless Cuk PFC converter with further reduced conduction losses and simple circuit structure. IEEE Trans. Ind. Electron. (2020). https://doi.org/10.1109/TIE.2020.3031527

18. Kushwaha, R., Singh, B., Khadkikar, V.: An improved PQ Zeta converter with reduced switch voltage stress for electric vehicle battery charger. Proceedings of 2020 IEEE Energy Conversion Congress and Exposition, Detroit (2020)

19. Khodabandeh, M., Afshari, E., Amirabadi, M.: A family of Cuk, Zeta, and SEPIC based soft-switching DC–DC converters. IEEE Trans. Power Electron. 34(10), 9503–9519 (2019)

20. Martins, D., Oliveria, A., Barbi, I.: Three-phase rectifier Using a sepic DC–DC converter in continuous conduction mode for power factor correction. Proceedings of Twentieth International Telecommunications Energy Conference, San Francisco (1998)

21. Ayyanar, R., Mohan, N., Sun, J.: Single-stage three-phase power-factor-correction circuit using three isolated single-phase SEPIC converters operating in CCM. Proceedings of 31st IEEE Annual Power Electronics Specialists Conference, Galway (2002)

22. Kwon, J.-M., et al.: Continuous-conduction-mode SEPIC converter with low reverse-recovery loss for power factor correction. IEE Proceedings - Electric Power Applications 153(5), 673–681 (2006)

23. Simonetti, D., Sebastian, J., Uceda, J.: The discontinuous conduction mode sepic and Cuk power factor preregulators: Analysis and design. IEEE Trans. Ind. Electron. 44(5), 630–637 (1997)

24. Tibola, G., Barbi, I.: Isolated three-phase high power factor rectifier based on the SEPIC converter operating in discontinuous conduction mode. IEEE Trans. Power Electron. 28(11), 4962–4979 (2013)

25. Shi, C., Khaligh, A., Wang, H.: Interleaved SEPIC power factor preregulator using coupled inductors in discontinuous conduction mode with wide output voltage. IEEE Trans. Ind. Appl. 52(4), 3461–3471 (2016)

26. Costa, P., et al.: Unidirectional three-phase voltage-doubler SEPIC PFC rectifier. IEEE Trans. Power Electron. 36(6), 6761–6773 (2021)

27. Gao, S., et al.: A DCM high frequency high step up SEPIC-based converter with extended ZVS range. IEEE Journal of Emerging and Selected Topics in Power Electronics 1–10 (2021)

28. Singh, A., et al.: An integrated converter with reduced components for electric vehicles utilizing solar and grid power sources. IEEE Trans. Transp. Electrif. 6(2), 439–452 (2020)

29. Gupta, J., Maurya, R., Arya, S.R.: On-board electric vehicle battery charger with improved power quality and reduced switching stress. IET Power Electron. 13, (13), 2885–2894 (2020)

30. Pandey, R., Singh, B.: PFC-SEPIC converter-fed half-bridge LLC resonant converter for e-bike charging applications. IET Electr. Syst. Transp. 10(3), 225–233 (2020)

31. Singh, B., Kushwaha, R.: A PFC based EV battery charger using a bridgeless isolated SEPIC converter. IEEE Trans. Ind. Appl. 56(1), 447–487 (2020)

32. Garcia, O., et al.: Single phase power factor correction: A survey. IEEE Trans. Power Electron. 18(3), 749–755 (2003)

33. Gangavarapu, S., Rathore, A.K., Fulwani, D.M.: Three-phase single-stage-isolated Cuk-based PFC converter. IEEE Trans. Power Electron. 34(2), 1798–1808 (2019)

34. Tse, K.K., et al.: A novel maximum power point tracker for PV panels using switching frequency modulation. IEEE Trans. Power Electron. 17(6), 980–989 (2002)

35. Singh, B., Bist, V.: DICM and DCVM of a PFC-based SEPIC-fed PMBLDCM drive. IETE Journal of Research 59(2), 141–149 (2013)

36. Chetty, P.: Current injected equivalent circuit approach to modeling of switching DC–DC converters in discontinuous inductor conduction mode. IEEE Trans. Ind. Electron. IE-29(3), 230–234 (1982)

37. Graovac, D., Purschel, M., Kiep, A.: MOSFET power losses calculation using the data-sheet parameters. Infineon Technologies (2006)

38. An, L., Lu, D.: Power loss analysis of a single-switch non-isolated DC/DC converter. Proceedings of IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney (2015)