IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 24, 2019, accepted January 9, 2020, date of publication January 13, 2020, date of current version January 24, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2966048

Hybrid Modular Multilevel Converter With Arm-Interchange Concept for Zero-/Low-Frequency Operation of AC Drives

AHMED ELSEROUGI [1], (Senior Member, IEEE), IBRAHIM ABDELSALAM [2], (Member, IEEE), AHMED MASSOUD [3], (Senior Member, IEEE), AND SHEHAB AHMED [4], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Alexandria University, Alexandria 21544, Egypt
[2]Department of Electrical Engineering, Arab Academy for Science, Technology and Maritime Transport, Cairo 1029, Egypt
[3]Department of Electrical Engineering, Qatar University, Doha, Qatar
[4]Computer, Electrical, and Mathematical Science and Engineering Division, KAUST University, Thuwal 23955, Saudi Arabia

Corresponding author: Ahmed Massoud (ahmed.massoud@qu.edu.qa)

This work was supported in part by the NPRP through the Qatar National Research Fund under Grant 9-092-2-045, and in part by the Qatar National Library.

ABSTRACT DC-AC Modular Multilevel Converter (MMC) is a promising candidate for high-power AC drive applications. The main challenge of operating the MMC in AC drive applications is its performance during low-frequency conditions, as high voltage ripple is associated with the low-frequency operation, which results in voltage stresses on the involved semiconductor devices. To keep capacitor voltages balanced and bounded in low-frequency operation, different techniques have been proposed in literature, which can be classified into software and hardware approaches. In this paper, a hybrid MMC with arm-interchange concept is proposed to ensure operating successfully during low-frequency conditions. The hybrid MMC consists of two-stages. The first stage is a front-end Integrated Gate Commutated Thyristor (IGCT)-based H-bridge converter, while the second stage is a Full-Bridge Sub-Module (FBSM)-based MMC, where FBSMs is able to generate positive, zero, and negative voltage states. Detailed illustration and design of the hybrid MMC are introduced. Simulation results of the proposed converter are presented to show the effectiveness during low-frequency and normal frequency conditions in AC drive applications. Finally, a scaled-down prototype is employed for experimental validation.

INDEX TERMS AC drive, induction machine, low-speed operation, modular multilevel converter.

I. INTRODUCTION

Medium-voltage AC drives are commonly used in different applications, where different converter topologies can be employed. Unlike two-level converters, multilevel converters such as neutral point clamped converter [1] and flying capacitor converter [2] can be operated to generate stepped output voltage with lower dv/dt stresses and lower harmonic content. But these converters can be used up to a limited number of voltage levels [3]. Recently, the modular multilevel converter (MMC) has been proposed for high-voltage high-power applications due to its modularity, scalability, and output voltage quality [4]–[7], which makes it suitable for high-power AC drive applications. However, the main challenge of employing MMC-based AC drives is the low-frequency operation at the rated torque, since the voltage ripple of the SMs capacitance is inversely proportional to the converter output frequency. This means high voltage ripple is associated with the low-frequency operation, which results in voltage stresses.

Different techniques have been reported in literature to resolve this issue. Some techniques are based on software solutions, while others are based on hardware solutions.

Regarding the hardware solutions, several approaches have been reported in literature to reduce the voltage ripple of Sub-Modules (SMs) capacitors during low-frequency operation, which is summarized as follows. In [8], a semiconductor device in series with the input terminals along with a snubber circuit connected across the DC-link has been employed with the conventional Half-Bridge SM (HBSM)-based MMC

The associate editor coordinating the review of this manuscript and approving it for publication was Alexander Micallef.

structure to reduce the voltage ripple of the SMs capacitors at the low-frequency condition. The main drawback of this approach is that the converter draws discontinuous input current.

In [9], an active cross-connected HBSM-based MMC has been proposed to enhance the performance of the loaded motor drive from standstill to rated speed. In this configuration, a cross-connection through an additional arm exists between upper and lower arm middle taps. By controlling the high-frequency current passing through the cross-connected arm, the energy balance is achieved between the upper and lower arms of the same leg at low-frequency loaded conditions without introducing common-mode voltage, but a large number of HBSMs are employed. In [10], an MMC has been proposed, where the upper three arms and lower three arms are cross-connected through two sets of FBSM-based star-channel branches. These branches are used to re-balance the energy among the converter legs without injecting common-mode voltage. The energy balance results in reducing capacitor voltage ripple during low frequency. In [11] and [12], the back-to-back FBSM-based MMC drive system, which consists of grid-side MMC and motor-side MMC, has been employed. This arrangement is controlled to drive a three-phase motor from zero speed to full-load speed with balanced and bounded capacitor voltages, but a large number of FBSMs are employed. In [13], the energy equalization modules concept has been presented to ensure the energy balance between the upper and lower arms of MMC during the low-frequency condition. Dual active bridge equalization channels concept has been proposed in [14]–[16] for different types of machine drives, while the shared capacitor SM concept has been proposed in [17] for open-winding machine drives. In the energy equalization modules' concept, a large number of extra hardware components are needed to implement the energy equalization modules, which increases the cost and complexity of the converter.

Regarding the software solutions, injecting high frequency circulating current into MMC arms [18]–[23] is one of the main proposed approaches. High-frequency injection results in higher current stresses, higher power loss, and common-mode voltage at motor terminals. In [24], an optimal selection of the average capacitor voltage of MMC-based drive has been investigated at rated torque and below base speed condition. Neither hardware changes nor any energy exchange between upper and lower arms is required in this method, but it can be applied successfully for a certain range of speed (from 0.3 pu to 1 pu, i.e., high-speed range). In [25], a speed-based control strategy for arm capacitor voltage of MMC-based AC drive has been proposed, which results in extending the motor speed range and improving the low-speed control capability, yet at the cost of control system complexity.

In [26], an asymmetric control mode for MMC-based AC drive at low-frequency conditions has been proposed. This technique ensures operating with bounded arms power levels. This method is not suitable for the cases at which the motor requires high driving voltage at low frequency.

In [27], a quasi-two-level PWM of MMC-based drive has been presented, which allows operating with small capacitance, but the multilevel output voltage is sacrificed. In [28], exploitation to additional degrees of freedom of multi-phase MMC-based AC drive system was proposed to keep the capacitor voltage balancing during zero-/low-speed operation via injecting secondary current components in the load current with specific magnitude and frequency during zero-/low-speed intervals. In this approach, multi-phase MMC and multi-phase machines should be employed, i.e., it is not suitable for three-phase AC Drive systems.

In this paper, a hybrid MMC is proposed to maintain balanced and bounded capacitor voltages with limited voltage ripple from zero-frequency to the full-load frequency at the rated torque in AC motor drive applications. The proposed configuration consists of two stages. The first stage is a front-end IGCT-based H-bridge converter where its input is connected to the DC-link voltage, while its output terminals are the input terminals of the second stage. The second stage is a conventional three-phase FBSM-MMC. To limit the voltage ripple of the SMs capacitors during loaded zero-/low-frequency condition, the proposed architecture is operated under arm-interchange concept, where positive, zero and negative voltage stages of FBSMs are employed, while the front-end IGCT-based H-bridge is used to convert the DC-link voltage input into a square-wave output with a predetermined frequency (swapping frequency, f_b). Alternatively, the FBSM-MMC is operated under conventional MMC control during normal frequency condition, i.e., negative voltage states of the involved FBSMs are not employed, and the front-end H-bridge is operated to pass the input DC-link voltage without reversing its polarity. It is worth mentioning that the low switching frequency operation of the front-end H-bridge allows employing low switching frequency devices such as IGCTs and reduces the converter switching losses. In addition, IGCTs have low conduction losses, which enhance the efficiency of the front-end converter.

It has to be noted that (i) the proposed method needs FBSM-MMC as its second stage to ensure successful DC-AC conversion during low-speed operation. But, during the high-speed operation, the FBSM-MMC works the same as HBSM-MMC, which might make the design costly. However, the proposed system is devoted to zero-speed/low-speed medium-voltage drive applications such as cranes, scraper conveyors, hoists, rolling mills, tractions, and internal mixers (high-torque capability with starting and/or low-speed operation) [29]–[31], (ii) the proposed architecture provides successful operation at low-frequency conditions with lower current stresses on the involved semiconductor devices compared to the conventional HBSM-MMC converter with high-frequency circulating current injection method, but with a higher number of employed switches. In order to highlight that, a comparison between the performance of the

aforementioned two options during low-frequency operation is presented in the simulation section.

Detailed illustration of the proposed architecture operational concept, design, and control are presented. Simulation results for the proposed approach are presented with discussion. Finally, a scaled-down prototype is employed for experimental validation.

II. OPERATIONAL CONCEPTS OF THE CONVENTIONAL HBSMS-BASED THREE-PHASE MMC

The three-phase HBSMs-based MMC consists of three legs where each leg consists of upper (u) and lower (L) arms, as shown in Fig.1. The arm consists of (N-1) cascaded HBSMs in series with arm inductor, where N is the number of converter voltage levels. During DC-AC conversion, the voltage references of each upper and lower arms are defined by;

$$v_{uj} = \frac{V_{dc}}{2} - v_{oj} \quad (1)$$

$$v_{Lj} = V_{dc} - v_{uj} \quad (2)$$

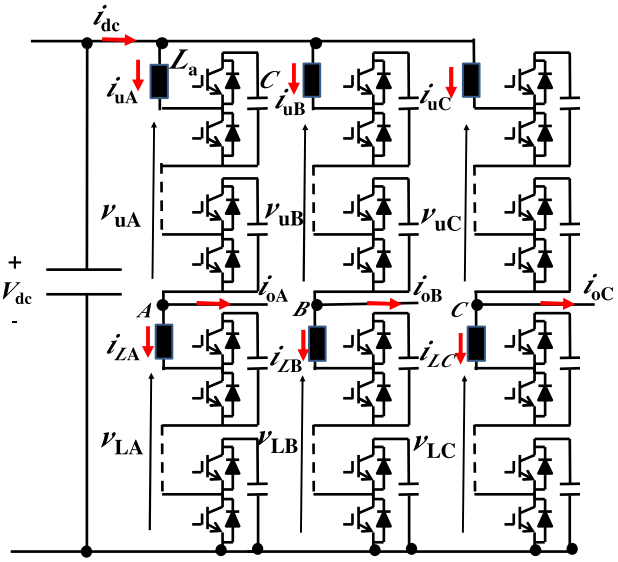


FIGURE 1. The Conventional three-phase HBSM-MMC based AC motor drive.

where, subscripts j denotes the phase name (A or B or C), and v_{oj} is the desired AC output voltage of phase j with a peak of up to $V_{dc}/2$ as in (3), where M is the modulation index ($M \leq 1$), i.e., overmodulation is not considered and θ_j is the phase shift of the phase j.

$$v_{oj} = \frac{MV_{dc}}{2} \sin(\omega t - \theta_j) = V_m \sin(\omega t - \theta_j) \quad (3)$$

For each leg of the converter legs, certain procedures are applied to ensure generating the desired output voltage, where the defined upper arm voltage is translated into a number of SMs to be activated in the upper arm (N_{uj}) with the help of any proper modulation technique. In the presented work, Phase Disposition (PD) modulation technique is employed. Based on the extracted number of SMs to be activated in upper arms, the SMs to be activated in lower arms can be extracted simply, as their sum should be N, i.e., $N_{Lj} = N - N_{uj}$. Based on the upper/lower arm current directions, proper SMs in the upper/lower arm will be activated to ensure operating with balanced capacitor voltage [32]. The per-phase current (i_{oj}) is given by (4);

$$i_{oj} = \frac{MV_{dc}}{2Z} \sin(\omega t - \theta_j - \varphi) = I_m \sin(\omega t - \theta_j - \varphi) \quad (4)$$

where, Z and φ are the magnitude of load impedance and load phase angle, respectively.

The input dc current is given by (5) assuming well-suppressed circulating currents.

$$I_{dc} = \frac{3I_m V_m \cos\varphi}{2V_{dc}} = \frac{3I_m M \cos\varphi}{4} \quad (5)$$

The upper/lower arm current has DC and AC components as in (6) and (7), where the DC component is one-third of the input DC current ($I_{dc}/3$), while the AC component is half of the phase output current ($i_{oj}/2$).

$$i_{uj} = (I_{dc}/3 + i_{oj}/2) = \frac{I_m M \cos\varphi}{4} + \frac{I_m}{2} \sin(\omega t - \theta_j - \varphi) \quad (6)$$

$$i_{Lj} = (I_{dc}/3 - i_{oj}/2) = \frac{I_m M \cos\varphi}{4} - \frac{I_m}{2} \sin(\omega t - \theta_j - \varphi) \quad (7)$$

The arm currents are bipolar, which allows charging and discharging of SMs capacitors during the operation, which results in operating with balanced capacitor voltages. The frequency and phase current magnitude affect the voltage ripple of the SMs capacitors as in (8) ;

$$v_C(t) = V_{C0} + \frac{1}{C}\int i_C \, dt = V_{c0} + \frac{1}{C}\int i_{arm} \frac{v^*_{arm}}{V_{dc}} dt \quad (8)$$

where, V_{c0} is the capacitor pre-charged voltage, v^*_{arm} is the voltage reference of arm voltage and i_{arm} is the arm current.

For the upper arm of phase "A" with $\theta_A = 0$,

$$v_C(t) = V_{c0} + \frac{I_m}{8\omega C}\int [M\cos\varphi + 2\sin(\omega t - \varphi)] \times [1 - M\sin\omega t] d\omega t \quad (9)$$

Based on (9), the capacitor voltage ripple is proportional to the phase current magnitude and inversely proportional to the operating frequency, which necessitates the employment of bulky capacitors to limit the capacitor voltage ripple during low-frequency operation which is not a cost-effective solution. On the other hand, the conventional MMC operation does not provide balanced capacitor voltage during DC operation, wherein the capacitor voltages diverge.

In this work, a new hybrid modular multilevel converter is proposed to provide successful operation with balanced and bounded capacitor voltages during zero-/low-frequency operation at rated torque.

III. THE PROPOSED HYBRID MODULAR CONVERTER

The proposed three-phase hybrid modular multilevel converter for AC motor drive applications is shown in Fig.2. The proposed architecture consists of two cascaded stages.

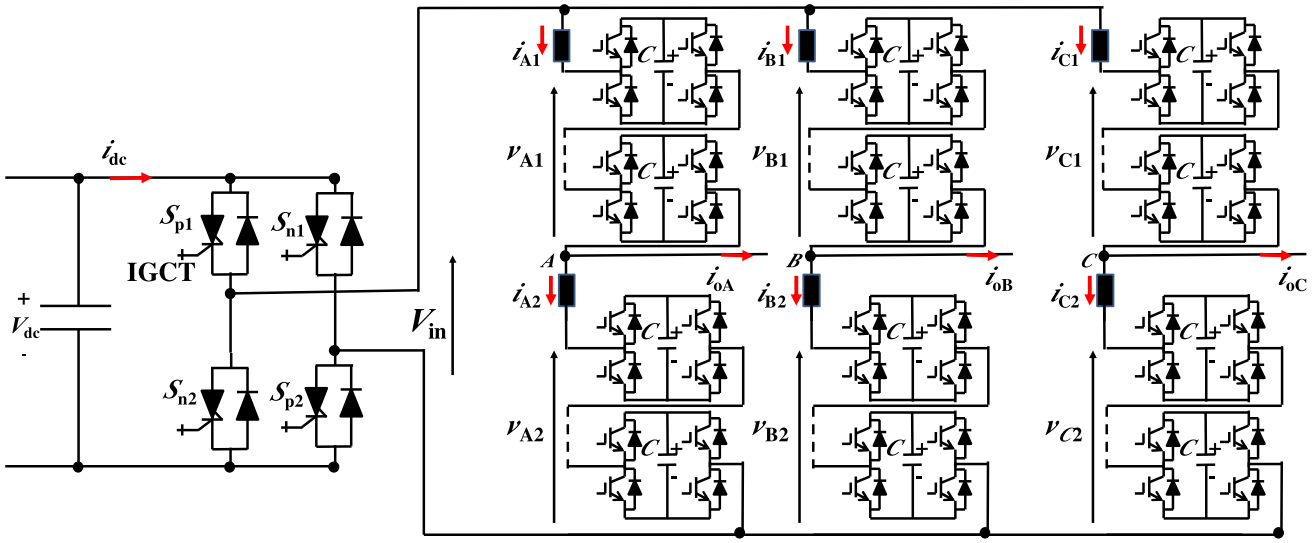


FIGURE 2. The Proposed three-phase hybrid MMC-based AC motor drive.

The first stage is a front-end IGCT-based H-bridge converter, which can be used to generate positive V_{in} ($V_{in} = +V_{dc}$) via turning-on the switches (S_{P1} and S_{P2}). On the other hand, negative V_{in}($V_{in} = -V_{dc}$) can be achieved via turning-on the switches (S_{n1} and S_{n2}). A bipolar two-level square-wave can be generated from the front-end H-bridge with a certain predetermined swapping frequency ($f_b = 1/T_b$) via alternating the turning-on of the switches (S_{P1} and S_{P2}) and (S_{n1} and S_{n2}) each $T_b/2$. IGCTs are employed as the front-end H-bridge is operated with a relatively low switching frequency, which is suitable for the IGCTs switching capabilities. In addition, IGCTs also have low conduction losses.

The second stage is a conventional FBSM-MMC, where each arm consists of cascaded FBSMs. Based on the desired speed (i.e., the operating frequency of the motor), each FBSM of the involved FBSMs is controlled to generate positive, zero or negative voltage state. The operational modes of the proposed hybrid MMC-converter in AC drive applications are presented as follows.

A. ZERO-/LOW-FREQUENCY OPERATIONAL MODE

In this mode, the front-end IGCT-based H-bridge is controlled to generate a bipolar square-wave with a predetermined swapping frequency ($f_b = 1/T_b$). The arm voltages are controlled to ensure generating the desired motor terminal voltages with the swapping of the input voltage (V_{in}) between positive and negative polarity. To ensure that, positive and negative voltage states of the involved FBSMs should be employed.

Fig.3. shows the corresponding arm voltages in the loaded zero-/low-frequency operational mode. Fig.3a shows the values and directions of the arm voltages during positive V_{in}, where the involved FBSMs are operated to generate zero and positive voltage states (as in the conventional MMC control), therefore generating positive arm voltages.

On the other hand, Fig.3b shows the values and directions of arm voltages during negative V_{in}, where the involved FBSMs are operated under zero and negative voltage states to generate negative arm voltages.

Reversing the FBSMs voltage state from positive (Fig.3a) to negative (Fig.3b) ensures the charging and discharging of the involved capacitors, which results in operating with balanced and bounded capacitor voltages. The capacitor voltage ripple mainly depends on the swapping frequency ($f_b = 1/T_b$).

The swapping between the two circuits shown in Fig.3a and Fig.3b is achieved continuously during the loaded zero-/low-frequency condition each $T_b/2$ time interval, where the circuit shown in Fig.3a is operated during positive V_{in} for $kT_b < t \leq (k+0.5)T_b$ where $k = 0, 1, 2, ..$ etc., while the circuit shown in Fig.3b is operated during negative V_{in} for $(k+0.5)T_b < t \leq (k+1)T_b$.

The input voltage (V_{in}), arm voltages reference, and arm currents during zero-/low-frequency conditions for phase A are given by (10), (11) and (12), respectively. Similarly, for the other phases.

$$V_{in} = \begin{cases} V_{dc} & \text{for } kT_b < t \leq (k+0.5)T_b \\ -V_{dc} & \text{for } (k+0.5)T_b < t \leq (k+1)T_b \end{cases} \tag{10}$$

$$V_{A1}^* = \begin{cases} \frac{V_{dc}}{2} - v_{oA}^* & \text{for } kT_b < t \leq (k+0.5)T_b \\ -[\frac{V_{dc}}{2} + v_{oA}^*] & \text{for } (k+0.5)T_b < t \leq (k+1)T_b \end{cases}$$

$$V_{A2}^* = \begin{cases} \frac{V_{dc}}{2} + v_{oA}^* & \text{for } kT_b < t \leq (k+0.5)T_b \\ -[\frac{V_{dc}}{2} - v_{oA}^*] & \text{for } (k+0.5)T_b < t \leq (k+1)T_b \end{cases} \tag{11}$$

$$i_{A1} = \begin{cases} \frac{i_{dc}}{3} + \frac{i_{oA}}{2} & \text{for } kT_b < t \leq (k+0.5)T_b \\ -\frac{i_{dc}}{3} + \frac{i_{oA}}{2} & \text{for } (k+0.5)T_b < t \leq (k+1)T_b \end{cases} \tag{12a}$$

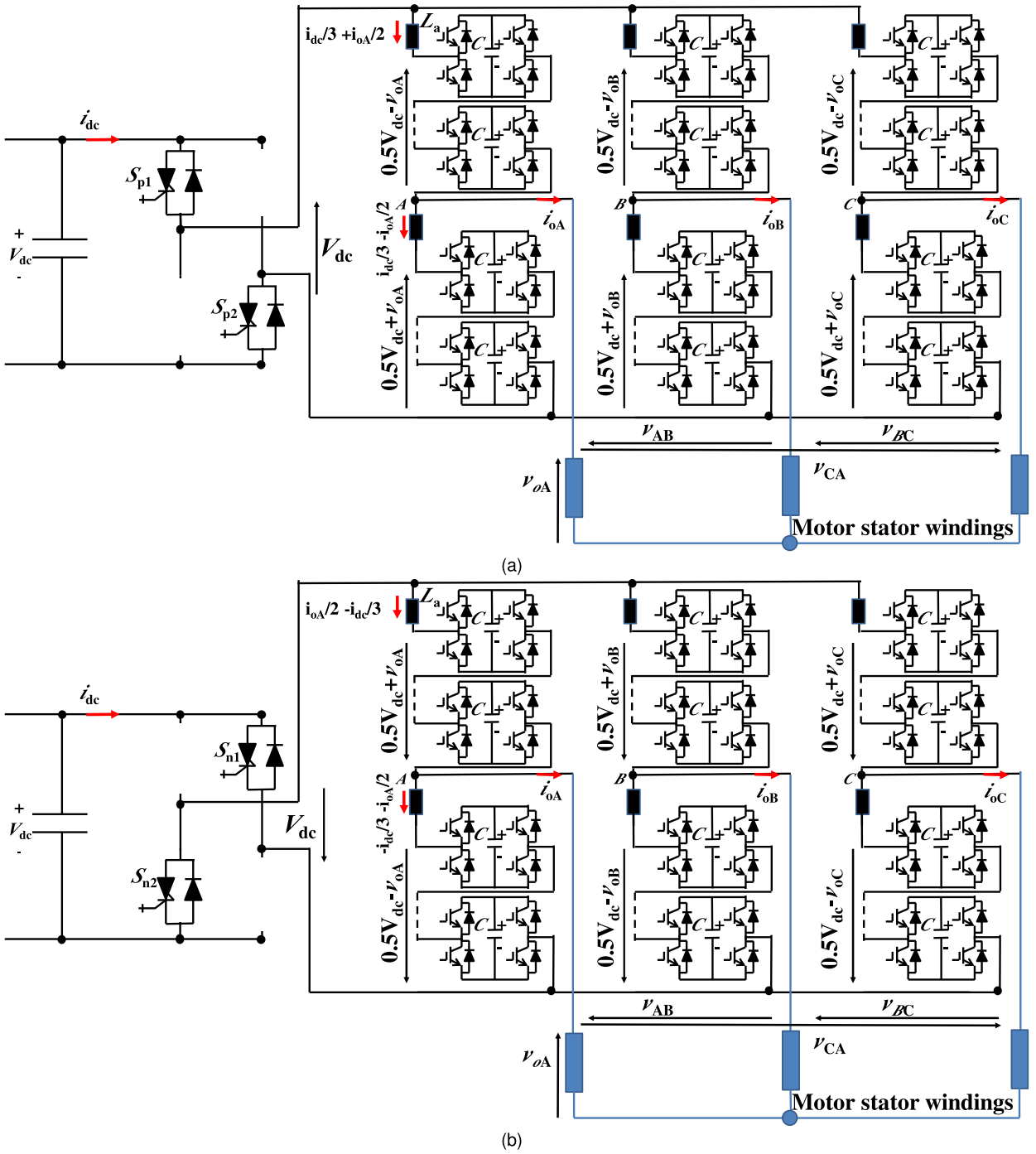


FIGURE 3. The operational concept of the proposed hybrid MMC-based AC drives during loaded zero-/low-frequency condition where the operation is swapped between (a) and (b) continuously each $T_b/2$. (a) arm voltages and currents during positive V_{in} for $kT_b < t \leq (k+0.5)T_b$ where $k = 0, 1, 2, ..$ etc, and (b) arm voltages and currents during negative V_{in} for $(k+0.5)T_b < t \leq (k+1)T_b$.

$$i_{A2} = \begin{cases} \dfrac{i_{dc}}{3} - \dfrac{i_{oA}}{2} & \text{for } kT_b < t \leq (k+0.5)T_b \\ -\dfrac{i_{dc}}{3} - \dfrac{i_{oA}}{2} & \text{for } (k+0.5)T_b < t \leq (k+1)T_b \end{cases} \tag{12b}$$

Based on the defined arm voltage reference and the arm's current polarity, a certain number of FBSMs will be activated in each arm with a positive or negative voltage state according to the arm voltage polarity. While other FBSMs in the same arm will be bypassed, i.e., operated under zero voltage state. A voltage balancing algorithm is needed to select proper FBSMs to be activated to ensure operating with balanced capacitor voltages, i.e., capacitor voltages and arm currents measurements are mandatory. It is worth to mention that based on Fig.3, the absolute value of arm voltage reference is interchanged between arms of the same leg due to swapping

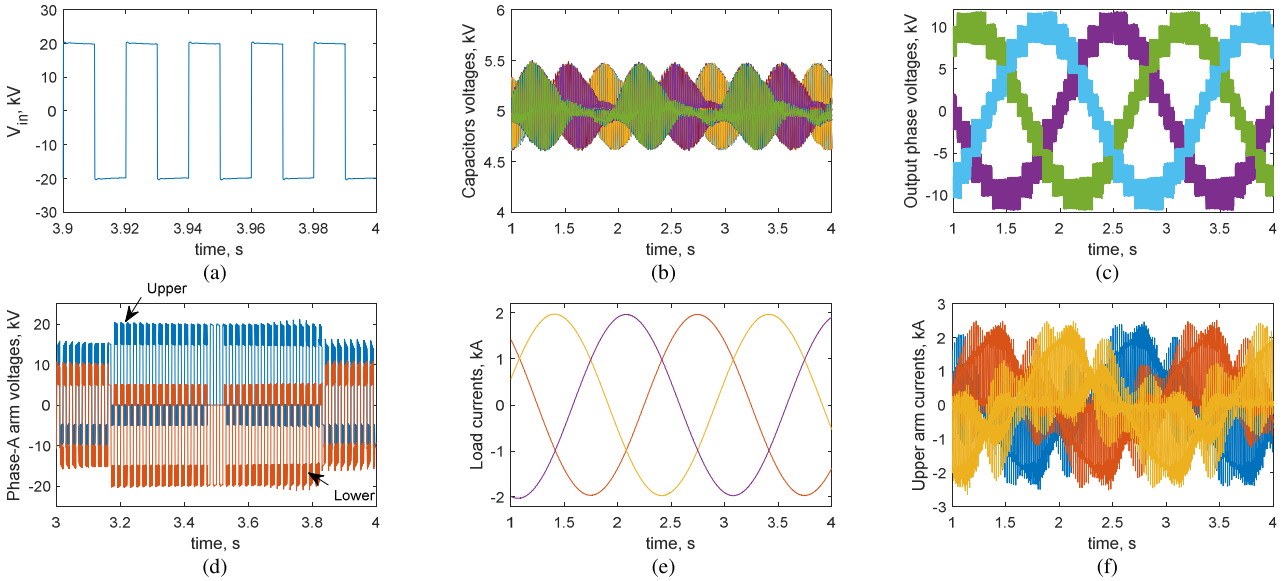


FIGURE 4. Simulation results at 0.5Hz output frequency (arm-interchange concept is activated). (a) Input voltage, V_{in}, (b) capacitors voltages, (c) Output phase voltages, (d) Phase-A arm voltages, (e) Output phase currents, and (f) upper arm currents.

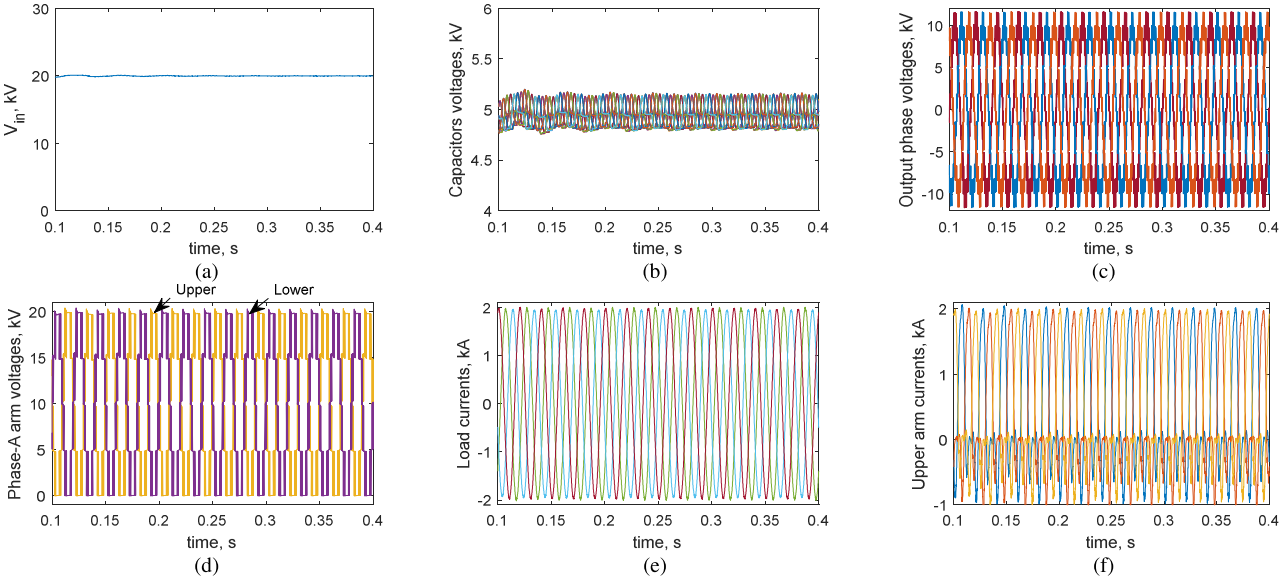


FIGURE 5. Simulation results at 50 Hz output frequency (arm-interchange concept is deactivated). (a) Input voltage, V_{in}, (b) capacitors voltages, (c) Output phase voltages, (d) Phase-A arm voltages, (e) Output phase currents, and (f) upper arm currents.

of the input voltage V_{in} to keep the same output voltage at the motor terminals.

B. NORMAL FREQUENCY OPERATIONAL MODE

When the desired output frequency is above a certain defined output frequency, namely, frequency limit (f_{d}), the proposed arm-interchange concept is deactivated, where the frequency limit is the lowest frequency that gives an acceptable capacitor voltage ripple with the conventional operation of MMC. In normal frequency conditions, the front-end H-bridge is operated to generate positive $V_{\text{in}}(V_{\text{in}} = +V_{\text{dc}})$ while the FBSMs-MMC is operated under conventional MMC control, i.e., FBSMs are operated to generate zero and positive voltage states (negative voltage state of FBSMs is not used).

The corresponding input voltage (V_{in}) and arm voltage reference, in this case, are as shown in Fig.3a which are given by (13) and (14) respectively;

$$V_{in} = V_{dc} \tag{13}$$

$$V^*_{A1} = \frac{V_{dc}}{2} - v^*_{oA}, \quad V^*_{A2} = \frac{V_{dc}}{2} + v^*_{oA} \tag{14}$$

and the corresponding arm currents are given by (15);

$$i_{A1} = \frac{i_{dc}}{3} + \frac{i_{oA}}{2}, \quad i_{A2} = \frac{i_{dc}}{3} - \frac{i_{oA}}{2} \tag{15}$$

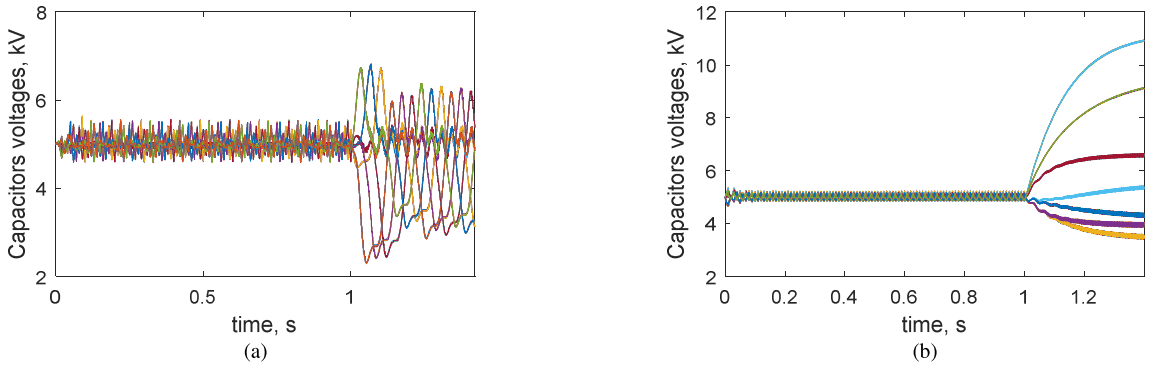


FIGURE 6. Effect of deactivation of the proposed arm-interchange concept on the capacitor voltages (a) 5Hz and (b) 0 Hz.

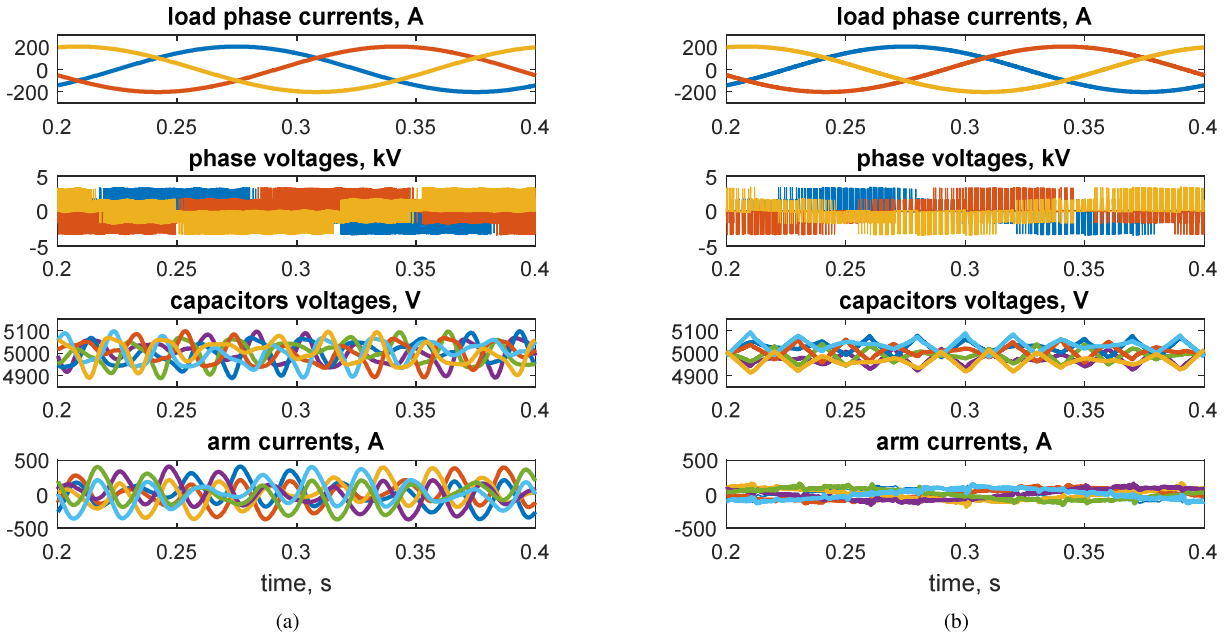


FIGURE 7. Performance of two different techniques during low-frequency operation (5Hz output frequency). (a) conventional MMC, along with high frequency circulating current injection and (b) the proposed approach along with interchange arm concept.

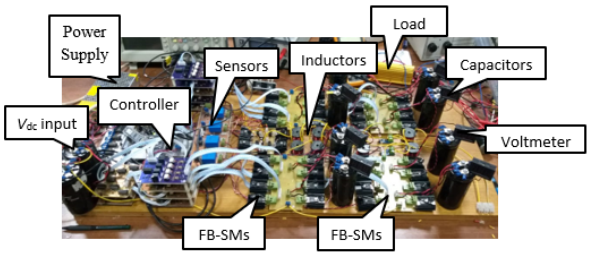


FIGURE 8. Experimental setup.

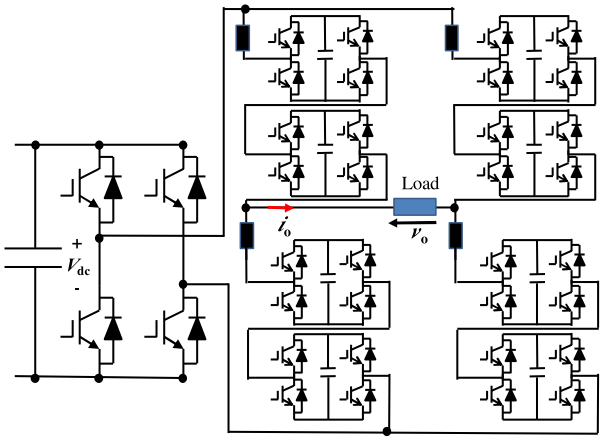


FIGURE 9. Hardware configuration of the experimental setup.

IV. DESIGN OF THE PROPOSED CONVERTER

A. SUBMODULE CAPACITORS AND SWAPPING FREQUENCY (F_B)

The SM capacitors are selected such that the total energy stored in all capacitors equals 30-40 kJ/MVA [33], where MVA refers to the converter rating. This ratio guarantees a 10% capacitor voltage ripple at rated frequency and rated power. During zero-/low-frequency condition, the capacitors are either charged or discharged during $T_b/2$ period based on the arm voltage and arm current polarity.

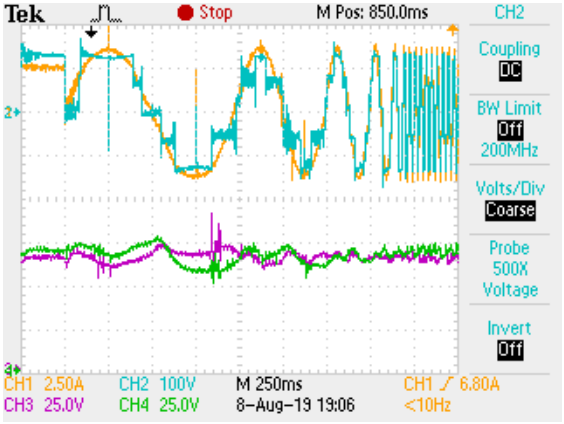


FIGURE 10. Performance of the proposed hybrid modular converter during the zero-/low-frequency operation where CH1 shows the load current, CH2 the load voltage, and CH3 and CH4 show the capacitor voltages.

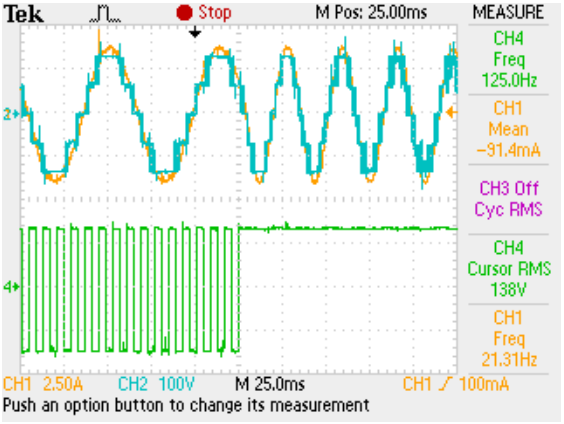


FIGURE 11. Experimental results for output frequency change from 16 Hz to 32Hz, where CH1 shows the load current, CH2 the load voltage, and CH3 shows the input voltage, V_{in}.

The relation between the capacitor current and voltage during the $T_b/2$ period is given by (16);

$$i_c = C dv_c/dt \tag{16a}$$

$$i_{arm}\frac{v^*_{arm}}{V_{dc}} = \frac{2C\Delta v}{T_b} \tag{16b}$$

where, i_{arm} and $v*_{arm}$ are the arm current and voltage reference during this period, respectively. For the desired capacitor voltage ripple, Δv, and assuming worst-case condition, the proper swapping frequency is given by (17);

$$f_b \approx \frac{i_{arm-pk}}{2C\Delta v} \tag{17}$$

B. ARM INDUCTOR (L_A)

The arm inductor should be selected such that the steady-state condition after swapping is achieved as fast as possible, i.e., the natural frequency of the LC circuit per leg is higher than the double of the swapping frequency ($2f_b$). Based on that, the suitable arm inductance for the proposed architecture is given by (18), where L_a, C, and N are the arm inductor, SM capacitor, and number of SMs per arm, respectively.

$$L_a < \frac{N}{32\pi C f_b^2} \tag{18}$$

V. SIMULATION

A. PERFORMANCE OF PROPOSED CONVERTER

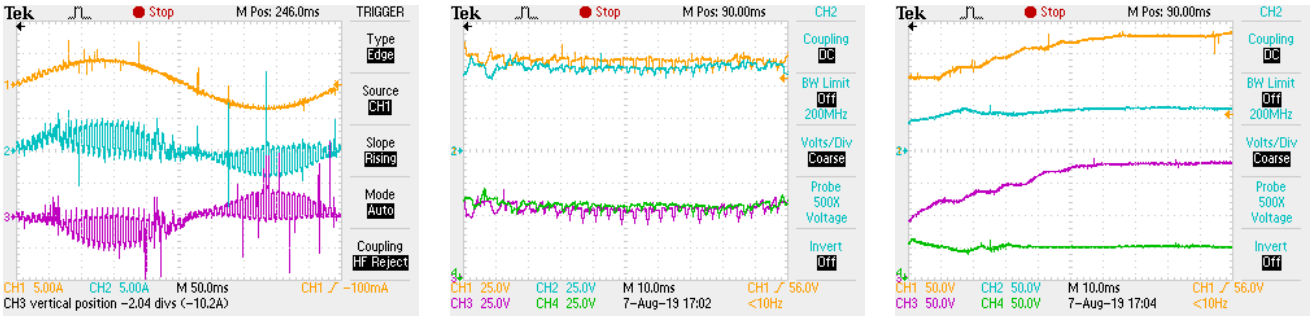
A simulation model of the proposed three-phase hybrid MMC-based converter with the parameters shown in Table 1 has been built. The proposed arm-interchange concept is applied from 0 to 30 Hz output frequency (f_d = 30Hz), i.e., positive and negative voltage states of the involved FBSMs are employed and the front-end H-bridge is used to generate bipolar square-wave output as illustrated in section III-A. For an output frequency above the 30 Hz, conventional MMC control is applied, as illustrated in section III-B.

TABLE 1. Simulation and experimental parameters.

Parameter	Simulation	Experimental
Input DC voltage, V_{dc}	20kV	140 V
Modulation index, M	1	1
Frequency limit (f_d)	30Hz	30Hz
Number of FBSMs per arm	4	2
Arm inductor, L_a	0.1 mH, 0.1Ω	0.4 mH
SM capacitance	5 mF	360 µF
Load current peak	2 kA	4 A
Swapping frequency, f_b	50 Hz	120 Hz
Modulation technique	PD, 2.4kHz carrier	PD, 2.5k Hz carrier

The simulation results for 0.5 Hz and 50 Hz output frequencies are shown in Figs. 4 and 5, respectively. In case of 0.5 Hz output frequency, the proposed arm-interchange concept is applied where negative voltage states of the involved FBSMs are employed. to ensure operating with balanced and bounded capacitors voltages. Swapping between the circuits shown in Fig.3a and Fig.3b is applied each 10ms ($T_b/2$). Fig.4a shows that the input voltage V_{in} is a square wave with a frequency of 50Hz, which is the defined swapping frequency (f_b). The square wave is generated successfully with the help of the front-end H-bridge converter. Fig.4b shows that the FBSMs capacitors voltages are balanced and bounded while generating AC output voltage with 0.5 Hz frequency. Figs.4c and 4d show the output phase voltages and the phase-A arm voltages, respectively. Finally, Figs.4e and 4f show the corresponding load currents and the upper arm currents.

On the other hand, in case of 50Hz output frequency, the proposed arm-interchange concept is deactivated as the desired output frequency is above 30Hz, which is the defined frequency limit (f_d = 30Hz). In this case, the front-end H-bridge converter is operated to generate positive V_{in}, i.e., $V_{in} = V_{dc}$, while the MMC is operated under conventional control where negative voltage states of FBSMs are not employed. The corresponding simulation results are shown in Fig.5.



(a) (b) (c)

FIGURE 12. Experimental results for an output frequency of 2 Hz. (a) load current (CH1) along with arm currents (CH2 and Ch3), (b) capacitors voltages when the proposed arm-interchange concept is activated, and (c) capacitors voltages when the proposed arm-interchange concept is deactivated.

To show the effect of the proposed arm-interchange concept on the capacitor voltage ripple during low-/zero-frequency conditions, the proposed concept is activated for 1s then it is deactivated. The deactivation of the suggested approach shows the performance of the drive system when conventional MMC is employed. The deactivation is made by operating the front-end H-bridge to generate positive V_{in} and operating the FBSM-MMC under conventional control without employing negative voltage states of the involved FBSMs. The corresponding capacitors voltages variations for 5Hz output frequency is shown in Fig. 6a. The results show that the effectiveness of the proposed arm-interchange concept in reducing the capacitor voltage ripple during low-frequency operation. Finally, the effect of the proposed concept deactivation during the zero-frequency operation is shown in Fig.6b, where the capacitor voltages diverge after deactivation of the proposed concept, while they are balanced and bounded during its activation period, which elucidates the effectiveness of the proposed arm-interchange concept in zero-frequency operation.

B. PROPOSED METHOD VERSUS CIRCULATING CURRENT INJECTION

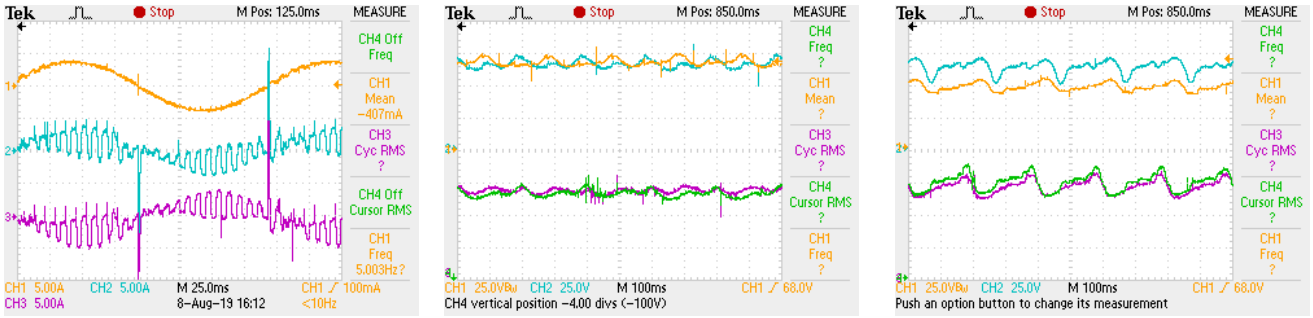
In this section, a comparison between the performance of the proposed architecture along with the interchange arm concept and the performance of the conventional HBSM-based MMC along with high-frequency circulating current injection during low-frequency operation is held to show the merits of the proposed approach. To achieve that, two simulation modes for both systems have been built and tested for the same operating condition. The parameters of both systems are defined as follows: DC input voltage is 20kV, number of SMs per arm is 4, SM capacitance of 5mF is employed, arm inductors of 2mH and 0.1mH with 0.1Ω internal resistance are employed in the conventional MMC and the proposed options respectively, frequency of the injected current is 50Hz, carrier frequency of 2.4 kHz, V/f ratio is kept constant, load current of 200 A peak (at rated torque). The performances of both systems during 5Hz output frequency at rated torque condition are shown in Fig. 7. In the 5Hz output frequency, in order to maintain V/f ratio constant, the converter output voltage is reduced to 1 kV to keep constant machine flux. Fig.7a shows that the conventional MMC along with high-frequency circulating current injection method is able to keep the voltages of the capacitors with low voltage ripple magnitude during the low-frequency operation, but with large arm current due to large injected circulating currents (arm current peak $\sim = 400$A at 200A load current peak). This, in turn, means operating with high current stresses on the employed semiconductor devices. On the other hand, Fig.7b shows the performance of the proposed architecture along with the interchange arm concept for the same operating condition.

The results show that the proposed approach is able to be operated successfully with bounded and balanced capacitors voltages during low-frequency condition with lower current stresses. The arm currents are limited to approximately 125A peak at 200A load current peak, i.e., switches with low current ratings can be employed with the proposed approach. This means that the proposed approach provides lower current stresses compared to the conventional MMC along with high-frequency circulating current injection technique.

VI. EXPERIMENTAL VALIDATION

A single-phase scaled-down prototype of the proposed hybrid MMC was implemented, as shown in Fig.8, where its schematic diagram is shown in Fig.9. The experimental setup parameters are given in Table 1. The experimental setup has been used to show different scenarios. Fig.10 shows the output voltage and current along with capacitors voltages when the output frequency is changed from 0 Hz to 30 Hz while applying the proposed arm-interchange concept. Fig.10 shows that the capacitor voltages are balanced and bounded along with the whole range of the output frequency.

Fig.11 shows the experimental results in case of output frequency change for 16 Hz to 32 Hz. In case of 16Hz (i.e., below the frequency limit, f_{d}), the proposed arm-interchange concept is applied, and front-end H-bridge is operated to generate bipolar square-wave, as shown in Fig.11. On the other hand, in case of 32 Hz (i.e., above the frequency limit), the arm-interchange concept is deactivated, and the front-end



(a) (b) (c)

FIGURE 13. Experimental results for an output frequency of 5 Hz. (a) load current (CH1) along with arm currents (CH2 and Ch3), (b) capacitors voltages when the proposed arm-interchange concept is activated and (c) capacitors voltages when the proposed arm-interchange concept is deactivated.

H-bridge is operated to generate positive input voltage, i.e., positive V_{in}. Fig.10shows that the output voltage and current are generated successfully with the desired frequency across the load.

Finally, Figs.12 and 13 show the performance of the proposed hybrid MMC converter at 2 Hz and 5Hz output frequency, respectively. Figs.12a and 13a show the load current along with the arm currents in each case. The load current is generated successfully with the desired frequency, while the arm currents have two frequency components, the output frequency component and the swapping frequency component due to applying the arm-interchange concept. Figs.12b and 13b show the corresponding capacitor voltages.

VII. CONCLUSION

In this paper, a new hybrid MMC-based converter is proposed for AC drives applications. The proposed configuration has a multilevel output voltage with low dv/dt stresses. The proposed configuration, along with the proposed arm-interchange concept, can provide successful operation for loaded zero-/low-frequency conditions in AC motor drive systems, where balanced, bounded capacitors voltages with low voltage ripple are guaranteed with the proposed approach without increases the arm current stresses. Detailed illustration and design of the proposed architecture have been presented. Simulation and experimental results are presented to show the viability of the proposed approach for AC motor drive application.

ACKNOWLEDGMENT

The statements made herein are solely the responsibility of the authors.

REFERENCES

[1] A. Bendre, G. Venkataramanan, D. Rosene, and V. Srinivasan, "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 718–726, Jun. 2006.

[2] I.-D. Kim, E.-C. Nho, H.-G. Kim, and J. Ko, "A generalized undeland snubber for flying capacitor multilevel inverter and converter," *IEEE Trans. Ind. Electron.*, vol. 51, no. 6, pp. 1290–1296, Dec. 2004.

[3] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[4] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[5] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts—Part II: Experimental validation and comparison for HVDC application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4536–4545, Oct. 2013.

[6] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J.-C. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, Jun. 2013.

[7] O. Cwikowski, H. R. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, "Modular multilevel converter DC fault protection," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 291–300, Feb. 2018.

[8] B. Li, S. Zhou, D. Xu, S. J. Finney, and B. W. Williams, "A hybrid modular multilevel converter for medium-voltage variable-speed motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4619–4630, Jun. 2017.

[9] S. Du, B. Wu, K. Tian, N. R. Zargari, and Z. Cheng, "An active cross-connected modular multilevel converter (AC-MMC) for a medium-voltage motor drive," *IEEE Trans. Ind. Appl.*, vol. 63, no. 8, pp. 4707–4717, Aug. 2016.

[10] S. Du, B. Wu, and N. R. Zargari, "A star-channel modular multilevel converter for zero/low-fundamental-frequency operation without injecting common-mode voltage," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2857–2865, Apr. 2018.

[11] Y. S. Kumar and G. Poddar, "Control of medium-voltage AC motor drive for wide speed range using modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2742–2749, Apr. 2017.

[12] Y. S. Kumar and G. Poddar, "Medium-voltage vector control induction motor drive at zero frequency using modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 125–132, 2018.

[13] M. Sleiman, M. Koteich, H. F. Blanchette, H. Kanaan, and K. Al-Haddad, "Energy equalization module for modular multilevel converters in variable speed motor drives," in *Proc. 3rd Int. Conf. Renew. Energies Developing Countries (REDEC)*, Jul. 2016.

[14] M. S. Diab, A. M. Massoud, S. Ahmed, and B. W. Williams, "A dual modular multilevel converter with high-frequency magnetic links between submodules for MV open-end stator winding machine drives," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5142–5159, Jun. 2018.

[15] M. S. Diab, B. W. Williams, D. Holliday, A. M. Massoud, and S. Ahmed, "A modular multilevel converter with isolated energy-balancing modules for MV drives incorporating symmetrical six-phase machines," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Oct. 2017.

[16] M. S. Diab, A. M. Massoud, S. Ahmed, and B. W. Williams, "A modular multilevel converter with ripple-power decoupling channels for three-phase MV adjustable-speed drives," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4048–4063, May 2019.

[17] M. S. Diab, A. M. Massoud, S. Ahmed, and B. W. Williams, "Dual modular multilevel converter with shared capacitor sub-module for MV open-end stator winding machine drives," *J. Eng.*, vol. 2019, no. 17, pp. 4401–4405, Jun. 2019.

[18] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the Modular Multi-Level Converter," in *Proc. IEEE Energy Convers. Congr. Exposit.*, Atlanta, GA, USA, Sep. 2010, pp. 3993–3997.

[19] S. Debnath, J. Qin, and M. Saeedifard, "Control and stability analysis of modular multilevel converter under low-frequency operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5329–5339, Sep. 2015.
[20] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.
[21] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter AC motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May 2014.
[22] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression method of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.
[23] B. Li, S. Zhou, D. Xu, R. Yang, D. Xu, C. Buccella, and C. Cecati, "An improved circulating current injection method for modular multilevel converters in variable-speed drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7215–7225, Nov. 2016.
[24] A. Antonopoulos, L. Angquist, L. Harnefors, and H.-P. Nee, "Optimal selection of the average capacitor voltage for variable-speed drives with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 227–234, Jan. 2015.
[25] B. Tai, C. Gao, X. Liu, and Z. Chen, "A novel flexible capacitor voltage control strategy for variable-speed drives with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 128–141, Jan. 2017.
[26] R. Yang, B. Li, G. Wang, C. Cecati, S. Zhou, and D. Xu, "Asymmetric mode control of MMC to suppress capacitor voltage ripples in low-frequency, low-voltage conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4219–4230, Jun. 2017.
[27] A. Mertens and J. Kucka, "Quasi two-level PWM operation of an MMC phase leg with reduced module capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6765–6769, Oct. 2016.
[28] M. I. Daoud, A. A. Elserougi, A. M. Massoud, R. Bojoi, A. S. Abdel-Khalik, and S. Ahmed, "Zero-/low-speed operation of multiphase drive systems with modular multilevel converters," *IEEE Access*, vol. 7, pp. 14353–14365, 2019.
[29] F. Liu, B. Wu, M. Pande, and N. R. Zargari, "Zero-speed operation of high-power PWM current-source-inverter-fed induction motor drive," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3020–3027, Jun. 2012.
[30] F. Zhao, G. Xiao, T. Zhu, X. Zheng, Z. Wu, and T. Zhao, "A coordinated strategy of low-speed and start-up operation for medium-voltage variable-speed drives with a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 709–724, Jan. 2020.
[31] W. Kawamura, K.-L. Chen, M. Hagiwara, and H. Akagi, "A low-speed, high-torque motor drive using a modular multilevel cascade converter based on triple-star bridge cells (MMCC-TSBC)," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 3965–3974, Sep. 2015.
[32] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.
[33] B. Jacobson *et al.*, "VSC-HVDC transmission with cascaded two-level converters," Cigre, Paris, France, Tech. Rep. B4-110, 2010.

AHMED ELSEROUGI (Senior Member, IEEE) was born in Alexandria, Egypt, in September 1982. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Faculty of Engineering, Alexandria University, Egypt, in 2004, 2006, and 2011, respectively. He is currently an Associate Professor with the Electrical Engineering Department, Alexandria University. His research interests include power electronics, HVDC and FACTS, renewable energy, and pulsed power applications.

IBRAHIM ABDELSALAM (Member, IEEE) received the B.Sc. degree (Hons.) and the M.Sc. degree in electrical engineering from the Arab Academy for Science and Technology and Maritime Transport, Egypt, in 2006, (Alexandria campus) and 2009 (Cairo campus), respectively, and the Ph.D. degree in power electronics from the University of Strathclyde, Glasgow, U.K., 2016. He is currently a Lecturer with the Department of Electrical Engineering, Arab Academy for Science and Technology and Maritime Transport, Cairo. His research interests are power electronic converters and their applications in wind energy conversion systems, and advanced control strategies of the multilevel voltage and current source converters.

AHMED MASSOUD (Senior Member, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees from the Faculty of Engineering, Alexandria University, Alexandria, Egypt, in 1997 and 2000, respectively, and the Ph.D. degree in electrical engineering from Heriot-Watt University, Edinburgh, U.K., in 2004. He is currently a Professor with the Department of Electrical Engineering, College of Engineering, Qatar University. He holds five U.S. patents. He has published more than 100 journal articles in the fields of power electronics, energy conversion, and power quality. His research interests include power electronics, energy conversion, renewable energy, and power quality.

SHEHAB AHMED (Senior Member, IEEE) received the B.Sc. degree from Alexandria University, Alexandria, Egypt, in 1999, and the M.Sc. and Ph.D. degrees from the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX, USA, in 2000 and 2007, respectively. He was with Schlumberger Technology Corporation, Houston, TX, USA, from 2001 to 2007, where he was involved in developing downhole mechatronic systems for oilfield service products. He was with Texas A&M University at Qatar, from 2007 to 2018. He is currently a Professor of electrical engineering with the CEMSE Division, King Abdullah University of Science and Technology, Saudi Arabia. His research interests include mechatronics, solid-state power conversion, electric machines, and drives.