

## Research Article

# Two-Step Single Slope/SAR ADC with Error Correction for CMOS Image Sensor

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Received 5 August 2013; Accepted 28 November 2013; Published 22 January 2014

Academic Editors: C. Grimm and P. Novak

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Conventional two-step ADC for CMOS image sensor requires full resolution noise performance in the first stage single slope ADC, leading to high power consumption and large chip area. This paper presents an 11-bit two-step single slope/successive approximation register (SAR) ADC scheme for CMOS image sensor applications. The first stage single slope ADC generates a 3-bit data and 1 redundant bit. The redundant bit is combined with the following 8-bit SAR ADC output code using a proposed error correction algorithm. Instead of requiring full resolution noise performance, the first stage single slope circuit of the proposed ADC can tolerate up to 3.125% quantization noise. With the proposed error correction mechanism, the power consumption and chip area of the single slope ADC are significantly reduced. The prototype ADC is fabricated using 0.18  $\mu\text{m}$  CMOS technology. The chip area of the proposed ADC is 7  $\mu\text{m} \times 500 \mu\text{m}$ . The measurement results show that the energy efficiency figure-of-merit (FOM) of the proposed ADC core is only 125 pJ/sample under 1.4 V power supply and the chip area efficiency is 84 k  $\mu\text{m}^2$ -cycles/sample.

## 1. Introduction

Column-parallel readout scheme is widely applied in high resolution CMOS image sensor designs. Compared with arraywise ADC schemes, column-parallel readout circuit could be realized with mediate speed, low power ADC, whose channel has much simple design complexity. Column-parallel single slope ADC is the most popular scheme used in the mass produced consumer electronic devices [1]. Although the architecture of the single slope ADC is very simple, the operation speed is low as well as the energy efficiency; thus, it is difficult to be applied in a high speed CMOS image sensor. SAR ADC is one of the best energy efficient ADC schemes [2]. However, in order to guarantee the linearity, SAR ADC either requires large chip area or calibration [3]. Although split capacitor technique can significantly reduce the total capacitance, capacitor array is still difficult to be matched

for a quantization resolution larger than 10 bits. Cyclic ADC has similar operation speed as the SAR ADC which can generate  $N$ -bit output code with  $N$  quantization cycles [4]. The drawback of the cyclic ADC is that its performance is highly dependent on the amplifier design, which consumes large power. Two-step single slope ADC was proposed in the prior art [5, 6] in order to solve the operation speed issue of the traditional single slope ADC. However, multitramp signals are required for the proposed scheme and the first single slope ADC must meet a full resolution noise specification.

In this paper, we report an 11-bit hybrid ADC for CMOS image sensor. The quantization circuit consists of a single slope ADC and a SAR ADC. The single slope ADC generates 3-bit quantization code and 1 redundant bit. After combining with the following 8-bit SAR ADC code using the error correction algorithm, the proposed 11-bit ADC could tolerate up to 3.125% of single slope quantization noise. The power

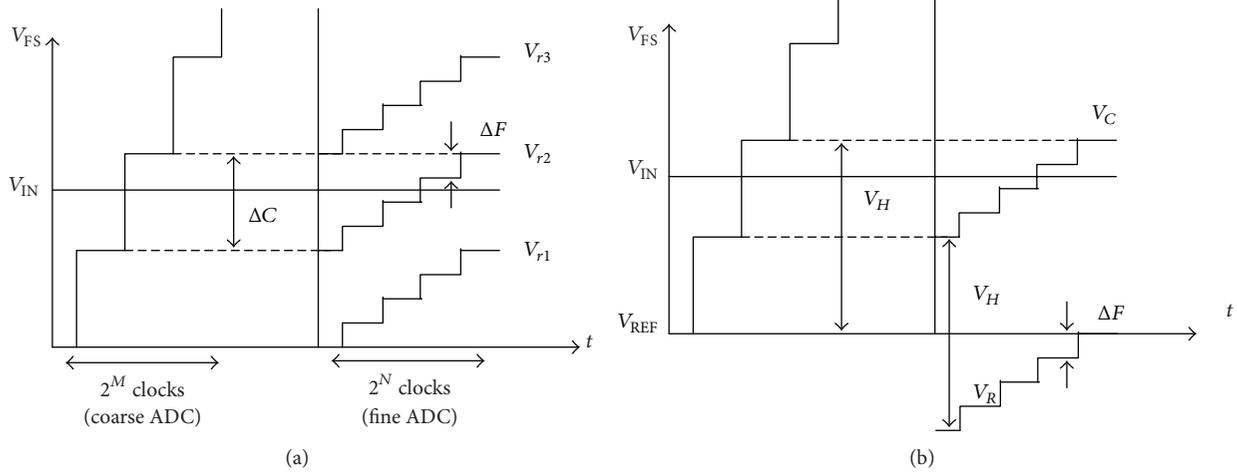


FIGURE 1: The principle of the conventional two-step single slope ADC [7].

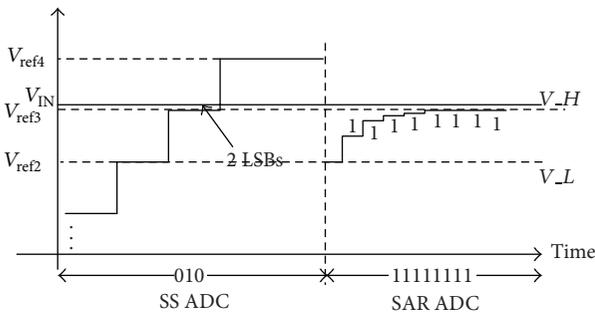


FIGURE 2: The example of how missing code is generated by the first stage ADC noise.

consumption and chip area of the single slope ADC can be significantly reduced.

This paper is organized as follows. Section 2 introduces the related prior art. Section 3 describes the proposed ADC with error correction mechanism and the ADC circuit implementation. Section 4 demonstrates the prototype experimental results. Section 5 delivers the conclusion.

## 2. Related Work

The principle of the conventional two-step single slope ADC is shown in Figure 1 [7]. Firstly, the input signal is quantized by the 3-bit single slope ADC. Then, the quantized 3-MSB code selects a certain reference from 8 slope voltages, if assuming that  $M = 3$  and  $N = 8$ . Secondly, the input signal is quantized by the following 8-bit single slope ADC and the final output code is generated by combing the 11-bit code.

Although the two-step single slope ADC increases the quantization speed by a factor of 10 compared with the traditional scheme, about 100 quantization cycles are still required. In order to further increase the energy efficiency, an 8-bit SAR ADC could be adopted in the second ADC stage instead of another 8-bit single slope ADC. Thus, the number of quantization cycles can be reduced from 100

to less than 25. Although two-step ADC can increase the quantization energy efficiency, either two-step single slope or single slope/SAR scheme has a drawback that the first single slope ADC requires full resolution noise performance. Figure 2 shows an example, where the input signal is set to 2-LSB higher than  $V_{ref3}$ .

If we assume that the quantization noise of the first 3-bit single slope ADC is larger than 2-LSB, the output quantization result of the first ADC stage probably equals "010" instead of the ideal value "011." Then,  $V_{ref2}$  and  $V_{ref3}$  are selected as the high reference voltage  $V_H$  and low reference voltage  $V_L$ , respectively, for the following SAR ADC quantization. Since the input signal  $V_{IN}$  is 2-LSB higher than  $V_H$ , the SAR ADC enters into the saturation region and finally an upper limit code "11111111" is generated. After combing these two codes, a quantization result "0101111111" is generated which is 2-LSB smaller than the expected output "011000010." As a result, missing code happens even if the SAR ADC is perfectly implemented.

## 3. Proposed ADC with Error Correction Mechanism

Designing an ultralow noise single slope ADC could solve the missing code problem; however, perfect single slope ADC requires large power consumption and chip area for the comparator design. Another way to solve the missing code issue is introducing assistant algorithm such as digital error correction mechanism.

The proposed two-step single slope/SAR ADC principal is shown in Figure 3. The single slope ADC generates 4-bit code which consists of 3-MSB code and 1 redundant bit. The 4-bit code selects reference voltages  $V_H$  and  $V_L$  for the SAR ADC, where  $V_H - V_L = V_{ref_n} - V_{ref_{n-2}}$ . Assuming that the first stage single slope quantization noise could be ignored, the 4-bit output code should be "0011." After SAR quantization, a "01000010" code is generated. Then, the redundant bit "1" is recombined with the SAR ADC code by using the error

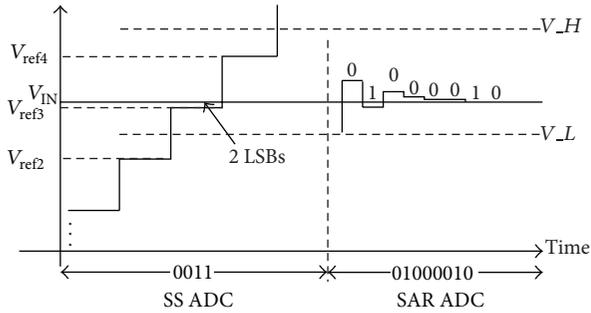


FIGURE 3: The operating principal of the proposed ADC without quantization noise.

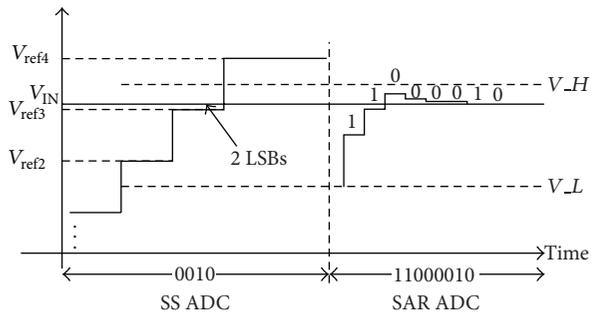


FIGURE 4: The operating principal of the proposed ADC with quantization noise.

correction algorithm as shown in (1). Finally, the proposed ADC generates an ideal digital result “00111000010” (450):

$$\begin{aligned}
 &0010 \\
 + &11000010 \\
 \hline
 &00111000010.
 \end{aligned} \tag{1}$$

If the quantization noise of the first stage single slope ADC cannot be ignored, the 4-bit output code is “0010,” as shown in Figure 4. The 4-MSB code selects other  $V_H$  and  $V_L$ , which are one-step voltage lower than the case shown in Figure 3. After SAR quantization, “11000010” is generated. Similarly, the 3-MSB, the 1 redundant bit “0010,” and “11000010” are recombined as “00111000010” (450) with the error correction algorithm being as shown in (2). It is clear that the final results both with and without quantization noise are the same. Thus the missing code due to the first stage ADC quantization noise is eliminated by adopting the error correction mechanism. The proposed error correction algorithm can be expressed as in (3):

$$\begin{aligned}
 &0011 \\
 + &01000010 \\
 \hline
 &00111000010,
 \end{aligned} \tag{2}$$

$$D_{out} = D[11 : 8] 2^7 + D[7 : 0]. \tag{3}$$

The noise margin is defined as the voltage difference between the input voltage  $V_{IN}$  and  $V_H$ , where  $\Delta V$  equals

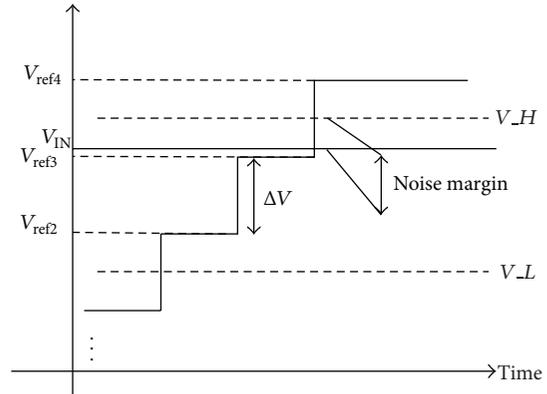


FIGURE 5: The noise margin definition of the proposed error correction mechanism.

$V_{pp}/2^4$ . The maximum noise margin is  $\Delta V/2$ , when the single slope ADC quantization noise can be ignored. Therefore, the error correction algorithm can tolerate up to  $\Delta V/2$  first stage quantization noise. If the input signal has 1.2 V voltage range  $V_{pp}$  up to 37.5 mV (3.125%) single slope ADC noise can be corrected (Figure 5).

Since the single slope ADC has a large noise margin, the design complexity can be significantly relaxed. This work adopts an ultralow power single slope ADC scheme as shown in Figure 6. Two main input referred noise sources of the single slope ADC include the  $KT/C$  noise introduced by capacitor  $C_{os}$  during reset phase (S1) and the random noise of inverter transistors. A transient noise simulation is performed with  $C_{os} = 50$  fF and 1.2 V power supply. The simulated noise frequency band is up to  $\times 1000$  clock frequency. Minimum transistor size is applied in order to reduce the short circuit current consumption. 50 simulations indicate that the peak input referred single slope ADC noise is smaller than  $18$  mV<sub>pp</sub> while maintaining more than 1/2 noise margin. Although the capacitor  $C_{os}$  can be further scaled down, the saved chip area is insignificant when the entire 11-bit ADC area is taken into account.

The SAR ADC takes charge of the 8-bit LSB quantization. With standard structure as described in [2], more than 128 unit capacitors are required, leading to an unaffordable chip area. In order to reduce the capacitor array size, this work adopts 5-bit/3-bit split capacitor scheme, where only 32 unit capacitors are required. The schematic of the SAR ADC is shown in Figure 7. According to the Monte-Carlo simulation, the SAR ADC can achieve 8-bit linearity with 30 fF and  $5 \mu\text{m} \times 5 \mu\text{m}$  metal-insulator-metal (MIM) unit capacitor.

#### 4. The Experimental Result

The proposed two-step single slope/SAR ADC is fabricated using  $0.18 \mu\text{m}$  CMOS process and the chip layout is shown in Figure 8. Each ADC channel occupies  $7 \mu\text{m} \times 500 \mu\text{m}$  chip area in order to integrate more than 1000 channels in an ADC array for high pixel resolution CMOS image sensor applications. The signal source follower is used to buffer the pixel analog voltage. The digital buffer is designed to scan out

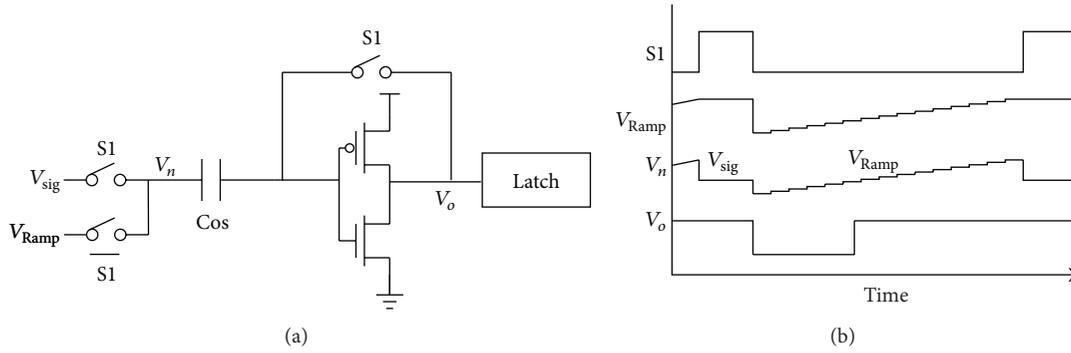


FIGURE 6: The schematic and operating timing sequence of the single slope ADC.

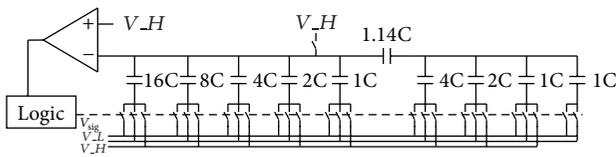


FIGURE 7: The schematic of the SAR ADC.

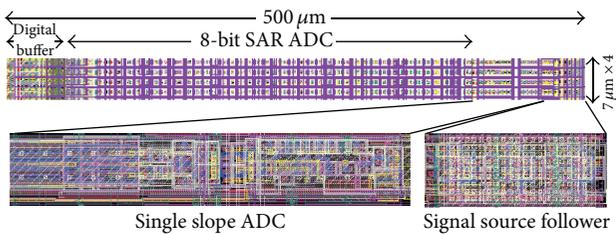


FIGURE 8: The fabricated chip layout of the proposed ADC.

the ADC array digital output data. Therefore, the ADC core only occupies less than  $7 \mu\text{m} \times 400 \mu\text{m}$  area and the first stage single slope ADC requires only 13% chip area of the ADC core.

The integrated nonlinearity (INL) of the first stage single slope ADC is shown in Figure 9. The nonlinearity indicates the input offset voltage of the single slope ADC. According to Figure 9, about 20 LSBs systematic offset voltage exists for 12-bit quantization resolution. This offset voltage is much less than 37.5 mV, which can be easily corrected by the error correction algorithm without degrading the ADC performance. The differential nonlinearity (DNL) of the SAR ADC is shown in Figure 10. A  $+0.5/-1$  LSB DNL is achieved leading to an 8-bit linearity. Only two DNL tones are  $-1$  LSB, while others are located within  $+0.5/-0.5$  LSB region. The SAR ADC output random noise is measured as shown in Figure 11. With 10,000 samples, the SAR ADC indicates a standard deviation random noise about 1.2-LSBrms. Since the DAC reference voltage is 150 mV for a 1.2 V input signal range, 1.2-LSB refers to 0.7 mVrms quantization noise.

The power consumption distribution of the whole column-parallel circuit is shown in Figure 12, including the source follower, ADC, and scan buffer. The power consumption of the proposed two-step single slope/SAR ADC is  $5 \mu\text{W}$

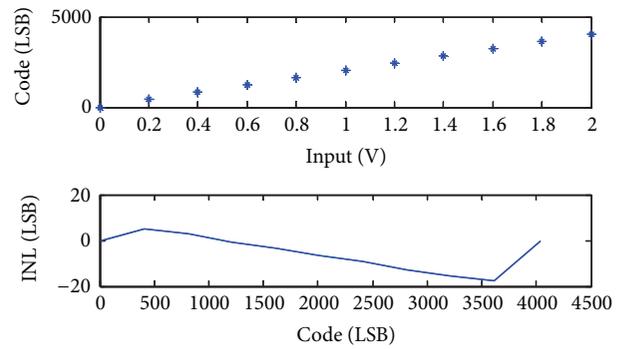


FIGURE 9: The measured INL of the single slope ADC.

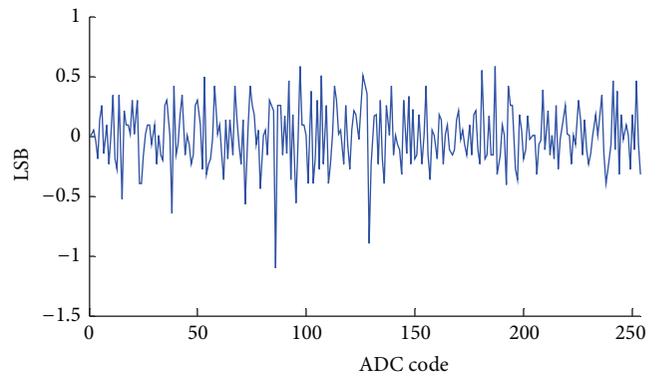


FIGURE 10: The measured DNL of the SAR ADC.

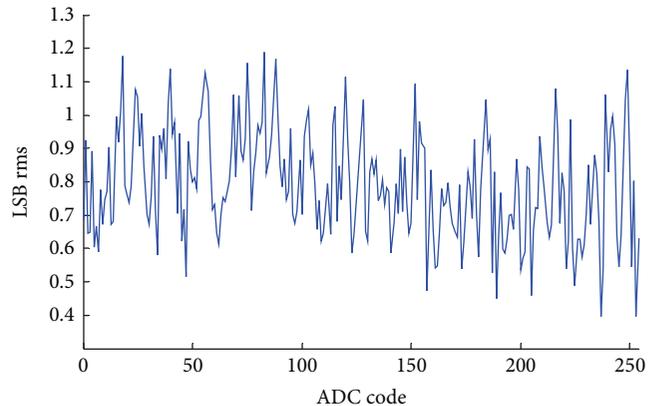


FIGURE 11: The measured SAR ADC output noise.

TABLE 1: The summarized comparison with other types of column-parallel architectures.

| Specification           | This work                                  | Two-step SSADC [5]                   | Cyclic ADC [4]                             | Calibrated SAR ADC [3]                     |
|-------------------------|--|--------------------------------------|--|--|
| Process                 | 0.18 $\mu\text{m}$                         | 0.25 $\mu\text{m}$                   | 0.25 $\mu\text{m}$                         | 0.18 $\mu\text{m}$                         |
| Quantization resolution | 11-bit                                     | 10-bit                               | 12-bit                                     | 10-bit                                     |
| Chip area               | $7 \times 500 \mu\text{m}^2$               | $7.4 \mu\text{m}$ pitch              | $40 \times 2200 \mu\text{m}^2$             | $14 \times 700 \mu\text{m}^2$              |
| Power consumption       | $5 \mu\text{W}$<br>at 40 Ksamples/s        | $75 \mu\text{W}$<br>at 60 Ksamples/s | 1.9 mW (full chip)<br>at 1.9 Msamples/s    | 1.5 mW (full chip)<br>at 2 Msamples/s      |
| Quantization cycles     | 24 cycles/sample                           | >160 cycles/sample                   | 12 cycles/sample                           | 13 cycles/sample                           |
| DNL                     | +0.5/-1 LSB                                | <+/-1 LSB                            | +0.76/-0.81 LSB                            | 0.34 LSB                                   |
| FOM1                    | 125 pJ/sample                              | 1250 pJ/sample                       | 1 nJ/sample                                | 750 pJ/sample                              |
| Energy efficiency       | ADC core                                   | ADC core                             | full chip                                  | full chip                                  |
| FOM2                    | 84 k                                       | —                                    | 1056 k                                     | 127 k                                      |
| Area efficiency         | $\mu\text{m}^2 \cdot \text{cycles/sample}$ | —                                    | $\mu\text{m}^2 \cdot \text{cycles/sample}$ | $\mu\text{m}^2 \cdot \text{cycles/sample}$ |

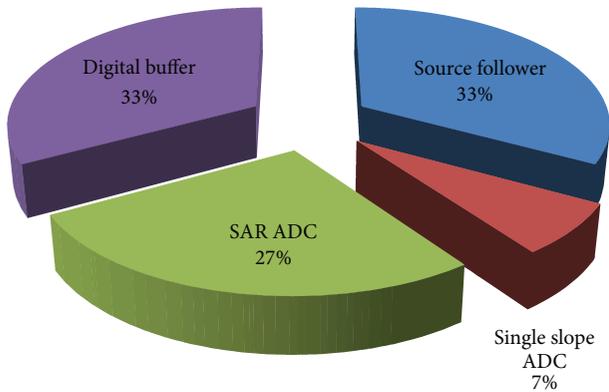


FIGURE 12: The measured power consumption distribution of the column-parallel circuit.

with 1.2 V power supply under 40 Ksamples/s. The single slope ADC consumes  $1 \mu\text{W}$ , while the SAR ADC consumes the rest  $4 \mu\text{W}$ . The specification of the proposed ADC is summarized with some other prior arts in CMOS image sensor field as shown in Table 1. Two figure-of-merits (FPM) are compared including the energy efficiency and chip area efficiency. The energy efficiency of the proposed ADC could be estimated as 125 pJ/sample. The chip area efficiency is defined as the chip area  $\times$  quantization cycles per sample, resulting in  $84 \text{ k} \mu\text{m}^2 \cdot \text{cycles/sample}$  of this work.

### 5. Conclusion

This paper presents a high energy efficiency high chip area efficiency column-parallel ADC for CMOS image sensor applications. The proposed ADC consists of a single slope ADC and a SAR ADC. The single slope ADC generates 3-MSB code and 1 redundant bit, which is combined with the following 8-bit SAR ADC quantization result using the proposed error correction algorithm. Up to 3.125% quantization noise of the first stage ADC can be tolerated; thus, the chip area and power consumption of the single slope ADC are significantly reduced. The ADC prototype

is fabricated using  $0.18 \mu\text{m}$  CMOS process. Measurement results show a 125 pJ/sample core energy efficiency and  $84 \text{ k} \mu\text{m}^2 \cdot \text{cycles/sample}$  chip area efficiency.

### Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

### Acknowledgment

This paper was made possible by NPRP Grant no. NPRP 5-080-2-028 from Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

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