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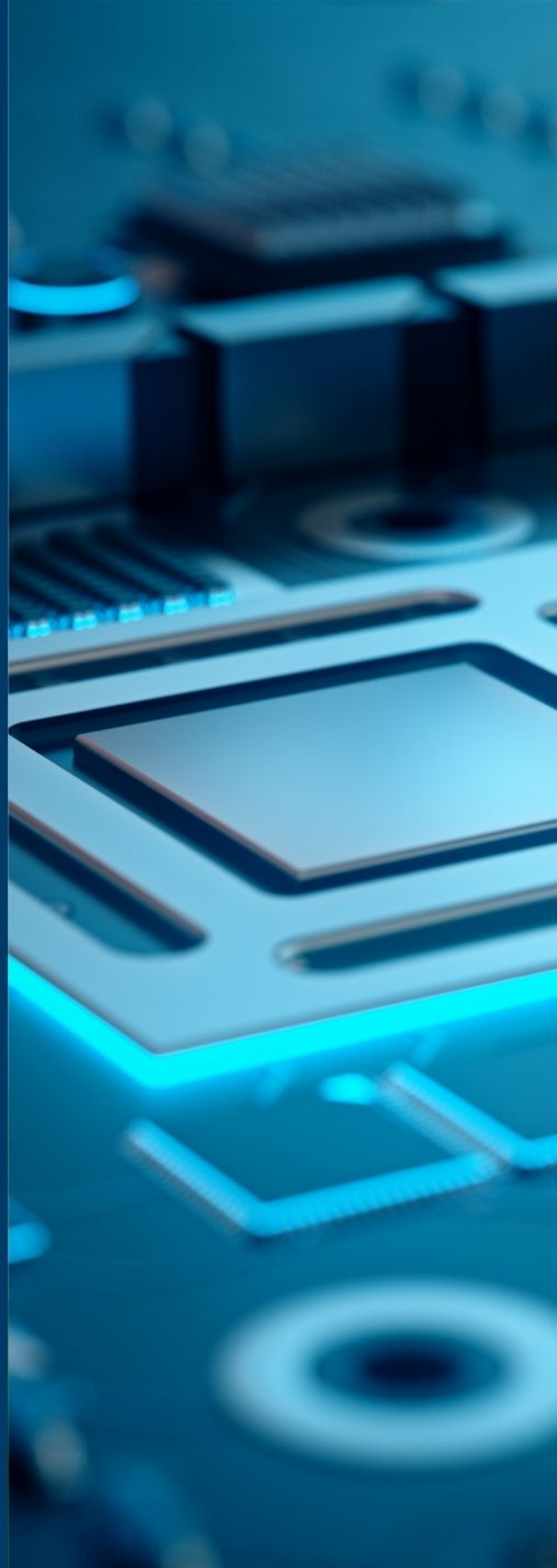
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ORIGINAL RESEARCH

Performance analysis and control of a novel 7-level active neutral point clamped (ANPC) topology

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Abstract

This paper introduces a novel 7-level active neutral-point clamped (ANPC) switched capacitor multilevel inverter (SCMLI) with voltage-boosting capabilities. The proposed converter can produce seven levels and a voltage boosting of 1.5 times with a single dc source. For boosting the voltage, two self-balanced switched capacitors and two dc link capacitors with active neutral point are used with nine switches. For controlling the output voltage, the level-shifted modulation technique and modified nearest level control technique is used. The performance of the converter is evaluated with both modulation techniques. The operation of the proposed SCMLI and the design of capacitors for the proposed circuit is discussed in detail. The proposed topology can eliminate the leakage current and has reduced voltage stress across switches which makes it suitable for solar photovoltaic applications. The proposed converter is compared with some other recently introduced converters in terms of voltage gain, the number of components used, and the voltage stress across the switches. For verifying the performance of the proposed circuit, the experimental and simulation results are presented in the paper. The experimental results closely agree with the simulation and theoretical studies. The total harmonic distortion (THD) in the output voltage and efficiency is compared with both modulation techniques.

1 | INTRODUCTION

For high-power applications, the conventional two-level inverters cannot be used owing to various problems like high voltage (dv/dt) stress, high total harmonic distortion (THD) in output voltage and low efficiency. The MLIs are useful in high and medium-power applications in renewable energy, ac drives, transportation, fuel cells and electric vehicles. The key benefits of MLIs [1] are low voltage stress on switches, the improved harmonic profile of output waveform, high efficiency and small filter requirements.

There are generally three categories of standard MLIs including neutral-point-clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). In the hybrid MLI, flying capacitors (FCs) are critical for generating intermediate voltage levels. For maintaining capacitor voltage balancing issues in NPC and FC, additional balancing circuits, voltage and current sensors,

or algorithms with complex structures are required [2]. Further, only half of the source voltage is generated at the load terminals. Moreover, for achieving high AC voltage, more bulky and expensive inverter system with a front-end DC-DC boost converter or a load-end transformer is required. All of this leads to more complexity in the control system, as well as a decline in performance. Renewable energy sources, such as solar photovoltaic systems and fuel cells, have low voltage at the output and should be converted to higher ac-voltage [3, 4]. A common approach is to combine a back-end MLI with a typical front-end DC-DC booster conversion stage [5, 6].

Efforts are made by researchers to boost the output voltage level without using any transformers and inductors in the output. The switched-capacitors (SCs) inverters have advantages such as high voltage gain and a high stepped output voltage waveform. These inverters are better suited for medium and high-voltage applications [7, 8]. In [9–27], the

different topologies have been presented by researchers utilizing switched-capacitors with the multilevel inverter to synthesize switched-capacitor multilevel inverter (SCMLI). There are benefits and drawbacks to each of the topologies proposed by the researchers.

The SCMLI circuit presented in [9, 10] has a voltage-boosting factor of increased gain. A variety of voltages can be generated by the SC structures and the H-bridge generates varied output polarities. In addition, to achieve greater voltage levels, the topologies suggested in [9, 10] necessitate a significant number of capacitors, diodes, and other semiconductor circuitry. Voltage stress is also present in switches of H-bridges, which are involved in polarity generation, among the various semiconductor devices. To solve the double-stage boost MLIs problem, the authors in [11–13] have suggested a single-stage inverter circuit. Such topologies are modular and do not require an H-bridge to produce zero or negative levels.

In [26] the topology consists of two capacitors, nine unidirectional switches, and one diode. The switch voltage stress in the converter is high and the voltage gain is $4V_{in}$. New SCMLI topologies with reduced voltage stress are shown in [17, 24]. Although the number of semiconductor devices are high, the voltage stress on each device is reduced. A novel quadratic voltage boost-type inverter is described in [19, 20, 27], and to maximize high voltage gain and decrease switch count. The topology in [27] utilizes two SCs with voltage ratings of V_{in} and $2V_{in}$ and twelve switches having voltage stress equal to $2V_{in}$. A novel boost type 9L inverter topology is recommended in [20] to minimize the total number of switches, although the overall switches are still high and bearing the voltage stress of $4V_{in}$. Although the three SCs in [5] are employed with voltage ratings of V_{in} and $2V_{in}$, the number of on-state conducting devices and overall power components is significant. Additionally, the switch is under $4V_{in}$ of voltage stress. A different quadratic boost topology with more power components is suggested in [21]. In [22], a novel compact quadratic voltage boost (CQB) inverter with less number of components is proposed.

A 7L mid-point-clamped inverter [28] with an overall voltage gain of 1.5 and nine active power switches can be made using one full-bridge cell that has been SC-integrated. In terms of achieving the same number of output voltage levels, a similar strategy is also employed in [29]. An SC-integrated cell is employed in topologies proposed in [30–32] and it can be determined that the two additional capacitors are charged through the combination of the switches and diodes. The topologies mentioned in [33–38] are the form of midpoint clamped MLIs known as active boost neutral point clamped (ABNPC) MLI topology. The authors in [33] have suggested two distinct circuit topologies for the mid-point-clamped SC-MLIs to boost both the number of output voltage levels and the converter's total voltage gain. A similar topology is developed in [34, 35, 39] with ten power switches, the same number of output voltage levels, and the same gain. The decreased switch-count mid-point-clamped SC-MLI is proposed in [36] and can provide 7L output voltage and voltage gain of 1.5 times. Another application of such topologies is the 7L-mid-point-clamped inverter introduced in [37], which requires an additional switch in com-
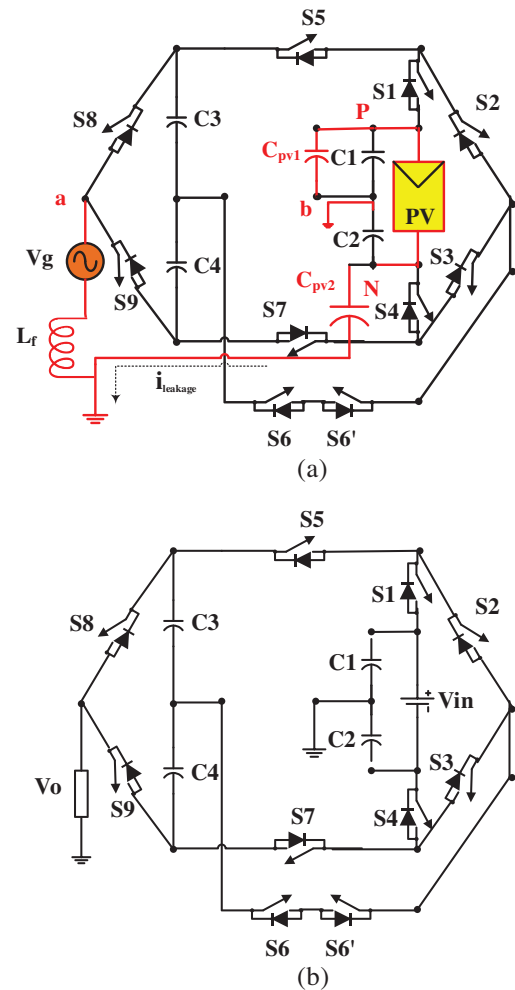

FIGURE 1 (a) Leakage current in grid-connected PV applications. (b) Proposed 7L ANPC SCMLI topology.

parison to the 8-switch-based 7L mid-point-clamped inverter. The methodology improves the production of a highly efficient converter in regards to output power ratio, but it constrains the modulation index. The authors in [38] employs a similar method but with the assistance of an SC-integrated FB cell.

A 7L neutral point clamped SCMLI is presented in [40] with twelve switches and improved efficiency. In [41, 42], another 7L ANPC topology is presented with a reduced number of power switches and self-balanced capacitors but the performance parameters are not much improved. Due to their high efficiency and low cost, transformerless inverter topologies have gained increased attention in photovoltaic (PV) generation systems. Transformerless grid-tied PV inverters must carefully address the leakage current in order to adhere to safety standards. Using the neutral point clamped (NPC) architecture, leakage current can be effectively reduced. The equivalent circuit is drawn in the figure below. While, P and N represents input terminals of the input dc source (i.e. PV arrays), respectively. Whereas V_{aN} and V_{bN} are the output voltages of the proposed inverter relative to the N terminal of the PV as shown in Figure 1a. Here, a and b are the output terminals of the differ-

ential mode voltage (V_{dm}), and Cpv1 and Cpv2 are photovoltaic (PV) parasitic capacitors against the ground. The leakage current is given by $i_{CM} = C \frac{dV_{CMT}}{dt}$ is because of common mode voltage given by $(V_{an} + V_{bn})/2$ and differential voltage given by $V_{an} - V_{bn}$. In this topology if VCMT is made constant, then the leakage current will be effectively made to zero. The detailed derivation is shown in [40] and it is shown that for mid-point-based topologies VCMT is equal to V_{bN} which is equal to V_{C2} which is constant at $0.5V_{in}$. From this analysis, it is clear that the variation of the CMT remains constant at $0.5V_{in}$ at each switching for the proposed seven-level circuit topology. Therefore, the proposed topology naturally maintains the total CMV constant at $0.5V_{in}$ because of the dc-link capacitor bridge arm which practically eliminates the leakage current.

In this paper, a 7-level ANPC SC-MLI with voltage boosting of 1.5 has been proposed. The ANPC MLI is a suitable option since the output voltage is evaluated with reference to the neutral point and they are based on dc-link neutral-balanced capacitors. As a result, the issue of leakage current in grid-connected PV applications can be significantly avoided, while at the same time a single input dc source provides the multilevel load voltage waveform. The proposed inverter can be used for the applications [43] like grid tied PV systems, variable frequency drives, ventilators, pumps, roll mills, laminators, downhill conveyers etc.

Most of the work in [28–42] has used only one modulation technique to control the output voltage of the inverter. In this work we have compared the performance of the inverter with low and high frequency modulation techniques. The proposed inverter can be used for the applications like grid tied PV systems, variable frequency drives, ventilators etc.

2 | PROPOSED 7L ANPC SC-MLI TOPOLOGY

For the proposed 7-level ANPC based SCMLI, a comprehensive description of the schematic circuitry and its modes of operation are detailed.

The organization of the remaining portion of the paper is as follows. The modelling, structural configuration and switching modes are discussed in Section 2. The performance analysis of output voltage under level shifted pulse width modulation (LSPWM) and nearest level control (NLC) scheme is addressed in Section 3. NLC control strategy displays the more efficient and improved harmonic results than LSPWM scheme because the switching frequency in NLC is equal to the fundamental frequency. The output harmonics and THD can be significantly controlled in NLC. However, for other applications like grid connected operation of inverter, high frequency level shifted PWM is more popular and practical than NLC because frequency change is much easier in LSPWM as compared to NLC. Section 4 deals with the power loss analysis including conduction losses, switching losses and ripple losses. The comparison of LSPWM and NLC scheme is studied in Section 5. In Section 6, the comparative study is explained. The implementation of hardware is presented in Section 7. Finally, the paper concludes in Section 8.

TABLE 1 Switching sequence for proposed 7L inverter topology
↑= charging, ↓= discharging.

Modes	V_O	C_1	C_2	C_3	C_4	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
I	$0V_{in}$	↑	↑↓	↓	-	0	0	1	1	0	1	0	1	0
II	$0.5V_{in}$	↑↓	↑	↑	↑	1	0	0	1	1	0	1	1	0
III	$1V_{in}$	↑↓	↑	↓	-	1	1	0	0	0	1	0	1	0
IV	$1.5V_{in}$	↑↓	↑	↓	↓	1	1	1	0	0	0	1	1	0
V	$-0.5V_{in}$	↑	↑↓	-	-	0	0	0	1	0	0	1	0	1
VI	$-1V_{in}$	↑	↑↓	-	↓	0	0	1	1	0	1	0	0	1
VII	$-1.5V_{in}$	↑	↑↓	↓	↓	0	1	1	1	1	0	0	0	1

2.1 | 7L inverter topology configuration

The proposed 7L inverter topology configuration with boosting of 1.5 consists of eight (unipolar) plus one (bipolar) switch, two SCs (C_3 and C_4) and a single dc-source as depicted in Figure 1b. All the capacitors are charged up to $0.5V_{in}$. The capacitors (C_1, C_2) are charged to $0.5V_{dc}$ as these are connected in parallel with the input dc-source. The switches (S_1, S_4, S_5 and S_7) are conducting to charge the capacitors (C_3, C_4) and these capacitors are discharged based on the demand of the load. The switching states of switches and charging/discharging of capacitors are illustrated in Table 1.

2.2 | Operating modes of proposed 7L inverter topology

The various mode of operations of 7L ANPC SC-MLI topology are depicted in Figure 2 and also the charging and discharging paths are shown. The switching modes are given as $0V_{in}$, $0.5V_{in}$, $1V_{in}$, $1.5V_{in}$, $-0.5V_{in}$, $-1V_{in}$ and $-1.5V_{in}$, respectively.

Mode I ($-V_{C2} + V_{C3}$): In Figure 2a, the SC C_4 is not connected to load or source, but the C_2 and C_3 are discharging through load. It yields the output voltage of $0V_{in}$.

- For charging: $V_{in} \rightarrow↑ C_1 \rightarrow↑ C_2$
- For output: ↓ $C_2 \rightarrow S_4 \rightarrow S_3 \rightarrow S_6' \rightarrow S_6 \rightarrow↓ C_3 \rightarrow S_8 \rightarrow V_O$

Mode II (V_{C1}): In Figure 2b, the SC C_3 and C_4 are connected through V_{in} source for charging, but the C_1 is discharging through the load. It yields the output voltage of $0.5V_{in}$.

- For charging: $V_{in} \rightarrow↑ C_1 \rightarrow↑ C_2$ and $V_{in} \rightarrow S_1 \rightarrow S_5 \rightarrow↑ C_3 \rightarrow↑ C_4 \rightarrow S_7 \rightarrow S_4$
- For output: ↓ $C_1 \rightarrow S_1 \rightarrow S_5 \rightarrow S_6 \rightarrow S_8 \rightarrow V_O$
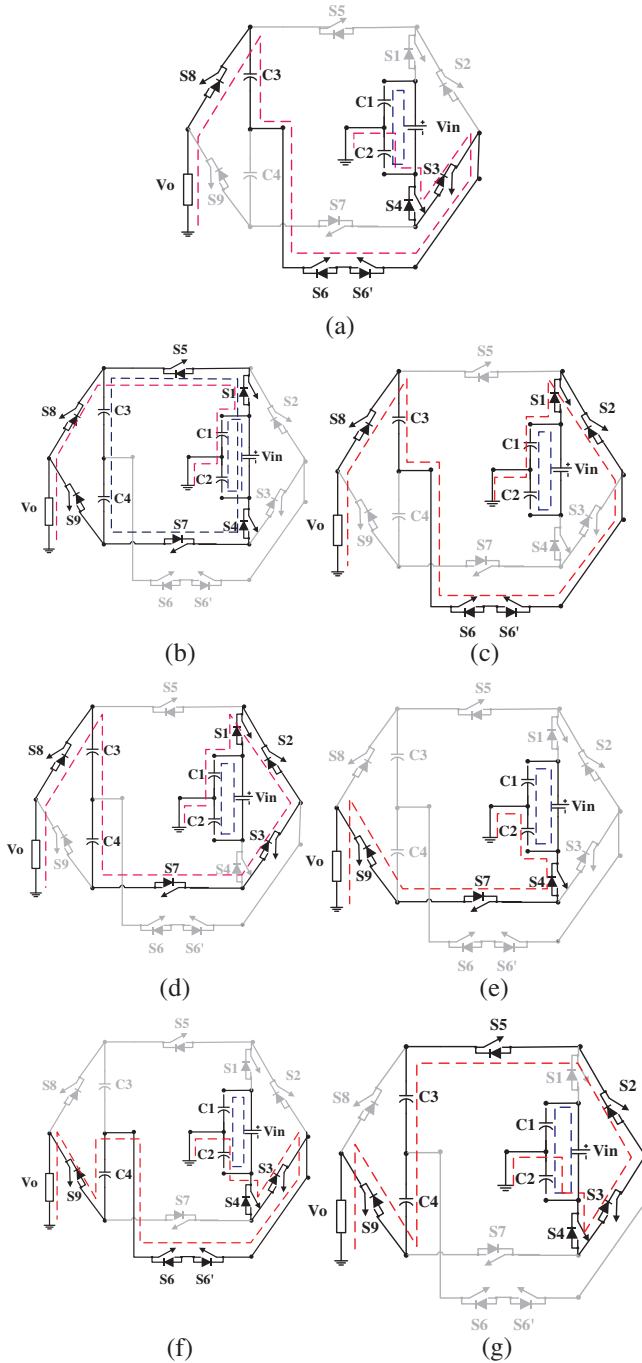
FIGURE 2 Operating modes of proposed 7L inverter topology. (a) Mode I operation. (b) Mode II operation. (c) Mode III operation. (d) Mode IV operation. (e) Mode V operation. (f) Mode VI operation. (g) Mode VII operation.

Mode III ($V_{C1} + V_{C3}$): In Figure 2c, the SC C_4 is not connected to load or source, but the C_1 and C_3 are discharging through the load. It yields the output voltage of $1V_{in}$.

- For charging: $V_{in} \rightarrow \uparrow C_1 \rightarrow \uparrow C_2$
- For output: $\downarrow C_1 \rightarrow S_1 \rightarrow S_2 \rightarrow S_6{'} \rightarrow S_6 \rightarrow \downarrow C_3 \rightarrow S_8 \rightarrow V_O$

Mode IV ($V_{C1} + V_{C4} + V_{C3}$): In Figure 2d, the SC C_1, C_3 and C_4 are discharging through load and C_1 and C_2 are continuously charging. It yields the output voltage of $1.5V_{in}$.

- For charging: $V_{in} \rightarrow \uparrow C_1 \rightarrow \uparrow C_2$
- For output: $\downarrow C_1 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_7 \rightarrow \downarrow C_4 \rightarrow \downarrow C_3 \rightarrow S_8 \rightarrow V_O$

Mode V ($-V_{C2}$): In Figure 2e, the SC C_3 and C_4 are not connected to load or source, but the C_2 is discharging through the load. It yields the output voltage of $-0.5V_{in}$.

- For charging: $V_{in} \rightarrow \uparrow C_1 \rightarrow \uparrow C_2$
- For output: $\downarrow C_2 \rightarrow S_4 \rightarrow S_7 \rightarrow S_9 \rightarrow V_O$

Mode VI ($-V_{C2} - V_{C4}$): In Figure 2f, the SC C_3 is not connected to load or source, but the C_2 and C_4 are discharging through the load. It yields the output voltage of $-1V_{in}$.

- For charging: $V_{in} \rightarrow \uparrow C_1 \rightarrow \uparrow C_2$
- For output: $\downarrow C_2 \rightarrow S_4 \rightarrow S_3 \rightarrow S_6{'} \rightarrow S_6 \rightarrow \downarrow C_4 \rightarrow S_9 \rightarrow V_O$

Mode VII ($-V_{C2} - V_{C3} - V_{C4}$): In Figure 2g, the SC C_2, C_3 and C_4 are discharging through load and C_1 and C_2 are continuously charging. It yields the output voltage of $-1.5V_{in}$.

- For charging: $V_{in} \rightarrow \uparrow C_1 \rightarrow \uparrow C_2$
- For output: $\downarrow C_2 \rightarrow S_4 \rightarrow S_3 \rightarrow S_2 \rightarrow S_5 \rightarrow \downarrow C_3 \rightarrow \downarrow C_4 \rightarrow S_9 \rightarrow V_O$

3 | MODULATION SCHEME FOR OUTPUT VOLTAGE CONTROL

The output voltage of the proposed 7-level ANPC topology has been controlled using a high-frequency modulation scheme namely level shifted pulse width modulation (LSPWM) and a low-frequency modulation scheme i.e. nearest level control (NLC). The performance under the two modulation schemes has been evaluated.

3.1 | Level shifted pulse width modulation (LSPWM) scheme

The suggested topology adopts the common multi-carrier level-shifted pulse width modulation technique, as illustrated in Figure 3a. M_r, $2M_r$ and $3M_r$ are the amplitudes of the carrier signals. For increase of each amplitude, the carrier signal has kept at the same frequency and phase. Comparing the basic waveform reference (V_{ref}) and the carrier signal reference signal (M_{ref}) having magnitudes (M_r, $2M_r$ and $3M_r$), the switching angles α_1, α_2 and α_3 are obtained. The logic functions are used to create the matching pulse signals. Figures 3b and c depict the simulated output current and voltage waveform and THD obtained in output voltage waveform (22.23%) using LSPWM
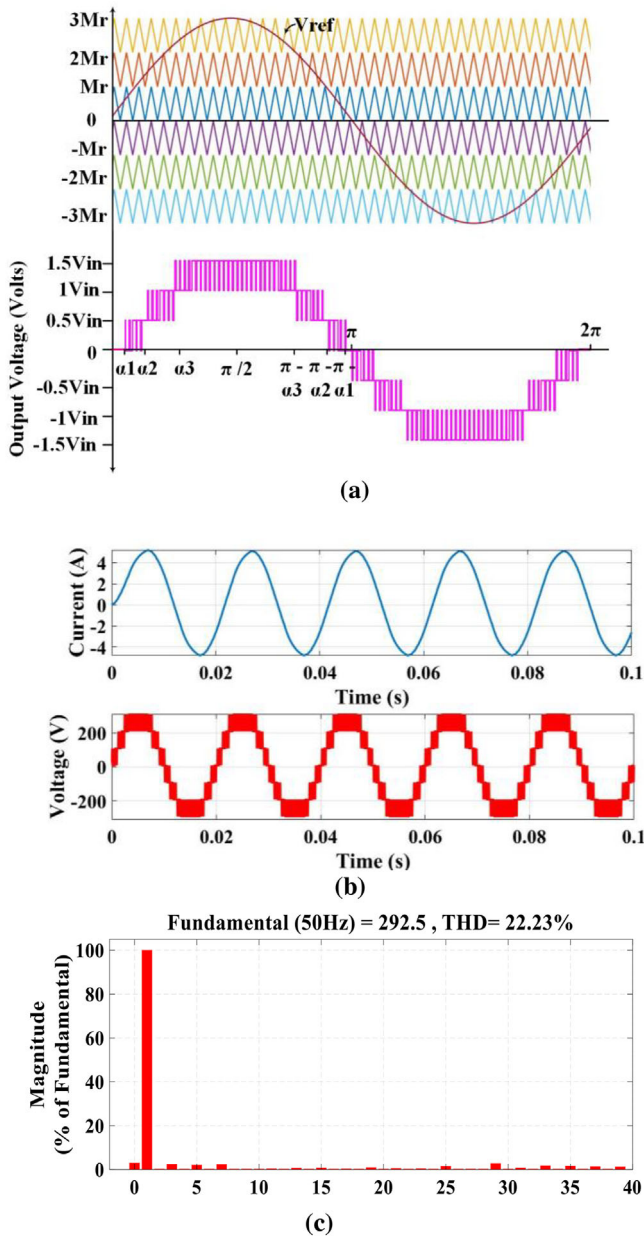
FIGURE 3 (a) Implementation of LSPWM. (b) Output voltage and current waveforms. (c) THD obtained in output voltage.

scheme, respectively. The circuit diagram of LSPWM scheme is shown in Figure 4.

3.2 | Nearest level control scheme (NLC)

A schematic operation of NLC is depicted in Figure 5a. Since the load requirement and power signal are both sinusoidal, the reference signal is often a sine wave. This sine signal is quantized with a reference to the necessary levels. The quantized signal is then sent to the pulse generator, which uses it to generate pulses while keeping track of the inverter's parameters. It is possible to generate a signal whose average value is the desired value by applying each voltage level for a certain amount

of time. NLC gives more accurate results for a higher modulation index ($m > 0.7$). In NLC, the modulation index is varied with a change in reference voltage (V_{ref}) keeping output level (N) constant. Figures 5b and c illustrate the simulated output current and voltage waveform, and THD obtained in the output voltage waveform (12.21%) using NLC scheme respectively. The circuit diagram of the NLC modulation scheme is shown in Figure 6.

3.3 | Design of capacitors

The selection of capacitors for proposed SCMLI is based on largest discharge time of capacitors. As can be seen from Figure 7, the largest discharge time for SC3 is [α_2 to $(\pi - \alpha_2)$] (mode III and IV), and for SC4 is [$(\pi + \alpha_2)$ to $(2\pi - \alpha_2)$] (mode VI and VII). The maximum charge needed for the capacitor is presented in Equation (1), where i_L stands for the load current, $\omega = 2\pi f$, and α_1, α_2 and α_3 are the firing angles when the output is first time changing from 0 to V_{in}, V_{in} to $2V_{in}$ and $2V_{in}$ to $3V_{in}$, respectively. The value of firing angles α_1, α_2 and α_3 can be obtained from Equation (2).

$$\Delta Q = \int_{\alpha_2}^{\pi - \alpha_2} \frac{i_L}{\omega} d\omega t \tag{1}$$

$$\left. \begin{aligned} \alpha_1 &= \sin^{-1}\left(\frac{2A_t}{M_{ref}}\right)/2\pi f_{ref} \\ \alpha_2 &= \sin^{-1}\left(\frac{3A_t}{M_{ref}}\right)/2\pi f_{ref} \\ \alpha_3 &= \sin^{-1}\left(\frac{4A_t}{M_{ref}}\right)/2\pi f_{ref} \end{aligned} \right\} \tag{2}$$

$$\Delta Q_{c_3} = \frac{4V_{in}}{2\pi f R_L}\left((\pi - \alpha_2) - \alpha_2\right) \tag{3}$$

$$\Delta Q_{c_4} = \frac{4V_{in}}{2\pi f R_L}\left((2\pi - \alpha_2) - (\pi + \alpha_2)\right) \tag{4}$$

where A_t is the magnitude of the triangle signal, and M_{ref} is the magnitude of the reference signal.

At the purely resistive load, the maximum value of voltage ripple and discharge occurs. Therefore, for capacitors C_3 and C_4, the Q (charge quantity flowing from capacitors) may be determined as in Equations (3) and (4), respectively.

Since R_L is the resistive load and f is the inverter output voltage frequency, one can use Equation (5) to get the ripple value (V_{rip}) across the capacitor C_3. The best value for each capacitor (C_{opt}) is shown in Equation (6), where the minimal capacitance needed to store the necessary energy required to be supplied. Similarly, the V_{rip} and C_{opt} can be discovered for C_4.

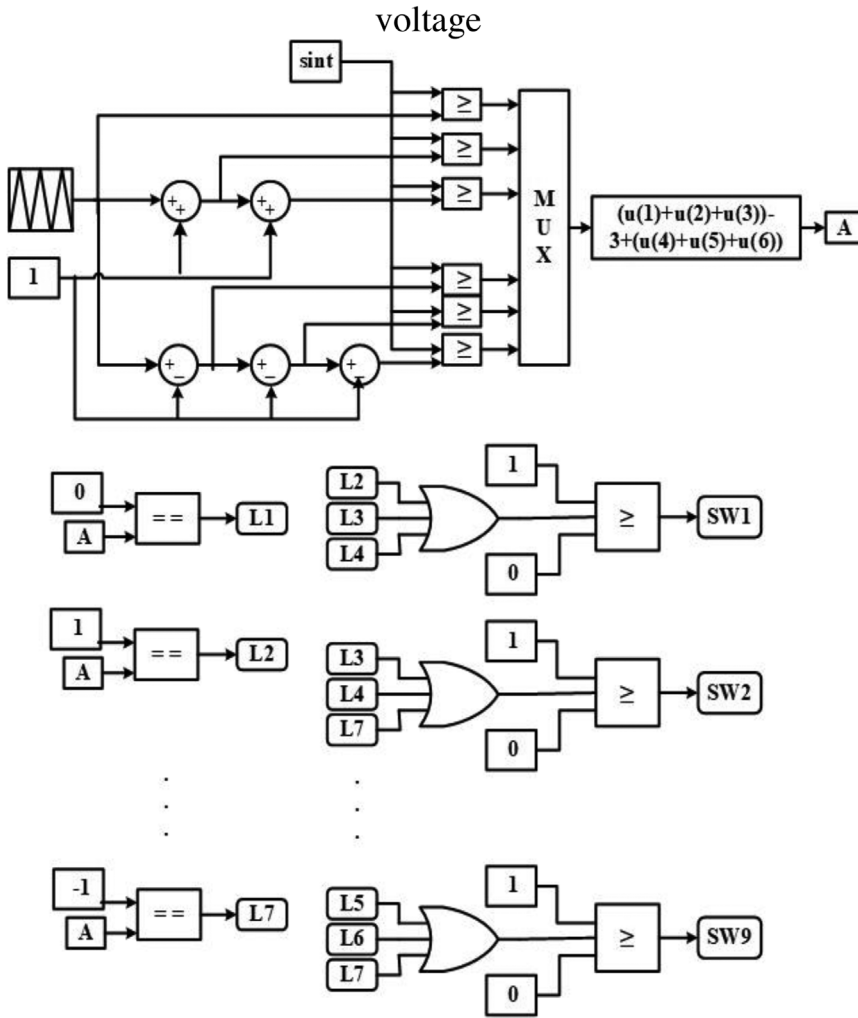$$\Delta V_{rip} = \frac{4V_{in}}{2\pi f R_L C} \times (\pi - 2\alpha_2) \tag{5}$$

FIGURE 4 LSPWM circuit diagram.

$$C_{\mathrm{opt}} = \frac{4V_{\mathrm{in}}}{2\pi f R_{\mathrm{L}} \Delta V_{\mathrm{rip}}} \times (\pi - 2\alpha_2) \qquad (6)$$

The voltage across the capacitor is identical to the voltage across the dc source when the capacitor and dc source are connected in parallel. For positive and negative cycles, the charging and discharging durations for each of the four SCs vary. According to Figure 8, the parasitic and discharging paths are used to determine the charging current and capacitor voltage at different modes. Equations (7)–(15) can be obtained for a load with a unity power factor.

$$V_{\mathrm{in}} - V_{c_1} - V_{c_2} - (i_{c_1} + i_{c_2})\, r_{\mathrm{ESR}} = 0 \qquad (7)$$

$$V_{c2} - V_{c3} + i_{c2} r_{\mathrm{ESR}} - i_{c3}\, (4r_{\mathrm{DS}} + r_{\mathrm{ESR}}) = 0 \qquad (8)$$

$$V_{\mathrm{in}} - V_{c3} - V_{c4} + 2r_{\mathrm{DS}}\, (i_{c1} - i_{c2} - i_{c3}) - i_{c3}\, (2r_{\mathrm{ESR}}) = 0 \qquad (9)$$

$$V_{c2} - V_{c3} - V_{c4} - r_{\mathrm{DS}}\, (i_{c1} - i_{c2}) + i_{c2} r_{\mathrm{ESR}} - 2i_{c3}\, r_{\mathrm{ESR}} = 0 \qquad (10)$$

$$V_{c1} - V_{c3} + i_{c1} r_{\mathrm{ESR}} - i_{c3}\, (5r_{\mathrm{DS}} + r_{\mathrm{ESR}}) = 0 \qquad (11)$$

$$V_{c1} - V_{c3} - V_{c4} + i_{c1} r_{\mathrm{ESR}} - i_{c3}\, (5r_{\mathrm{DS}} + 2r_{\mathrm{ESR}}) = 0 \qquad (12)$$

$$V_{c2} - V_{c3} + i_{c2} r_{\mathrm{ESR}} - i_{c3}\, (5r_{\mathrm{DS}} + r_{\mathrm{ESR}}) = 0 \qquad (13)$$

$$V_{c2} - V_{c3} - V_{c4} + i_{c2} r_{\mathrm{ESR}} - i_{c3}\, (5r_{\mathrm{DS}} + 2r_{\mathrm{ESR}}) = 0 \qquad (14)$$

$$i_{c_3} = i_{c_4} \qquad (15)$$

The capacitor voltages can be derived from Equations (7)–(15) while charging. Where r_{ESR}, r_{DS} and $V_{\mathrm{D,sw}}$ represent capacitance equivalent resistances, switch-resistance, and on-state voltage drop of the switch, respectively. The $i_{\mathrm{C,avg}i}$ ($i = 1, 2$) and τ are the average current in the route and the time constant, and they are the same as the product of the equivalent circuit capacitance and resistance. The capacitor C_1 and C_2 are acting as voltage divider having magnitude $0.5V_{\mathrm{in}}$. The voltage balancing of switched capacitor C_4 can be obtained by considering mode $\pm1.5V_{\mathrm{in}}$ and assuming the

(a)

(b)

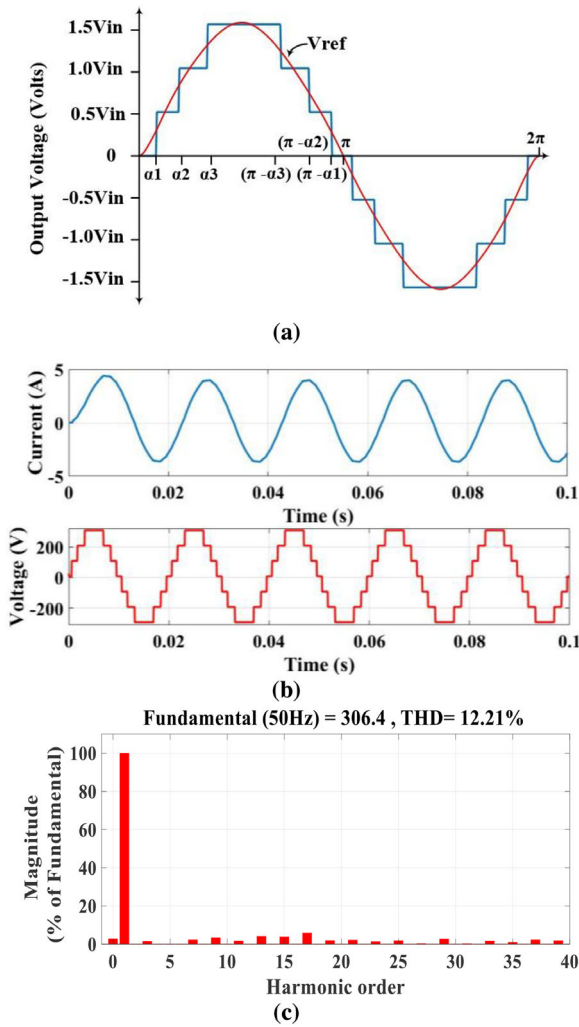Fundamental (50Hz) = 306.4 , THD= 12.21%

(c)

FIGURE 5 (a) Implementation of NLC. (b) Output voltage and current waveforms. (c) THD obtained in output voltage.

lumped impedance Z using Equations (16)–(18).

$$I_{C4} (+) = \frac{V_o - V_{C1} - V_{C3} - V_{C4}}{Z} = \frac{0.5 V_{in} - V_{C4}}{Z} \quad (16)$$

$$I_{C4} (-) = \frac{V_o - V_{C2} - V_{C3} - V_{C4}}{Z} = \frac{-0.5 V_{in} + V_{C4}}{Z} \quad (17)$$

$$\Delta Q = (I_{C4} (+) - I_{C4} (-))T = \frac{V_{in} - 2V_{C4}}{Z} \quad (18)$$

For $\Delta Q = 0$, $V_{C4} = 0.5 V_{in}$. Similarly, the voltage balancing of C_3 can be calculated using any mode. It is concluded that both the switched capacitors are balancing at $0.5 V_{in}$ in steady state.

3.4 | Cost function (CF)

The cost function is evaluated using different values of weight coefficient (δ). The low value of δ means that the number of

components is given more weight, and high means that the TSV is given more weight. The comparison of CF for different types of SCMLI is tabulated in Table 2 using Equation (19)

$$CF = \frac{S + D + G + C + T_{ms} + \delta \times TSV_{pu}) T_{dc}}{N_l} \quad (19)$$

where T_{ms} is the maximum number of switches in the conduction, T_{dc} is the total number of dc sources in the circuit and N_l is the number of level.

4 | POWER LOSS ANALYSIS

In this section, power loss analysis has been carried out. The power losses may be primarily divided into switching losses and conduction losses. When current flows through power equipment, a forward drop in voltage and parasite resistors result in the loss of conduction. As there are two types of current in an SC-based inverter (one that flows into condensers, or the charge current, and other that runs through the load, or the load current).

4.1 | Conduction losses

The internal resistance of the switches, which are employed in the suggested topology to block the voltage in one direction and permit the current flow in both directions, is used to determine the conduction losses. The conduction loss of the switches and the antiparallel connected diode are calculated using Equations (20) and (21):

$$P_{c,sw} = V_{o,sw} \, i \, (t) + R_{sw} i^{\beta} \, (t) \quad (20)$$

$$P_{c,d} = V_{o,d} \, i \, (t) + R_d i^2 \, (t) \quad (21)$$

where $P_{c,sw}$ and $P_{c,d}$ account for the conductive loss of the switch and the diode having current $i(t)$, respectively. Switch and diode ON-state voltage drops are designated as $V_{o,sw}$ and $V_{o,d}$, respectively. On-mode switch and diode resistance are represented by R_{sw} and R_d. Here, β is a constant which can be found from the datasheet and corresponds to transistor characteristics.

4.2 | Switching losses

The switching losses (P_{sw}) have a considerable impact on the effectiveness of the inverter. It may be computed using Equation (21). Its computation is based on the switch blocking voltage (V_{bv}), the current (I_{savg}) flowing through it, and the times at which the switch is turned ON (t_{ON}) and OFF (t_{OFF}). The switching losses are taken from the loss analysis in Piecewise Linear Electrical Circuit Simulation (PLECS) software which can also be computed using Equation (22) as mentioned
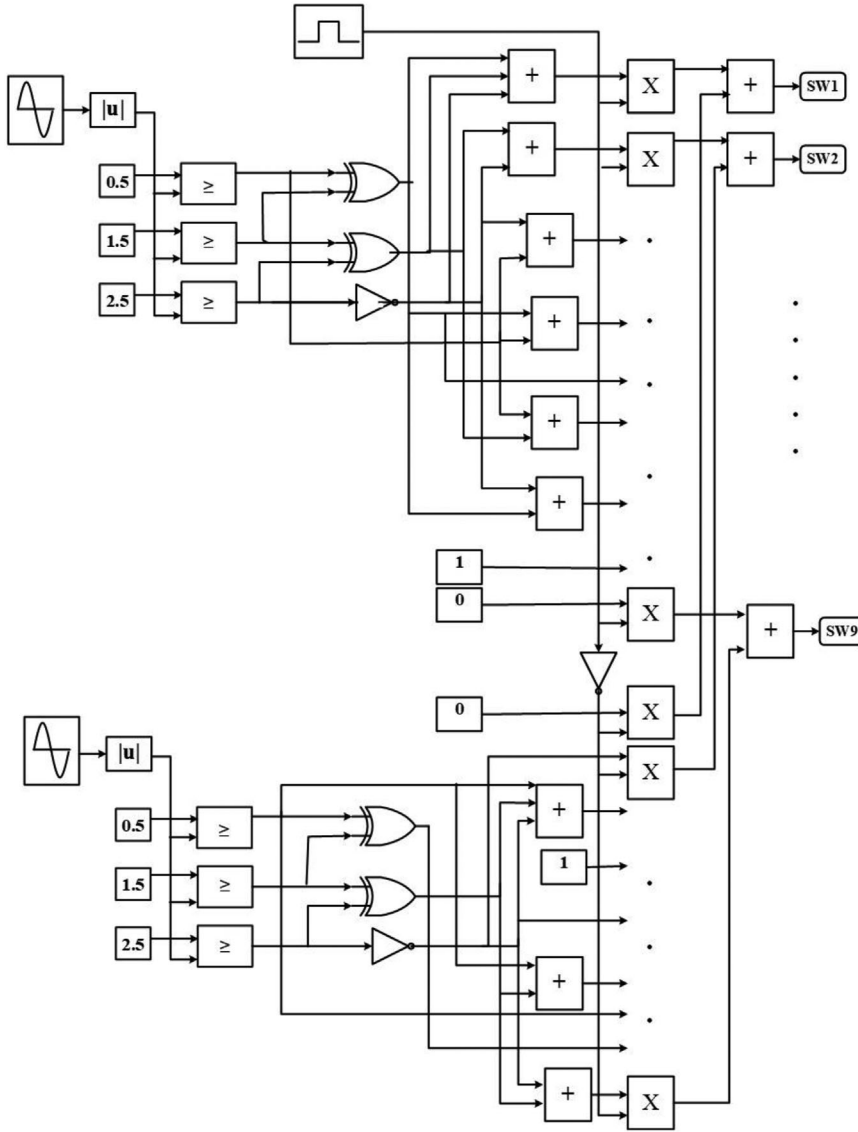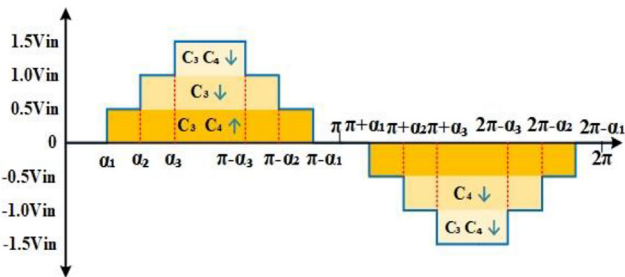
FIGURE 6 NLC circuit diagram.

FIGURE 7 Charging and discharging period of capacitors C_3 and C_4.

in [44].

$$P_{sw} = \frac{f_s}{6} \times \left[\int_0^{t_{ON}} V_{bv} I_{savg} dt + \int_0^{t_{OFF}} V_{bv} I_{savg} dt \right] \quad (22)$$

where f_s is the switching frequency.

4.3 | Ripple losses

Ripple losses (P_{ripple}) develop in the capacitors as a result of the discrepancy between capacitor voltage and charging voltage. Switch ON-resistance, capacitor equivalent series resistance (ESR), and diode forward voltage in the charging loop would be able to absorb the power loss during the charging process. The capacitor ripple losses may be computed using Equation (23) in which $\Delta V_{ripple-i}$ represents the ripple voltage of capacitor C_i.

$$P_{ripple} = \frac{f_s}{2} \times \sum_{i=1}^{2} \Delta V_{ripple-i} \times C_i \quad (23)$$

The PLECS software has been used to conduct a power loss study of the suggested topology. Figures 9a and b show the breakdown of power loss for each component (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8 and S_9) in LSPWM and NLC control scheme respectively. The switches S_1 and S_4 have larger

TABLE 2 A comparative study of different mid-point-clamped 7L SC-MLIs.

Type of SCMLI	Number of components				THD (%)	Overall voltage gain/caps voltage	Max. no. of ON-switches	Max. no. of switches in charging path	TSV (p.u.)/ MVS	MBV	CF		Rated efficiency
	S	D	C	G							$\delta = 0.5$	$\delta = 1.5$	
Sym SC [28, 29]	9	1	3	8	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	4	3	$5/V_{in}$	V_{in}	3.93	4.64	97%@150 W
ANPC [30, 31, 32]	9	0	3	8	19.3	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	5	4	$5.3/V_{in}$	V_{in}	3.95	4.71	96.7%@250 W
ABNPC [33]	9	0	3	8	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	4	4	$5.33/V_{in}$	V_{in}	3.81	4.57	96%@50 W
Dual T-Type [39]	10	0	4	8	NA	$1.5/V_{in}(2)$, $0.5V_{in}(2)$	3	4	$7.33/V_{in}$	$2V_{in}$	4.095	5.14	98%@100 W
ABNPC [34]	10	0	4	8	NA	$1.5/V_{in}(2)$, $0.5V_{in}(2)$	5	4	$6.66/V_{in}$	V_{in}	4.33	5.28	97%@100 W
ABNPC [35]	10	0	3	9	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	5	4	$6.6/V_{in}$	V_{in}	4.32	5.27	96%@450 W
ABNPC [37]	8	1	3	7	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	4	3	$5.33/V_{in}$	V_{in}	3.67	4.42	NA
ABNPC [38]	8	0	3	8	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	3	2	$7.3/V_{in}$	V_{in}	3.66	4.71	96%@800 W
ANPC [42]	8	0	4	8	NA	$1.5/0.5V_{in}(4)$	4	2	$6.67/V_{in}$	V_{in}	4.14	4.45	96%@100 W
NPC [40]	12	4	4	-	16.5	$1.5/0.5V_{in}$	5	2	$7/V_{in}$	V_{in}	5.20	5.90	96.2@800 W
ANPC [41]	7	6	3	7	NA	$1.5/V_{in}(1)$, $0.5V_{in}(2)$	3	2	$6.5/V_{in}$	V_{in}	4.18	5.10	96.40%@100 W
Proposed	9	0	4	8	12.2	$1.5/0.5V_{in}(4)$	5	4	$5/V_{in}$	V_{in}	4.09	4.78	97.55%@100 W

S: number of switches; D: number of diodes; C: number of capacitors; G: driver circuits; THD: total harmonic distortion; TSV (p.u.)/MSV: total standing voltage (in per unit) per maximum voltage stress; MBV: maximum blocking voltage.

losses because these switches are switching on and off more frequently than other switches and these have high blocking voltage.

5 | PERFORMANCE COMPARISON OF NLC AND LSPWM

The control of output voltage of the proposed topology has been carried out by LSPWM and NLC modulation technique. The performance comparison of both the modulation scheme in terms of conduction losses, switching losses, total losses and efficiency is discussed in this section.

Finally, Figures 10a, 10b and c illustrate the conduction, switching and total losses of switches for varying output power at unity power factor, respectively. The losses obtained in LSPWM control strategy are higher than the NLC strategy. Figure 11 depicts the efficiency plot of the proposed topology at unity power factor. From Figure 11 it is clear that the efficiency in the case of NLC is higher than the LSPWM strategy. This is because of low switching losses in NLC.

The efficiency and total losses of the proposed topology at 100 W obtained are 97.55% (NLC), 97.30% (LSPWM) and 2.33 W (NLC), 2.51 W (LSPWM), respectively.

6 | COMPARISON WITH OTHER TOPOLOGIES

All of the mid-point-clamped 7L SC-MLIs mentioned above have been compared in Table 2 in terms of the number of switches (S), diodes (D), capacitors (C), driver circuits (G), total harmonic distortion (THD), overall voltage per capacitor voltage, the maximum number of ON switches, the maximum number of switches in charging path, total standing voltage (TSV) per maximum voltage stress (MVS), maximum blocking voltage (MBV), cost function (CF) and rated efficiency.

From Table 2, it is found that the proposed ANPC topology has higher efficiency than symmetrical SC topologies in [28, 29]. There is no diode used in the proposed topology. In the comparison of proposed ANPC topology with already published ANPC topologies in [30–32], the proposed topology has lesser THD and TSV/MVS and higher efficiency. The proposed topology has lesser TSV/MVS and higher efficiency than ABNPC [33].The dual T-type [39] circuit has more number of switches and very high TSV/MVS as compared to proposed topology.

Further, the proposed topology consists of lesser number of switches, lesser standing voltage, lesser CF and more efficient than the ABNPC topology presented in [34]. The proposed topology is more superior to the ABNPC topology presented in [35] due to the less number of switches and gate driver circuits required, has lesser TSV/MVS, CF and higher efficiency.

The proposed topology has less TSV/MVS compared with ABNPC topology presented in [37, 38]. In [40], the power components, THD, TSV and CF are more which make the proposed topology superior. The efficiency and cost factor of the proposed is much improved as compared to topologies in [41, 42].

7 | HARDWARE IMPLEMENTATION

The hardware implementation of the proposed topology consists of input DC source voltage of magnitude 120 V, IGBTs (FGA25N120) of rating1200 V/25 A, driver circuits of rating $10 - 35$ V/± 1.5 A and controller (TMS320F28379D). The experimental values of all the parameters and equipment that are
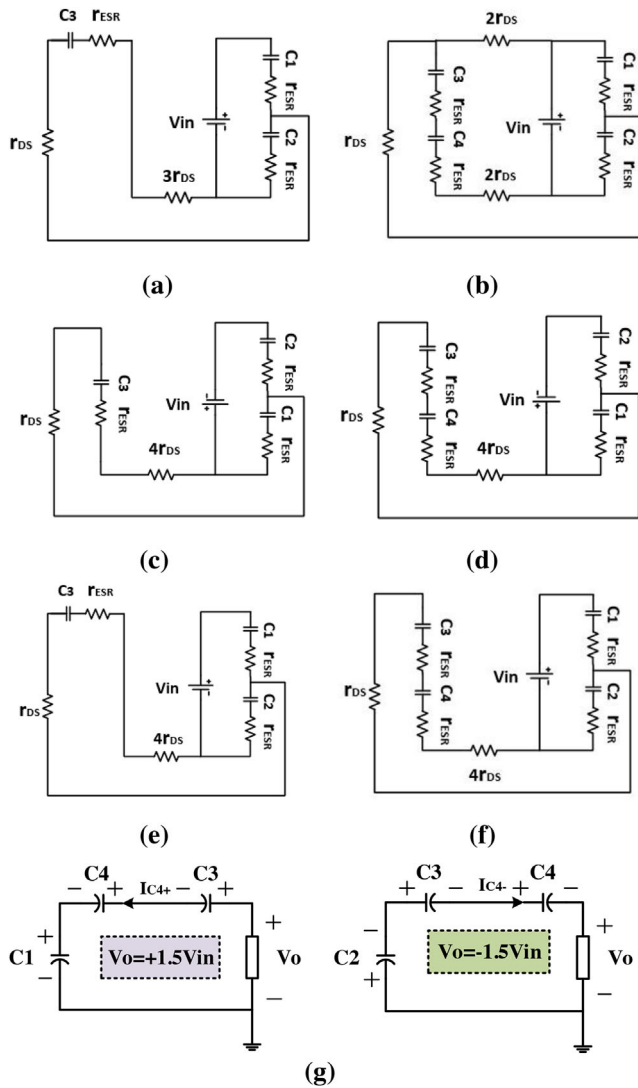
FIGURE 8 Charging/discharging of parasitic capacitances (a) C_3 discharging (mode I), (b) C_3 and C_4 charging (mode II), (c) C_3 discharging (mode III), (d) C_3 and C_4 discharging (mode IV), (e) C_4 discharging (mode VI), (f) C_3 and C_4 discharging (mode VII) and (g) equivalent diagram of proposed topology during $V_o = \pm 1.5 V_{in}$.

TABLE 3 Experimental values of the parameters.

Parameters	Ratings
Voltage source	160 V
Capacitors C_1 C_2 C_3 C_4	2200 ⁻F/200 V
IGBT	1200 V/25 A (FGA25N120)
Driver	10 − 35 V/ ± 1.5 A (ICTLP250)
Controller	TMS320F28379D

used in the hardware implementation are tabulated in Table 3. The dead time is not required in NLC modulation scheme because we are switching at fundamental frequency. A dead time of 1e−5s is provided in LSPWM technique through the microcontroller programming.
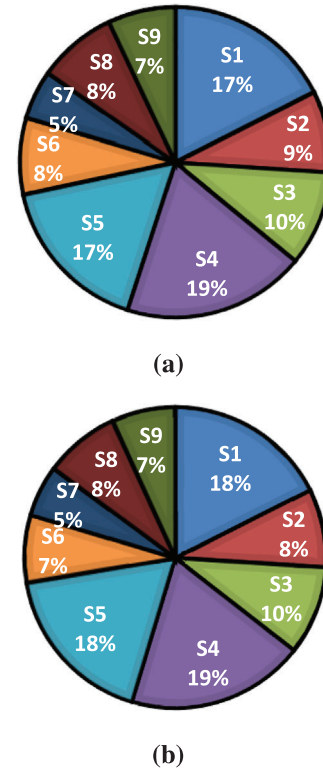
FIGURE 9 Distribution of power loss analysis @350 W in (a) LSPWM, and (b) NLC.

All the desired gate pulses or control signals (as obtained from LSPWM/NLC technique) are generated by microcontroller TM320F28379D. These signals are given to switches through the driver circuit. Driver circuits are connected to trigger the IGBTs by extending the voltage output of the microcontroller to the value so that the IGBTs are triggered. Each driver circuit has major functioning ICTLP250 which drives the IGBT. The R/RL load is connected at the output of the topology. The ammeter and voltmeter are connected to obtain output current and voltage. The switching logic is designed to produce 7-level output. The outputs are displayed in digital storage oscilloscope (DSO). The pictorial view of hardware setup is shown in Figure 12.

The maximum ripple per cent is determined to be 5%, and the SC $C_1 = C_2 = $, $C_3 = C_4 = 200$ ⁻F/100 V are chosen based on Equations (7)–(10), with a switching frequency of 5 kHz. $R = 40$, $L = 170$ mH and $R = 60$, $L = 260$ mH are the two distinct resistive-inductive loads employed. Figures 13a and b depict the waveforms of output voltage and current with dynamic R (100 Ω and 150 Ω) load using NLC and LSPWM, respectively. As a result of the fact that the current waveform for an R load imitates the voltage waveform, the current waveforms also contains seven distinct levels. At the output, the peak voltage of 180 V or 1.5 times the input dc voltage is generated. The peak current drawn by a 100 Ω and 150 Ω loads are around 3 A and 2 A, respectively. Figures 13c and d depict the waveforms of output voltage and current at different m (1, 0.8 and 0.5) using NLC and LSPWM, respectively. Figures 13e and f show the
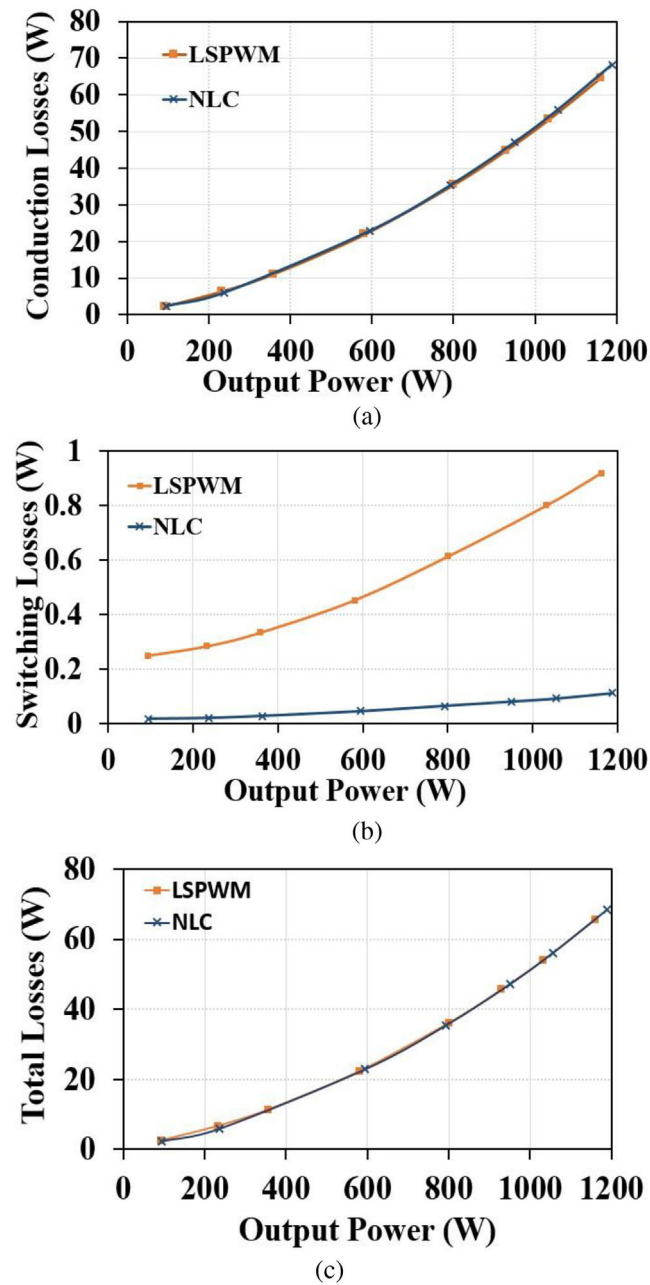
FIGURE 10 Change in (a) conduction losses, (b) switching losses and (c) total losses with varying output power.

FIGURE 11 Variation of efficiency in proposed topology.
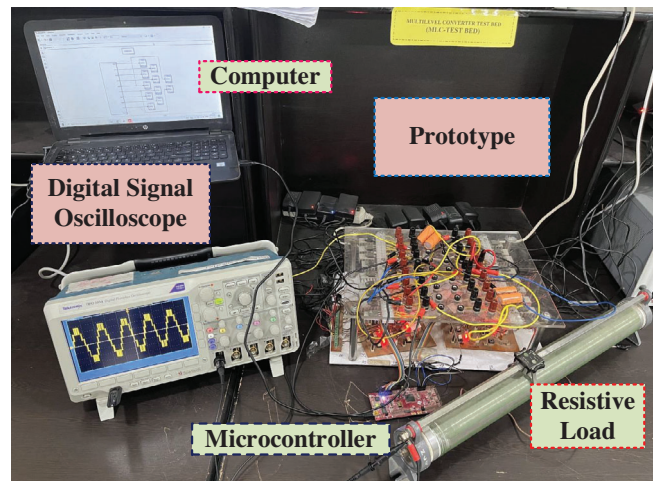
FIGURE 12 Experimental setup.

output voltage waveform at different m (1, 0.8 and 0.5) using NLC and LSPWM, respectively. The number of levels in VO is 7, 5 and 3 for the modulation index of unity, 0.8 and 0.5, respectively, as illustrated in Figure 13c–f. The voltage and current waveforms across through the capacitor C_3 and C_4 for dynamic load using LSPWM are illustrated in Figures 13g and h, respectively. The voltage and current waveform across through the capacitor C_3 and C_4 for dynamic load using NLC are illustrated in Figures 13i and j, respectively. The change in the output voltage and current waveforms due to changes in output frequency (50 and 100 Hz) are depicted in Figure 13k. It can be

used for many applications like variable frequency control drives etc.

Figure 13l depicts the output voltage and current waveforms at constant RL (60 Ω and 260 mH) load. The load current waveform obtained for an RL load is sinusoidal in nature with a peak value of 2 A. Figure 13m depicts the output voltage and current waveforms at dynamic RL (40 Ω, 170 mH and 60 Ω, 260 mH) load. Here, the peak value of current decreases as the load value increases. Figures 13n, 13o and p display the total harmonic distortion at $m = 1$, 0.8 and 0.5, respectively. The % THD obtained are 12.2%, 15.7% and 28.9% at $m = 1$, 0.8 and 0.5, respectively at unity power factor. Figure 13q–s shows the voltage stress across the switches. It can be seen that the maximum voltage stress on all the devices is V_{in} or $V_{in}/2$. It is concluded that the % THD decreases as the value of modulation index increases.

8 | CONCLUSION

The paper presents a 7-level active neutral point clamped (ANPC) inverter topology with boosting factor of 1.5. It consists of a single input dc source, eight unipolar switches, one bipolar switch and four switched capacitors. In this work the
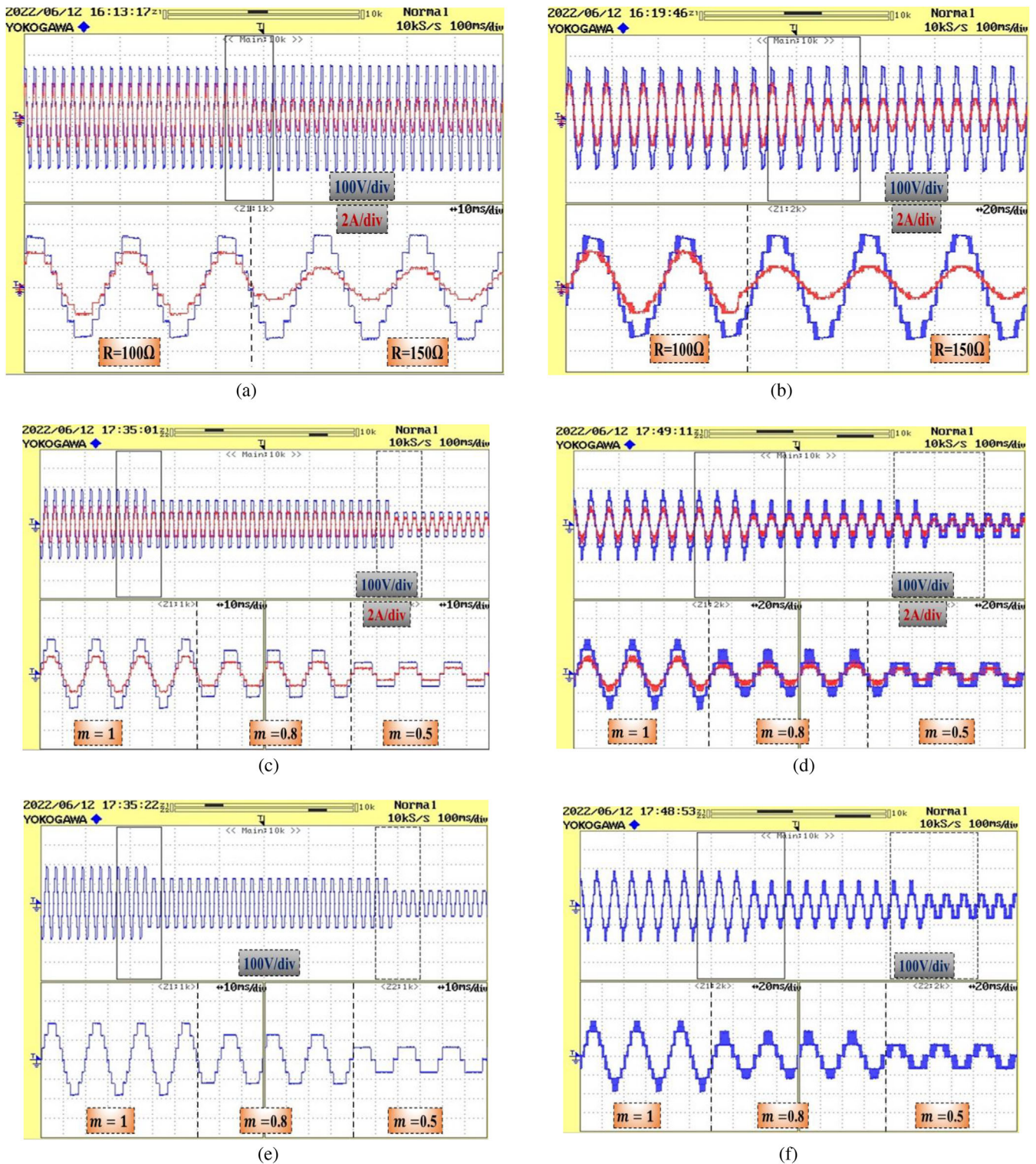
FIGURE 13 Experimental results. (a) Output voltage and current waveform for dynamic R load in NLC at unity power factor. (b) Output voltage and current waveform for dynamic R load in LSPWM at unity power factor. (c) Output voltage and current waveform at $m = 1$, 0.8 and 0.5 in NLC at unity power factor. (d) Output voltage and current waveform at $m = 1$, 0.8 and 0.5 in LSPWM at unity power factor. (e) Output voltage waveform at $m = 1$, 0.8 and 0.5 in NLC at unity power factor. (f) Output voltage waveform at $m = 1$, 0.8 and 0.5 in LSPWM at unity power factor. (g) Voltage and current waveform across C_3 for dynamic load in LSPWM. (h) Voltage and current waveform across C_4 for dynamic load in LSPWM. (i) Voltage and current waveform across C_3 for dynamic load in NLC. (j) Voltage and current waveform across C_4 for dynamic load in NLC. (k) Output voltage and current waveform for changing switching frequency (50 and 100 Hz) for R load. (l) Output voltage and current waveform at constant RL load at 0.8 power factor. (m) Output voltage and current waveform at dynamic RL load. (n) THD at $m = 1$ unity power factor. (o) THD at $m = 0.8$ at unity power factor. (p) THD at $m = 0.5$ unity power factor. (q) Voltage stress of switches 1, 2 and 3. (r) Voltage stress of switches 4, 5 and 6. (s) Voltage stress of switches 7, 8 and 9.
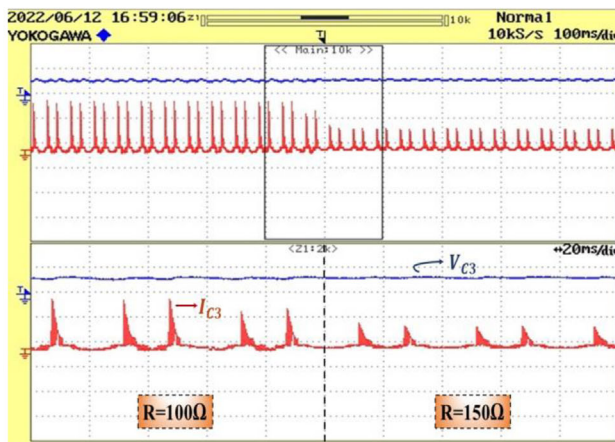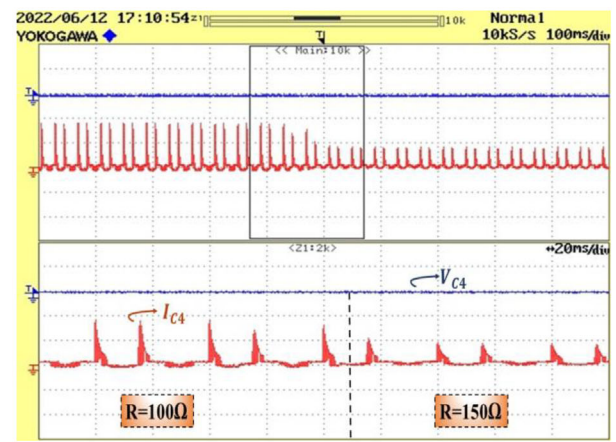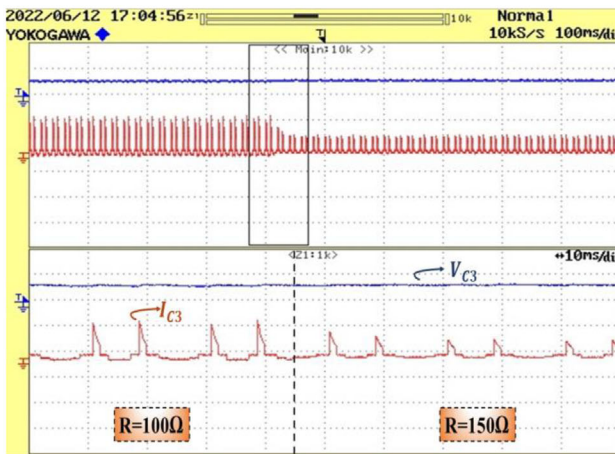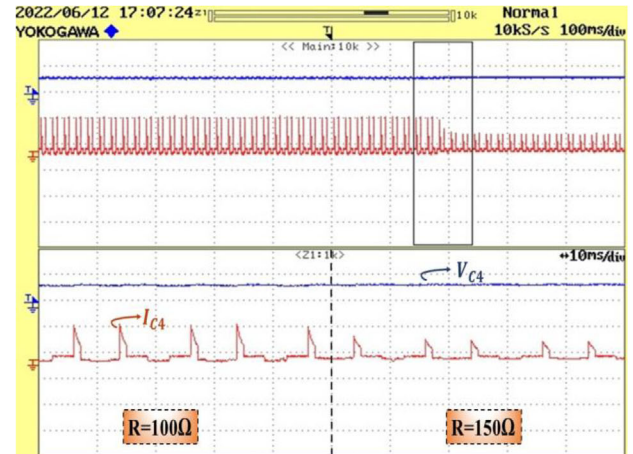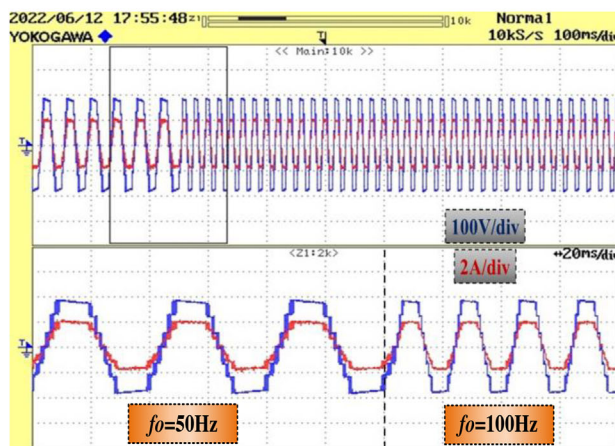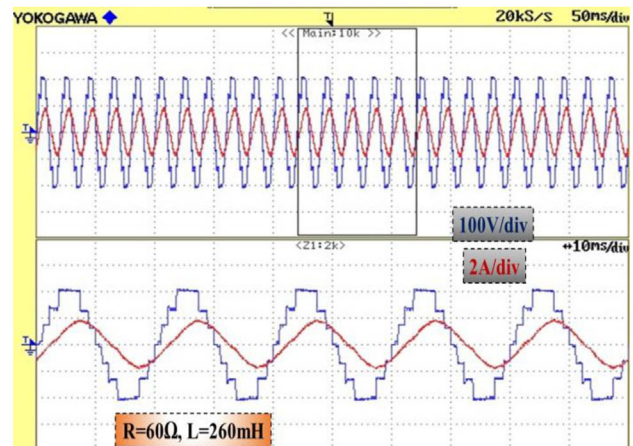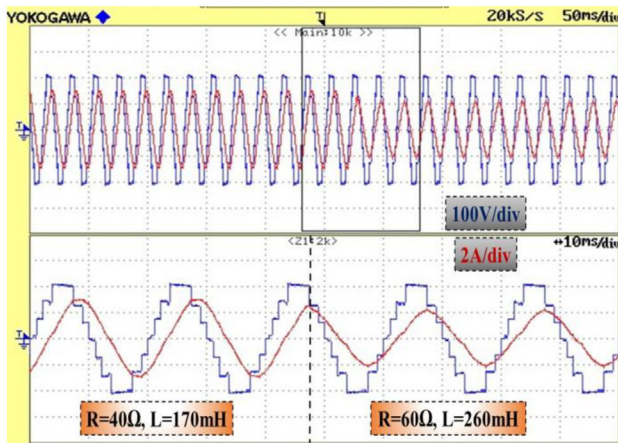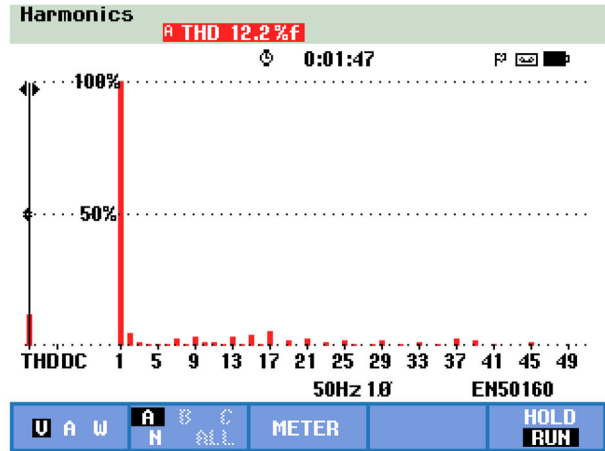
FIGURE 13 Continued

topology presented is a combination of good features of an ANPC inverter and switched capacitors are combined to generate a boosted voltage waveform, with self-balancing of capacitor with low voltage stress. The proposed topology has been anal-
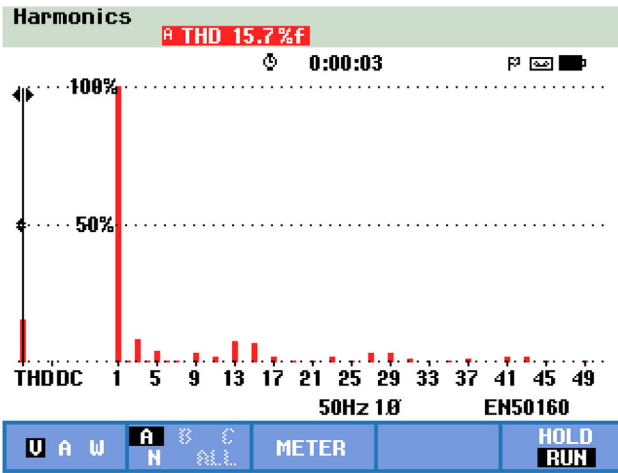
ysed by using two control techniques, that is, level shifted pulse width modulation (LSPWM) and nearest level control (NLC). For analysis, first the simulation model of the proposed topology has been developed and then the obtained simulation results
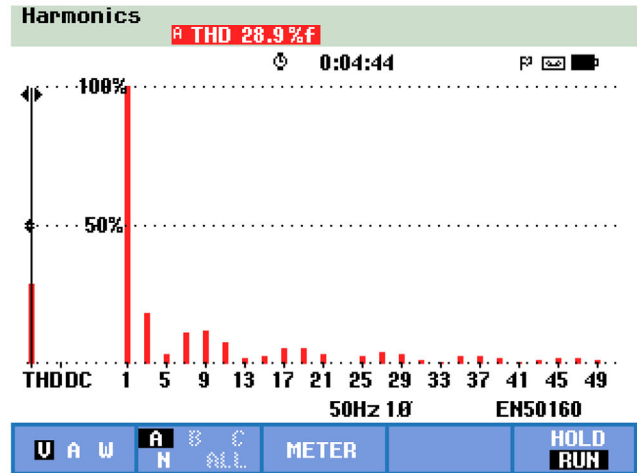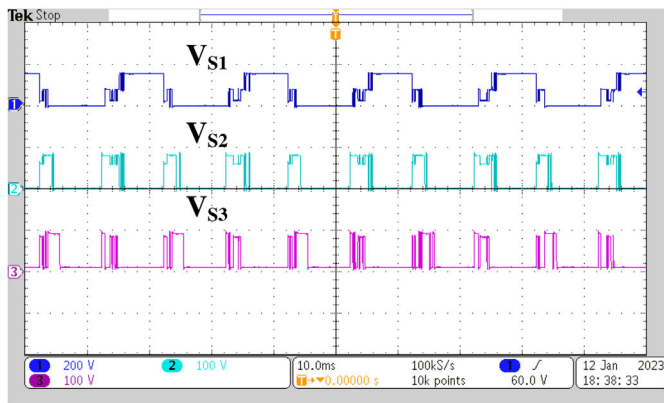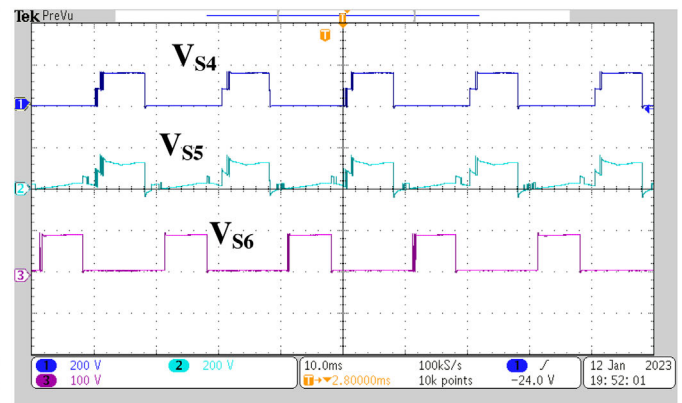
(m)

(n)

(o)

(p)

(q)

(r)

FIGURE 13 Continued

are validated by hardware implementation. The inverter has a maximum stress of only $V_{in}/2$ and V_{in} only. Hence only two types of switches are required in the inverter which makes the converter modular NLC control strategy displays the more efficient results than LSPWM scheme due to the less switching losses. The proposed inverter topology is superior to the other midpoint clamped 7L topologies in reference to the number of semiconductor devices, dc sources, gate driver circuits, THD, TSV/MVS, MBV, CF and efficiency. It is useful for the elimination of leakage current, especially in solar photovoltaic applications.
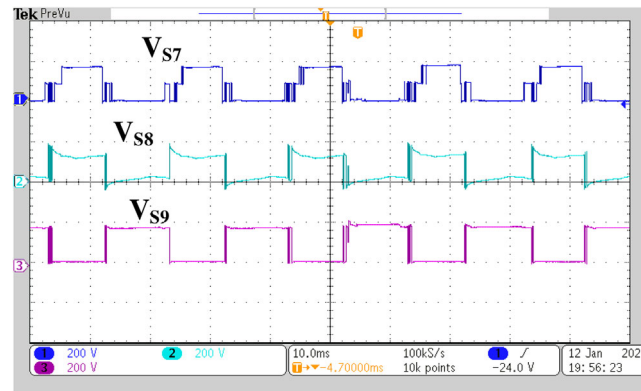
(s)

FIGURE 13 Continued

AUTHOR CONTRIBUTIONS

Adil Sarwar: Data curation; Investigation; Supervision; Visualization; Writing - review and editing. Mohammad Tayyab: Conceptualization; Data curation; Methodology; Resources; Supervision; Writing - review and editing. Atif Iqbal: Data curation; Formal analysis; Validation; Visualization; Writing - review and editing. Akbar Ahmad: Data curation; Formal analysis; Validation; Visualization; Writing - review and editing.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are openly available in repository, research publication etc., references are cited in manuscript.

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