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RESEARCH ARTICLE

# Symmetric and Asymmetric Multilevel Inverter Topologies With Reduced Device Count

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**ABSTRACT** In this work, two new topologies of single-phase hybrid multilevel inverters for symmetrical and asymmetrical configurations are presented for use in drives and control of electrical machines and the connection of renewable energy sources. The proposed topology uses 2 dc sources, 12 switches, 1 flying capacitor, and 3 diodes to generate boosted 13-levels and 17-levels for symmetric and asymmetric configuration, respectively. Self-voltage balancing of its capacitor voltage regardless of load type, load dynamics, or modulation index is a key advantage of the suggested design. The higher performance of proposed topologies in terms of the total number of switches, TSV, THD, switch stress, and dc sources are demonstrated by comparing those with recently published topologies. In addition, a widely employed nearest level control modulation approach is used to provide output voltage levels with low THD. Finally, experiments were undertaken to validate the performance of the suggested topology.

**INDEX TERMS** Multilevel inverter (MLI), switched-capacitor, nearest level control (NLC), total standing voltage (TSV).

## I. INTRODUCTION

Multilevel inverters (MLIs) have been widely employed, notably in renewable energy conversion systems, variable speed motor drive applications, UPS systems, reactive power compensators, distributed generation, electric vehicles, and other medium-high applications because of appealing qualities such as increased power quality, high voltage gain, electromagnetic characteristics, and reduced power loss [1], [2]. Increasing the input voltage is important in renewable energy applications, particularly in photovoltaic panels, in addition to delivering high-quality power to the grid.

Conventional MLIs can be classified into three types: Neutral point clamped (NPC) MLI, Flying capacitor (FC) MLI, and Cascaded H-bridge (CHB) MLI. For generating a specific output voltage level (up to five levels), conventional MLIs have proven quite popular in various industrial applications. However, a huge number of components are required to achieve a higher level output voltage waveform. As the number of levels in the output voltage increases, these conventional MLIs suffer from a number of problems, including the need for more components, such as clamping diodes in diode clamped MLIs, flying capacitors in FC-MLIs, and additional dc sources in CHB-MLIs [3]. Furthermore, capacitor voltage balancing in diode clamped and FC-MLIs necessitates sophisticated control algorithms, these traditional MLIs lack voltage boosting features, and voltage stress across switches is also high.

Several efforts are being undertaken to generate high voltage levels with fewer components, lesser dc sources, self-voltage balancing properties, and boosting capabilities. Capacitors have received a lot of interest as a technology that generates intermediate levels. In the hybrid MLI, flying capacitors (FCs) are essential for generating intermediate voltage levels. But, to keep the capacitor voltages at the required level, a complicated control circuitry is necessary. Furthermore, only half of the source voltage is generated at the load terminals. Thus, efforts are later made to boost the

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output voltage without utilizing any inductors or transformers across the output terminals. Switched capacitor-based voltage boost structures are preferred to create appropriate voltage for low or medium-voltage applications since these sources usually produce electric power at low voltage. In these arrangements, a parallel connection of the capacitor to the isolated dc voltage source results in capacitor charging, whereas a series connection results in capacitor discharging. When switched-capacitor sub-modules are connected in series, the magnitude of the output voltage increases [4], [5]. This concept of switched-capacitor was given by Ronald Marusarz [6] in 1989. Since then, plenty of switched-capacitor based MLIs has been suggested in the literature, each with its own set of advantages and disadvantages.

SCMLIs (switched capacitor MLIs) are a type of MLI that can generate a boosted sinusoidal output voltage with a lesser number of dc power supply. Capacitors are used as alternate dc sources in SCMLI. It does not require any extra circuits or sophisticated control algorithms to balance the capacitor voltages. Various configurations of SCMLIs have been reported in the literature in recent years. Various 13 and 17-level SC-MLI with single-phase ac output voltage are reported in [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], and [26]. In [21], [22], [23], and [24], two-stage 13-level SC-MLI configurations are discussed, which involve the boosting operation dc voltage in one stage and the production of ac output voltage in another stage. However, these configurations require switches with a high voltage stress value, which increases the SC-MLI cost. Therefore, two-stage configurations are less preferred. To ensure high voltage gain output ac voltage in SC-MLI requiring less switches with reduced voltage stress and less number of passive components like capacitors, single-stage SC-MLI configurations are preferred.

Depending upon the number of dc input sources, these 13 and 17-level configurations are further classified as the SC-MLIs requiring a single voltage source and SC-MLIs requiring multiple voltage sources. The 13 and 17-level SC-MLI requiring multiple sources are reported in [7], [8], [14], [15], [16], [19], [20], [21], and [27]. The 13 and 17-level SC-MLIs requiring only single source are discussed in [5], [10], [11], [12], [13], [17], [18], [22], [23], and [28]. In [5], two SC-MLI configurations are suggested, which are used to provide 13-level output ac voltage requiring switches having reduced values of voltage stresses and PIV or switch stress. Due to the reduction in PIV and TSV, the SC-MLI suggested in [5] is considered the most suitable candidate for low applications. The suggested topology offers improved voltage balancing across the capacitors. However, all these features are achieved at the cost of switches with high values of TSV and diodes requiring a large value of PIV. To relax the voltage stress and PIV rating of diodes, an improved SC-MLI configuration is suggested in [29]. The reduced value of TSV and PIV leads to an improvement in the efficiency of the converter. To improve the self-voltage balancing across the capacitors while including switches with reduced

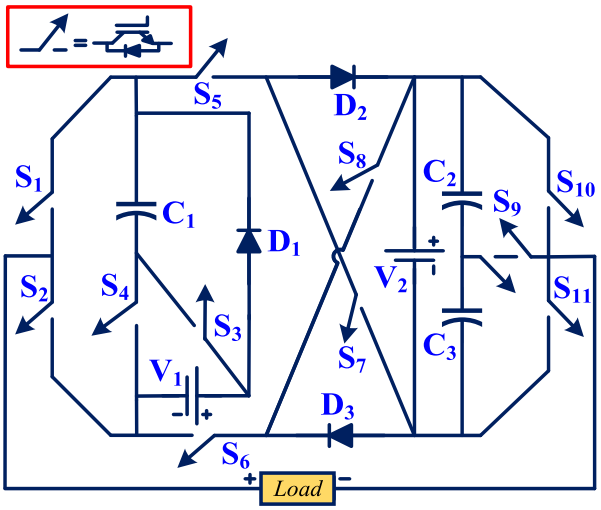


**FIGURE 1.** Proposed SCMLI topology.

TSV, SC-MLI is suggested in [26]. The suggested topology includes one dc source and cascaded-crisscross capacitor units. Each unit includes three switches, and the addition of one unit in the suggested SC-MLI leads to production of 4 additional levels. However, the suggested converter require high switch count to furnish 13-level single phase ac output voltage. To reduce the switch count, an improved SC-MLI topology which includes K-type repeating units to improve the voltage gain with reduced number of switches is suggested in [9]. The suggested topology requires only 12 switches for the production of 13-level ac output voltage. To reduce the TSV of converter switches, 13-level SC-MLI is proposed in [10]. However, the switch count of the suggested topology is high which makes it less economical. The 13-level SC-MLI is further simplified in [11]. The component count of the suggested topology is moderate. However, at low values of modulation index, the self-balancing of capacitor voltages becomes poor.

To improve the self-voltage balancing at low value of modulation index, improved 13-level SC-MLI configurations are suggested in [12], [13], and [28]. The topology suggested in [12] offers switches having a reduced value of PIV. However, the suggested topology requires capacitors of bigger sizes. The capacitor size is reduced in the 13-level SC-MLI suggested in [13]. However, the value of the PIV of switches and TSV of switch string is high [13]. To overcome the above limitations, SC-MLI is suggested in [28]. The suggested topology requires capacitors of reduced size. The 17-level SC-MLI, including single input dc source, is suggested in [17] and [18]. The SC-MLI configuration suggested in [17] offers a high value of TSV of the switch string. To ensure 17-level output ac voltage using switches having low value of TSV, an improved 17-level SC-MLI topology is suggested in [18].

The SC-MLI configurations suggested in [5], [10], [11], [12], [13], [17], [18], [22], [23], and [28] require single

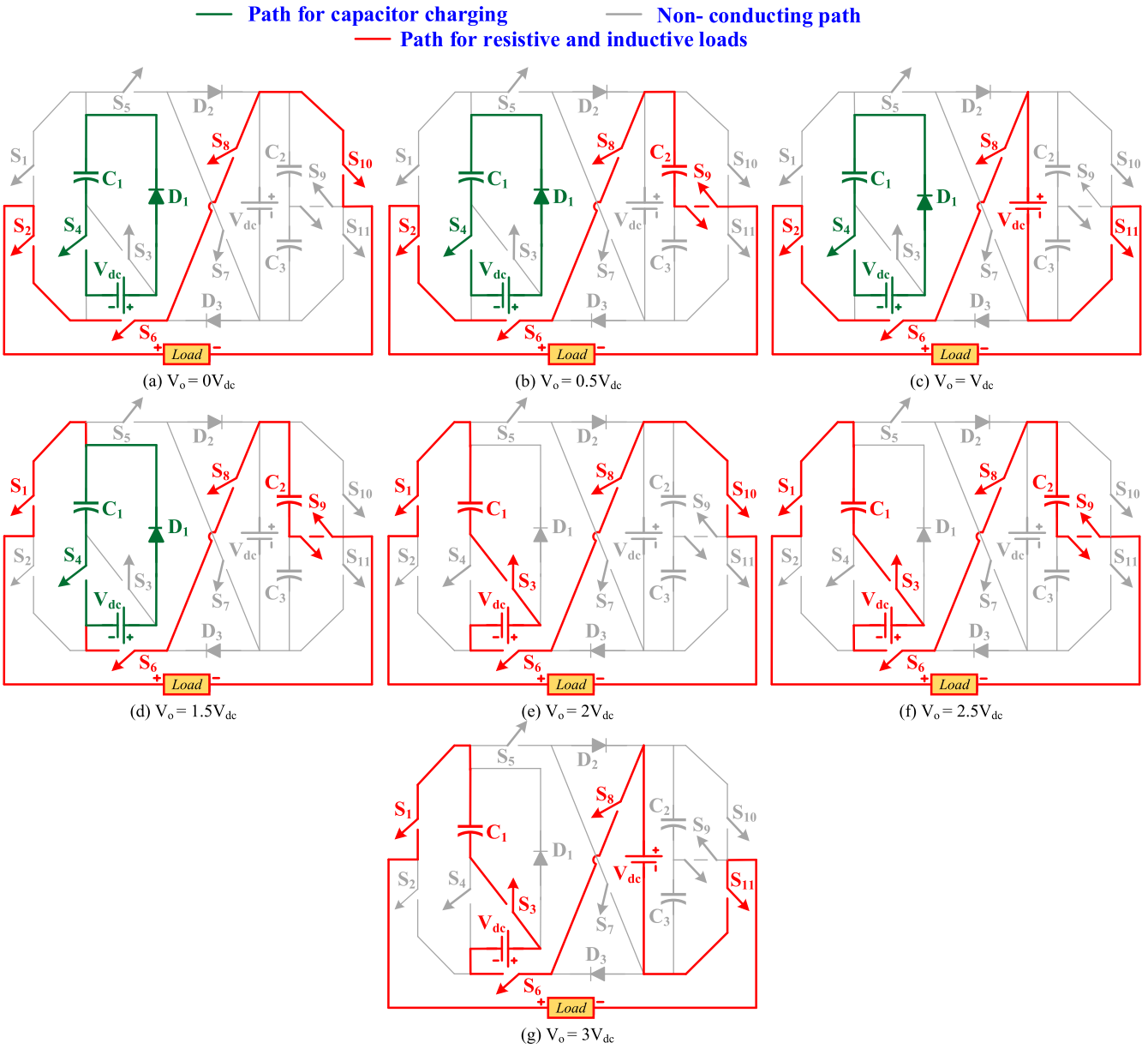


**FIGURE 2.** Positive switching states for symmetrical configuration of the proposed topology.

dc input voltage source for generation of 13 and 17-level ac output voltage. A single source is used to charge the capacitors, and a series connection of this source and capacitors may be used to charge other capacitors. However, this approach may lead to the requirement of large capacitors for high power factor load applications. The large value of capacitors may lead to large spikes appearing in the source current during the charging operation of switched capacitors. These spikes restrict the use of SC-MLI in high-power applications. The switches of higher power ratings are used to compensate for current spikes. The snubber circuits are used in parallel with switches. The series-connected inductor placed at the input dc source may also be used to suppress the spikes appearing in the charging current. However, these options lead to an increment in the cost of the SC-MLI.

To resolve these issues, SC-MLI with multiple input sources is a good option. This leads to a reduction in the size of capacitors used in SC-MLI, which further reduces the spikes appearing in the source current during the charging of capacitors. The 13 and 17-level SC-MLIs including multiple input sources are suggested in [7], [8], [14], [15], [16], [19], [20], [21], and [27]. The SC-MLI suggested in [15] requires four input sources. The 13-level SC-MLI suggested in [7], [8], [19], [21], and [27] and the proposed SC-MLI requires two input sources. By modifying the dc voltage of one voltage source with respect to other sources in a symmetrical and asymmetrical manner, the various levels of the ac output

voltage can be generated. The topology suggested in [27] requires switches having high values of voltage stresses, and the TSV of the switch string is more. To ensure switches having reduced values of voltages stresses, the improved topologies are suggested in [7], [8], and [19]. However, the switch count in these topologies is high.

This paper introduces a semiconductor configuration that uses a combination of DC sources and capacitors as DC links and also as a flying capacitor to extract the maximum possible voltage levels from DC sources, thereby reducing the implementation cost and improving the power quality. The proposed topology is a combination of an SC cell introduced in [30] and the cross-connected SC part given in [31]. The main motive to design this topology is to generate higher levels having voltage gain with lesser number of components, lower TSV with the increase in voltage levels, modular in structure, redundancies in voltage levels. The proposed topology can generate 13-levels and 17-levels for symmetrical and asymmetrical configurations. The proposed 13-level SC-MLI topology (P1) has low switch count which enhance the power density of the proposed 13-level SC-MLI. Further, the proposed 13-level SC-MLI includes switches having less value of PIV and TSV of switch string is reduced. The 17-level SC-MLI suggested in [15] and [16] requires 4 input sources which may not be possible in practical scenarios. The 17- level SC-MLI suggested in [14] and [19] requires only two input sources. However, the switch count is more for the topology suggested in [19]. The switch count of both topologies is also identical. However, the proposed 17-level topology (P2) requires fewer gate drivers, which enhances its power density. As compared to [14], the proposed 17-level SC-MLI requires fewer capacitors and the TSV of the switch string is also less. The low value of TSV reduces the converter's cost, making it an economical option for high-power and high-efficiency applications.

## II. PROPOSED SCMLI TOPOLOGY

This section discusses the structure of the proposed 13 and 17-level inverter and its working principle.

### A. CIRCUIT DESCRIPTION

The circuit diagram of the proposed topology is shown in Fig. 1. It consists of 2 dc sources ($V_1$, $V_2$), 11 unidirectional switches ($S_1$-$S_8$, $S_{10}$, $S_{11}$), 1 bidirectional switch ($S_9$), 1 flying capacitor ($C_1$), 2 dc-link capacitors ($C_2$, $C_3$), and 3 diodes ($D_1$- $D_3$). The switch pairs ($S_1$, $S_2$), ($S_3$, $S_4$), ($S_5$, $S_6$), and ($S_7$, $S_8$) are complementary to each other, thus reducing the control complexity and reducing the number of drivers. Dc-link capacitors $C_1$ and $C_2$ share equally the dc source voltage $V_2$. The proposed structure works for both symmetrical and asymmetrical voltage sources. For the symmetrical case, i:e, $V_1 = V_2$, 13 output voltages are generated. For the asymmetrical case, the voltage sources are taken in the ratio $V_1$: $V_2$ = 3: 2, which helps in generating 17 output levels. The proposed inverter can be typically used in applications involving equal dc sources or unequal dc sources (with a ratio 3:2). Applications with multiple DC source systems, like photovoltaic farms, can take advantage of the module and its cascade connection to create a modular topology with several voltage levels.

**TABLE 1.** Switching table for symmetrical configuation.

| Switches | | | | | | | | | | | $C_1$ | $V_0$ ($\times V_{dc}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | -- | +3 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | -- | +2.5 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -- | +2 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | ↑ | +1.5 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | ↑ | +1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | ↑ | +0.5 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | ↑ | +0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | ↑ | −0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ↑ | −0.5 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | ↑ | −1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ↑ | −1.5 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | -- | −2 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | -- | −2.5 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -- | −3 |

**TABLE 2.** Switching table for asymmetrical configuation.

| Switches | | | | | | | | | | | $C_1$ | $V_0$ ($\times V_{dc}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | -- | +8 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | -- | +7 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -- | +6 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | ↑ | +5 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | ↑ | +4 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | ↑ | +3 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | ↑ | +2 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | ↑ | +1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | ↑ | +0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | ↑ | −0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ↑ | −1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | ↑ | −2 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | ↑ | −3 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ↑ | −4 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | ↑ | −5 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | -- | −6 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | -- | −7 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -- | −8 |

### B. WORKING PRINCIPLE AND CAPACITOR SELF-VOLTAGE BALANCE

The following section discusses the working of the different operating states for the symmetrical and asymmetrical configurations.

#### 1) SYMMETRICAL CONFIGURATION

Fig. 2 and Table 1 demonstrate the conduction paths for positive levels and the switching states for all 13 levels for the symmetrical configuration of the topology when both the voltage sources are equal in magnitude ($V_1 = V_2 = V_{dc}$). Capacitor $C_1$ is being charged to $V_1 = V_{dc}$ by turning ON the switch $S_4$, as in the levels ±0, ±1, ±2, and ±3. Capacitors $C_2$, and $C_3$ are always charged to 0.5 $V_{dc}$, as they

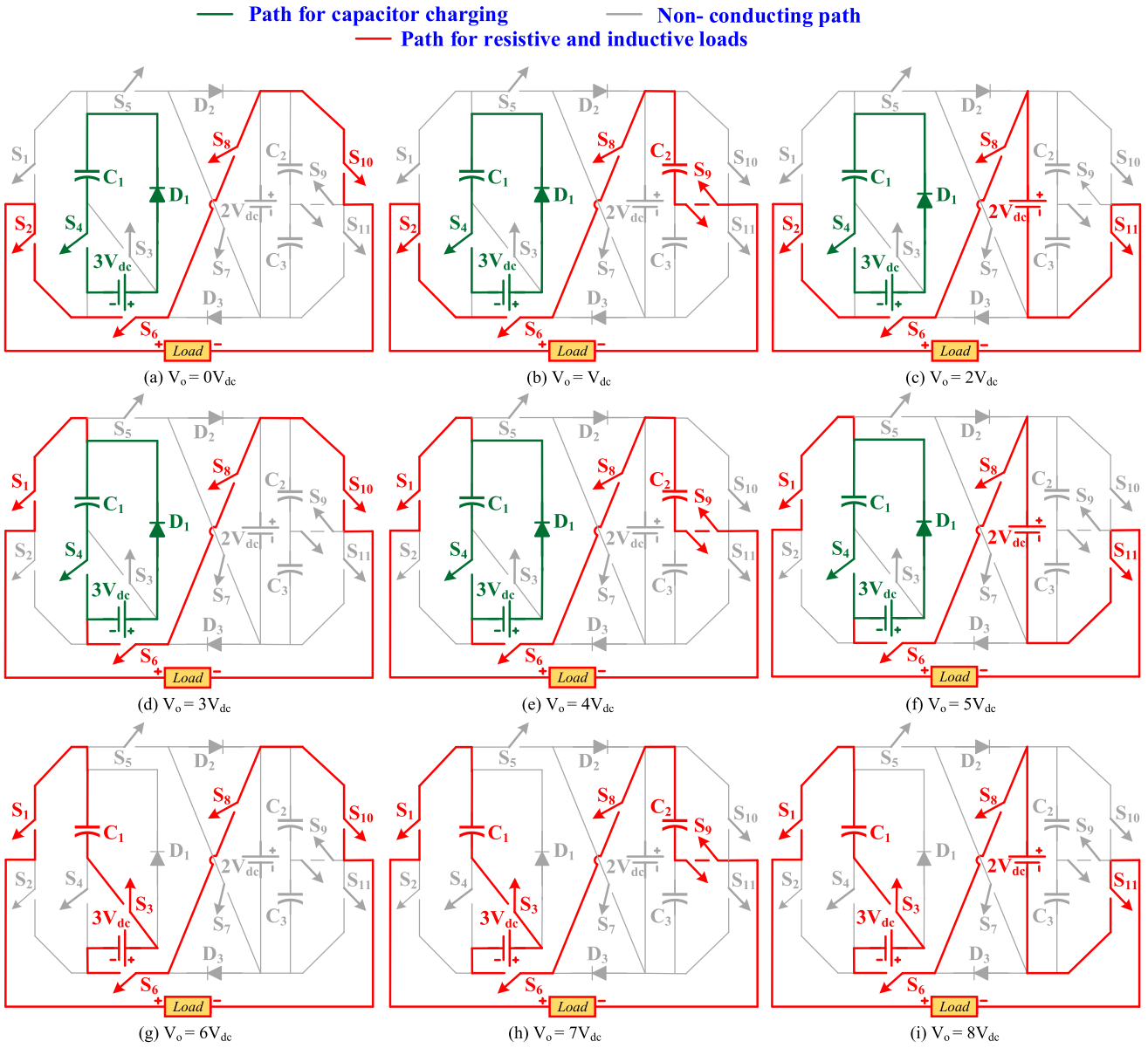


**FIGURE 3.** Positive switching states for asymmetrical configuration of the proposed topology.

are directly connected in parallel to $V_2$. Taking positive levels into consideration,

$0^{th}$ *level:* The load terminals are shorted through the switches $S_2$, $S_6$, $S_8$, and $S_{10}$. Also, $S_4$ is turned ON for charging capacitor $C_1$ as shown in Fig. 2 (a).

$1^{st}$ *level:* Voltage across $C_2$, $0.5V_{dc,}$ is reflected at the output by turning ON the switches $S_2$, $S_6$, $S_8$, and $S_{9,}$ as shown in Fig. 2 (b). In the same state switch, $S_4$ is also turned ON for charging $C_1$.

$2^{nd}$ *level:* In the second state, the voltage across $V_2$ and $V_{dc}$ is reflected at the output by turning ON the switches $S_2$, $S_6$, $S_8$, and $S_{11}$. In this state, capacitor $C_1$ is also getting charged by turning ON the switch $S_4$.

$3^{rd}$ *level:* The voltage across $C_1$ and $C_2$ are added in series by turning ON $S_1$, $S_4$, $S_6$, $S_8$, and $S_9$, thus delivering $1.5V_{dc}$ at the output. $C_1$ is also being charged as switch $S_4$ is ON.

$4^{th}$ *level:* In this level, the voltage across $C_1$ and the dc source $V_1$ are in series, delivering $2V_{dc}$ at the output via the switches $S_1$, $S_3$, $S_6$, $S_8$, and $S_{10}$.

*5th level:* Here, capacitors $C_1$ and $C_2$ are in series with the dc source V1 through the switches $S_1$, $S_3$, $S_6$, $S_8$, and $S_9$, thus delivering 2.5Vdc at the output.

$6^{th}$ *level:* In this level, both the sources are in series with $C_1$ by turning ON the switches $S_1$, $S_3$, $S_6$, $S_8$, and $S_{11}$. Thus, the output voltage of $3V_{dc}$ is obtained, as shown in Fig. 2 (g).

Similarly, all 13 switching states can be easily visualized using the switching table given in Table 1. The voltage gain of this configuration is 1.5 ($3V_{dc}/2$ $V_{dc}$), which is one of its merits. The total standing voltage (TSV) is an important

**TABLE 3.** Comparison table for different sc-based topologies with proposed topology.

| References | $N_{dc}$ | $N_L$ | $N_{Sw}$ | $N_{gd}$ | $N_d$ | $N_c$ | PIV (*$V_{dc}$) | TSV (*$V_{dc}$) | Efficiency (%) | THD (%) |
|---|---|---|---|---|---|---|---|---|---|---|
| [5] | 1 | 13 | 14 | 14 | 4 | 3 | 3 | 33 | 96.7 | 1 |
| [7] | 2 | 13 | 16 | 16 | 2 | 4 | 3 | 34 | 92.1 | 7.57 |
| [8] | 2 | 13 | 14 | 11 | 0 | 2 | 1 | 32 | 95.35 | 3.87 |
| [9] | 1 | 13 | 12 | 11 | 0 | 4 | 3 | 18 | 98.12 | 5.3 |
| [10] | 1 | 13 | 29 | 29 | 0 | 5 | 1 | 29 | 89 | 15 |
| [12] | 1 | 13 | 13 | 12 | 1 | 3 | 2 | 17 | 96.5 | 7.2 |
| [20] | 4 | 15 | 15 | 15 | 6 | 3 | 7 | 37 | 97.21 | 4.1 |
| [21] | 2 | 13 | 14 | 14 | 4 | 4 | 6 | 32 | 93.4 | 3.4 |
| [22] | 1 | 13 | 19 | 19 | 0 | 5 | 6 | 39 | 84.9 | 18.9 |
| [23] | 1 | 13 | 10 | 10 | 4 | 4 | 6 | 33 | 97.2 | 1 |
| [26] | 1 | 13 | 18 | 18 | 0 | 4 | 2 | 15.5 | 96.81 | 0.87 |
| [27] | 2 | 13 | 11 | 10 | 0 | 1 | 6 | 38 | 95 | 6.37 |
| [29] | 1 | 13 | 12 | 12 | 4 | 4 | 2 | 13 | 95.29 | 2.1 |
| [19] | 2 | 13 | 14 | 14 | 2 | 4 | 2 | 34 | 91 | 7.45 |
| [24] | 1 | 13 | 13 | 13 | 13 | 5 | 6 | 34 | 93 | 2.5 |
| [25] | 1 | 13 | 13 | 13 | 2 | 3 | 6 | 44 | 94.1 | 3.26 |
| [11] | 1 | 13 | 14 | 14 | 1 | 3 | 3 | 33 | 94.5 | 2.9 |
| [13] | 1 | 13 | 15 | 15 | 0 | 3 | 3 | 30 | 97.3 | 9.7 |
| [28] | 1 | 13 | 13 | 13 | 3 | 3 | 4 | 30 | 96.5 | 9.2 |
| [P1] | 2 | 13 | 12 | 11 | 3 | 3 | 3 | 16 | 95.8 | 5.39 |
| [19] | 2 | 17 | 18 | 18 | 2 | 6 | 6 | 30 | 91 | 7.45 |
| [14] | 2 | 17 | 12 | 12 | 0 | 4 | 5 | 27 | 99.4 | 4.79 |
| [15] | 4 | 17 | 16 | 14 | 0 | 4 | 2 | 11 | 95.3 | 4 |
| [16] | 4 | 17 | 10 | 10 | 0 | 0 | 2 | 40 | 95.2 | 4.09 |
| [17] | 1 | 17 | 12 | 10 | 2 | 3 | 4 | 38 | 97.8 | 6.96 |
| [18] | 1 | 17 | 16 | 16 | 10 | 4 | 2 | 23.5 | 96.5 | 7.6 |
| [34] | 1 | 17 | 14 | 10 | 2 | 3 | 8 | 45 | 96.3 | -- |
| [35] | 1 | 17 | 14 | 12 | 2 | 3 | 8 | 50 | 96.29 | -- |
| [P2] | 2 | 17 | 12 | 11 | 3 | 3 | 4 | 21.5 | 97 | 3 |

$N_L$= Number of levels, $N_{IS}$= number of input dc sources, $N_{sw}$ = Number of switches, $N_d$=number of diodes in parallel with switches, $N_{ad}$= number of auxiliary diodes, $N_{gd}$= number of gate driver circuit, $N_c$ = number of capacitor, TSV=Total standing voltage, PIV = Peak inverse voltage, VRC = voltage rating of capacitors, $\eta$ = Efficiency, THD = total harmonic distortion, [P1] = proposed 13-level topology, [P2] = proposed 17-level topology.

consideration in the design of MLI topology. It is defined as the total of the maximum voltage stress occurring across the switch for all output levels [32], [33]. The maximum stress across each switch is given as follows:

$$V_{S1} = V_{S2} = 2V_{dc} \quad (1)$$
$$V_{S3} = V_{S4} = V_{dc} \quad (2)$$
$$V_{S5} = V_{S6} = 3V_{dc} \quad (3)$$
$$V_{S7} = V_{S8} = 0.5V_{dc} \quad (4)$$
$$V_{S9} = V_{S10} = V_{S11}3V_{dc} \quad (5)$$

where, $V_{S1}$, $V_{S2}$, $V_{S3}$, $V_{S4}$, $V_{S5}$, $V_{S6}$, $V_{S7}$, $V_{S8}$, $V_{S9}$, $V_{S10}$, and $V_{S11}$ are the maximum voltage stress across the switches $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, $S_6$, $S_7$, $S_8$, $S_9$, $S_{10}$, and $S_{11}$. Therefore, TSV of the symmetrical topology will be,

$$TSV = 2 \times 2V_{dc} + 2 \times V_{dc} + 2 \times 3V_{dc} + 2 \times 0.5V_{dc} + 3 \times V_{dc} = 16V_{dc} \quad (6)$$

As the peak output voltage is $3v_{dc}$, hence

$$TSV_{pu} = \frac{16V_{dc}}{3V_{dc}} = 5.33 \quad (7)$$

### 2) ASYMMETRICAL CONFIGURATION

For asymmetrical configuration, when $V_1$ is taken as $3V_{dc}$ and $V_2$ is taken as $2V_{dc}$ ($V_1/V_2 = 1.5$), the proposed topology is able to generate 17 output levels with a gain of 1.6 ($8V_{dc}/5$ $V_{dc}$). Fig. 3 and Table 2 demonstrate the conduction paths for positive levels and the switching states for all 17 levels for the

asymmetrical configuration of the topology. Capacitor $C_1$ is being charged to $3V_{dc}$, equal to dc source $V_1$, by turning ON switch $S_4$. Capacitors $C_2$ and $C_3$ are always charged to $V_{dc}$ as they share $V_2$ equally. Considering the positive levels,

$0^{th}$ *level:* The load terminals are shorted through the switches $S_2$, $S_6$, $S_8$, and $S_{10}$, and $S_4$ is turned ON for charging capacitor $C_1$.

*1st level:* Voltage across $C_2$, $V_{dc}$ is reflected at the output by turning ON the switches $S_2$, $S_6$, $S_8$, and $S_9$. In the same state switch, $S_4$ is also turned ON for charging $C_1$, as shown in Fig. 3 (a).

*2nd level:* Fig. 3 (b) shows the second state, where the voltage across $V_2$, $2V_{dc}$ is reflected at the output by turning ON the switches $S_2$, $S_6$, $S_8$, and $S_{11}$. In this state, capacitor $C_1$ is also getting charged by turning ON the switch $S_4$.

*3rd level:* The voltage across $C_1$, $3V_{dc}$ is delivered at the output through the switches $S_1$, $S_4$, $S_6$, $S_8$ and $S_{10}$. Simultaneously,

charging of capacitor $C_1$ also takes place as the switch $S_4$ is ON in this state.

*4th level:* Capacitor voltages of $C_1$ and $C_2$ are added in series via the switches $S_1$, $S_4$, $S_6$, $S_8$ and $S_9$, thus delivering $4V_{dc}$ at the output. $C_1$ is also getting charged as $S_4$ is ON.

*5th level:* $C_1$ and dc source $V_2$ ($2V_{dc}$) are connected in series through the switches $S_1$, $S_4$, $S_6$, $S_8$ and $S_{11}$, hence $5V_{dc}$ appears at the output. Charging of $C_1$ takes place in this state also. *6th level:* $C_1$ and dc source $V_1$($3V_{dc}$) are connected in series by turning ON the switches $S_1$, $S_3$, $S_6$, $S_8$ and $S_{10}$, reflecting

$6V_{dc}$ at the output.

*7th level:* Capacitors $C_1$ and $C_2$ are connected in series with the dc source $V_1$ via the switches $S_1$, $S_3$, $S_6$, $S_8$ and $S_{10}$, thus delivering $7V_{dc}$ at the output.

*8th level:* Fig. 3 (i) shows this state, where both the dc sources are in series with the capacitor $C_1$ through the switches $S_1$, $S_3$, $S_6$, $S_8$ and $S_{11}$, providing $8V_{dc}$ at the output.

Similarly, all 17 output levels can be visualized using the switching table given in Table 2. Maximum voltage stress across the switches in asymmetrical configuration is given as,

$$V_{S1} = V_{S2} = 3V_{dc} \tag{8}$$
$$V_{S3} = V_{S4} = 1.5V_{dc} \tag{9}$$
$$V_{S5} = V_{S6} = 4V_{dc} \tag{10}$$
$$V_{S7} = V_{S8} = V_{dc} \tag{11}$$
$$V_{S9} = 0.5V_{dc} \tag{12}$$
$$V_{S10} = V_{S11} = V_{dc} \tag{13}$$

Therefore, TSV of the asymmetrical topology will be,

$$TSV = 2 \times 3V_{dc} + 2 \times 1.5V_{dc} + 2 \times 4V_{dc} + 2 \times V_{dc} + 0.5V_{dc} + 2 \times V_{dc} = 21.5V_{dc} \tag{14}$$

3) AS THE PEAK OUTPUT VOLTAGE IS $8V_{DC}$, HENCE

$$TSV_{pu} = \frac{21.5V_{dc}}{8V_{dc}} \tag{15}$$

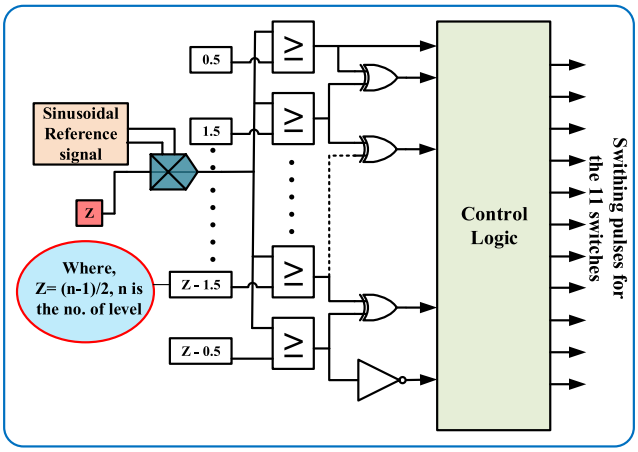


**FIGURE 4.** Nearest level modulation working principle.

The flying capacitor's voltage is self-balanced to its proper voltage level by the parallel connection of the capacitor to the source and in series with the load at various periods. The time it takes for the capacitor to fully charge at any voltage level is always available because the charging loops' time constant and overall parasitic resistance are negligible.

## III. MODULATION TECHNIQUE

For multilevel inverters, numerous modulation techniques have been tested and deployed. Here, the proposed architecture uses Nearest Level Control (NLC) technique to control the switches and produce the desired output waveform. The goal is to employ the NLC approach in an inverter with a large number of levels in order to lessen and streamline the processor's calculation. Fig. 4 depicts the working mechanism of the NLC method. A sampled waveform is produced by comparing the reference sinusoidal waveform to the desired output waveform. To generate switching signals for the respective IGBTs, the resulting waveform is then rounded off to the nearest level and compared using the switching logic shown in Table 1 and Table 2 for symmetrical and asymmetrical configuration, respectively.

## IV. COMPARATIVE ANALYSIS

In this section, the comparative analysis of the proposed 13 and 17-level SC-MLI is carried out with various SC-MLI configurations reported in the literature. The comparison is carried out in reference to the parameters like $N_L$ = Number of levels, G= voltage boost ratio, $N_{IS}$ = number of input dc sources, $N_{sw}$ = Number of switches, $N_d$ =number of diodes in parallel with switches, $N_{ad}$ = number of auxiliary diodes, $N_{gd}$ = number of the gate driver circuit, $N_c$ = number of the capacitor, TSV=Total standing voltage, PIV = Peak inverse voltage or switch stress, VRC = voltage rating of capacitors, $\eta$ = Efficiency, THD = total harmonic distortion. Table 3 shows the entries of these parameters for the proposed and reported SC-MLI configurations.

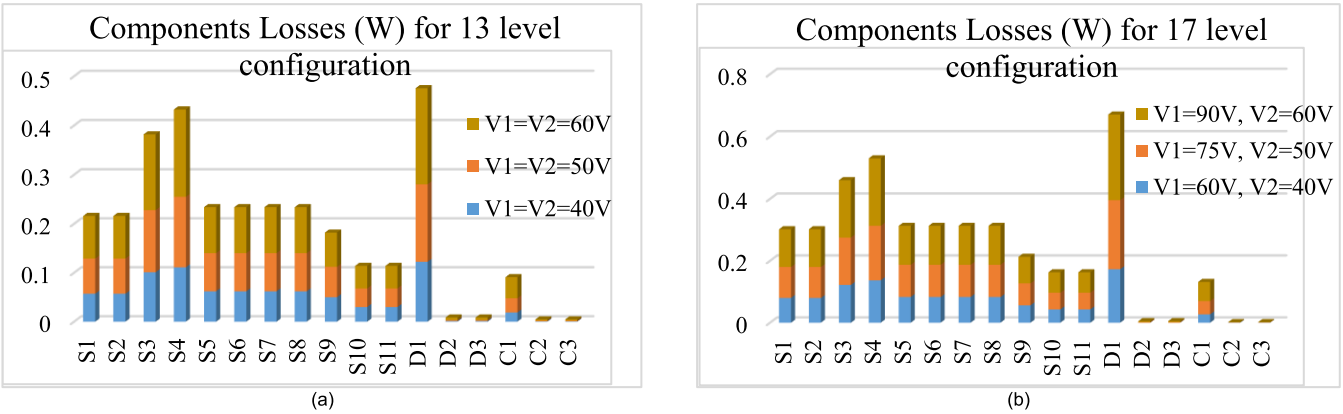


**FIGURE 5.** Power loss distribution with change in dc source voltage for the (a) symmetrical configuration (b) asymmetrical configuration.

The 13 and 17-level SC-MLI configurations, including single source, are reported in [5], [10], [11], [12], [13], [17], [18], [22], [23], [28], [34], and [35] the SC-MLIs including single source used for charging the capacitors require a large value of capacitors to maintain self-voltage balancing when high power factor loads are connected across the output of these SC-MLI. Further, the charging action of the capacitors may be restricted at low values of modulation indexes. Large capacitors may lead to the production of spikes in source current during the charging of capacitors. This issue can be resolved by using snubbers across the switches and overrating the switches and external inductors in series with the input source. However, these options lead to an increment in the cost of the converter. To reduce the value of the capacitors required SC-MLI, SC-MLIs, including multiple sources, are preferred. The 13 and 17-level SC-MLIs including multiple sources are discussed in [7], [8], [14], [15], [16], [19], [20], [21], and [27]. The 13 and 17-level SC-MLI discussed in [15], [16], and [20] require 4 input dc sources. However, fulfilling the requirement of 4 sources is not practically feasible, and the cost of the converter increases. The 13 and 17-level SC-MLI including two input sources are discussed in [7], [8], [14], [19], and [27]. The switch count of the 13-level SC-MLI suggested in [7] is the highest, which makes it a costly one. The switch count of the 13-level topologies suggested in [8] and [19] is moderate. However, the switches switch count and number of gate drivers required in the 13-level topology suggested in [27] are the lowest. The switch and gate driver count in the proposed topology is slightly higher than that in [27].

The 13-level topologies suggested in [8] and [27] require no auxiliary diode. The total auxiliary diode and capacitor count of the topologies discussed in [7] and [19] and the proposed topology [P1] are identical, which is equal to 6. The value of PIV across the switches is more in the case of [27] as compared to [7], [8], and [19], and the proposed 13-level SC-MLI. The voltage stress is lowest in case of [8] as compared to [7], [19], [27], [P1]. The PIV is moderate in the case of [7],

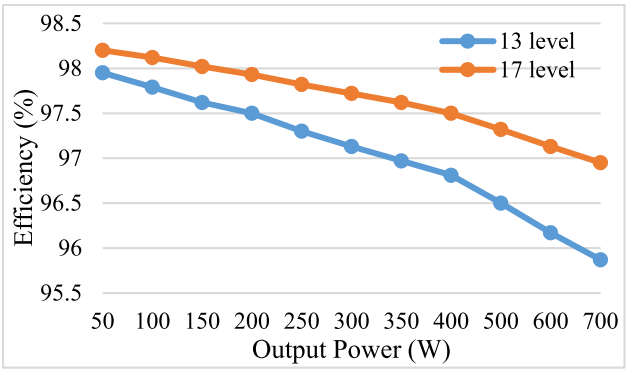


**FIGURE 6.** Efficiency with respect to output power for both the configurations.

[P1]. It can be observed from Table 3 that the value of TSV across the switch string is very high in the case of [27], while the value of TSV for the switches string connected in the proposed 13-level SC-MLI [P1] has the lowest value.

The efficiency of the 13-level inverters, including two input dc sources, is the lowest in the case of [19], while its value is highest for the proposed 13-level SC-MLI [P1]. The proposed 13-level SC-MLI offers an efficiency of 95.8% at a rated load of 700 W which is evaluated using an analytical method. Among the 13-level SC-MLI, including two input dc sources, the THD value of single-phase ac output voltage is highest for the converter suggested in [22] at 18.9%, while its value is 5.39% for the proposed 13-level SC-MLI [P1].

Further, the switch and gate driver counter is more in [19] as compared to [14], [P2]. The 17-level SC-MLI suggested in [14] requires no auxiliary diode, while the [19] requires only 2 and [P2] requires 3 diodes. The topology in [14] and [19] require 6 and 4 capacitors, while the proposed topology [P2] requires only 3 capacitors. The topology discussed in [14], [19], [34], and [35] requires switches having a high value of PIV and the TSV of the switch string is also high. However, the switches connected in the proposed 17-level SC-MLI [P2]

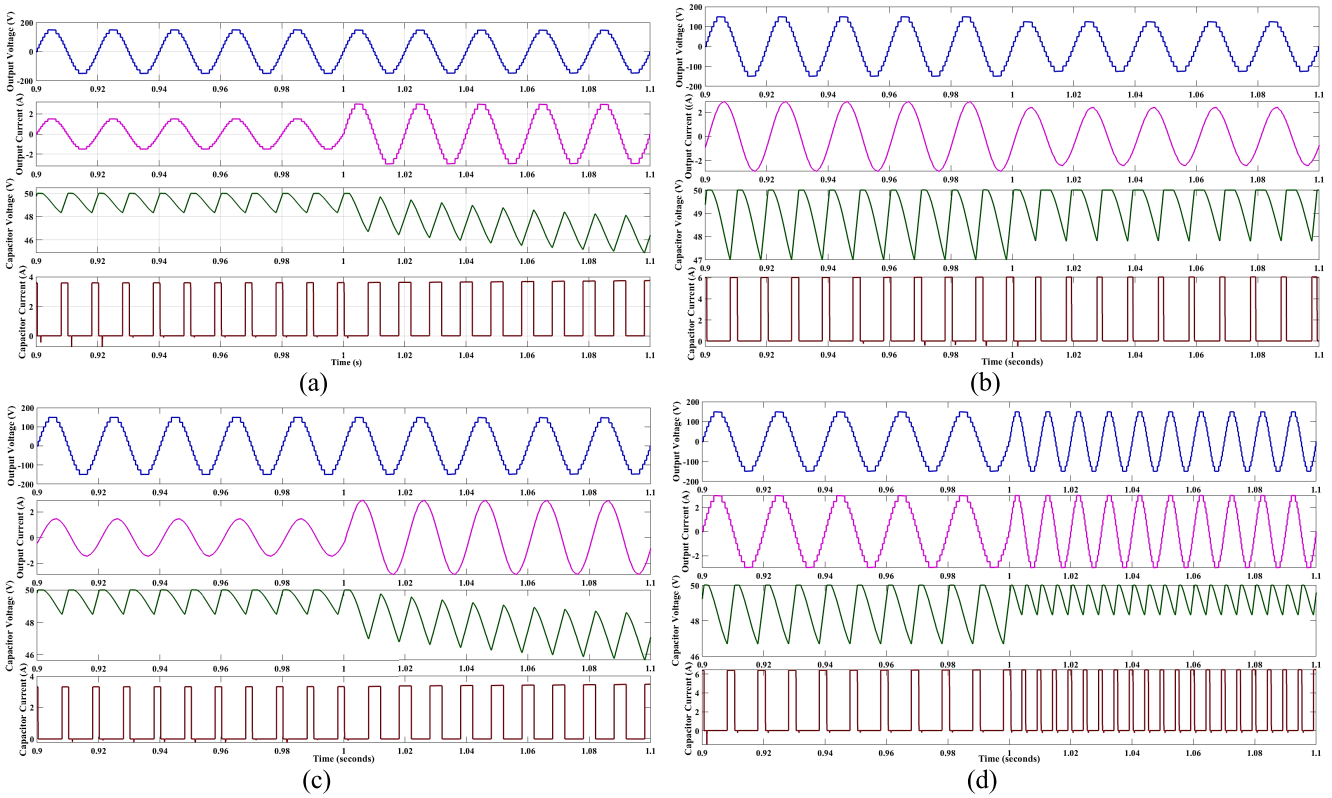


**FIGURE 7.** Simulation results for the symmetrical topology. Output voltage, output current, voltage and current across capacitor $C_1$ for (a) dynamic change of R-load (b) dynamic change of RL-load (c) change in frequency of the reference sinusoidal signal (d) change in Modulation Index (MI).

undergo less voltage stress, and the TSV of the switches is significantly reduced as compared to [14] and [19]. The efficiency of the converter discussed in [14] is the highest, which is 99.4%. The efficiency of the proposed converter [P2] is 97% when evaluated at a rated load of 700W using an analytical method. The THD value of output ac voltage in the case of the proposed converter is 3% of the fundamental value of ac output voltage, which is the lowest as compared to the other 17-level topologies. The above comparison validates the efficacy of the proposed 13 and 17-level SC-MLI.

## V. POWER LOSS ANALYSIS

Power loss for the proposed 13 and 17-level SCMLIs are presented in this section. A topology's power loss is a crucial consideration in the design process. The power semiconductor devices, including switches and diodes, are responsible for the majority of a topology's losses [17], [36], [37]. PLECS software is used to estimate the proposed structure's losses. The proposed topology's efficiency is estimated using these losses. The software's thermal modelling component is used to compute various losses in switches, capacitors, and diodes. This study takes into account the following losses: conduction losses ($P_c$) of all semiconductor devices, switching losses ($P_s$), and capacitor Equivalent Series Resistance (ESR) losses ($P_{esr}$) [18].

There is a loss of energy whenever a switch is turned ON or OFF, and this is referred to as switching losses [38]. Whenever a switch is turned on or off, the voltage across the switch and the current through the switch are not zero. This causes switching losses in semiconductor switches.

Power loss during turn-on,

$$P_{S,N,j} = f \int_0^{t_{on}} v(t)\, i(t)\, dt$$
$$= f \int_0^{t_{on}} \left(\frac{V_{S,j}}{t_{on}} t\right) \left(-\frac{I_j}{t_{on}} (t - t_{on})\right)$$
$$dt = \frac{1}{6} f V_{S,j} I_j \tag{16}$$

Power loss during turn-off,

$$P_{S,F,j} = f \int_0^{t_{off}} v(t)\, i(t)\, dt$$
$$= f \int_0^{t_{off}} \left(\frac{V_{S,j}}{t_{off}} t\right) \left(-\frac{I'_j}{t_{off}} (t - t_{off})\right)$$
$$dt = \frac{1}{6} f V_{S,j} I'_j t_{off} \tag{17}$$

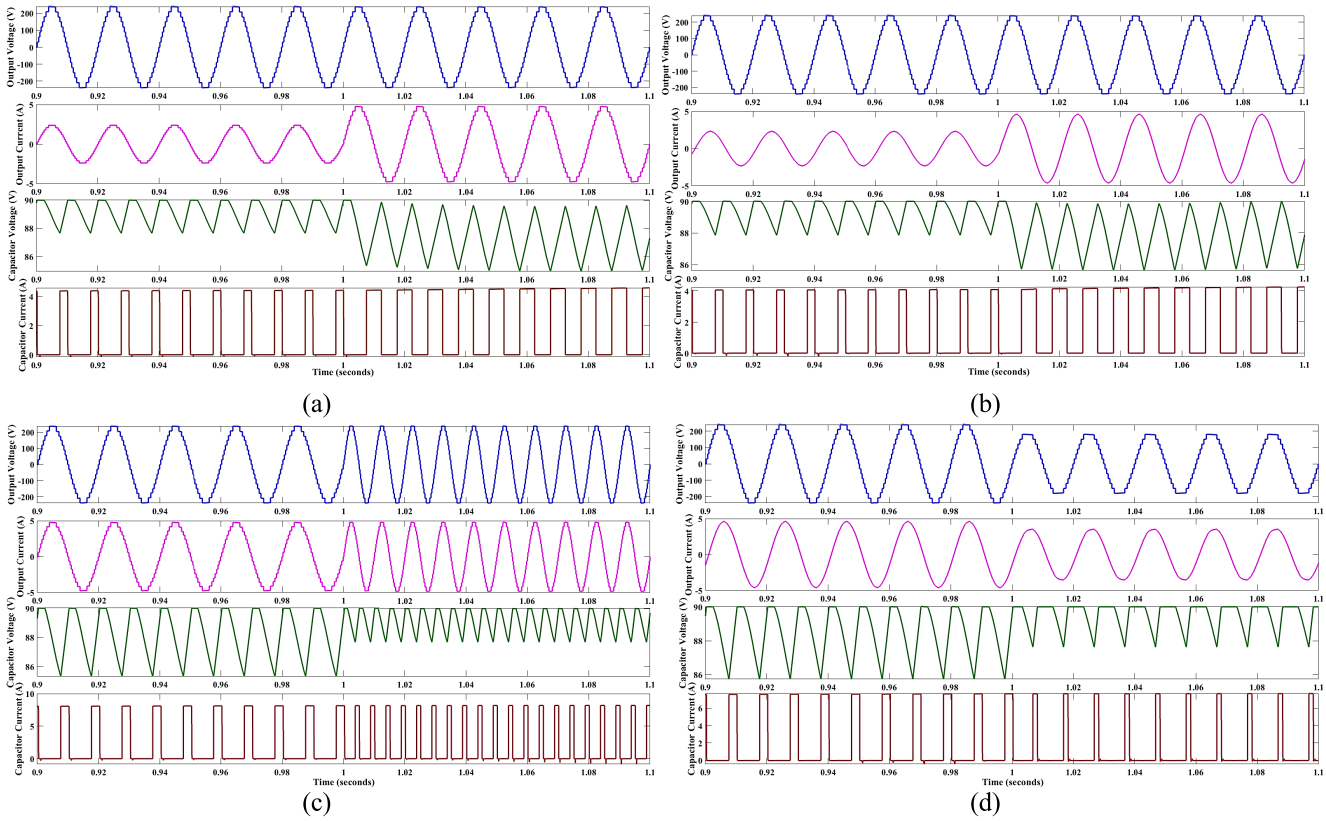


**FIGURE 8.** Simulation results for the asymmetrical topology. Output voltage, output current, voltage and current across capacitor $C_1$ for (a) dynamic change of R-load (b) dynamic change of RL-load (c) change in frequency of the reference sinusoidal signal (d) change in Modulation Index (MI).

where $I_j$ and $I_j'$ represent the currents flowing through the j$^{th}$ switch at turn-on, and before turn-off, respectively, f represents the switching frequency, and $V_{s,j}$ represents the voltage stress across the switch. The total switching loss can be calculated by multiplying the number of ON switching states ($N_N$) and number of OFF switching states ($N_F$) in one cycle with (16) and (17), respectively,

$$P_S = \sum_{j=1}^{13} \left( \sum_{n=1}^{N_N} P_{S,N,jn} + \sum_{n=1}^{N_F} P_{S,F,jn} \right) \tag{18}$$

The primary contributors to conduction loss are the on-state resistances and the forward voltage drop across the devices that are in the path of the load current [39]. In order to determine the conduction losses of any MLI power device, we can use the following expression [40]:

$$P_C = \frac{1}{f} \times m_i \left( \frac{V_R - V_S}{I_R} \times I^2 + V_S \times \mathrm{I} \right) \tag{19}$$

where $m_i$ is the modulation ratio of the MLI topology, $V_R$ and $V_S$ are the switch voltages at rated and saturation currents, $I_R$ is the rated switch current, and $I$ is the current through the switch.

The frequency of the current that passes through the capacitor is a factor that determines the equivalent series resistance of the capacitors [41]. It is possible to describe it as the conduction loss that is brought on by the internal resistance of the capacitor. The internal resistance of all the capacitors is taken as 0.1 ohms for this discussion [42], [43]. Because of the thermal stress and heat dispersion that are induced by these losses, the lifespan of capacitors is also negatively

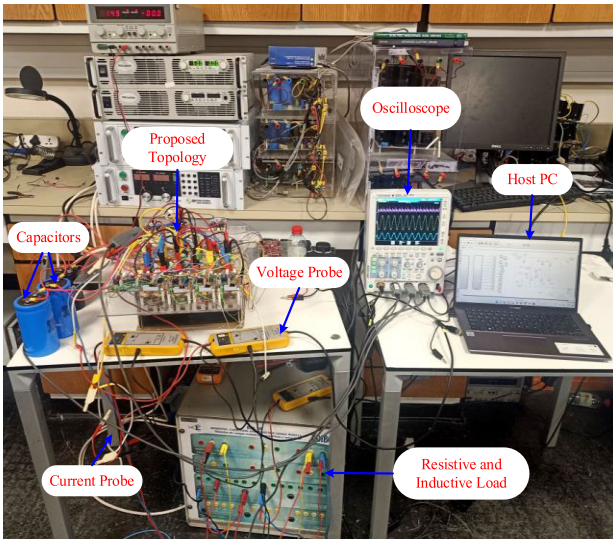


**FIGURE 9.** Experimental setup for the proposed topology.

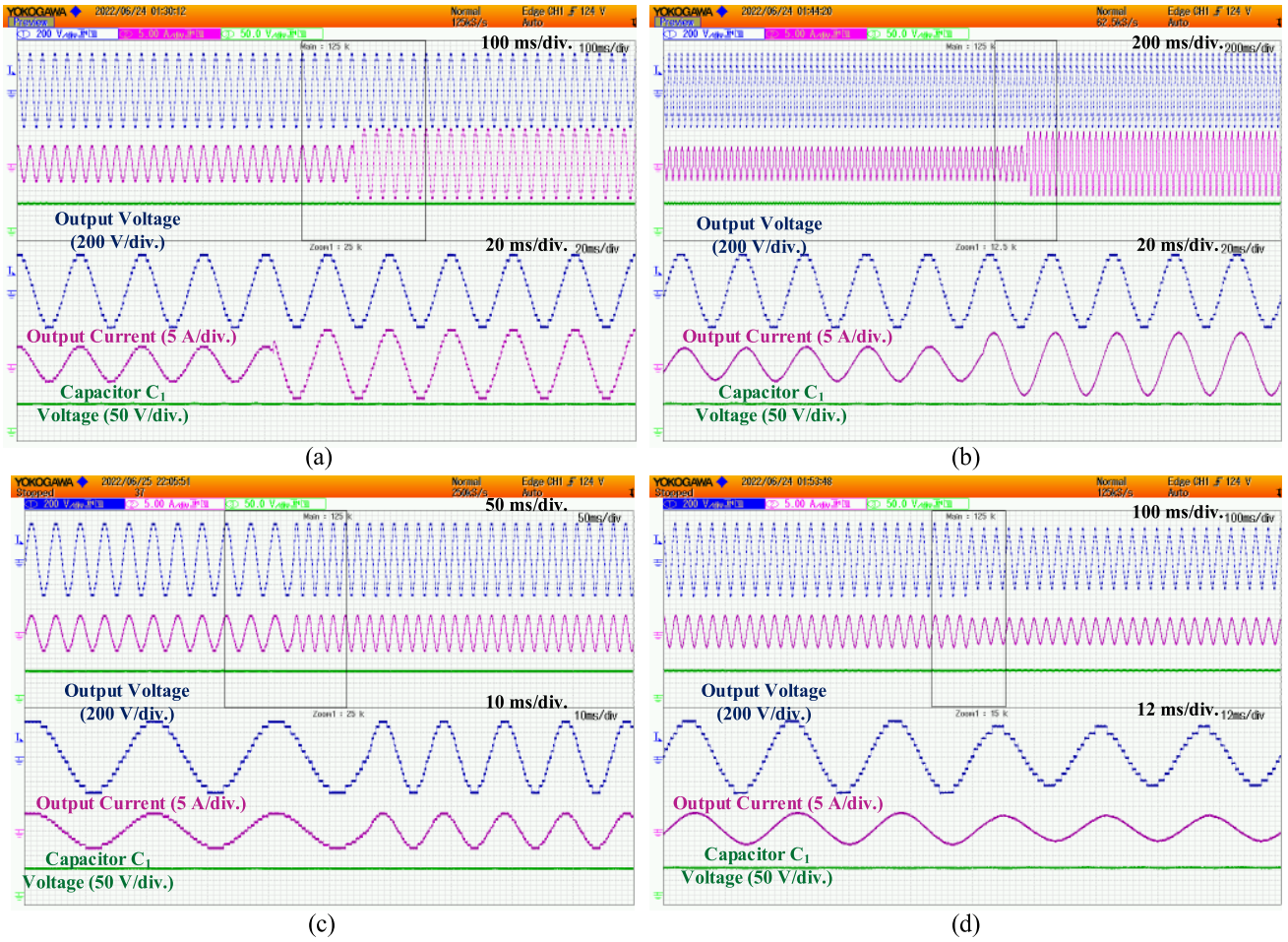


**FIGURE 10.** Experimental results for the symmetrical topology. Output voltage, output current and voltage across capacitor $C_1$ for (a) dynamic change of R-load (b) dynamic change of RL-load (c) change in frequency of the reference sinusoidal signal (d) change in Modulation Index (MI).

impacted. In PLECS, each of these three losses is modelled and simulated. Fig. 5 shows the power loss distribution among all the circuit components, while Fig. 6 shows the efficiency of both inverter configurations. Loss distribution for the symmetrical configuration generating 13 output levels with a change in dc source voltage is shown in Fig. 5 (a) at an output power of 100W. Fig. 5 (b) depicts the loss distribution for the asymmetrical configuration generating 17 output levels with a change in dc source voltage at an output power of 100W. Both of these graphs lead us to the conclusion that an increase in the dc source voltage will likewise result in a rise in losses. The efficiency versus output voltage curve for both symmetric and asymmetric topologies is shown in Fig. 6. The efficiency curve of 17 level topology is better than the 13-level topology. But both the inverter's efficiency is quite good for a large range of output power.

## VI. SIMULATION AND EXPERIMENTAL RESULTS

### A. SIMULATION RESULTS

To evaluate the performance of the proposed topology and control strategy, a simulation model is developed in MATLAB/Simulink Environment. Fig. 7 shows the various simulation results for the symmetrical 13-level configuration. Both the dc sources are taken as 50V. A small inductor is used in the charging circuit to limit the charging current. Fig. 7 (a) shows the output voltage, output current, capacitor voltage of $C_1$ and capacitor current through $C_1$ for a dynamic load change from 100Ω to 50Ω. Capacitor $C_1$ is getting charged to 50V, whereas $C_2$ and $C_3$ are always having 25V each as they are directly connected in parallel to $V_2$. Thus, 13-levels are being generated with a step of 50V and the peak voltage being close to 300V. The dynamic performance of the system for an inductive load is observed in Fig. 7 (b) when the load is changed from Z=100Ω+100mH to Z=50Ω+50mH. The effect of frequency change from 50Hz to 100Hz of the reference sinusoidal wave is shown in Fig. 7 (c). The number of levels decreases as the Modulation Index (MI) is decreased. The number of output levels changes from 13 to 11 as the MI is changed from 1 to 0.8, as shown in Fig. 7 (d).

For asymmetrical topology, which generates 17-levels at the output, dc sources $V_1 = 90V$ and $V_2 = 60V$ are taken.

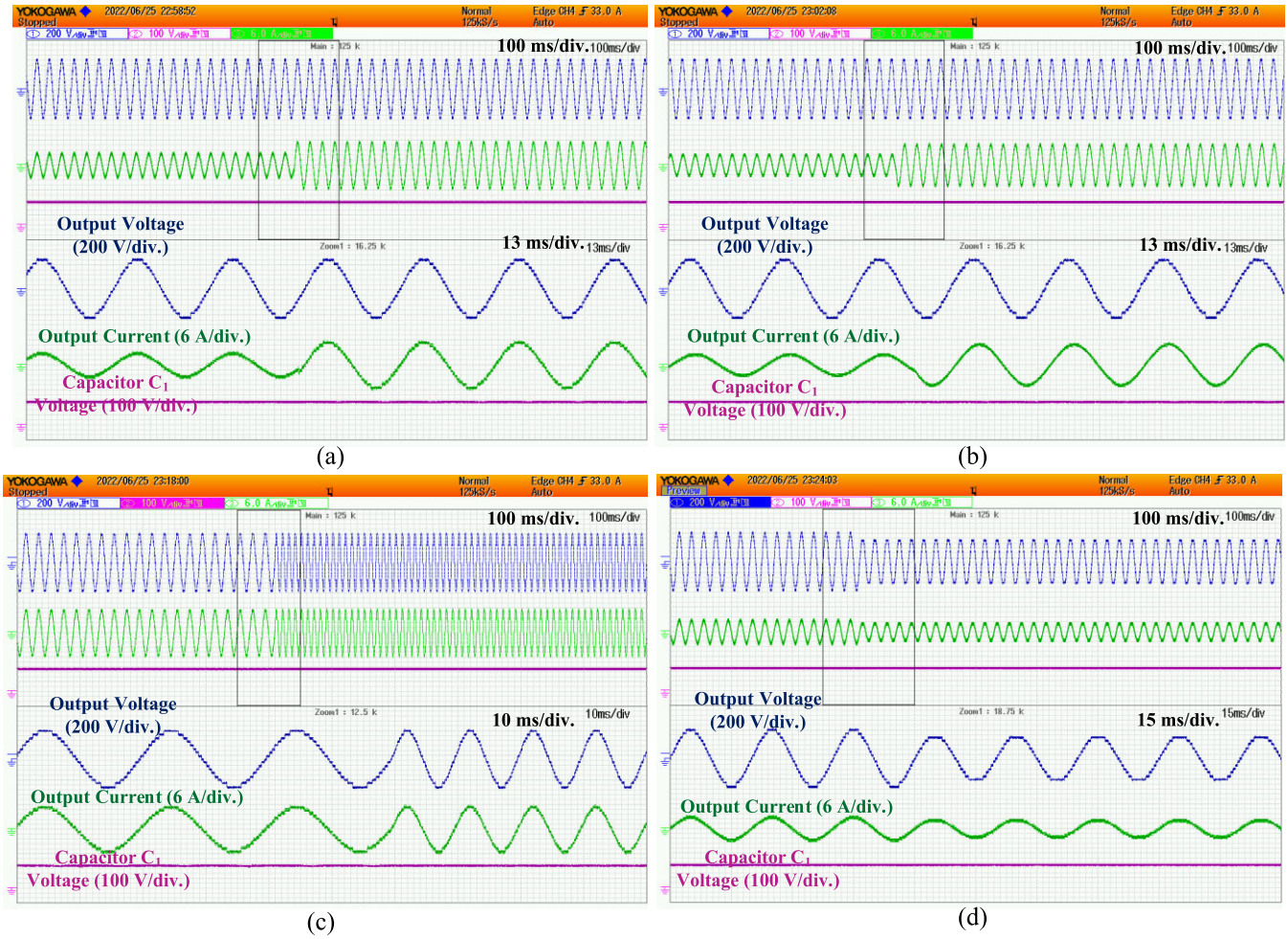


**FIGURE 11.** Experimental results for the asymmetrical topology. Output voltage, output current and voltage across capacitor $C_1$ for (a) dynamic change of R-load (b) dynamic change of RL-load (c) change in frequency of the reference sinusoidal signal (d) change in Modulation Index (MI).

Capacitor $C_1$ is getting charged equal to $V_1$ (90V), whereas $C_2$ and $C_3$ divide equally the dc source $V_2$. This asymmetrical configuration generates 17-levels at the output with a step voltage of 30V and a peak voltage of 240V, as shown in Fig. 8 (a), which also proves the gain of 1.6. It also shows the output voltage, output current, voltage across capacitor $C_1$ and the capacitor current through $C_1$ for a dynamic load change from 100Ω to 50Ω. The inverter configuration is also tested for inductive load change. Fig. 8 (b) shows the output waveforms for a sudden change of the inductive load from Z=100Ω+100mH to Z=50Ω+50mH. Output waveforms when the frequency of the reference wave is changed from 50 Hz to 100 Hz are shown in Fig. 8 (c). Fig. 8 (d) shows the output voltage, output current, voltage across capacitor $C_1$ and the capacitor current through $C_1$ for a MI change from 1 to 0.8 resulting in a reduction of the output voltage levels from 17 to 13.

### B. EXPERIMENTAL RESULTS

An experimental test circuit of 1-kW rating consisting of 12 IGBT switches (SKM75GB128D:1200 V), 3 capacitors (PG-6DI, $C_1$-4700$\mu$F, $C_2$, $C_3$-2200$\mu$F), and 3 diodes is designed in the lab in order to determine whether or not the proposed 13-level and 17-level SCMLI topologies are technically feasible. The experimental setup is shown in Fig. 9. A gate driver circuit GDX-4A2S1, based on Texas Instrument's UCC21520 high performance gate driver IC is used for pulse generation. For the purpose of sending gating signals to the switches, a digital signal processor (DSP) TMS320F28379D is utilized. Two dc sources (TDK-Lambda) are used.

For symmetrical configuration generating 13-levels at the output, both the dc sources are taken as 50V. Capacitor $C_1$ is getting charged to 50V, whereas $C_2$ and $C_3$ are always having 25V each as they are directly connected in parallel to $V_2$. Thus, 13-levels are being generated with a step of 50V and the peak voltage being close to 300V as shown in Fig. 10 (a) which verifies the gain of 1.5. The same waveform shows the output voltage, output current and voltage across capacitor $C_1$ for dynamic load change from 100Ω to 50Ω. Output waveforms for a sudden inductive load change from Z=100Ω+100mH to Z=50Ω+50mH is shown in Fig. 10 (b).

The effect of frequency change from 50Hz to 100Hz of the reference sinusoidal wave is shown in Fig. 10 (c). Number of levels decreases as the Modulation Index (MI) is decreased. The number of output levels changes from 13 to 11 as the MI is changed from 1 to 0.8 as shown in Fig. 10 (d).

For asymmetrical topology which generates 17-levels at the output, dc sources $V_1$ =90V and $V_2$ = 60V are taen. Capacitor $C_1$ is getting charged equal to $V_1$ (90V), whereas $C_2$ and $C_3$ divide equally the dc source $V_2$. This asymmetrical configuration generates 17-levels at the output with a step voltage of 30V and the peak voltage of 240V as shown in Fig. 11 (a), which also proves the gain of 1.6. It also shows the output voltage, output current and voltage across capacitor $C_1$ for a dynamic load change from 100Ω to 50Ω. The inverter configuration is also tested for inductive load change. Fig. 11 (b) shows the output waveforms for a sudden change of the inductive load from Z=100Ω+100mH to Z=50Ω+50mH. Output waveforms when the frequency of the reference wave is changed from 50 Hz to 100 Hz is shown in Fig. 11 (c). Fig. 11 (d) shows the output voltage, output current and voltage across capacitor $C_1$ for a MI change from 1 to 0.8. As a result, output voltage levels are reduced from 17 to 13.

## VII. CONCLUSION

This paper presented a topology for symmetric and asymmetric configuration, which generates 13 and 17 output levels, respectively, with lesser components. TSV and THD are also quite low. Although it used 2 sources, it generates boosted output voltage for both configurations with the help of a flying capacitor. Utilizing the concept of a dc-link capacitor across the sources, the output levels are increased. All the capacitors are self-balanced without the need for extra control circuitry. The static and dynamic stability of a topology is determined by the findings obtained for various load scenarios. In addition, power loss analysis provides insight into the switch kinetics. On the basis of the comparative analysis, it can be determined that the proposed topology provides greater performance compared to other topologies in the literature that have been compared. The architecture is very efficient and well-suited for renewable energy applications such as solar PV systems that are grid-connected.

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## REFERENCES

[1] M. Sarebanzadeh, M. A. Hosseinzadeh, C. Garcia, E. Babaei, M. Hosseinpour, A. Seifi, and J. Rodriguez, "A 15-level switched-capacitor multilevel inverter structure with self-balancing capacitor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 1477–1481, Mar. 2022, doi: 10.1109/TCSII.2021.3123115.

[2] F. Esmaeili, H. R. Koofigar, and H. Qasemi, "A novel single-phase multilevel high-gain inverter with low voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 6084–6092, Oct. 2022, doi: 10.1109/JESTPE.2022.3166233.

[3] M. A. Hosseinzadeh, M. Sarebanzadeh, E. Babaei, M. Rivera, and P. Wheeler, "A switched-DC source sub-module multilevel inverter topology for renewable energy source applications," *IEEE Access*, vol. 9, pp. 135964–135982, 2021, doi: 10.1109/ACCESS.2021.3115660.

[4] N. Sandeep, "A 13-level switched-capacitor-based boosting inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 3, pp. 998–1002, Mar. 2021, doi: 10.1109/TCSII.2020.3017338.

[5] Y. Ye, G. Zhang, X. Wang, Y. Yi, and K. W. E. Cheng, "Self-balanced switched-capacitor thirteen-level inverters with reduced capacitors count," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 1070–1076, Jan. 2022, doi: 10.1109/TIE.2021.3050378.

[6] R. Marusarz, "A switched capacitor, inductorless DC to AC voltage step-up power converter," in *Proc. 20th Annu. IEEE Power Electron. Spec. Conf.*, vol. 1, Jun. 1989, pp. 99–103, doi: 10.1109/PESC.1989.48478.

[7] T. Roy, P. K. Sadhu, and A. Dasgupta, "Cross-switched multilevel inverter using novel switched capacitor converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8521–8532, Nov. 2019, doi: 10.1109/TIE.2018.2889632.

[8] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019, doi: 10.1109/TIE.2018.2868325.

[9] J. Zeng, W. Lin, D. Cen, and J. Liu, "Novel K-type multilevel inverter with reduced components and self-balance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4343–4354, Dec. 2020, doi: 10.1109/JESTPE.2019.2939562.

[10] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018, doi: 10.1109/TPEL.2017.2669377.

[11] K.-M. Kim, J.-K. Han, and G.-W. Moon, "A high step-up switched-capacitor 13-level inverter with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2505–2509, Mar. 2021, doi: 10.1109/TPEL.2020.3012282.

[12] P. Bhatnagar, A. K. Singh, K. K. Gupta, and Y. P. Siwakoti, "A switched-capacitors-based 13-level inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 644–658, Jan. 2022, doi: 10.1109/TPEL.2021.3098827.

[13] V. Anand and V. Singh, "A 13-level switched-capacitor multilevel inverter with single DC source," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 1575–1586, Apr. 2022, doi: 10.1109/JESTPE.2021.3077604.

[14] M. S. B. Arif, U. Mustafa, S. B. M. Ayob, J. Rodriguez, A. Nadeem, and M. Abdelrahem, "Asymmetrical 17-level inverter topology with reduced total standing voltage and device count," *IEEE Access*, vol. 9, pp. 69710–69723, 2021, doi: 10.1109/ACCESS.2021.3077968.

[15] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of seventeen level inverter with reduced components," *IEEE Access*, vol. 9, pp. 16746–16760, 2021, doi: 10.1109/ACCESS.2021.3054001.

[16] M. M. Zaid, H. Ahmad, S. Madanzadeh, and J.-S. Ro, "Symmetric and asymmetric configuration of parallel-switched D-type multilevel inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7867–7879, Dec. 2022, doi: 10.1109/JESTPE.2021.3103151.

[17] S. Chen, Y. Ye, and X. Wang, "Hybrid 17-level inverters based on T-type flying-capacitor and switched-capacitor," *Int. J. Circuit Theory Appl.*, vol. 50, no. 3, pp. 886–903, Mar. 2022, doi: 10.1002/cta.3186.

[18] S. Majumdar, B. Mahato, and K. C. Jana, "Analysis and implementation of a generalised switched-capacitor multi-level inverter having the lower total standing voltage," *IET Power Electron.*, vol. 13, no. 17, pp. 4031–4042, Dec. 2020, doi: 10.1049/iet-pel.2020.0458.

[19] T. Roy and P. K. Sadhu, "A step-up multilevel inverter topology using novel switched capacitor converters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 236–247, Jan. 2021, doi: 10.1109/TIE.2020.2965458.

[20] R. S. Alishah, K. Bertilsson, F. Blaabjerg, M. A. J. Sathik, and A. Y. Rezaee, "New grid-connected multilevel boost converter topology with inherent capacitors voltage balancing using model predictive controller," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, Sep. 2020, pp. 1–7, doi: 10.23919/EPE20ECCEEurope43536.2020.9215690.

[21] R. S. Alishah, S. H. Hosseini, E. Babaei, M. Sabahi, and A. Zare, "Extended high step-up structure for multilevel converter," *IET Power Electron.*, vol. 9, no. 9, pp. 1894–1902, Jul. 2016, doi: 10.1049/iet-pel.2015.0893.

[22] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012, doi: 10.1109/TIE.2011.2158768.

[23] Y. Ye, S. Chen, X. Wang, and K.-W.-E. Cheng, "Self-balanced 13-level inverter based on switched capacitor and hybrid PWM algorithm," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4827–4837, Jun. 2021, doi: 10.1109/TIE.2020.2989716.

[24] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Mar. 2014, doi: 10.1109/TIE.2014.2314052.

[25] P. Panda, P. R. Bana, and G. Panda, "A switched-capacitor self-balanced high-gain multilevel inverter employing a single DC source," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 3192–3196, Dec. 2020, doi: 10.1109/TCSII.2020.2975299.

[26] W. Lin, J. Zeng, J. Liu, Z. Yan, and R. Hu, "Generalized symmetrical step-up multilevel inverter using crisscross capacitor units," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7439–7450, Sep. 2020, doi: 10.1109/TIE.2019.2942554.

[27] M. D. Siddique, S. Mekhilef, A. Sarwar, A. Alam, and N. M. Shah, "Dual asymmetrical DC voltage source based switched capacitor boost multilevel inverter topology," *IET Power Electron.*, vol. 13, no. 7, pp. 1481–1486, 2020, doi: 10.1049/iet-pel.2019.1567.

[28] S. Islam, M. D. Siddique, A. Iqbal, and S. Mekhilef, "A 9- and 13-level switched-capacitor-based multilevel inverter with enhanced self-balanced capacitor voltage capability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7225–7237, Dec. 2022, doi: 10.1109/JESTPE.2022.3179439.

[29] K. P. Panda, P. R. Bana, and G. Panda, "A reduced device count single DC hybrid switched-capacitor self-balanced inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 3, pp. 978–982, Mar. 2021, doi: 10.1109/TCSII.2020.3018333.

[30] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014, doi: 10.1109/TIE.2013.2290769.

[31] M. J. Sathik, N. Sandeep, D. Almakhles, and F. Blaabjerg, "Cross connected compact switched-capacitor multilevel inverter ($C^3$-SCMLI) topology with reduced switch count," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3287–3291, Dec. 2020, doi: 10.1109/TCSII.2020.2988155.

[32] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019, doi: 10.1109/ACCESS.2019.2925277.

[33] M. R. Hussan, A. Sarwar, M. D. Siddique, A. Iqbal, and B. Alamri, "A cross connected asymmetrical switched-capacitor multilevel inverter," *IEEE Access*, vol. 9, pp. 96416–96429, 2021, doi: 10.1109/ACCESS.2021.3093826.

[34] A. K. Singh and R. K. Mandal, "A novel 17-level reduced component single DC switched-capacitor-based inverter with reduced input spike current," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 6045–6056, Oct. 2022, doi: 10.1109/JESTPE.2022.3166222.

[35] A. K. Singh and R. K. Mandal, "A new switched capacitor based multilevel inverter with fewer capacitors," *Int. J. Electron.*, vol. 2022, pp. 1–15, Jul. 2022, doi: 10.1080/00207217.2022.2094472.

[36] M. R. Hussan, A. Sarwar, M. D. Siddique, S. Mekhilef, S. Ahmad, M. Sharaf, M. Zaindin, and M. Firdausi, "A novel switched-capacitor multilevel inverter topology for energy storage and smart grid applications," *Electronics*, vol. 9, no. 10, p. 1703, Oct. 2020, doi: 10.3390/electronics9101703.

[37] M. Tayyab, A. Sarwar, I. Khan, M. Tariq, M. R. Hussan, S. Murshid, and W. Alhosaini, "A single source switched-capacitor 13-level inverter with triple voltage boosting and reduced component count," *Electronics*, vol. 10, no. 19, pp. 1–14, 2021, doi: 10.3390/electronics10192321.

[38] Z. Sarwer, A. Sarwar, M. Zaid, M. R. Hussan, M. Tariq, B. Alamri, and A. Alahmadi, "Implementation of a novel variable structure nearest level modulation on cascaded H-bridge multilevel inverter," *IEEE Access*, vol. 9, pp. 133974–133988, 2021, doi: 10.1109/ACCESS.2021.3113704.

[39] M. Ali, M. Tariq, A. Sarwar, and B. Alamri, "A 13-, 11-, and 9-level boosted operation of a single-source asymmetrical inverter with hybrid PWM scheme," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12817–12828, Dec. 2022, doi: 10.1109/TIE.2022.3144576.

[40] P. V. D. C. Agarwal and M. S. V. E. M. Khadkikar, "A novel 1-$\varphi$ dual input nine-level inverter topology with generalized modulation technique," *IEEE Trans. Energy Convers.*, vol. 37 no. 3, pp. 1789–1802, Sep. 2022, doi: 10.1109/TEC.2022.3140232.

[41] G. I. Orfanoudakis, S. M. Sharkh, and M. A. Yuratich, "Analysis of DC-link capacitor losses in three-level neutral point clamped and cascaded H-bridge voltage source inverters," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2010, pp. 664–669, doi: 10.1109/ISIE.2010.5637820.

[42] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016, doi: 10.1109/TIE.2016.2529563.

[43] M. J. Sathik, K. Bhatnagar, Y. P. Siwakoti, H. M. Bassi, M. Rawa, N. Sandeep, Y. Yang, and F. Blaabjerg, "Switched-capacitor multilevel inverter with self-voltage-balancing for high-frequency power distribution system," *IET Power Electron.*, vol. 13, no. 9, pp. 1807–1818, Jul. 2020, doi: 10.1049/iet-pel.2019.1249.

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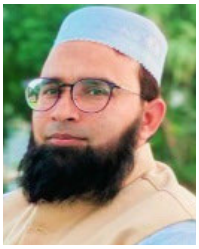

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