A Novel Modified Switched Inductor Boost Converter With Reduced Switch Voltage Stress

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***Abstract*—Recently, switched inductor (SI) and switched capacitor techniques in dc–dc converter are recommended to achieve high voltage by using the principle of parallel charging and series discharging of reactive elements. It is noteworthy that four diodes, one high-voltage rating switch, and two inductors are required to design classical SI boost converter (SIBC). Moreover, in classical SIBC, the switch voltage stress is equal to the output voltage. In this article, modified SIBC (mSIBC) is proposed with reduced voltage stress across active switches. The proposed mSIBC configuration in this article is transformerless and simply derived by replacing the one diode of the classical SI structure with an active switch. As a result, mSIBC required low-voltage rating active switches, since the total output voltage is shared into two active switches. Moreover, the proposed mSIBC is low in cost, provides higher efficiency, and requires the same number of components compared with the classical SIBC. The continuous conduction mode and discontinuous conduction mode analysis, the effect of nonidealities on voltage gain, design methodology, and comparison are presented in detail. The operation and performance of the designed 500-W mSIBC are experimentally validated under different perturbations.**

***Index Terms*—Boost converter, dc–dc converter, high voltage gain, switched inductor (SI), voltage stress reduction.**

I. Introduction

IN THE recent past years, attention toward the utilization of renewable energy sources to produce electricity has considerably increased throughout the world. Photovoltaic and fuel cells have gained sufficient attention as renewable energy generation sources. However, the output of these renewable energy sources is low, which is insufficient to use in all the applications [1]. Therefore, a highly efficient and high-gain dc–dc converter is required to be included in the system. In order to step-up the voltage or current with high gain, dc–dc power converters are essential in case of many applications, for e.g., photovoltaic and fuel cell energy conversion, uninterruptible power supply, dc microgrid, automobile, high-intensity discharged lamp ballast, LED, hybrid vehicle, etc., for the utilization of low-voltage sources [2], [3]. As far as the conventional boost converter is concerned, theoretically, it provides a high voltage gain at a duty cycle value closer to unity. However, practically, the converter voltage gain is restricted by the inductor's parasitic resistance, reverse diode recovery problem, electromagnetic interferences, use of extreme duty cycle (closer to unity), rating of semiconductor devices, high conduction loss at a switch, and effect of parasitic resistance of capacitor [4], [5].

In literature, many power converter topologies are recently published based on several boosting techniques [6]. In order to achieve high voltage and isolation, transformer-based converters, such as flyback, push–pull, and H-Bridge, could be good options. Nonetheless, these converter structures are bulky, large, and costly due to the requirement of a high-frequency transformer and supplementary circuitry for dealing with the leakage inductance energy [6]–[8]. Moreover, the active switches of these converters suffer from high-voltage stress due to transformer leakage inductance. Consequently, additional energy regeneration techniques and voltage clamping techniques are required to recycle the leakage energy and minimize the voltage stress of active switches [9], [10]. Coupled-inductor-based topologies can provide a solution to attain high voltage gain with or without isolation; however, additional clamped circuitry and input filter are required to reduce ripples and leakage inductor energy recovery schemes which increases the cost. Furthermore, extra losses associated with the clamp circuit will be introduced as well [11]–[13]. Moreover, these structures are complex, and the gain factor is dependent on the coupling coefficient of the coupled inductors. Cascaded and quadratic boost converter structures can be other possible solutions; however, there is still a requirement of high-voltage devices as the switch voltage stress is the same as the output voltage. Furthermore, the cascade structure of two or multiple dc–dc converters leads to circuit complexity and a higher cost. Moreover, the complex control is required since the voltage gain is highly nonlinear, and two or multiple power switches need to be synchronized [6], [14].

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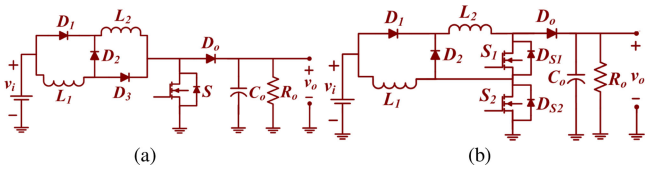

Fig. 1. Power circuitry. (a) Existing configuration of transformerless high step-up dc–dc converter or classical SIBC [17], [21]. (b) Proposed converter.

In order to overcome the drawbacks of the abovementioned converters, switched inductor (SI), hybrid switched-inductor and capacitor, interleaved front-end structure, and multiplier-based converters are possible solutions [14]–[18]. However, in most cases, several power stages are required, and the voltage stress across active switches is high or equal to the total output voltage. Moreover, the use of many multiplier cells leads to an increase in system size and cost. In order to reduce voltage and current stresses on the active switches and to attain a higher step-up voltage gain without a high duty cycle, converters topologies are proposed in [19]–[21]. However, the converters proposed in [19] and [20] required a large number of reactive components in the intermediate stage. Moreover, multiple stages are used to achieve high voltage. The circuits proposed in [21]–[23] are only suitable under floating load conditions, and there is no significant improvement in the voltage gain even by including more switches in the circuit. High-gain and double-duty triple-mode converters are proposed to achieve higher voltage gain without utilizing transformer, coupled inductor, voltage multiplier, and multiple voltage lifting techniques [22], [23]. These converters have a wide operating range of duty cycle and can achieve a high output voltage. However, the major drawbacks of these converters are their complex control algorithm because of the utilization of two duty cycles and the use of three switches, which increases complexity, size, and cost. Moreover, these converters are suitable only for floating output.

In this article, modified SI boost converter (mSIBC) is proposed with reduced voltage stress across active switches by modifying the structure of classical SI boost converter (SIBC). The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) analyses, the effect of unequal inductances, the effect of nonidealities, comparison, and design of mSIBC are presented in detail. The experimental results of mSIBC are presented to validate the proposed concept. This article is organized as follows. Section II presents the power circuitry, steady-state characteristics, small-signal modeling, and CCM and DCM analyses. The effect of unequal inductance is discussed in Section III. Subsequently, the effects of nonidealities of components/devices and efficiency analysis are discussed in Section IV. The comparison of the converters is given in Section V. Section VI deals with design methodology, closed-loop controller strategy, and experimental results of designed mSIBC. Finally, concluding remarks are provided in Section VII.

II. Modified SI Boost Converter

Fig. 1(a) shows the existing configuration of transformerless high step-up dc–dc converter or classical SIBC [17], [21]. In SIBC, SI circuitry is employed to achieve higher voltage gain compared with the classical boost converter. However, it is noteworthy that the voltage stress across switches increases with voltage gain and total output appears across the switch. Therefore, slight modification without increasing the number of components has been done in the power circuit of classical SIBC to reduce the voltage stress of switch and achieve the same voltage gain. The proposed dc–dc converter utilizes the inherent switched-inductor technique (parallel charging and series discharging of inductors) to achieve high step-up voltage gain.

A. Power Circuit

Fig. 1(b) shows the power circuit of the proposed mSIBC, which consists of two active switches S_1 and S_2, three diodes D_1, D_2, and D_o, two inductors L_1 and L_2, capacitor C_o, and load R_o. The proposed mSIBC configuration is transformerless and simply derived by replacing one diode of the SI network of classical SIBC with an active switch. It is noteworthy that the total number of components in the proposed mSIBC and classical SIBC is the same and provides the same voltage gain. However, in the proposed mSIBC, the total output voltage is distributed among the two active switches. Therefore, low-voltage rating switches can be employed to design the power circuit of the proposed mSIBC configuration. Initially, to analyze the steady-state characteristics of the proposed mSIBC configuration in CCM, all components are considered ideal and the voltage drop across semiconductor devices due to ON-state resistance is neglected, and the capacitor is large enough to provide ripple-free voltage. In this section, it is considered that the inductors L_1 and L_2 are equal in inductance that means $L_1 = L_2 = L$ (ideal case). Based on the circuitry, the currents through inductor L_1 and L_2 are equal and written as

$$i_L = i_{L1} = i_{L2}. \tag{1}$$

The typical waveforms of mSIBC for CCM and DCM are shown in Fig. 2(a) and (b), respectively; where T_{ON} is the time period for mode I (i.e., time t_0–t_1), and T_S is the total time period.

B. CCM—Operating Principle and Small-Signal Modeling

The working of the proposed mSIBC for CCM is divided into two modes; mode I when both switches S_1 and S_2 are turned ON (time t_0–t_1), and mode II when both switches S_1 and S_2 are turned OFF (time t_1–t_2).

1) Mode I (Time t_0–t_1): In this mode, inductor L_1 is magnetized by input supply (v_i) through switch S_2, and inductor L_2 is magnetized by input supply (v_i) through diode D_1 and switches S_1 and S_2. The capacitor C_o is discharged through the load R_o. During this mode, diodes D_2 and D_o are reversed biased, and diode D_1 is forward biased. The equivalent circuitry of mSIBC for this mode is shown in Fig. 3(a). It is noteworthy that both inductors are magnetized in parallel by input supply v_i with the equal current. The voltages across inductors L_1 and L_2 are obtained as

$$v_L = v_{L1} = v_{L2} = v_i. \tag{2}$$

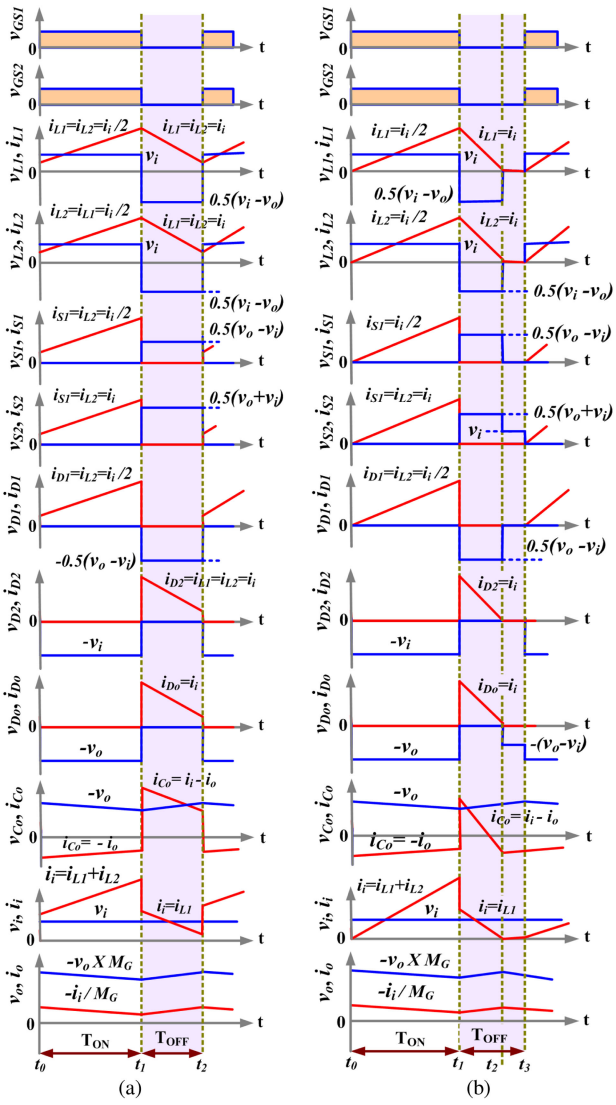

Fig. 2. Typical waveforms of mSIBC for (a) CCM and (b) DCM.

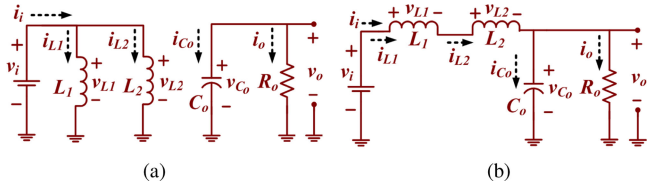

Fig. 3. Equivalent circuit. (a) ON state. (b) OFF state.

The input current i_i is obtained as

$$i_i = 2i_L = 2i_{L1} = 2i_{L2}. \tag{3}$$

The differential expression for the inductors L_1 and L_2 and capacitor C_o can be obtained as follows:

$$\frac{d\left(i_L\right)}{dt} = \frac{d\left(i_{L1}\right)}{dt} = \frac{d\left(i_{L2}\right)}{dt} = \frac{v_i}{L}, \quad \frac{d\left(v_{Co}\right)}{dt} = \frac{-v_o}{C_o R_o}. \tag{4}$$

2) Mode II (Time t_1–t_2): In this mode, both the inductors L_1 and L_2 are demagnetized in series with the input voltage v_i to provide energy to the load R_o and charged the capacitor C_o through diode D_2 and D_o. During this mode, diodes D_2 and D_o are forward biased, and diode D_1 is reversed biased. The equivalent circuit of mSIBC for this mode is shown in Fig. 3(b). The voltages across inductors L_1 and L_2 are obtained as

$$v_L = v_{L1} = v_{L2} = \left(v_i - v_o\right)/2. \tag{5}$$

The input current i_i is obtained as

$$i_i = i_L = i_{L1} = i_{L2}. \tag{6}$$

The differential expression for the inductor L_1 and L_2 and capacitor C_o can be obtained as follows:

$$\frac{d\left(i_L\right)}{dt} = \frac{d\left(i_{L1}\right)}{dt} = \frac{d\left(i_{L2}\right)}{dt} = \frac{v_i - v_o}{2L}, \frac{d\left(v_{Co}\right)}{dt} = \frac{1}{C_o}\left(i_L - \frac{v_o}{R_o}\right). \tag{7}$$

Assume, in general, $\langle x \rangle$ is the average value of variable x. Using (2)–(7), the average equations are obtained as follows:

$$\begin{cases} L\dfrac{d\left\langle i_L\right\rangle}{dt} = \dfrac{\left\langle v_i\right\rangle\left(1+d\right) - \left\langle v_o\right\rangle\left(1-d\right)}{2} \\ C_o\dfrac{d\left\langle v_{Co}\right\rangle}{dt} = \left\langle i_L\right\rangle\left(1-d\right) - \dfrac{\left\langle v_o\right\rangle}{R_o}, \left\langle i_i\right\rangle = \left\langle i_L\right\rangle\left(1+d\right) \end{cases} \tag{8}$$

where d is a variable used for duty. In order to obtain the small-signal model from (8), perturbation variables are necessary. Therefore, small ac variation with small magnitude is assumed in each variable of (8). Therefore

$$\begin{cases} \left\langle v_i\right\rangle = V_i + \hat{v}_i, \left\langle v_{Co}\right\rangle = V_{Co} + \hat{v}_{Co}, \left\langle v_o\right\rangle = V_o + \hat{v}_o \\ \left\langle i_L\right\rangle = I_L + \hat{i}_L, \left\langle i_i\right\rangle = I_i + \hat{i}_i, d = D + \hat{d} \end{cases} \tag{9}$$

where

$$\left\{\left|\hat{v}_i\right| \ll V_i, \left|\hat{v}_{Co}\right| \ll V_{Co}, \left|\hat{v}_o\right| \ll V_o, \left|\hat{i}_L\right| \ll I_L, \left|\hat{i}_i\right| \ll I_i\right. . \tag{10}$$

Using (8)–(10)

$$\begin{cases} L\frac{d\left(I_L+\hat{i}_L\right)}{dt} = \frac{\left(V_i+\hat{v}_i\right)\left(1+D+\hat{d}\right)-\left(V_o+\hat{v}_o\right)\left(1-D-\hat{d}\right)}{2} \\ C_o\frac{d\left(V_{Co}+\hat{v}_{Co}\right)}{dt} = \left(I_L+\hat{i}_L\right)\left(1-D-\hat{d}\right) - \frac{V_o+\hat{v}_o}{R_o} \\ I_i+\hat{i}_i = \left(I_L+\hat{i}_L\right)\left(1+D+\hat{d}\right) \end{cases} . \tag{11}$$

Using (11), the dc variable equation can be obtained as follows:

$$0 = \frac{V_i\left(1+D\right) - V_o\left(1-D\right)}{2}, \quad 0 = I_L\left(1-D\right) - \frac{V_o}{R_o},$$

$$I_i = I_L\left(1+D\right). \tag{12}$$

Using (12), the voltage gain of the mSIBC is obtained as follows:

$$M = V_o/V_i = \left(1+D\right)/\left(1-D\right). \tag{13}$$

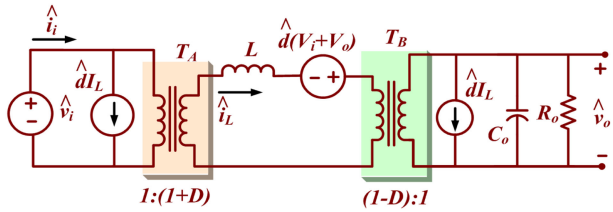

Fig. 4. Small-signal model of the proposed mSIBC converter ($L_1 = L_2 = L$).

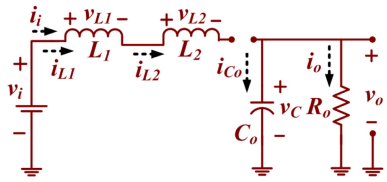

Fig. 5. Equivalent circuitry for the DCM mode.

where M is the voltage gain, and D is the duty cycle. It is observed that the voltage gain of mSIBC and classical SIBC is the same. By neglecting second-order term in (11), the small-signal ac equations are obtained as follows:

$$\begin{cases} L\dfrac{d\left(\hat{i}_L\right)}{dt} = \dfrac{\left(V_i+V_o\right)\hat{d}+\left(1+D\right)\hat{v}_i-\left(1-D\right)\hat{v}_o}{2} \\ C_o\dfrac{d\left(\hat{v}_{Co}\right)}{dt} = -I_L\hat{d}+\left(1-D\right)\hat{i}_L-\left(\hat{v}_o/R_o\right) \\ \hat{i}_i = I_L\hat{d}+\left(1+D\right)\hat{i}_L \end{cases}. \tag{14}$$

Using (14), the small-signal model is obtained and shown in Fig. 4, in which T_A and T_B are ideal transformers with the turn ratio 1:(1 + D) and (1 − D):1, respectively. Using the Laplace transform, the relation between $\hat{d}(S)$, $\hat{v}_i(S)$, and $\hat{v}_o(S)$ is obtained as follows:

$$\hat{v}_o(S) = M_i(S)\hat{v}_i(S) + M_d(S)\hat{d}(S) \tag{15}$$

where $M_i(S)$ and $M_d(S)$ are expressed as follows:

$$\begin{aligned} M_i(S) &= \left.\frac{\hat{v}_o(S)}{\hat{v}_i(S)}\right|_{\hat{d}(S)=0} \\ &= \frac{(1+D)/(1-D)}{1+2LS/R_o(1-D)^2+2LC_oS^2/(1-D)^2} \end{aligned} \tag{16}$$

$$\begin{aligned} M_d(S) &= \left.\frac{\hat{v}_o(S)}{\hat{d}(S)}\right|_{\hat{v}_i(S)=0} \\ &= \frac{\left(V_i+V_o\right)/(1-D)-2I_LLS/(1-D)^2}{1+2LS/R_o(1-D)^2+2C_oLS^2/(1-D)^2}. \end{aligned} \tag{17}$$

C. DCM—Operating Principle and Analysis

The working of the proposed mSIBC for DCM is divided into three modes; one when switches S_1 and S_2 are turned ON (ON state), second when switches S_1 and S_2 are turned OFF and inductor currents are nonzero, and third when switches S_1 and S_2 are turned OFF and inductor currents are zero. Let us assume the inductor current reaches zero at time t_2, as shown in Fig. 2(b). In typical DCM characteristics [see Fig. 2(b)], K_1T_S or T_{ON} is mode I time period (i.e., time t_0–t_1), K_2T_S or $T_{\mathrm{OFF},1}$ (i.e., time t_1–t_2) is mode II time period, and K_3T_S or $T_{\mathrm{OFF},2}$ (i.e., time t_2–t_3) is mode III time period.

1) Mode I (t_0–t_1)—Switches S_1 and S_2 Are Turned on: For this mode, the operation of mSIBC and equivalent circuitry is the same as CCM mode I. In this mode, both inductors L_1 and L_2 are magnetized in parallel by input voltage v_i. At the starting of this mode (time t_o or $t_o + T_s$), both inductors L_1 and L_2 currents started from zero level and reached the maximum level at the end of this mode. The maximum current through inductors L_1 and L_2 can be obtained as follows:

$$I_{L,\max} = I_{L1,\max} = I_{L2,\max} = V_iK_1/Lf_s \tag{18}$$

where $I_{L1,\max}$ and $I_{L2,\max}$ are the maximum currents through inductor L_1 and L_2, respectively, and $f_s = 1/T_S$ is the switching frequency. The current ripples of inductors L_1 and L_2 can be obtained as

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = V_iK_1/Lf_s \tag{19}$$

where ΔI_{L1} and ΔI_{L2} are the current ripples of inductor L_1 and L_2, respectively.

2) Mode II (t_1–t_2)—Switches S_1 and S_2 Are Turned off and Inductor Currents Are Nonzero: For this mode, the operation of mSIBC and equivalent circuitry is the same as CCM mode II. In this mode, inductors L_1 and L_2 are demagnetized in series with input voltage v_i to charge capacitor C_o and provide energy to load R_o. At the starting of this mode (time t_1 or $t_1 + T_s$), both inductors L_1 and L_2 currents started from the maximum current level and reached zero level at the end of this mode (time t_2 or $t_2 + T_s$). Another expression for the maximum current level through inductor L_1 and L_2 can be obtained as follows:

$$I_{L,\max} = I_{L1,\max} = I_{L2,\max} = \left(V_o - V_i\right)K_2/2Lf_s. \tag{20}$$

The current ripples of inductors L_1 and L_2 can be obtained as

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = \left(V_o - V_i\right)K_2/2Lf_s \tag{21}$$

3) Mode III (t_2–t_3)—Switches S_1 and S_2 Are Turned off and Inductor Currents Are Zero: The equivalent circuitry for this mode is shown in Fig. 5. In this mode, switches S_1 and S_2 are turned OFF and inductors L_1 and L_2 currents are at zero level. Therefore, stored energies of inductors L_1 and L_2 are zero. All the diodes D_o–D_2 are reversed biased, and capacitor C_o is discharged through load R_o.

Using (19) and (20), the time period of mode II i.e., K_2T_s or $T_{\mathrm{OFF},1}$ can be obtained as

$$K_2T_s \text{ or } T_{\mathrm{OFF},1} = 2V_iK_1/\left(V_o - V_i\right)f_s. \tag{22}$$

It is known that

$$T_{\mathrm{ON}} + T_{\mathrm{OFF},1} + T_{\mathrm{OFF},2} = T_s. \tag{23}$$

The time period for mode I and mode III can be obtained as

$$T_{\mathrm{ON}} = \frac{K_1}{f_s}, K_3 T_s \text{ or } T_{\mathrm{OFF},2} = 1 - \frac{1}{f_s}\left[K_1 + \frac{2V_i K_1}{(V_o - V_i)}\right]. \tag{24}$$

From Fig. 2(b), the average current through capacitor C_o can be obtained as

$$I_{Co} = 0.5\,(K_2 \times I_{L,\max}) - I_o = 0.5\,(K_2 \times I_{L,\max}) - V_o/R_o. \tag{25}$$

By using (22) and (25)

$$I_{Co} = 0.5\left(\frac{2V_i K_1}{V_o - V_i} \times \frac{V_i K_1}{L f_s}\right) - \frac{V_o}{R_o}. \tag{26}$$

Under steady-state condition, any capacitor average current is always zero. Therefore, (26) can be rewritten as

$$\frac{2V_i K_1}{V_o - V_i} \times \frac{V_i K_1}{L f_s} = \frac{2V_o}{R_o}. \tag{27}$$

Using (27), the quadratic equation is obtained as

$$\left(\frac{V_o}{V_i}\right)^2 - \frac{V_o}{V_i} - \frac{{K_1}^2}{\xi_L} = 0. \tag{28}$$

where ξ_L is the normalized time constant for inductors L_1 and L_2, and its value is equal to Lf_s/R_o. Therefore, the variation in ξ_L is based on the value of L, f_s, and R_o. By solving (28), the voltage gain of mSIBC for DCM (M_{DCM}) can be obtained as

$$M_{\mathrm{DCM}} = \frac{V_o}{V_i} = \frac{1}{2} + \left(\frac{0.25\xi_L + {K_1}^2}{\xi_L}\right)^{1/2} = \frac{1}{2} + \left(\frac{1}{4} + \frac{{K_1}^2 R_o}{L f_s}\right)^{1/2}. \tag{29}$$

Suppose that the proposed mSIBC configuration is operated at the boundary of CCM and DCM, then the voltage gain of CCM and DCM is same. Therefore, by using (13) and (29)

$$\frac{V_o}{V_i} = 0.5 + \left(\frac{0.25\xi_{LB} + {K_1}^2}{\xi_{LB}}\right)^{1/2} = \frac{1+D}{1-D}. \tag{30}$$

It is known that the mode I for CCM and DCM is the same. Therefore, $K_1 = D$, and the normalized boundary time constant (ξ_{LB}) for inductors L_1 and L_2 can be obtained as

$$\xi_{LB} = 0.5\left(D^3 - 2D^2 + D\right)/(1+D). \tag{31}$$

Fig. 6 depicts the plot of ξ_{LB} versus D; where DCM and CCM regions are shown. If the value of ξ_{LB} is larger than ξ_{LB}, then the proposed mSIBC configuration operates in DCM.

III. Effect of Unequal Inductances on Voltage Gain

The operation of the proposed converter depends on the values of the inductors L_1 and L_2. Mainly, the current waveforms through inductor L_1 and L_2 are dependent on the values of L_1 and L_2.

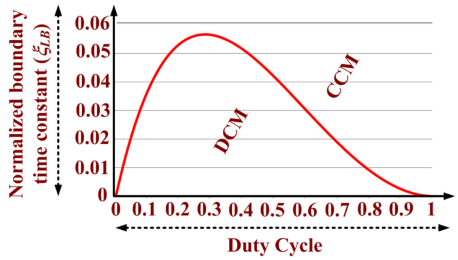

Fig. 6. Normalized boundary time constant versus duty cycle.

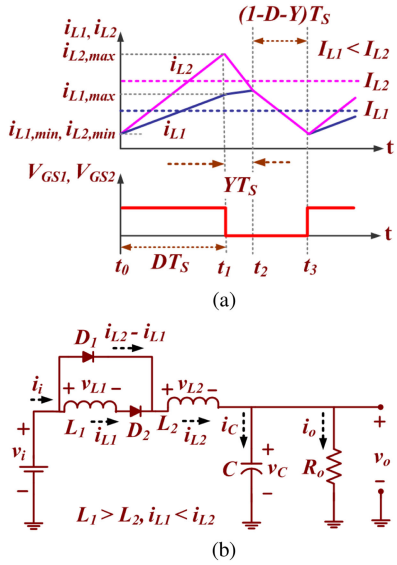

Fig. 7. When $L_1 > L_2$. (a) Inductor currents. (b) Mode II.

A. When the Value of L_1 is Larger Than the Value of L_2

The characteristic waveforms of the inductor L_1 and L_2 currents are shown in Fig. 7(a). In this case, the converter operates in three modes as follows.

1) Mode I (Time t_0–t_1): In this mode, switches S_1 and S_2 are turned ON, and equivalent circuitry is the same as mode I of CCM. In this mode, inductors L_1 and L_2 are magnetized by input supply v_i, diodes D_2 and D_o are reversed biased, diode D_1 is forward biased, and the capacitor C_o is discharged through the load R_o. The input current i_i is equal to sums of inductor currents, i.e., $i_i = i_{L1} + i_{L2}$. The slope of the inductor L_1 and L_2 currents can be obtained as follows:

$$\frac{d\,(i_{L1})}{dt} \approx \frac{v_i}{L_1}, \frac{d\,(i_{L2})}{dt} \approx \frac{v_i}{L_2}. \tag{32}$$

In this mode, the current through inductor L_1 is smaller than the current through inductor L_2 due to $L_1 > L_2$.

2) Mode II (Time t_1–t_2): This mode occurs for short duration [YT_s, as shown in Fig. 7(a)] when switches S_1 and S_2 are just turned OFF. The equivalent circuitry is shown in Fig. 7(b), where diodes D_1 and D_2 are forward biased. During this mode, the currents through inductor L_1 increase with small positive slope (approximately zero slope) and the currents through inductor L_2

decreases with a large negative slope. The inductor L_1 is magnetized and inductor L_2 is demagnetized through path $v_i - L_1 - D_2 - L_2 - (\mathrm{C_o}//R_o)$ and $v_i - D_1 - L_2 - (\mathrm{C_o}//R_o)$, respectively. The value of current through inductor L_2 is larger than the current through inductor L_1. Also, the input current i_i is equal to inductor L_2 currents, i.e., $i_i = i_{L2}$, and the resultant current through diode D_1 is the subtraction of inductors L_2 and L_1 currents, i.e., $i_{L2} - i_{L1}$. The slope of the inductor L_1 and L_2 currents is obtained as follows:

$$\frac{d\,(i_{L1})}{dt} \approx 0, \frac{d\,(i_{L2})}{dt} \approx \frac{v_i - v_o}{L_2}. \tag{33}$$

This mode ends as soon as the currents through inductor L_1 and L_2 are equal, and circuitry operates in mode III.

3) Mode III (Time t_1–t_2): In this mode, switches S_1 and S_2 are turned OFF, and equivalent circuitry is the same as CCM mode II. During this mode, diodes D_2 and D_o are forward biased, and diode D_1 is reversed biased. Throughout this mode, inductors L_1 and L_2 are discharged in series with input voltage v_i through load R_o. In this case, input current and the current through inductor L_1 and L_2 are equal, i.e., $i_i = i_{L1} = i_{L2}$. The voltage across inductor L_1 and L_2 is obtained as follows:

$$\frac{d\,(i_{L1})}{dt} = \frac{v_i - v_o}{L_1 + L_2}, \frac{d\,(i_{L2})}{dt} = \frac{v_i - v_o}{L_1 + L_2}. \tag{34}$$

Using small approximation and inductor volt second balance

$$\text{For } L_1 \Rightarrow v_i(D) + \frac{v_i - v_o}{L_1 + L_2} L_1(1 - D - Y) = 0 \tag{35}$$

$$\text{For } L_2 \Rightarrow v_i(D) + (v_i - v_o)Y + \frac{v_i - v_o}{L_1 + L_2} L_2(1 - D - Y) = 0. \tag{36}$$

Solving (35) and (36), the voltage gain of mSIBC is obtained as

$$V_o/V_i|_{L_1 < L_2} = (1 + D)\,/\,(1 - D)\,. \tag{37}$$

B. When the Value of L_1 is Smaller Than the Value of L_2

The typical waveforms of the inductor L_1 and L_2 currents are shown in Fig. 8(a). In this case, the converter operates in three modes as discussed in the following sections.

1) Mode I (Time t_0–t_1): In this mode, switches S_1 and S_2 are turned ON, and equivalent circuitry is the same as mode I of CCM. In this mode, inductors L_1 and L_2 are magnetized by input supply v_i, diodes D_2 and D_o are reversed biased, diode D_1 is forward biased, and the capacitor C_o is discharged through the load R_o. The input current i_i is equal to the addition of inductor currents, i.e., $i_i = i_{Li} + i_{L2}$. The slope of the inductor L_1 and L_2 currents can be obtained as follows:

$$\frac{d\,(i_{L1})}{dt} \approx \frac{v_i}{L_1}, \frac{d\,(i_{L2})}{dt} \approx \frac{v_i}{L_2}. \tag{38}$$

In this case, the current through inductor L_1 is larger than the current through inductor L_2 due to $L_1 < L_2$.

2) Mode II (Time t_1–t_2): This mode occurs for short duration [YT_s, as shown in Fig. 8(a)] when switches S_1 and S_2 are just turned OFF. The equivalent circuitry is shown in Fig. 8(b), where diodes D_1 and D_2 are reversed and forward biased, respectively.

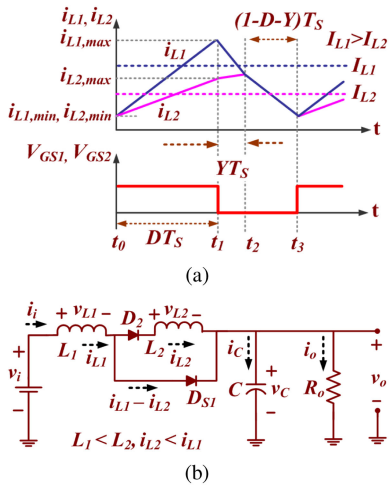

Fig. 8. When $L_1 < L_2$. (a) Inductor currents. (b) Mode II.

During this mode, the currents through inductor L_1 decreases with a large negative slope, and the currents through inductor L_2 increases with small positive slope (approximate zero slope). The value of current through inductor L_1 is larger than the current through inductor L_2. The inductor L_1 is demagnetized and inductor L_2 is magnetized through path $v_i - L_1 - D_{S1} - D_o - (\mathrm{C_o}//R_o)$ and $v_i - L_1 - D_2 - L_2 - D_o - (\mathrm{C_o}//R_o)$, respectively. However, the input current i_i is equal to inductor L_1 currents, i.e., $i_i = i_{L1}$, and the resultant current through diode D_{S1} is the subtraction of inductors L_1 and L_2 currents, i.e., $i_{L1} - i_{L2}$. The slope of the inductor L_1 and L_2 currents is obtained as follows:

$$\frac{d\,(i_{L1})}{dt} \approx \frac{v_i - v_o}{L_1}, \frac{d\,(i_{L2})}{dt} \approx 0. \tag{39}$$

This mode end as soon as the currents through inductors L_1 and L_2 are equal, and circuitry operates in mode III.

3) Mode III (Time t_1–t_2): In this mode, switches S_1 and S_2 are turned OFF, and equivalent circuitry is the same as CCM mode II. During this mode, diodes D_2 and D_o are forward biased, and diode D_1 is reversed biased. Throughout this mode, inductors L_1 and L_2 are discharged in series with input voltage v_i through load R_o. In this case, input current and the current through inductor L_1 and L_2 are equal, i.e., $i_i = i_{L1} = i_{L2}$. The voltage across inductor L_1 and L_2 can be obtained as follows:

$$\frac{d\,(i_{L1})}{dt} = \frac{v_i - v_o}{L_1 + L_2}, \frac{d\,(i_{L2})}{dt} = \frac{v_i - v_o}{L_1 + L_2}. \tag{40}$$

Using small approximation and inductor volt second balance

$$\text{For } L_1 \Rightarrow v_i(D) + (v_i - v_o)Y + \frac{v_i - v_o}{L_1 + L_2} L_1(1 - D - Y) = 0 \tag{41}$$

$$\text{For } L_2 \Rightarrow v_i(D) + \frac{v_i - v_o}{L_1 + L_2} L_2(1 - D - Y) = 0. \tag{42}$$

Solving (41) and (42), the voltage gain of mSIBC is obtained as

$$V_o/V_i|_{L_1 > L_2} = (1 + D)\,/\,(1 - D)\,. \tag{43}$$

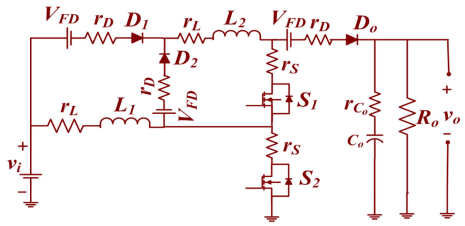

Fig. 9. Equivalent circuit of mSIBC configuration with nonidealities.

Therefore in case of unequal inductances, inductor average current is changed. However, voltage gain is $(1 + D)/(1 - D)$, which remains the same as (13).

IV. Effect of Nonidealities on Voltage Gain

To analyze the effect of the nonidealities of components and devices on the output voltage, the nonidealities are considered in the power circuit, as shown in Fig. 9. The equivalent series resistance (ESR) of inductors L_1 and L_2 is shown by resistances r_L. The ON-state resistance of switches S_1 and S_2 is shown by resistance r_S. The forward resistance and the threshold voltage of diodes D_1, D_2, and D_o are shown by resistances r_D and voltage V_{FD}, respectively. The ESR of capacitor C_o is shown by r_{Co}.

A. Effect of ESR of Inductors L_1 and L_2 on Voltage Gain

In order to analyze the effect of ESR of inductors L_1 and L_2, the anomaly arising due to other parasitic is ignored, i.e., $r_S = 0, r_D = 0, r_{Co} = 0$, and $V_{FD} = 0$. Considering this case, the voltages across inductor L_1 and L_2 are obtained as follows:

$$\text{ONstate} \Rightarrow \mathrm{v_{L1} \approx V_i - i_{L1}r_L, v_{L2} \approx V_i - i_{L2}r_L, V_o \approx v_{Co}} \quad (44)$$

$$\text{OFFstate} \Rightarrow \mathrm{v_{L1} + v_{L2} \approx V_i - i_{L1}r_L - i_{L2}r_L - V_o}. \quad (45)$$

Using (44) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{L1}r_L - i_{L2}r_L. \quad (46)$$

Using small approximation and inductor volt-sec balance principle

$$(2V_i - i_{L1}r_L - i_{L2}r_L)\, D = -(V_i - i_{L1}r_L - i_{L2}r_L - V_o) \times (1 - D). \quad (47)$$

Using (47), the voltage gain of mSIBC is obtained as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_L} = \frac{(1 + D) - \{(i_{L1}r_L + i_{L2}r_L)/V_i\}}{(1 - D)}. \quad (48)$$

If $L_1 = L_2$, the currents flow through both the inductors L_1 and L_2 are equal, i.e., $i_L = i_{L1} = i_{L2}$. Let us assume that the voltage drop due to ESR of the inductor is V_{d-L}, i.e.,$V_{d-L} = i_{L1}r_L = i_{L2}r_L$. Thus, (48) is rewritten as

$$\left.\frac{V_o}{V_i}\right|_{r_L} = \frac{(1 + D) - 2V_{d-L}/V_i}{(1 - D)}. \quad (49)$$

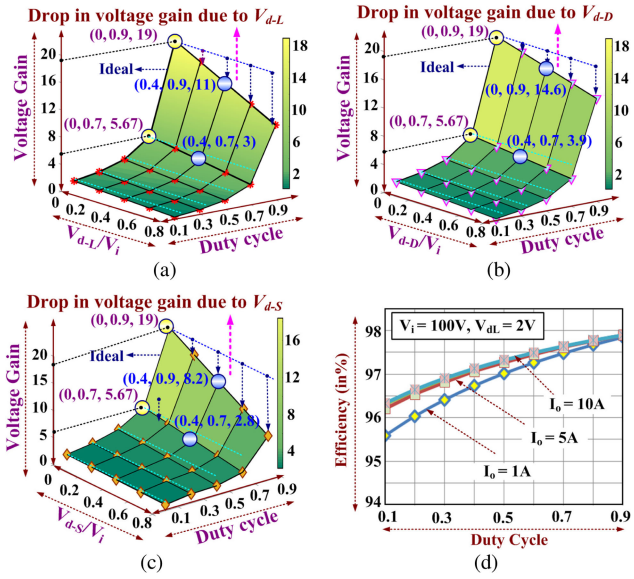

Fig. 10. Effect of nonidealities on voltage gain and duty cycle. (a) Nonidealities of inductors. (b) Nonidealities of diodes. (c) Nonidealities of switches. (d) Efficiency versus duty cycle.

Equation (49) is graphically plotted in Fig. 10(a) by considering the different values for V_{d-L}/V_i and duty cycle D; and the effect of ESRs of inductors on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of V_{d-L} and D. This fact guides that the ESR of inductance (r_L) and duty cycle (D) should not be too large.

B. Effect of Diodes D_1, D_2, and D_o on Voltage Gain

In order to analyze the effect of diodes D_1, D_2, and D_o, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0$, $r_{Co} = 0$, and $r_S = 0$. Considering this case, the voltages across inductors L_1 and L_2 are obtained as follows:

$$\text{ON state} \Rightarrow \mathrm{v_{L1} \approx V_i, \quad v_{L2} \approx V_i - i_{L2}r_D - V_{FD}} \quad (50)$$

$$\text{OFF state} \Rightarrow \mathrm{v_{L1} + v_{L2} \approx V_i - 2i_{L2}r_D - 2V_{FD} - V_o}. \quad (51)$$

Using (50) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{L2}r_D - V_{FD}. \quad (52)$$

Using small approximation and inductor volt-sec balance principle

$$(2V_i - i_{L2}r_D - V_{FD})\, D = -(V_i - 2i_{L2}r_D - 2V_{FD} - V_o) \times (1 - D). \quad (53)$$

Using (53), the voltage gain of mSIBC is obtained as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_D, V_{FD}} = \frac{(1 + D) - \{(i_{L2}r_D + V_{FD})(2 - D)/V_i\}}{(1 - D)}. \quad (54)$$

Let us assume that the voltage drop due to forward resistance and the threshold voltage of the diode is V_{d-D}, i.e.,$V_{d-D} =$

$i_{L2}r_D + V_{FD}$. Thus, (54) is rewritten as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_D,V_{FD}} = \frac{(1+D) - \{V_{d-D}(2-D)/V_i\}}{(1-D)}. \quad (55)$$

Equation (55) is graphically plotted in Fig. 10(b) by considering the different values for V_{d-D}/V_i and D, and the effect of diodes on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of V_{d-D}/V_i and D. This fact guides that the forward resistance and the threshold voltage of diodes should not be too large.

C. Effect of Switches S_1 and S_2 on Voltage Gain

In order to analyze the effect of switches S_1 and S_2, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0, r_{Co} = 0, r_D = 0$, and $V_{FD} = 0$. Considering this case, the voltages across inductor L_1 and L_2 are obtained as follows:

$$\text{ON State} \Rightarrow v_{L1} \approx V_i - i_{S2}r_S,\ v_{L2} \approx V_i - i_{S1}r_S - i_{S2}r_S \quad (56)$$

$$\text{OFF State} \Rightarrow v_{L1} + v_{L2} \approx V_i - V_o. \quad (57)$$

Using (56) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{S1}r_S - 2i_{S2}r_S. \quad (58)$$

Using small approximation and inductor volt-sec balance principle

$$(2V_i - i_{S1}r_S - 2i_{S2}r_S)\,D = -(V_i - V_o)(1-D). \quad (59)$$

Using (59), the voltage gain of mSIBC is obtained as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_S} = \frac{(1+D) - \{D(i_{S1}r_S + 2i_{S2}r_S)/V_i\}}{(1-D)}. \quad (60)$$

Assume that the voltage drops in switches S_1 and S_2 are the same, i.e.,$V_{d-S} = i_{S1}r_S = i_{S2}r_S$. Thus, (60) is rewritten as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_S} = \frac{(1+D) - 3D(V_{d-S})/V_i}{(1-D)}. \quad (61)$$

Equation (60) is graphically plotted in Fig. 10(c) by considering the different values for V_{d-S}/V_i and D; and the effect of ON-state resistance of switches on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of V_{d-S}/V_i and D. This fact guides that the ON-state resistance of switches should not be too large.

D. Effect of Capacitor C_o and Its ESR on Voltage Gain

In order to analyze the effect of ESR of capacitor C_o, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0$, $r_D = 0$, $V_{FD} = 0$, and $r_S = 0$. Let us assume that the voltage drop across resistance r_{Co} is V_{d-Co}. When switches are turned ON, the capacitor C_o is discharged through load R_o. The output voltage that is the voltage across capacitor C_o is dropped down, and instantaneous output voltage can be calculated as

$$v_o = V_o - V_{d-C_o} - \frac{I_o}{C_o}t = V_o\left(1 - \frac{1}{R_oC_o}t\right). \quad (62)$$

At the end of ON-state, change in output voltage (ΔV_o) is

$$\Delta V_o|_C = \frac{V_o}{R_oC_of} \times D. \quad (63)$$

This fact provides the guidance that the load resistance R_o, switching frequency f, and capacitance C_o should not be too small, and ESR and duty ratio should not be too large.

E. Combined Effect of Nonidealities on Voltage Gain

By considering the nonidealities of inductors L_1 and L_2, diodes D_1, D_2, and D_o, switches S_1 and S_2, and effect of ESR of capacitor C_o, the voltage gain can be obtained as follows:

$$\frac{V_o}{V_i} \approx \frac{1 + D - \frac{2V_{d-L}}{V_i} - (2-D)\frac{V_{d-D}}{V_i} - 3D\frac{V_{d-S}}{V_i} - \frac{V_{d-C_o}}{V_i}}{1-D}. \quad (64)$$

F. Efficiency Analysis

The currents through capacitor C_o in ON-state and OFF-state are obtained as follows:

$$i_{Co} = -v_o{R_o}^{-1} \text{ in ON} - \text{state},\quad i_i - v_o{R_o}^{-1} \text{ in OFF} - \text{state}. \quad (65)$$

In OFF state, the currents through inductors L_1 and L_2 are the same, i.e., $i_L = i_{L1} = i_{L2}$. Using (65), small approximation, and capacitor charge balanced principle

$$\int_0^{DT_S}\left(\frac{V_o}{R_o}\right)dt = \int_{DT_S}^{T_S}\left(I_L - \frac{V_o}{R_o}\right)dt \Rightarrow \frac{V_o}{R_o}D = \left(I_L - \frac{V_o}{R_o}\right)(1-D). \quad (66)$$

Using (66), the inductor currents are obtained as

$$I_L = I_{L1} = I_{L2} = \frac{V_o{R_o}^{-1}}{1-D}. \quad (67)$$

It is considered that $P_{\text{SW}-S1}$ and $P_{\text{SW}-S2}$ are the switching power losses due to switching of switches S_1 and S_2, respectively. The total loss during switching $P_{\text{SW}-T}$ is obtained as follows:

$$P_{\text{SW}-T} = \sum_{i=1,2} P_{\text{SW}-Si} = \frac{1}{T_S}\left\{\begin{matrix}(I_{S1}\times V_{S1})(t_{r-S1} + t_{f-S1}) \\ +(I_{S2}\times V_{S2})(t_{r-S2} + t_{f-S2})\end{matrix}\right\} \quad (68)$$

where rising and falling times of switches S_1 and S_2 are t_{r-S1}, t_{f-S1} and t_{r-S2}, t_{f-S2}, respectively; I_{S1}, V_{S1} and I_{S2}, V_{S2} are the average current and voltage through/across switches S_1 and S_2, respectively. The total power at the input and output ports is obtained as follows:

$$P_i\begin{cases} = V_i\{2I_LD + I_{L1}(1-D)\} + P_{\text{SW}-T} \\ = \dfrac{V_iV_o{R_o}^{-1}}{1-D}(1+D) + P_{\text{SW}-T}\end{cases}, P_o = \frac{{V_o}^2}{R_o}. \quad (69)$$

TABLE I
COMPARISON OF CONVERTERS

Converter		SIBC [17]	Converter in [21]	Converter in [23]	Proposed Converter (D)
C/I/D/S/T		1/2/4/1/8	1/2/1/2/6	1/2/2/3/8	1/2/3/2/8
Load Type		Grounded	Floating	Floating	Grounded
Voltage gain (M)		$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+D_1}{1-D_1-D_2}$	$\frac{1+D}{1-D}$
Switch Voltage	RMS	$V_o\sqrt{\frac{2}{b}}$	$V_{S1,2}=\frac{V_o\sqrt{2b}}{2(b-1)}$	$V_{S1,2}=\frac{V_o\left(\sqrt{D_2}-b\sqrt{1-D_1-D_2}\right)}{2(b-1)}$ $V_{S3}=\frac{V_o\left(\sqrt{D_1}-M\sqrt{1-D_1-D_2}\right)}{2M}$	$V_{S1}=V_o\frac{a}{2M}\sqrt{2/b}$ $V_{S2}=\frac{V_o}{2M}\sqrt{2b}$
	Peak	V_o	$V_{S1,2}=\frac{b}{2M}V_o$	$V_{S1,2}=\frac{V_o b}{2M}, V_{S3}=V_o$	$V_{S1}=\frac{V_o a}{2M}, V_{S2}=\frac{V_o b}{2M}$
	Avg.	$\frac{2V_o}{M+1}$	$V_{S1,2}=\frac{V_o}{M}$	$V_{S1,2}=\frac{V_o\left(b(1-D_1)-MD_2\right)}{2M}$ $V_{S3}=\frac{V_o(1-bD_1-MD_2)}{2M}$	$V_{S1}=\frac{V_o a}{Mb}, S_2=\frac{V_o}{M}$
Diode Voltage	RMS	$V_{D1,3}=\frac{aV_o}{2M}\sqrt{2/b}, V_{D2}=\frac{V_o}{M}\sqrt{2/a}, V_{Do}=V_o\sqrt{a/b}$	$V_o\frac{\sqrt{aM+1}}{M}$	$V_o\left(\frac{\left(b\sqrt{D_2}\right)}{M}+\sqrt{1-D_1-D_2}\right)$	$V_{D1,2}=\frac{a}{2M}\sqrt{\frac{2}{b}}V_o, V_{Do}=\sqrt{\frac{a}{b}}V_o$
	Peak	$V_{D1,3}=\frac{aV_o}{2M}, V_{D2}=\frac{V_o}{M}, V_{Do}=V_o$	$V_o b/M$	V_o	$V_{D1,2}=aV_o/2M, V_{Do}=V_o$
	Avg.	$V_{D1-3}=aV_o/Mb, V_{Do}=aV_o/b$	$V_o a/M$	$V_o(M-MD_1+D_2)/M$	$V_{D1,2}=aV_o/2M, V_{Do}=aV_o/b$
Inductor Current	RMS	$\sqrt{\frac{b^2}{4M^2}I_i^2+\frac{1}{12}\left(\frac{V_iD}{Lf}\right)^2}$	$\sqrt{\frac{b^2}{4M^2}I_i^2+\frac{1}{12}\left(\frac{V_iD}{Lf}\right)^2}$	$\sqrt{\frac{b^2}{4M^2}I_i^2+\frac{1}{48}\left(\frac{V_i(2D_1+D_2)}{Lf}\right)^2}$	$\sqrt{\frac{b^2}{4M^2}I_i^2+\frac{1}{12}\left(\frac{V_iD}{Lf}\right)^2}$
	Peak	$\frac{bI_i}{2M}+\frac{aV_i}{2Lfb}$	$\frac{bI_i}{2M}+\frac{aV_i}{2Lfb}$	$\frac{aI_i}{2M}+\frac{V_i(2D_1+D_2)}{4Lf}$	$\frac{bI_i}{2M}+\frac{aV_i}{2Lfb}$
	Avg.	$I_i b/2M$	$I_i b/2M$	$I_i b/2M$	$I_i b/2M$
Switch Current	RMS	$\sqrt{\left(\frac{a}{b}\right)^3 I_i^2+\frac{1}{12}\left(\frac{a}{b}\right)^3\left(\frac{V_i}{Lf}\right)^2}$	$I_{S1,2}=\sqrt{\left(\frac{a}{b}\right)^3\frac{I_i^2}{4}+\sqrt{\left(\frac{a}{b}\right)^3\left(\frac{V_i}{2\sqrt{3}Lf}\right)^2}}$	$I_{S1,2}=\sqrt{\left(\frac{a}{b}\right)^3\left[\frac{I_i^2}{4}+\frac{1}{12}\left(\frac{V_i}{Lf}\right)^2\right]}$ $I_{S3}=\sqrt{D_2^3\left(I_i^2+\frac{1}{48}\left(\frac{V_i}{4Lf}\right)^2\right)}$	$I_{S1}=\sqrt{\left(\frac{a}{b}\right)^3\left(\frac{I_i^2}{4}+\frac{1}{12}\left(\frac{V_i}{Lf}\right)^2\right)}$ $I_{S2}=\sqrt{\left(\frac{a}{b}\right)^3\left(I_i^2+\frac{1}{12}\left(\frac{V_i}{Lf}\right)^2\right)}$
	Peak	$\frac{a}{b}\left(I_i+\frac{V_i}{2Lf}\right)$	$I_{S1,2}=\frac{a}{b}\left(\frac{I_i}{2}+\frac{V_i}{2Lf}\right)$	$I_{S1,2}=\frac{I_iD_1}{2}+\frac{V_iD_1}{2Lf}, I_{S3}=I_iD_2+\frac{V_iD_2}{4Lf}$	$I_{S1}=\frac{I_iD}{2}+\frac{V_iD}{2Lf}, I_{S2}=I_iD+\frac{V_iD}{2Lf}$
	Avg.	$I_i a/b$	$I_{S1,2}=I_i a/2b$	$I_{S1,2}=I_iD_1/2, I_{S3}=I_iD_2$	$I_{S2}=I_i a/b, I_{S1}=I_i a/2b$
Diodes Current	RMS	$I_{D1,3}=\frac{a}{b}\sqrt{\frac{a}{b}\left(\frac{I_i^2}{4}+\left(\frac{V_i}{2\sqrt{3}Lf}\right)^2\right)}$ $I_{D2,o}=\frac{1}{b}\sqrt{\frac{8}{b}I_i^2+\frac{1}{24M}\left(\frac{V_o a}{Lf}\right)^2}$	$\sqrt{\frac{b}{2M}I_i+\frac{1}{12}\left(\frac{V_iD}{Lf}\right)^2}$	$\sqrt{I_i^2(p)^3+\left(\frac{(V_i-V_o)p}{4\sqrt{3}Lf}\right)^2}$	$I_{D1}=\frac{a}{b}\sqrt{\frac{a}{b}\left(\frac{I_i^2}{4}+\left(\frac{V_i}{2\sqrt{3}Lf}\right)^2\right)}$ $I_{D2,o}=\frac{1}{b}\sqrt{\frac{8}{b}I_i^2+\frac{1}{24M}\left(\frac{V_o a}{Lf}\right)^2}$
	Peak	$I_{D1,3}=\frac{aI_i}{2b}+\frac{V_i a}{2bLf}, I_{D2,o}=\frac{2I_i}{b}+\frac{(V_i-V_o)a}{4Lfb}$	$\frac{bI_i}{2M}+\frac{aV_i}{2Lfb}$	$I_ip+\frac{(V_i-V_o)p}{4Lf}$	$I_{D1}=\frac{I_i a}{2b}+\frac{V_i a}{2Lbf}, I_{D2,o}=\frac{2I_i}{b}+\frac{(V_i-V_o)a}{4Lfb}$
	Avg.	$I_{D1,3}=I_i a/2b, I_{D2,o}=I_i/2b$	$2I_i/b$	I_iP	$I_{D1}=I_i a/2b, I_{D2,o}=I_i/2b$
Efficiency		95.2%	92.7%	93.1%	97.17%

Using (64)–(69), the efficiency is obtained as follows:

$$\eta_{\text{mSIBC}}=\frac{1+D-\frac{2V_{d-L}}{V_i}-\frac{(2-D)V_{d-D}}{V_i}-\frac{3DV_{d-S}}{V_i}-\frac{V_{d-C_o}}{V_i}}{(1+D)+P_{\text{SW}-T}\frac{R_o(1-D)}{V_oV_i}}. \tag{70}$$

In order to analyze the effect of load and inductors on the efficiency of the converter, the anomaly arising due to other parasitic effects is ignored. Therefore

$$\eta_{\text{mSIBC}}=\frac{1+D-2V_{d-L}}{(1+D)+\frac{R_o(1-D)}{V_oV_i}}. \tag{71}$$

Fig. 10(d) shows the efficiency plot versus the duty cycle for different values of load cases.

V. COMPARISON OF CONVERTERS

Recently numerous converters are proposed to achieve high output voltage with additional boosting techniques. In this section, the proposed converter is compared with recently suggested converters whose voltage gain is equal to the proposed converter. The detailed comparison in terms of number of components, voltage and current stresses, efficiency, etc., is shown in Table I.

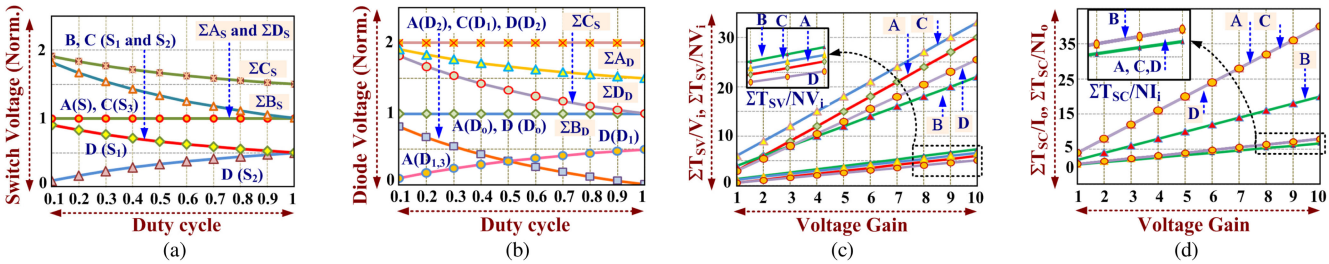

Fig. 11. Comparison. (a) Switch voltages versus duty cycle. (b) Diode voltages versus duty cycle. (c) $\sum \mathrm{T_{SV}/V_i}, \sum \mathrm{T_{SV}/NV_i}$ versus voltage gain. (d) $\sum \mathrm{T_{SC}/I_o}, \sum \mathrm{T_{SC}/NI_o}$ versus voltage gain. *Note:* A represents SIBC [17], B represents converter [21], C represents converter [23], D represents the proposed converter. [In general, *X*(*Z*) mean voltage stress across *Z* of converter X, and $\sum X_{\mathrm{S}}, \sum X_{\mathrm{D}}$ are total voltage stress across switches and diodes for converter X].

The total number of components required for the classical SIBC [see Fig. 1(a)] [17] and suggested converters in [21] and [23] are 8, 6, and 8, respectively. It is observed that the total requirement of components for the proposed mSIBC is the same as SIBC and suggested converter in [23]. In converters presented in [21] and [23], input and outputs are not at common ground, thus these converters are suitable only for floating loads. The efficiency of the converters is dependent on several factors, e.g., total number components, voltage and current ratings, and their types. The plot of normalized voltage stress across switches and diodes is shown in Fig. 11(a) and (b), respectively. In Fig. 11(a) and (b), converters are also compared in terms of total voltage stress across switches and diodes, respectively.

The total voltage stress across semiconductor devices ($\sum T_{SV}$) is the sum of total voltage stresses across diode and switches, the total current stress for semiconductor devices ($\sum T_{SC}$) is the sum of total current stresses of diode and switches. The comparison plot of total voltage and current stress for converters is shown in Fig. 11(c) and (d), respectively. The relation between total voltage and current stress for converters is as follows:

$$\underbrace{V_i\,(3M+3)}_{\text{Con.[23]}} > \underbrace{3V_iM}_{\text{SI}} > \underbrace{\frac{V_i}{2}\,(5M+1)}_{\text{Proposed}} > \underbrace{2V_i\,(M+1)}_{\text{Con.[21]}} \quad (72)$$

$$\underbrace{4I_oM}_{\text{SI}} = \underbrace{4I_oM}_{\text{Con.[23]}} = \underbrace{4I_oM}_{\text{Proposed}} > \underbrace{2I_oM}_{\text{Con.[21]}}. \quad (73)$$

Notably, the cost of the components is increasing in a parabolic way with components ratings, i.e., high rating, higher cost, and high ON-state resistance The total voltage and current stress per components is calculated as follows:

$$\underbrace{\frac{2V_i}{3}\,(M+1)}_{\text{Con.[21]}} > \underbrace{\frac{3V_i}{5}\,(M+1)}_{\text{Con.[23]}} > \underbrace{\frac{3V_i}{5}M}_{\text{SI}} > \underbrace{\frac{V_i}{2}\left(M+\frac{1}{5}\right)}_{\text{Proposed}} \quad (74)$$

$$\underbrace{2I_oM/3}_{\text{Con.[21]}} > \underbrace{4I_oM/5}_{\text{SI}} = \underbrace{4I_oM/5}_{\text{Con.[23]}} = \underbrace{4I_oM/5}_{\text{Proposed}}. \quad (75)$$

The comparison plots of total voltage and current stress per semiconductor devices of converters are shown in Fig. 11(c) and (d), respectively. Based on the relations (74) and (75), on an average, the proposed converter required lower rating components, and hence, the total cost of the converter is less than classical SIBC and converters presented in [21] and [23]. The proposed mSIBC configuration is transformerless and simply derived by replacing one diode of the SI network of classical SIBC with an active switch. As a result, the total output voltage is distributed among the two active switches. Therefore, low-voltage rating switches can be employed to design the power circuit of the proposed mSIBC configuration. In general, the ON-state resistance of any devices increases with their ratings. It is analyzed that the proposed converter required lower rating components. The efficiencies of the classical SIBC and suggested converter in [21], and [23] are 95.2%, 92.7%, and 93.1%, respectively, and the proposed converter efficiency is 97.17%. Therefore, the proposed converter provides higher efficiency compared with SI converter and converters presented in [21]–[23]. The total switching losses of classical SIBC [see Fig. 1(a)] and proposed mSIBC [see Fig. 1(b)] are obtained as follows:

$$P_{\mathrm{Sw}}{}^{\mathrm{SIBC}} = (E_S + E_{D1} + E_{D2} + E_{D3} + E_{Do})\, f_s \quad (76)$$

$$P_{\mathrm{Sw}}{}^{\mathrm{mSIBC}} = (E_{S1} + E_{S2} + E_{D1} + E_{D2} + E_{Do})\, f_s \quad (77)$$

where E is energy loss during switching, and its subscript defines the components. The difference between switching losses of the proposed mSIBC and classical SIBC is obtained as follows:

$$P_{\mathrm{Sw}}{}^{\mathrm{mSIBC}} - P_{\mathrm{Sw}}{}^{\mathrm{SIBC}} = \begin{pmatrix} E_{\mathrm{on},S1} + E_{\mathrm{off},S1} \\ +E_{\mathrm{on},S2} + E_{\mathrm{off},S2} \end{pmatrix} f_s - \begin{pmatrix} E_{\mathrm{on},S} + E_{\mathrm{off},S} \\ +E_{\mathrm{on},D3} + E_{\mathrm{off},D3} \end{pmatrix} f_s \quad (78)$$

where E_{on} and E_{off} define the turn ON and OFF energy losses, respectively. By solving (78)

$$P_{\mathrm{Sw}}{}^{\mathrm{mSIBC}} - P_{\mathrm{Sw}}{}^{\mathrm{SIBC}} = \begin{pmatrix} V_{S1}I_{S1} + V_{S2}I_{S2} \\ -V_SI_S \end{pmatrix} (t_r + t_f)\, f_S - E_{D3} f_S \quad (79)$$

where t_r and t_f are rise time and fall time, respectively. Using (79), the final difference in the switching losses is obtained as

$$P_{\mathrm{Sw}}{}^{\mathrm{mSIBC}} - P_{\mathrm{Sw}}{}^{\mathrm{SIBC}} = -\frac{M+1}{4M} V_o I_i D\left(t_r + t_f\right) f_S - E_{D3} f_s < 0. \quad (80)$$

The solution of (80) is always negative. Therefore, it can be concluded that the switching losses in mSIBC are less than classical SIBC. It is also notable that the proposed converter switches are simultaneously turned ON and OFF and arranged in half-bridge structure, as a result, a single half-bride driver module is suitable to drive switches. Hence, no additional driver is required to control switches of the proposed converter. It is observed that the mSIBC provides a viable solution to achieve given voltage gain with reduced voltage stress, low cost, and higher efficiency.

VI. Design and Results

The mSIBC converter is designed by considering the typical input voltage of 100 V, output power of 500 W, output voltage of 400 V, and switching frequency of 100 kHz to validate functionality and performance.

A. Design and Selection of Reactive Components

In order to have good performance, the reactive components are designed by considering the worst efficiency (η_w). Thus, by considering the worst efficiency 90%, the required duty cycle is calculated as

$$D|_{\eta_w=90\%} = \frac{M-1}{(M+1)\,\eta_w} = \frac{4-1}{(4+1)\,0.90} \approx 66.67\%. \quad (81)$$

The critical values of inductors L_1 and L_2 are obtained as

$$L_1|_{\mathrm{critical}} = L_2|_{\mathrm{critical}} = \frac{V_i}{\Delta I_L} DT_S = \frac{V_i}{40\%\text{ of }I_L} DT_S. \quad (82)$$

Using (77), the critical values of inductor L_1 and L_2 are calculated by considering the peak to peak ripple of inductor currents is 2.5A as follows:

$$L_1|_{\mathrm{critical}} = L_2|_{\mathrm{critical}} = \frac{100\text{ V} \times 0.67}{2.5\text{A} \times 100\text{ kHz}} \approx 268\mu\text{H}. \quad (83)$$

The inductance and current rating of the inductors L_1 and L_2 must be higher than critical inductance and input current, respectively. Thus, ferrite E type core inductors with rating 700 μH/10 A, $r_L = 75$ mΩ are selected to design the prototype. The critical capacitance of output-side capacitor C_o is obtained as

$$C_o|_{\mathrm{critical}} = \frac{P_o}{V_o \Delta V_{C_o}} DT_S. \quad (84)$$

The critical capacitance value of capacitor C_o by considering the peak to peak voltage ripple of the capacitor, i.e., 4 V is calculated as follows:

$$C_o|_{\mathrm{critical}} = \frac{500\text{ W} \times 0.67}{400\text{ V} \times 4\text{ V} \times 100\text{ kHz}} \approx 2.1\mu\text{F}. \quad (85)$$

The voltage rating of the capacitor C_o must be greater than output voltage i.e., 400 V. Therefore, a film-type capacitor with rating 2.2 μF/450 V ($r_{Co} = 4$ mΩ) is selected to design the prototype.

B. Design and Selection of Semiconductor Devices

The voltage stresses across switches S_1 and S_2 are obtained as

$$V_{S1}|_{\mathrm{stress}} = \frac{V_o - V_i}{2}, \quad V_{S2}|_{\mathrm{stress}} = \frac{V_o + V_i}{2}. \quad (86)$$

The minimum voltage ratings of the switches S_1 and S_2 are calculated as follows:

$$V_{S1} = \frac{400\text{ V} - 100\text{ V}}{2} = 150\text{ V}, \; V_{S2} = \frac{400\text{ V} + 100\text{ V}}{2} = 250\text{ V}. \quad (87)$$

The current rating of selected switches S_1 and S_2 must be greater than the input current. Therefore, FDP19N40-ND MOSFET ($r_s = 200$m Ω) and FDP18N20-ND MOSFET ($r_s = 140$ mΩ) are selected.

The peak inverse voltage (PIV) ratings of diodes D_1, D_2, and D_o are calculated as follows:

$$V_{D1}|_{\mathrm{PIV}} = \frac{V_i - V_o}{2}, \quad V_{D2}|_{\mathrm{PIV}} = -V_i, \quad V_{Do}|_{\mathrm{PIV}} = -V_o. \quad (88)$$

For the given parameters, the minimum PIV ratings of diodes D_1, D_2, and D_o are calculated as follows:

$$\begin{cases} V_{D1}|_{\mathrm{PIV}} = \frac{-(100-400)}{2} = -250\text{ V}, \; V_{D2}|_{\mathrm{PIV}} = -100\text{ V} \\ V_{Do}|_{\mathrm{PIV}} = -400\text{ V}. \end{cases} \quad (89)$$

The current rating of selected diodes D_1, D_2, and D_o must be greater than the input current. Therefore, diodes DPG10I400PM (400 V/10 A, $r_D = 19.8$ mΩ, $V_{FD} = 0.77$ V) and C3D10060A-ND (600 V/14 A, $r_D = 55.2$ mΩ, $V_{FD} = 0.91$ V) are selected.

C. Controller Design

The transfer function between the output voltage and duty cycle for the designed values is obtained as

$$\frac{\hat{v}_o(S)}{\hat{d}(S)} = \frac{-0.02734S + 1250}{1 + 2.73 \times 10^{-5} S + 1.92 \times 10^{-8} S^2}. \quad (90)$$

The Bode plot for the open-loop transfer function is shown in Fig. 12(a). It is observed that the converter is inherently unstable. In order to operate the converter in closed loop, the open-loop transfer function is given with the proportional–integral controller, and the stability is analyzed using the Bode plot. The tuning of the controller is done with the help of the SISO toolbox. The controller is realized using the following controller transfer function:

$$\frac{C(S)}{E(S)} = \frac{(1+4S)(1+3.3 \times 10^{-6} S)}{(1+0.0012S)\,(-0.02734S + 1250)}. \quad (91)$$

The stability of the system increases due to the placement of zero and poles at the left side of the S plane. The closed-loop transfer function Bode plot is shown in Fig. 12(b), and it can be concluded that the system is stable at 100 kHz with phase margin 64° and infinite gain margin. The tuned system with controller

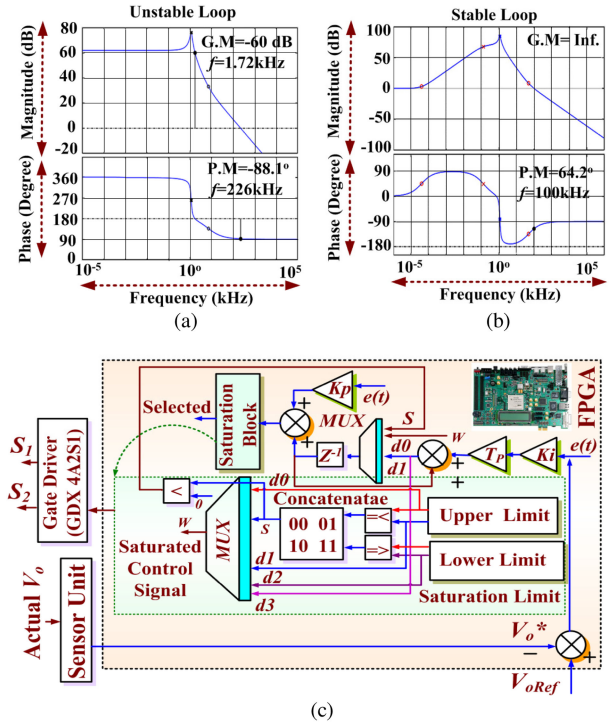

Fig. 12. Control Scheme. (a) Bode plot in open loop. (b) Bode plot in closed loop. (c) Controller blocks.

operates at the desired point with enough phase margin (PM) and infinite gain margin (GM) at the desired frequency (100 kHz) of operation. The control scheme is designed with the help of FPGA, as shown in Fig. 12(c). The lower and upper saturation limits (0.2–0.9 duty cycle) are set to incorporate the physical restriction of the converter. PMODAD1 (12 Bit, 2 channel) analog-to-digital converter is used for the sensing load voltage signal. Sensing capability of 1 Mega samples for the 12-bit converter and Sallen Key filter with poles set to 500 kHz avoid any aliasing effect. The step size of 100 ns is selected for FPGA to achieve at least 100 steps in each switching period of 10 μs. The control gate pulses of switching frequency 100 kHz are generated and fed via driver GDX 4A2S1 to control switches S_1 and S_2.

D. Experimental Results

The performance and functionality of the proposed converter are tested experimentally. The obtained waveforms of output and input voltages and output and input currents are shown in Fig. 13(a). The observed average values of output voltage, input voltage, output current, and input current are 401.9 V, 100.1 V, 1.24 A, and 5.13 A, respectively. It is observed that input current is continuous, and the slope of the input current in ON-state and OFF-state is increasing and decreasing due to magnetizing and demagnetizing of both inductors L_1 and L_2, respectively. The obtained waveforms of voltage and current across/through inductors L_1 and L_2 are shown in Fig. 13(b). It is observed that both the inductors are magnetizing in ON-state with an input voltage of 99.8 V (approx.), and both the inductors L_1 and L_2 are demagnetizing in OFF-state with a voltage -151.3 V approximately. The observed average value of current through inductors L_1 and L_2 are 3.17 A and 3.19 A, respectively. In practice, the average value of voltage across inductors L_1 and L_2 is 0.57 V and 0.43 V, respectively. The obtained waveforms of voltage across switches S_1 and S_2 and diode D_o are shown in Fig. 13(c), and inductor L_2 current waveform is also shown for reference and validation purpose. It is observed that both switches are turned-ON and -OFF simultaneously. The average and peak values of voltage across switches S_1 and S_2 are 56.9 V and 94.46 V, 151.3 V and 251.2V, respectively. Therefore, it is notable that the voltage stress for both switches S_1 and S_2 is lower than the output voltage. It is observed that the diode D_o is forward biased when switches conducted. The average value of voltage across diodes D_o is -249.1 V and PIV is -402.1 V. The waveform of current through switches S_1 and S_2 is observed and shown in Fig. 13(d); where the voltage across switch S_1, current through inductor L_2, and input current are also shown for reference and validation purposes. The average currents through switches S_1 and S_2 are 1.62 A and 3.10 A, respectively. In ON-state, it is observed that the slope of current through switch S_1 is equal to the slope of inductor L_2 current; and the slope of current through switch S_2 is equal to the slope of input current. The obtained waveform of voltage and current across/through diodes D_1 and D_2 is shown in Fig. 13(e), and inductor L_2 and input currents waveforms are also shown for reference and validation purposes. It is observed that diodes D_1 and D_2 are forward and reversed biased in ON and OFF states, respectively. The average value of voltage across diodes D_1 is -57.91 V and PIV is -150.3 V. The average value of voltage across diodes D_2 is -61.03 V and PIV is -99.8 V. The average value of currents through diodes D_1 and D_2 are 1.62 A and 2.57 A, respectively. In ON-state, it is observed that the slope of current through diode D_1 is equal to the slope of inductor L_2 current, and in OFF state, the slope of current through diode D_2 is equal to the slope of inductor L_2 current, which are expected. In order to test the performance of the designed converter in the DCM mode, the converter operates in low power (40 W) by connecting to 1-kΩ resistive load and output voltage reference is set to 200 V. The obtained input voltage and current and output voltage and current are shown in Fig. 13(f). In the presented waveforms, the OFF mode is split into two parts mode II and mode III, i.e., DCM. It is observed that the input current is nonzero in mode II and zero in mode III, which confirms that the converter operates in DCM mode. It is observed that 200.7 V output voltage is achieved, and the input current is zero in mode III. The performance of the converter is also tested with an unequal inductance ($L_1 = 700$ μH, $L_2 = 450$ μH), and output voltage reference is set at 400 V. The obtained waveform of current through inductor L_1 and L_2 currents and voltage across diodes D_1 and D_2 are shown in Fig. 13(g). The one switching period is split into three modes. It is observed that in mode I, the current through inductor L_2 is higher than the current through L_1. In mode II, the current through inductor L_2 is decreased with a higher rate than the current through inductor L_1. In mode III, the currents through inductors L_1 and L_2 are equal. It is investigated that the average current through inductor L_2 is a little higher (0.6 A) than L_1, which is expected since $L_1 > L_2$.

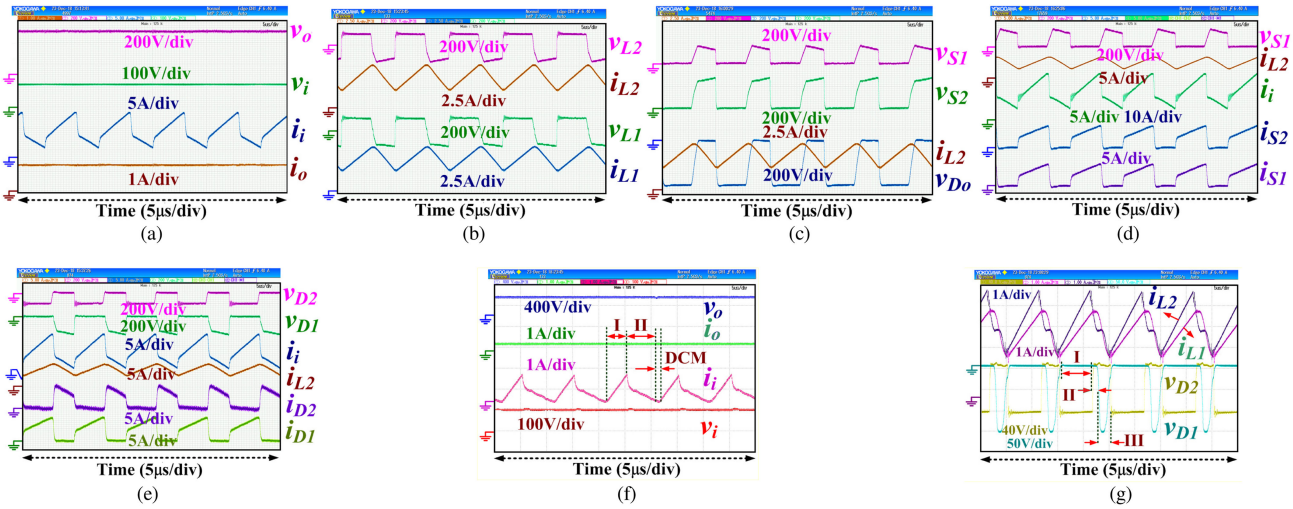

Fig. 13. Experimental results. (a) Bottom to top: output current, input current, input voltage, and output voltage. (b) Bottom to top: inductor L_1 current and voltage, inductor L_2 current and voltage. (c) Bottom to top: diode D_o voltage, inductor L_2 current, and switches S_2 and S_1 voltage. (d) Bottom to Top: switches S_1 and S_2 currents, input current, inductor L_2 current, and switches S_1 voltage. (e) Bottom to Top: diode D_1 and D_2 currents and inductor L_2 current, input current, diodes D_1 and D_2 voltage.(f) Bottom to Top: input voltage, input current, output current, output voltage in DCM. (g) Bottom to top: diode D_1 and D_2 voltage and inductor L_1 and L_2 currents when $L_1 > L_2$.

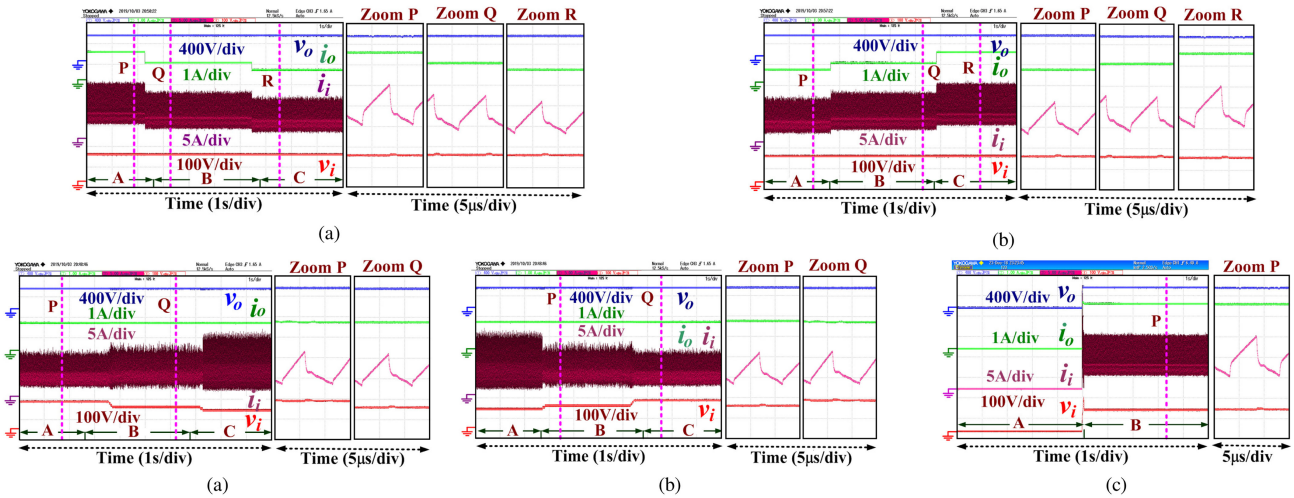

Fig. 14. Experimental results (input and output voltages, input and output currents) of the proposed converter with perturbation. (a) When load power decreased. (b) When load power increased. (c) When input voltage decreased. (d) When input voltage increased. (e) Initial starting condition.

It is also investigated that the diodes D_1 and D_2 are forward biased in Mode II.

In order to test the performance of the converter under a perturbed condition, the perturbation is introduced from load and source sides. Fig. 14(a) shows that constant 401.1 V is achieved at the load when the input voltage is constant i.e., 100 V, and load power decreased from 500 to 400 W and 400 to 320 W [i.e., A to B and B to C in Fig. 14(a)]. Fig. 14(b) shows that constant 401.2 V is achieved at the load when the input voltage is constant, i.e., 100 V and even when load power increased from 320 to 400 W and 400 to 500 W [i.e., A to B and B to C in Fig. 14(b)]. The zoomed waveform at P, Q, and R is shown in Fig. 14(a) and (b), and it is observed that duty cycles in A, B, and C are the same; however, the magnitude of input and output current is changed accordingly to maintain power balance at the input and output side. Fig. 14(c) shows that constant 400.9 V is achieved at the load when load power is constant, i.e., 500 W and input voltage decreased from 105 to 90 V and 90 to 85 V [i.e., A to B and B to C in Fig. 14(c)]. Fig. 14(d) shows that constant 400.7 V is achieved at the load when load power is constant, i.e., 500 W and input voltage increased from 85 to 9 0V and 90 to 105 V [i.e., A to B and B to C in Fig. 14(d)]. The zoomed waveforms at P and Q are shown in Fig. 14(c) and (d), and it is observed that the duty cycle is adjusted according to the input voltage to maintain the constant output voltage. Moreover, it is also observed that there is no change in output current even input current changed according to the input voltage.

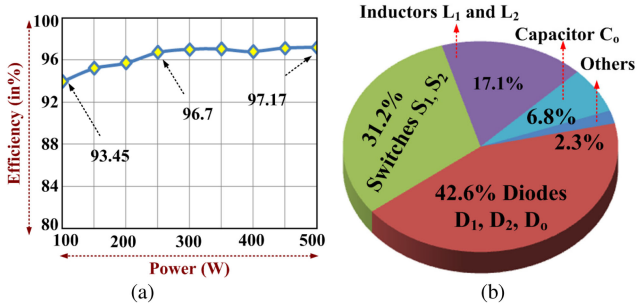

Fig. 15. Experimental test plots. (a) Efficiency versus power. (b) Loss distribution at 500 W.

In order to investigate the dynamics of the converter in the initial starting condition, the load power and input voltage is set at 500 W and 100 V, respectively, and the converter is suddenly turned ON from OFF (rest) mode [A to B in Fig. 14(e)]. The observed waveforms are shown in Fig. 14(e). It is investigated that the steady state 401.7 V is achieved at the output and the settling time of the converter is approx. 0.12 s. The performance of the converter is investigated at various power levels to investigate the efficiency of the designed prototype. The plot of efficiency versus power and loss distribution at 500 W is shown in Fig. 15. It is found that most of the power loss takes place in the diodes. At power 500 W, the efficiency of the designed prototype is 97.17%.

VII. Conclusion

In this article, the mSIBC was proposed with reduced voltage stress across switches. The voltage gain of the mSIBC was higher than the classical boost converter and equal to the classical SI boost converter. Compared with the classical SIBC, the proposed converter required less number of diodes and voltage stress across switches was low compared with the output voltage. Therefore, the requirement of high-voltage rating active switches was eliminated. Furthermore, the cost of the converter can be reduced due to the utilization of lower rating active switches and the elimination of one diode. The detail CCM and DCM operating principle, voltage gain, boundary conditions, and effect of nonidealities were discussed. The proposed converter was compared with a similar converter and found that the proposed converter provides a viable solution to achieve higher voltage with low-voltage rating switches. The experimental results were presented, which validated the theoretical analysis and functionality, and the efficiency of the designed converter was 97.17%.

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