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Non-Isolated DC–DC Power Converter With High Gain and Inverting Capability

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ABSTRACT As the voltage gain of converter increases with the same ratio, the current gain also increases, this increase in current gains will affect the size of the input and the output capacitor. To reduce the ripple in the input current with simultaneous decreasing the input current ripple, a novel current fed interleaved high gain converter is proposed by utilizing the interleaved front-end structure and Cockcroft Walton (CW)-Voltage Multiplier (VM). The ''current fed'' term is used because, in proposed circuitry, all the capacitors of CW-VM are energized by a current path via inductors of the interleaved structure. The proposed converter can be applied as an input boost up the stage for low voltage battery energy storage systems, photovoltaic (PV) and fuel cell (FC) based DC-AC applications. The anticipated topology consists of the two low voltage rating switches. The main benefits of the anticipated converter configuration are the continuous (ripple free) input current, high voltage gain, reduced switch rating, high reliability, easy control structure and a high percentage of efficiency. The proposed converter's working principle, mathematical based steady-state analysis, and detailed component design are discussed. The parasitic of the components has been considered in the analysis to show the deviation from the ideal cases. A detailed comparison with the other available converters is presented. The experimental results of the 300W prototype are developed to confirm the performance and functionality of the anticipated DC-DC converter.

INDEX TERMS Non-isolated, inverting, interleaved, high gain, renewables, current fed, voltage multiplier.

I. INTRODUCTION

Nowadays, switching power converters gaining popularity with the development of high-frequency components. High frequency allows the reduction in converter size and weight. Furthermore, based on the selection of the DC-DC converters it can be possible to achieve the inverting and the non-inverting outputs. Based on the choice of DC-DC converters one can generate both inverting and non-inverting voltage at the output. There are several applications where the inverting DC-DC converters are employed, such as telecommunications modules, Data acquisition systems (DAS), OLED microdisplay boards, random Access memory (RAM), and also solar PV systems [1]–[4]. Furthermore, high gain DC-DC converters are required for the utility grid-DC bus application and standalone inverter–load applications. To achieve the required high gain, conventional negative output converters are not suitable because they have to operate at higher duty ratios, which increases the high losses in the semiconductors. To address this several high step-up converters such as Z or qZ source converters, inductor coupled, and transformer isolated converters, switch inductor, cascaded and quadratic, and switched capacitor converters are proposed. Z and qZ source converters [5], have greater advantages, such as reduced number of semiconductors in the step-up stage, continuous nearly constant input current, high reliability because unaffected to shoot-through stages. The fundamental drawbacks of these topologies are the voltage stress of the semiconductors is very high. Isolated higher gain DC-DC converters usually accomplished by coupled inductors and the transformers, proposed in [6]–[8]. Even though they provide galvanic-isolation among the two ports

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(input and output), but their leakage inductances and the capacitances of the various windings at the higher switching frequencies creates the voltage and current spikes on the MOSFETs. Therefore, this configuration required higher rating components and additional clamping circuitry and filter. In [9]–[11] several soft switched (resonant) converters based on Zero Voltage Switching (ZVS) and the Zero Current Switching (ZCS) are proposed. If the voltage stress on the semiconductors is low, it helps in choosing the less ON resistance MOSFETs which decreases the losses of the converter which intern increase the efficiency. Here, the soft switching reducing the voltage stress and snubber circuit for the output diodes are not required for the protection of the output diodes. But in [11], to achieve ZVS central MOSFET switch purely rest on the energy deposited in the leakage inductance. Hence, to achieve ZVS of the main MOSFET additional leakage inductance and capacitance or an additional inductor is necessary, which leads to the reduction in gain (duty cycle loss) and increases the components. To compensate for these issues, the converter has to function at a greater duty cycle which further increases the RMS currents in the devices leading to more losses.

Recently Switched Capacitor (SC) principle based power electronic has grabbed the attention because of the no inductive components and can be extended to the higher power densities with full monolithic structure [12]. However, the main drawbacks are pulsating input current, large active switches and capacitors, and complex control for the capacitor current. Incorporating the coupled inductor with SC has been proposed in [13]. This topology eliminated the problems of the SC, but voltage and current spikes occur at the semiconductors. In [14]–[16], a combination of the switched inductor (SL) and SC structures with the basic single inductor (buck, boost, buck-boost, sepic and cuk) has been proposed. These converters are modular in structure, diminish the voltage stress of the MOSFETs, and improve the gain. Capacitor Diode-Voltage Multipliers (CD-VM) [17]–[19] based configuration are recently proposed to achieve a higher output voltage. These topologies can be a good solution for high voltage conversion due to uniform voltage stress across all the semiconductors devices and capacitors, multiple capacitor stages at the output, simple structure, higher voltage gain devoid of extreme duty cycle, suitable to feed multilevel inverters, and easy to add or remove the number of stages without disturbing the main boosting circuitry. In [19], the interleaved converter is proposed by combining positive and negative multiplier to obtained a high voltage conversion ratio. However, the circuitry is derived by just duplicating the components of the multiplier. Hence, the circuitry required a high number of capacitor and diodes. Moreover, in converters [17]–[19], energy is transferred from capacitor to capacitor, which creates sudden transient in the current. Therefore, current dependent voltage droop and the voltage ripple are the foremost complications associated with the CDVMs at a higher number of the VM stages. To address these drawbacks and the number of stages, a new interleaved converter is proposed for high gain. Charging of each capacitor through inductor current is the additional feature of this configuration. It is noteworthy that, current fed CDVMs are the appropriate solution for the power electronic interface for renewable applications. However, the suggested circuitry required an additional high voltage diode-capacitor filter stage at the output side. Moreover, two input boost stages are used. To lessen the VM stages, a new interleaved converter with a Dickson voltage multiplier is proposed [21]–[30]. However, the limitations with these DC-DC converter topologies are, circuit complexity, a higher number of VM stages, unable to attain high gain with inverting capability, higher input ripples, etc.,

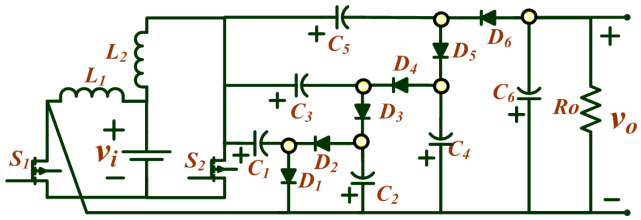

FIGURE 1. Proposed inverting High gain DC-DC converter.

In this paper, for achieving the low current ripple at the input side, high voltage gain, and current fed configuration using a minimum number of components and stages, a new non-isolated current fed interleaved multilevel interleaved boost converter. The potential benefits of the proposed converter are,

- Ripple free input current profile for minimizing the input side filter requirements and passive elements in the circuit
- High voltage gain with minimal components in the circuit
- Inverting voltage capability
- Minimal switch ratings of the converter
- Highly efficient
- Simple control of charging and discharging of capacitors in VM cells.

The organization of this paper is as follows; the proposed converter configuration, operating principle, steady state analysis for CCM and DCM, voltage gain analysis are discussed in Section II. The comparative analysis and study with the high gain DC-DC converters have presented in Section III. The experimental validation and the respective results, the discussion is presented in Section IV. The concluding statements are given at the end of this paper.

II. INTERLEAVED STRUCTURED CURRENT FED HIGH GAIN CONVERTER

Fig. 1 represents the power circuitry of the novel interleaved high gain converter configuration for the three stages of the VM's. The basic interleaved boost converter is connected with the inverting VM cells to achieve the maximum possible voltage gain. Each VM cell (stage) consists of one diode and one capacitor, unlike the two each in the half-wave VM cells. This helps in achieving a higher gain with the fever number

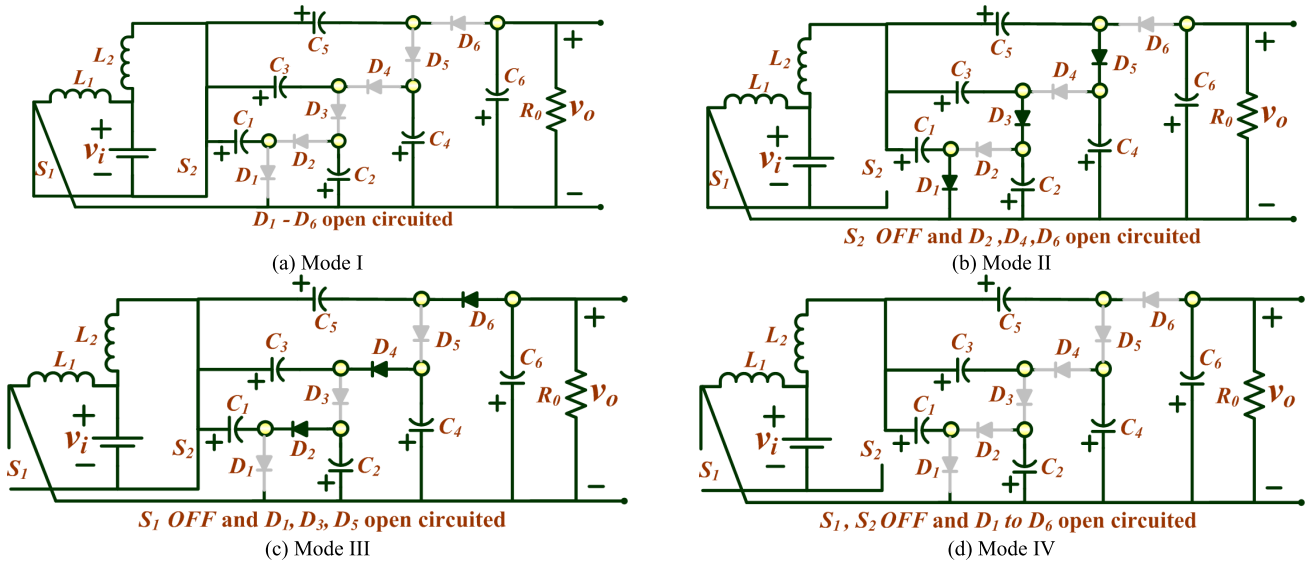

FIGURE 2. Operating modes of the proposed DC-DC converter topology.

of components. The MOSFET's switches are phase shifted by the 180degrees to achieve the maximum number of operating levels. All the operating stages and the voltage gains are derived in the coming sections.

A. OPERATING MODES

Mode I: during Mode I, MOSFET's S_1 and S_2 are ON and the corresponding circuitry is shown in Fig. 2(a). During this Mode I, both the inductors(L_1 & L_2) are charged from the input voltage v_i. The capacitor C_6 is discharged via the resistance (R_o-load). The respective mathematical representation for this mode is shown below,

$$\left.\frac{di_{L1}}{dt}=\frac{v_i}{L_1}=\frac{V_i+\Delta v_i}{L_1}\approx\frac{V_i}{L_1},\ \frac{di_{L2}}{dt}=\frac{v_i}{L_2}=\frac{V_i+\Delta v_i}{L_2}\approx\frac{V_i}{L_2}\right\} \tag{1}$$

The diode D_1 to D_6 are blocked & the C_6 is supplying the load.

Mode II: During Mode II, the MOSFETs S_1 & S_2 are turned ON and OFF, respectively. Fig. 2(b) shows the equivalent circuitry for Mode II. The L_1 is energized from the supply voltage through S_1. The supply voltage v_i and the inductor L_2 form boost stage & energized the C_1 via D_1 and S_1. The capacitor C_2, supply voltage v_i, and inductor L_2 energized the C_3 via D_3 and S_1. The capacitor C_4, supply voltage v_i, and inductor L_2 energized the C_5 via D_5 and S_1. The slope of the inductor L_1 and L_2 currents be able to represented as below,

$$\left.\frac{di_{L1}}{dt}=\frac{v_i}{L_1}=\frac{V_i+\Delta v_i}{L_1}\approx\frac{V_i}{L_1},\quad \frac{di_{L2}}{dt}\approx\frac{V_i-V_{C1}}{L_2}\right\} \tag{2}$$

D_1, D_3, & D_5 are forward biased & simultaneously D_2, D_4, & D_6 are reverse biased. All the capacitors with odd numbers (C_1, C_3, and C_5) are charged through the combination of the input voltage v_i, inductor L_2, and the even number capacitors (C_2, and C_4), respectively. The capacitor C_6 is de-energized via load.

Mode III: during Mode III, the S_1 and S_2 are made OFF & ON, respectively. Fig. 2(c) shows the equivalent circuitry. The L_2 is energized from the supply voltage v_i via S_2. The capacitor C_1, supply voltage, and inductor L_1 are together energized the capacitor C_2 via D_2 & S_2. The capacitor C_3, supply voltage v_i, and inductor L_1 energized the C_4 via D_4 & S_2. The capacitor C_5, input voltage v_i, and inductor L_1 delivers power to load and at the same time also charged the capacitor C_6 through diode D_6 and switch S_2.

During this mode, D_2, D_4, and D_6 are forward biased and the diodes D_1, D_3, and D_5 are reverse biased. All the capacitors with odd numbers (C_2, C_4, and C_6) are charged through by the combination of the input voltage v_i, inductor L_2, and the even number capacitors (C_1, C_3, and C_5), respectively. The slope of the inductor L_1 & L_2 currents be able to represented as follows,

$$\left.\frac{di_{L2}}{dt}=\frac{V_i}{L_2},\quad \frac{di_{L1}}{dt}=\frac{v_i-v_{C2}+v_{C1}}{L_1}=\frac{V_i-V_{C1}}{L_1}\right\} \tag{3}$$

Mode IV: In this mode, both MOSFETs S_1 & S_2 are made OFF and corresponding circuitry is presented in Fig. 2(d). During this mode, the current flowing via inductors L_1 and L_2 become zero because all the D_1-D_6 are reversed biased. Generally, this mode is avoided in order to operate converter in CCM. Therefore, both switches are operated with duty cycles greater than the 50% to avoid this mode.

B. CCM ANALYSIS

The steady-state operation of a power converter is presented in Fig. 3 & semiconductor MOSFETs of the converter are triggered in such a way that Mode I occur exactly in the middle of the mode II & III. Non-idealities of semiconductor

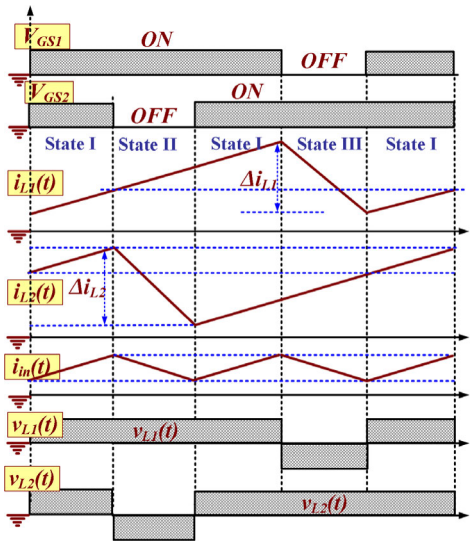

FIGURE 3. Steady state operation and respective waveforms of proposed high gain converter in different modes of operation.

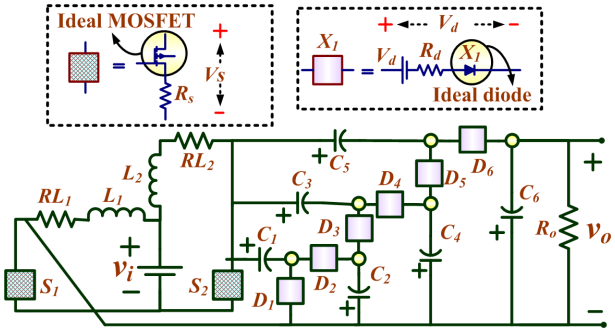

FIGURE 4. Proposed converter circuit by considering Non-idealities.

components & the L_1 *and* L_2 are considered for the calculation of the voltage conversion ratio. The equivalent circuitry with non-idealities is presented in Fig. 4. The Equivalent series resistance (ESR) of the inductors L_1 and L_2 are represented as the R_{L1} & R_{L2}, respectively. The drop across each S_1 & S_2; and D_1 & D_2 are considered as V_S and V_d, respectively. For simplicity, it's assumed that all the C_1-C_6 are designed to maintain the constant voltage.

When switch S_1 is switched ON for the time d_1T_S, the inductor L_1 voltage follows,

$$v_{L1} = V_i - V_S - i_{L1}R_{L1} \tag{4}$$

When the switch S_1 made OFF during time $(1\text{-}d_1)T_S$, the L_1 voltage can be represented as follows,

$$\left.\begin{aligned} v_{L1} &= V_i + V_{C1} - V_{C2} - V_S - i_{L1}R_{L1} - V_d \\ v_{L1} &= V_i + V_{C3} - V_{C4} - V_S - i_{L1}R_{L1} - V_d \\ v_{L1} &= V_i + V_{C5} - V_{C6} - V_S - i_{L1}R_{L1} - V_d \end{aligned}\right\} \tag{5}$$

The time when S_2 is switched ON for time d_2T_S, L_2 voltage can be represented as follows,

$$V_{L2} \approx V_i - V_S - i_{L2}R_{L2} \tag{6}$$

When the switch S_2 is switched OFF during time $(1\text{-}d_2)T_S$, the L_2 voltage can be represented as follows,

$$\left.\begin{aligned} V_{L2} &= V_i - V_{C1} - V_S - i_{L2}R_{L2} - V_d \\ V_{L2} &= V_i + V_{C2} - V_{C3} - V_S - i_{L2}R_{L2} - V_d \\ V_{L2} &= V_i + V_{C4} - V_{C5} - V_S - i_{L2}R_{L2} - V_d \end{aligned}\right\} \tag{7}$$

The voltage across odd number capacitors is calculated as follows,

$$\left.\begin{aligned} V_{C1} &= \frac{V_i - V_S - i_{L2}R_{L2}}{(1-d_2)} - V_d \\ V_{C3} &= \frac{V_i - V_S - i_{L2}R_{L2} + (V_{C2} - V_d)(1-d_2)}{(1-d_2)} \\ V_{C5} &= \frac{V_i - V_S - i_{L2}R_{L2} + (V_{C4} - V_d)(1-d_2)}{(1-d_2)} \end{aligned}\right\} \tag{8}$$

The voltage across the even number capacitors (C_2, C_4 & C_6) & output voltage (V_o) is found as follows,

$$\left.\begin{aligned} V_{C2} &= \frac{V_i - V_S - i_{L1}R_{L1}}{(1-d_1)} + V_{C1} - V_d \\ V_{C4} &= \frac{V_i - V_S - i_{L1}R_{L1} + (V_{C3} - V_d)(1-d_1)}{(1-d_1)} \\ V_{C6} &= \frac{V_i - V_S - i_{L2}R_{L2} + (V_{C5} - V_d)(1-d_1)}{(1-d_1)} = -V_o \end{aligned}\right\} \tag{9}$$

It can be observed that the voltages across the capacitors are asymmetrical and are progressively increasing. The capacitor C_6 is connected across the load. When both the switches can function at the same percentage of the duty ratio ($d_1 = d_2 = d$), the capacitor voltages are calculated as below,

$$\left.\begin{aligned} V_{C1} &= \frac{V_i}{(1-d)}, \quad V_{C2} = \frac{2V_i}{(1-d)}, \\ V_{C3} &= \frac{3V_i}{(1-d)}, \quad V_{C4} = \frac{4V_i}{(1-d)}, \\ V_{C5} &= \frac{5V_i}{(1-d)}, \quad V_{C6} = \frac{6V_i}{(1-d)}, V_o = \frac{-6V_i}{(1-d)} \end{aligned}\right\} \tag{10}$$

Fig. 5 demonstrates the influence of the duty ratio on capacitor voltages. It can be concluded that voltage across capacitors is increasing as the amount of capacitors increases. At duty $d = 0.5$ and 0.7, the boosting gain is 12 and 20, respectively.

C. STEADY-STATE DCM ANALYSIS

It is presumed that the current in L_1 is rising for d_1T_S time, $d_1'T_S$ time is obligatory for current I_{L1} to touch zero and current of the inductor L_1 is zero for the $d_1''T_S$ time. Similarly, for switch S_2, d_2T_S, $d_2'T_S$, and $d_2''T_S$ are the time in which inductor L_2 current is rising, falling and zero current,

$$\left.\begin{aligned} T_S &= d_1T_S + d_1'T_S + d_1''T_S \\ T_S &= d_2T_S + d_2'T_S + d_2''T_S \end{aligned}\right\} \tag{11}$$

The relation between the voltage across the capacitors C_1 to C_6 and load as below,

$$\left.\begin{aligned} V_o &= -6V_{C1} = -3V_{C2} = -2V_{C3} \\ &= -1.5V_{C4} = -\tfrac{6}{5}V_{C5} = -V_{C6} \end{aligned}\right\} \tag{12}$$

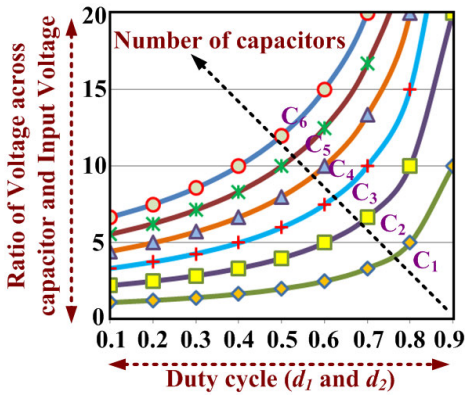

FIGURE 5. The variation of the capacitor voltages in the proposed circuit with respect to the duty cycle.

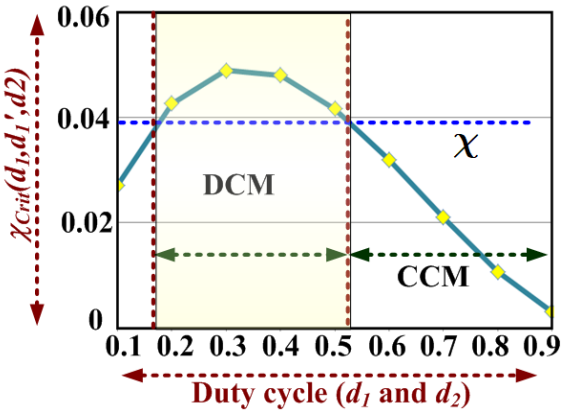

FIGURE 6. CCM and DCM boundary conditions of proposed converter.

During DCM the load current (I_o) is the same as current I_{L1}.

$$(d_1')I_{L1} = \frac{Vo}{R} \Rightarrow I_{L1} = \frac{4V_i}{2d'^2_1 R} + \frac{2V_i}{2d'_1 d'_2 R} \tag{13}$$

By solving (12) and (13), the boundary condition is obtained as follows, and the converter operates in DCM if (14) is satisfied.

$$\left.\begin{aligned} &I_{L1} = \frac{V_i}{2d_1' R_o}\left(\frac{4}{d_1'} + \frac{2}{d_2'}\right) < \frac{T_S V_i d_1}{L_1} \\ &\frac{L_1}{T_S R} < \frac{2d_1 d_1'}{\left(\frac{4}{d_1'} + \frac{2}{d_2'}\right)}, \quad \frac{L_2}{T_S R_o} < \frac{2d_1 d_1'}{\left(\frac{4}{d_1'} + \frac{2}{d_2'}\right)} \\ &\chi < \chi_{Crit}(d_1, d_1', d_2); \quad where,\ \chi = \frac{L_2}{T_S R} \end{aligned}\right\} \tag{14}$$

Applying the principle of volt-second balance to L_1 and L_2, the output voltage for DCM mode is obtained as follows,

$$V_o = -\frac{(d_1 + d_1')\begin{pmatrix} V_i - V_S \\ -i_{L1}R_{L1} \end{pmatrix} + d_1'\,(V_{C5} - V_d)}{d_1'} \tag{15}$$

Fig. 6 shows the borderline between the CCM & DCM for the proposed converter.

D. PROPOSED CONVERTER CONTROL STATES

By varying duty ratios of switches $S_1(d_1)$ and $S_2(d_2)$, the desired voltage across the load can be achieved. The primary condition for the operation is that the gate pulses for both switches should be phase shifted by the 180°. In Table-1, the details about the voltage stress across the switches, capacitor voltages, operating modes and their states and type of the inductor current is given. If $d_1 < d_2$ then the summation of voltages of C_2, C_4, & C_6; lesser than the summation of voltages of C_1, C_3, & C_5, else summation of voltages of the C_2, C_4, & C_6 higher than the summation of voltages of C_1, C_3, & C_5. Also, if $d_1 < d_2$ then switch voltage stress $V_{S1} < V_{S2}$. In order to operate in CCM steady state mode, $d_1 >= 0.5$ & $d_2 >= 0.5$ has to be satisfied.

III. COMPONENT DESIGN AND COMPARISON

The critical inductances L_1 and L_2 is calculated as follows,

$$\left.\begin{aligned} L_{1,crit.} = \frac{V_i \times d_1 \times T_S}{\Delta i_{L1}}; \quad L_{2,crit.} = \frac{V_i \times d_2 \times T_S}{\Delta i_{L2}} \end{aligned}\right\} \tag{16}$$

The average inductor current rating must satisfy the following,

$$IL_1 > \frac{3Io}{(1-d_1)}, \quad IL_2 > \frac{3Io}{(1-d_2)} \tag{17}$$

The voltage stresses of switches is obtained as below,

$$\left.\begin{aligned} V_{S1} = \frac{V_i}{1-d_1}; \quad V_{S2} = \frac{V_i}{1-d_2} \end{aligned}\right\} \tag{18}$$

The blocking voltages across the diodes for all the modes are given as follows,

$$\left.\begin{aligned} &mode{-}I, \quad V_{Dodd} = \frac{-V_i}{1-d_1};\ V_{Deven} = \frac{-V_i}{1-d_2} \\ &mode{-}II, \quad V_{Dodd} = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2};\ V_{Deven} = 0 \\ &mode{-}III, \quad V_{Dodd} = 0;\ V_{Deven} = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2} \\ &mode{-}III, \quad V_{Dodd} = \frac{-V_i}{1-d_1};\ V_{Deven} = \frac{-V_i}{1-d_2} \\ &\left(PIV = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2}\right) \end{aligned}\right\} \tag{19}$$

The critical capacitance values are calculated as follows,

$$\left.\begin{aligned} C_{odd} = \frac{V_o T_S}{R_o \Delta V_{Codd}} d_1, \quad C_{even} = \frac{V_o T_S}{R_o \Delta V_{Codd}} d_2 \end{aligned}\right\} \tag{20}$$

The detailed comparison of the recently proposed high gain converters with the presented converter is reported in Table 2. In this table, gain, number of components (diodes, switches, inductors, capacitors) and stress across components and efficiency details are discussed. It is notable that compared to the existing converter, the proposed converter configuration required fewer components to attain the desired voltage gain for a given input. Furthermore, voltage stress across the switches, diodes is low compared to the other converters presented in Table. 2.

TABLE 1. All possible operating conditions at different duty cycle ranges.

Operation Modes			States	Inductor Current	Voltage stress across switch	Capacitor Voltage For even number of levels
$d_1+d_2>1$	$d_1<d_2$	$d_1<0.5,\ d_2>0.5$	I, II, III, IV	*Discontinuous	$V_{S2}>V_{S1}$	$\sum_{i=1,3,5} V_{Ci} < \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.5,\ d_2>0.5$	I, II, III	Continuous		
		$d_1=0.5,\ d_2>0.5$	I, II, III	Continuous		
	$d_1>d_2$	$d_1>0.5,\ d_2>0.5$	I, II, III	Continuous	$V_{S2}<V_{S1}$	$\sum_{i=1,3,5} V_{Ci} > \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.5,\ d_2<0.5$	I, II, III, IV	*Discontinuous		
		$d_1>0.5,\ d_2=0.5$	I, II, III	Continuous		
	$d_1=d_2$	$d_1>0.5,\ d_2>0.5$	I, II, III	Continuous	$V_{S2}=V_{S1}$	$\sum_{i=1,3,5} V_{Ci} = \sum_{i=2,4,6} V_{Ci}$
$d_1+d_2=1$	$d_1<0.5,\ d_2>0.5$		I, II, III, IV	*Discontinuous	$V_{S2}>V_{S1}$	$\sum_{i=1,3,5} V_{Ci} < \sum_{i=2,4,6} V_{Ci}$
	$d_1>0.5,\ d_2<0.5$	$d_1<0.75,\ d_2>0.25$	I, II, III, IV	*Discontinuous	$V_{S2}<V_{S1}$	$\sum_{i=1,3,5} V_{Ci} > \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.75,\ d_2<0.25$	I, II, IV			
		$d_1=0.75,\ d_2=0.25$	I, II, IV			
	$d_1=d_2=0.5$		I, II	Continuous	$V_{S2}=V_{S1}$	$\sum_{i=1,3,5} V_{Ci} = \sum_{i=2,4,6} V_{Ci}$

TABLE 2. Comparison of proposed converter with existing converter.

Converter	Gain ($G=V_o/V_i$)	Inductors	Capacitors		Switches		Diodes		Efficiency
			Count	VS	Count	VS	Count	VS	
[12]	2/(1-d)	1	3	GV_i	1	$GV_i/2$	3	$GV_i/2$	94%
[13]	(3+d)/(1-d)	2	3	$(G+1)V_i/4$	2	$(G+1)V_i/4$	3	$(G+1)V_i/2$	92.5%
[16]	(3-d)/(1-d)	1	4	$(G-1)V_i/2$	1	$(G-1)V_i/2$	4	$(G-1)V_i/2$	94%
[18]	N/(1-d)	1	2N-1	GV_i/N	1	GV_i/N	2N-1	GV_i/N	89%
[19]	1/d(1-d)	2	3	$C_1=GV_i(1-d)$, $C_2=GV_id$	2	$S_1=GV_i(1-d)$, $S_2=GV_id$	3	$GV_i(1-d)$	91.5%
[21]	4/(1-d)	2	5	GV_i	2	$GV_i/2$	4	$GV_i/2$	91.4%
[20]	(N+1)/(1-d)	2	N+1	GV_i	2	$GV_i/5$	N+1	GV_i	92%
Proposed	N/(1-d)	2	N	$C_X=XGV_i/N$ where X=1,2,3..6	2	GV_i/N	N	$2GV_i/N$	94%

IV. HARDWARE RESULTS AND DISCUSSION

The hardware prototype is developed with a power rating of 300 W to confirm the performance of the proposed converters theoretical analysis. The voltage gain of 15 is achieved with input voltage 20V and output voltage 300V. Two E-type ferrite cores are utilized for making the inductors L_1 and L_2 with rating 200uH/20A. Six capacitors with 100uf/400V and Six SDUR3020W high-frequency diodes are used. Two FQH44N10 MOSFET's of 100V ratings are used and the two gate pulse with 180° phase shift, 200ns sampling, and switching frequency 50kHz is generated through FPGA to control switches. Both the switches are operated at the equal duty cycle and operated between 50% to 80% duty cycles.

Fig. 7 displays the waveform of the supply voltage (V_i), supply current, output voltage (V_o), & output current (I_o). Practically, it is investigated that output voltage "−304V" with "−0.925A" output current is achieved from the 20V input voltage and 15A input current. In Fig.8, the graphs of the voltage and current of the inductors L_1 & L_2 are shown. It is observed that when the S_1 or S_2 are switched ON, the voltage across inductors (L_1 & L_2) are the same as the input voltage and current is linearly increasing. Similarly, when S_1 or S_2 are switched OFF, the current through L_1 & L_2 are linearly reduced. The overlapping period of both switches ON is observed as presented in Fig. 9. As the anticipated converter is interleaved in nature, the input current ripple is reduced compared to ripples of the inductor L_1 and L_2 currents as shown in Fig. 9. It is noteworthy that the experimentation work is investigated at 60% duty cycle. As a result, little ripples are observed in the input current. However, it can be minimized to zero at the 50% duty for both the switches.

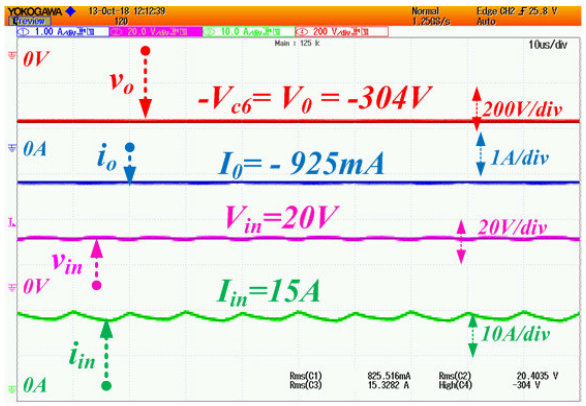

FIGURE 7. Input and output: voltage and current waveforms.

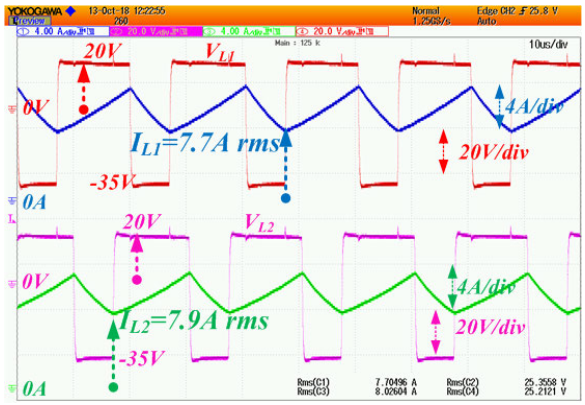

FIGURE 8. Inductor voltages and currents waveforms.

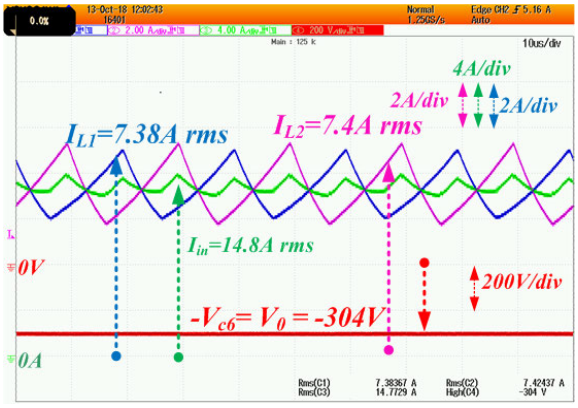

FIGURE 9. Input and inductor current waveforms.

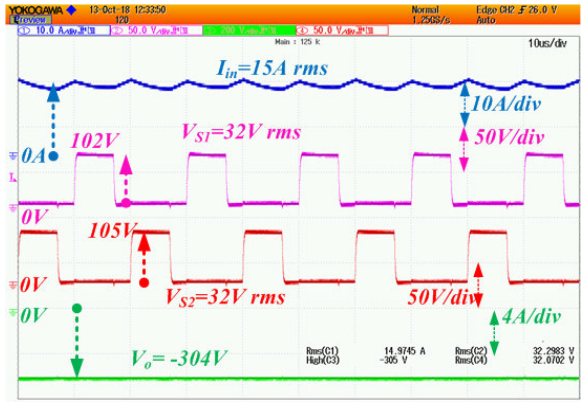

FIGURE 10. Switch voltages and input current and output voltage waveforms.

The switches S_1 and S_2 drain to source voltages waveforms are revealed in Fig.10. The experimentally observed voltage stress across S_1 & S_2 are 102V & 105V, respectively. The voltage (RMS) across switches S_1 & S_2 are −32.2V & 32.01V, correspondingly. The scope results of input current, the voltage across switches S_1 & S_2, and inductor L_2 current are shown in Fig. 11. It is validated that the inductor L_2 is charging when the voltage across switch S_2 is zero i.e the switch S_2 is conducting and the charging of inductor L_2 is independent of switch S_1. In Fig. 12, the voltage across D_1 & D_2 are shown with inductors L_1 and L_2 currents. It is observed

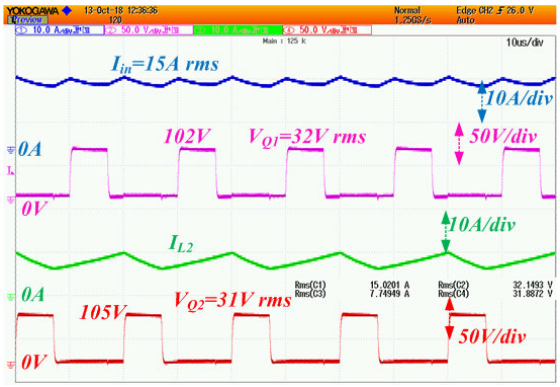

FIGURE 11. Switch voltages, input and inductor currents waveforms.

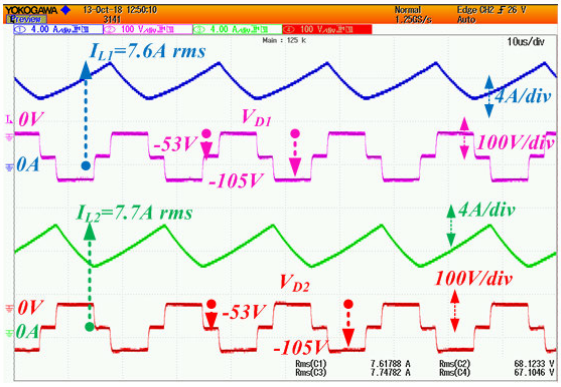

FIGURE 12. Diode D_1 and D_2 voltages and inductor currents waveforms.

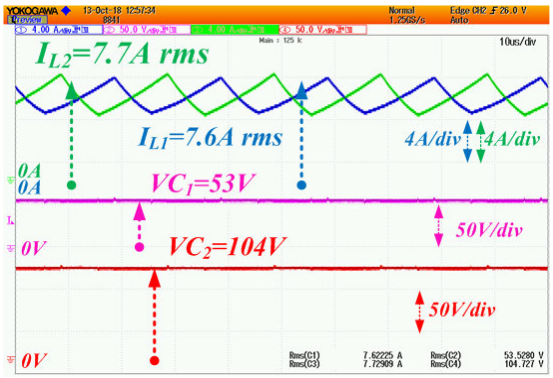

FIGURE 13. Capacitor across capacitor C_1 and C_2 waveforms.

that there are two steps in the blocking voltage across the diode. The voltage across diodes D_1 and D_2 in mode-I are −53V i.e means the voltage of capacitor C_1 directly appears across the diode D_1 and D_2. The Peak Inverse Voltage (PIV) of the D_1 & D_2 are −105V. However, the conduction of D_1 & D_2 is 180^o phase shift with each other. The RMS value of the voltage across the D_1 & D_2 is −68.12V and −67.1V, respectively.

The waveform of voltages across C_1 & C_2; & current through inductors L_1 and L_2 are presented in Fig. 13. The noted voltage across capacitor C_1 and C_2 are 53V and 104V, respectively. The voltages difference between capacitors and current through inductors L_1 are displayed in Fig. 14.

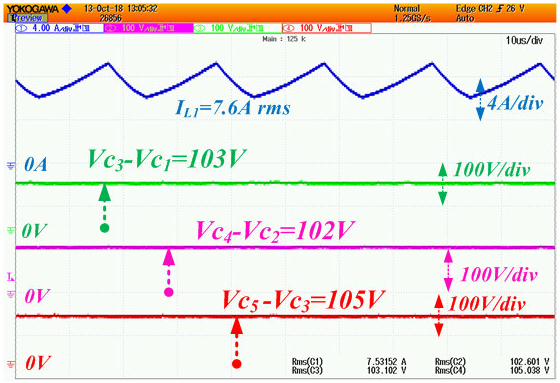

FIGURE 14. Voltage difference between capacitors waveforms.

The observed voltage across C_3-C_3, C_4-C_2, and C_5-C_3 is 103V, 102V, and 105V, correspondingly. It is recorded that the voltage difference is nearly the same. The average efficiency of the designed hardware sample is 93.07%.

V. CONCLUSION

A novel non-isolated current fed interleaved inverting high gain DC-DC power converter is reported for the renewable applications. The reported converter combines the feature of the interleaved fundamental boost converter & diode-capacitor stages. The full-wave voltage multiplier arrangement is incorporated to raise the voltage gain by using a very minimal number of devices. At the same duty cycle, the proposed converter be able to easily extend to the greater numeral of stages to increase the gain by adding only 1 diode & 1 capacitor for each VM stage increment. The detailed operating modes for CCM & DCM are studied with the help of practical design criterion. The practical and the theoretical voltage gains at the same duty ratios has been validated and they are approximately equal. The detailed comparison with the recently proposed other converter has shown that the anticipated converter is further superior over the available converter topologies. The fabricated prototype is tested at 300W and observed conversion is efficiency 93.07% and presented experimental results to confirm the performance and theoretical analysis. The closed-loop control, integration with renewable energy systems, soft switching of semiconductors devices and voltage stress minimization of semiconductor devices are the future tasks of the proposed converter.

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