QATAR UNIVERSITY

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DESIGN OF HIGH-GAIN DC-DC CONVERTERS FOR HIGH-POWER PV APPLICATIONS

BY

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ABSTRACT

Renewable energy sources are penetrating the market in an ever increasing rate, especially in terms of Wind and Solar energies, with the latter being more suitable for the GCC region. Typically, Photovoltaic (PV) strings' output voltage is limited to ~ 1500 V due to safety constraints, and thus requires boosting to higher DC levels (non-isolated step-up DC-DC transformer) suitable for High-Voltage DC (HVDC) and AC grid applications in order to provide the required DC-Link voltage level. Nevertheless, conventional non-isolated DC-DC converters provide a limited practical gain due to their parasitic elements. Other options include isolated DC-DC converters that utilize costly high-frequency transformers with limited power capability. Moreover, the isolation requirements of transformers in HVDC significantly increase the footprint of the converters. High-frequency transformers for high-power applications are hard to design and are usually associated with higher losses. Alternatively, connecting conventional DC-DC converters in different combinations can provide higher gains to the required levels, while maintaining the high efficiency requirements. This thesis proposes the cascade and/or series connection of DC-DC modules as a solution to the high-conversion ratio requirement, based on Cuk and Single-Ended Primary Inductor Converter (SEPIC) topologies, whose continuous input current is suitable for PV applications, and reduces the bulky capacitor filters at the input side. Detailed theoretical models of the proposed topologies are first derived, then their trends are practically verified by low power prototypes. Sensitivity analysis is also performed to assess the effect of small variations to the parasitic inductors' resistances on the overall system gain, where the input inductor is found to have a considerable effect, especially at higher duty

ratios (i.e. higher gains). High-power applications' scenarios with their considerations are simulated to compare the different topologies and the results show a comparable efficiency of the proposed converters for a 1 –MW application with efficiencies higher than 90%.

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Chapter 1 : Introduction

1.1. Background

The eventual depletion of fossil fuels, combined with their negative effects on the environment has led to a recent developing shift in the adopted energy sources on a global scale to more sustainable and renewable sources that are also considered environmentally friendly. Among these are the Wind Turbines, Fuel Cells and Photovoltaics (PV), with the latter being an attractive choice to the parts of the world subjected to relatively higher solar irradiance levels [1]. Nonetheless, integration of the high-power PV farms to the existing AC network grid, or HVDC systems requires the use of power electronics devices and technologies [2, 3]. The PV output voltage is constrained to low DC voltage levels, typically with an open circuit voltage that is limited to 1500V per string for safety considerations [4, 5]. In other words, connecting the modules in series to directly obtain very high-voltage levels is not permissible due to safety concerns. Thus, such relatively small output voltage requires boosting to a much higher DC level in order to provide the appropriate DC Link for HVDC system's connection or DC-AC conversion [2, 6]. However, many factors have to be taken into account while designing each power conditioning stage. Figure 1.1 shows a conventional power conditioning system for PVs integration to the grid, where the DC-DC conversion stage with its detailed aspects will be the main focus of this thesis.

Typically, DC-DC converters used for PV Power Conditioning Systems (PCS) can be divided into isolated and non-isolated types [6-8], where the latter possesses a higher efficiency for high-power applications since it does not need a transformer with the efficiency reduction

usually associated with its leakage inductance at highly rated applications [3, 7, 9]. As for the non-isolated type, several existing DC-DC converter types inherently have the capability of voltage boosting [6]. Though, it is usually desired to utilize a converter that provides continuous input current since PV source current should be continuous for reduced capacitor sizing and proper maximum energy extraction [10].

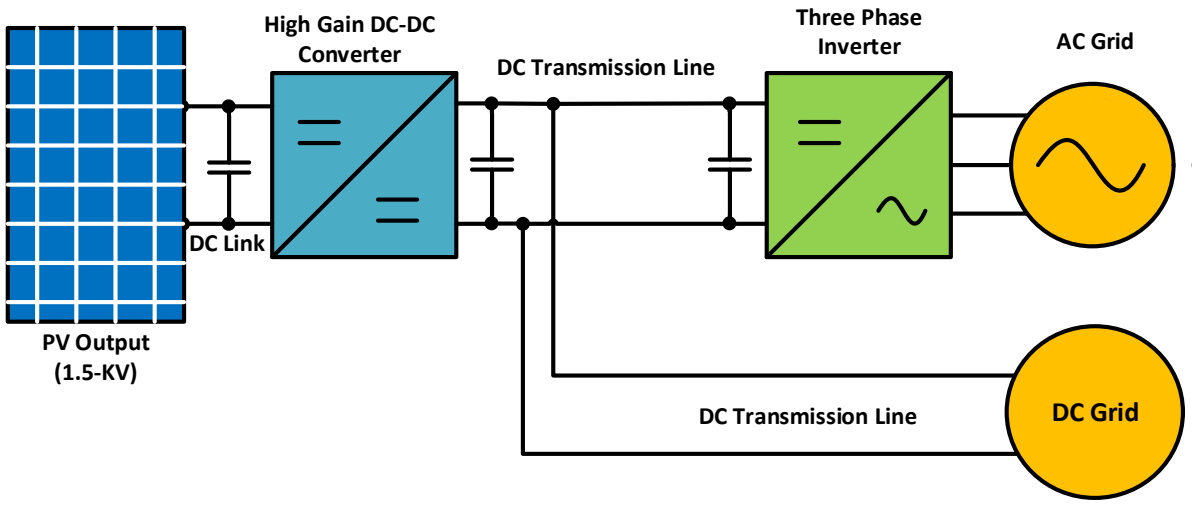
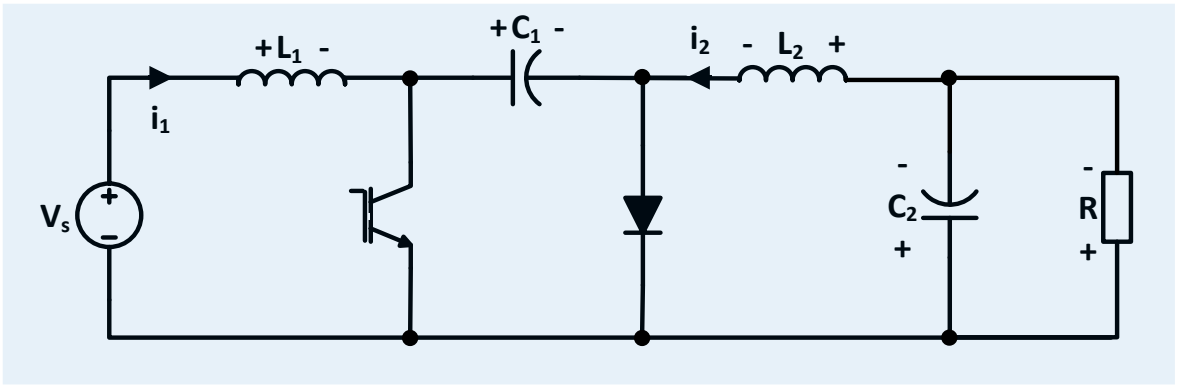


Figure 1.1: PV Power Conditioning System Grid Connection High Level Block Diagram

Such selection eliminates the need of installing bulky capacitor banks across the converter input to smooth the panels' output and to avoid their damaging by directly connecting them to a pulsating input. This saves the cost, and enhances the reliability of the system since these capacitors usually exhibit short lifetime [10-11]. The converter input current continuity is ensured by the input inductor when operating in the Continuous Conduction Mode (CCM). This also makes it more reliable to perform Maximum Power Point Tracking (MPPT) to

maximize the system's output power [10-11] . Typically, boost, Single Ended Primary Inductor Converter (SEPIC) and Cuk converters with their conventional topologies (shown in Figure 1.2, with a corresponding comparison shown in Table 1.1, fulfil the aforementioned requirements by providing a continuous input current with a low ripple factor associated with a proper compromise between the switching frequency, inductance and input power [11-12]. Consequently, the required high gains for such high-power applications can be ideally achieved by the simplest forms of conventional boost converters. Yet, practical limitations on the maximum achievable gain exist and have motivated investigating different alternatives. These limitations are essentially related to the parasitic resistances of the converter's components (e.g. inductors, capacitors and switches) [7, 13], as well as the switching losses of the semiconductor devices due to the deployed hard-switching technique, especially when high currents are involved [14]. The effect of these losses is mainly seen when the converter is operating at very high duty cycles to achieve high-voltage conversion ratio, and their overall effect is a dramatic decrease in the converter's efficiency and a massive gain deteriorations at extreme duty cycles [7, 13]. In addition, voltage and current stresses on switches is also considered as a key element to the overall performance assessment of DC-DC converters in high-power applications [7, 15]. That is, the increased stresses are directly related to an increased size of the used heat sinks and the number of switches per-string, as well as their managing and synchronization techniques, which results into more complications in terms of the physical size of the system [3]. Also, the voltage stress levels in Table 1.1 are comparable between the three converters for high-power PV applications. The required output voltage (V_o) is usually very high compared to the input voltage (V_s) [2, 6].



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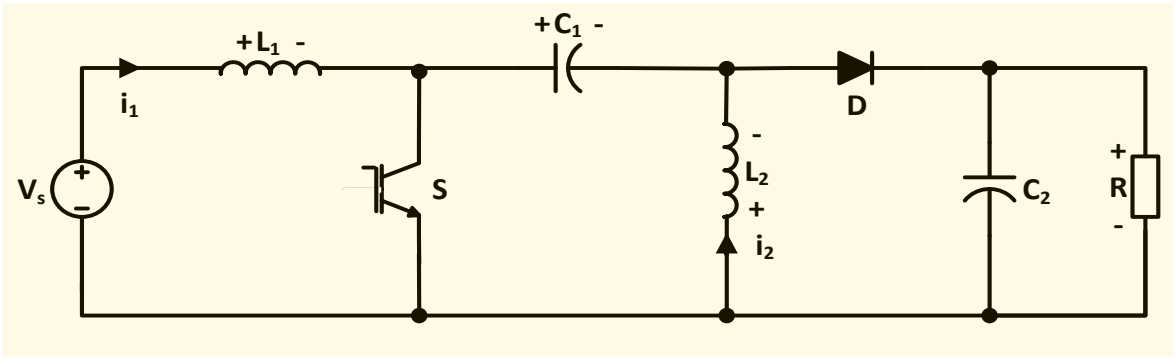

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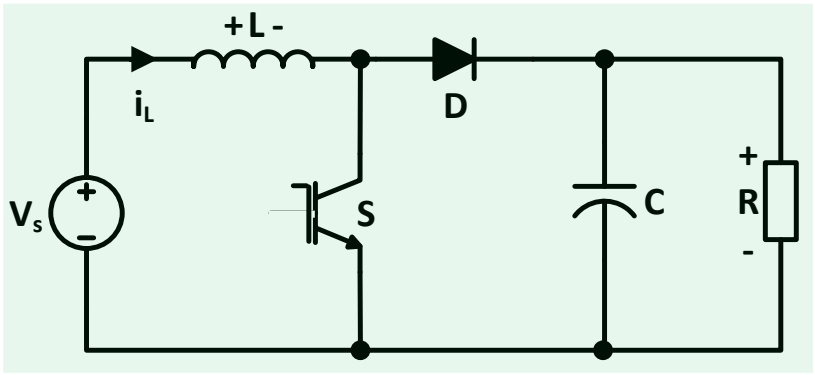


(c)

Figure 1.2: Conventional Topologies for (a) Cuk (b) SEPIC (c) Boost DC-DC Converters

Thus, a stress level of V_s+V_o does not differ by much from V_o. Having said that, the series connected switching devices have to be appropriately controlled to avoid any operating mismatch [3]. On the other hand, problems such as the reverse recovery losses associated of the diode can be tackled by proper selection of diodes (e.g. the emerging Silicon Carbide (SiC) Schottkey diode type that eliminates the reverse recovery problem) [16, 17]. Also, hard-switching of the semiconductor devices can be tackled by adopting soft switching techniques, which although add to the complexity of the system, they contribute to an overall loss minimization [7, 18]. Consequently, an overall efficient design has to take all of these factors into consideration in order to achieve reasonable tradeoffs based on the specific applications.

Table 1.1: Comparison between the main Boost converters for PV Applications

Converter	**Boost**	**Cuk**	**SEPIC**
Type	Step Up	Step Up/Down	Step Up/Down
Input Current	Continuous	Continuous	Continuous
Output Current	Discontinuous	Continuous	Discontinuous
Switches Voltage Stress	V_o	$V_s + V_o$	$V_s + V_o$
Switches Current Stress	I_o	$I_s + I_o$	$I_s + I_o$
Output Polarity	Positive	Negative	Positive
Energy Transfer	Direct	Indirect	Indirect

Different topological arrangements based on the basic ones discussed earlier, especially the boost converter, have been developed over time in order to practically maximize the achievable gain within a maximum acceptable efficiency margin (e.g. series, cascaded and isolated connections) [7], and some of them will be discussed thoroughly in the literature review chapter from a performance assessment point of view. Yet, this thesis focuses on a detailed study, analysis, implementation and assessment of different topologies based on the Cuk and SEPIC in terms of maximizing their practical gains. Although these two converters have a higher number of passive components (4^{th} order) compared to boost, in addition to higher voltage rating for their coupling capacitors with high RMS currents flowing through. On the other hand, a design optimization can tolerate higher ripple content for the coupling capacitors to reduce the overall cost, while properly selecting the component to minimize its Equivalent Series Resistance (ESR) and thus the corresponding losses. This tradeoff is important since increasing the capacitance would require connecting multiple parallel high-voltage bulky capacitor banks. Having said that, the standardized ripple content of the converters output capacitors must be maintained to meet the required grid-connection regulations. Consequently, these two basic topologies were selected in particular due to their continuous input current, smooth input/output energy transfer, and improved performance in high-power applications [11, 19]. Cuk is also advantageous in terms of its output filter capacitor independence from its load resistance, which is of great importance at higher power applications as converters equivalent resistance tends to decrease with increasing output voltage. However, and in order to fully assess the performance of the topologies to be proposed, a detailed modelling of both Cuk and SEPIC converters with any other auxiliary

converter is required in order to achieve accurate characterization in the different desired aspects.

1.2. Thesis Objectives:

The objective of this thesis is to investigate, design and test different connections of non-isolated DC-DC converters to achieve high voltage conversion ratio for High-Power PV applications to provide the required HVDC transmission level output as well as the appropriate DC-Link voltage for AC-Grid integration. The designs are based on Cuk and SEPIC topologies, using Cascade and Parallel-Input-Series-Output (Series) connections of these converters to overcome the limited gain associated to single-stage modules due to the parasitic losses, all while maintaining high efficiency levels for the overall conversion system.

1.3. Thesis Scope

The thesis report is structured firstly with an introductory overview tackling the high level system requirements in Chapter 1, followed by a literature survey on different topologies related to this work with their overall assessment in Chapter 2. A Comprehensive presentation of the proposed topologies and their assessment techniques is introduced in Chapter 3, whereas detailed modelling of the used converters (Cuk, SEPIC as well as the auxiliary Buck-Boost) with their parasitic elements and the major non-idealities is presented in Chapter 4, together with the practical verification of the derived models. Chapter 5

presents detailed efficiency comparison and performance assessment of the different proposed connections, where low-power prototypes are first tested as a proof-of-concept, followed by a projection of their findings on high-power PV applications. Sensitivity analysis is then performed to study the effect of slight variations of inductors parasitic resistance random variations on the overall system gain in Chapter 6. Finally, conclusions and possible ways of extending this work are presented.

Chapter 2 : Literature Review

The problem of DC-DC converters' design with a high practical conversion ratio has been investigated in several recent works in the literature, where many of which were directed at renewable energy systems and their applications [3,6,7,9-11,19-32]. The flow of this literature survey will be to first review some of the existing isolated and non-isolated DC-DC converters along with assessing their overall performance and efficiency for the given application, and to establish a criteria for selecting an appropriate topology that meets the thesis objectives. Figure 2.1 shows a comparison, in terms of the power-flow direction and stages, between isolated and non-isolated DC-DC converters.

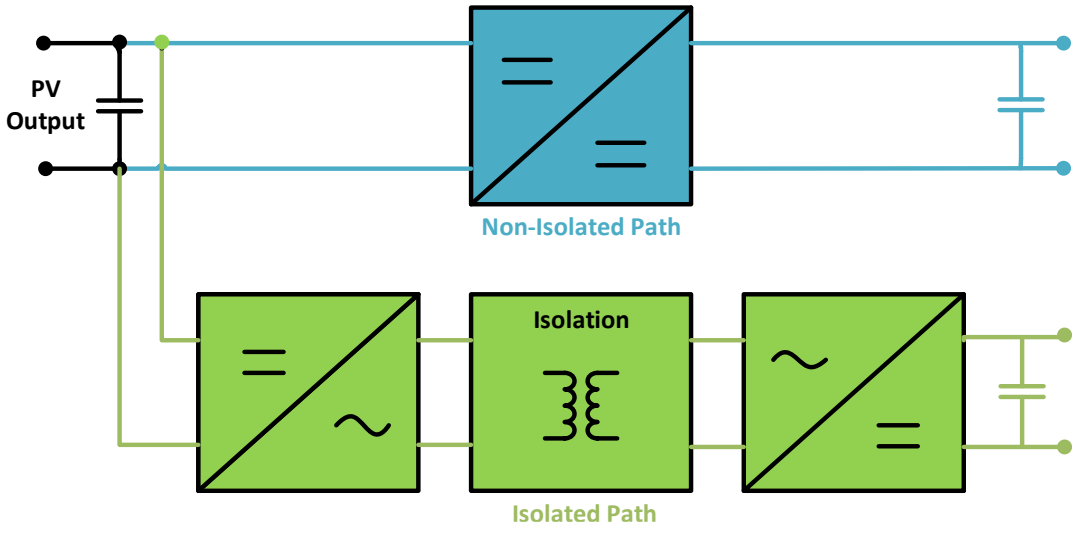


Figure 2.1: High level block diagram of isolated versus non-isolated DC-DC converters

One paper in the literature discussed the problem of high DC-DC from an operational point of view for the isolated dual-active bridge converters [20], and although the proposed technique showed promising results in terms of reducing the overall losses, it still lacks the direct ability of filtering the output current ripples. However, it states that a long dc-transmission cable of around 100-km would naturally filter the output [20]. This may provide a practical solution for the HVDC applications, but it still introduces the need to use bulky capacitor banks at the output terminals when DC-Link is required before the DC-AC conversion stage of the AC grid integration as stated earlier. Additionally, operating the used transformer at low frequencies (250-400 Hz) as the authors proposed would heavily increase the cost and size of the practical converter [20]. On the other hand, a recent published worked proposed a new mechanism for increasing the system efficiency by decreasing the switching losses and the output inductor requirements, based on paralleling the inputs of two full-bridge converters and summing their output voltages (parallel-input series-output) [9], where the main share of power is processed through a "main converter", whereas the second is labeled as "control converter" and transfers a minimal share of power that is enough to employ the control task of the system [9]. The results were also promising in terms of the overall system efficiency, where the losses in the main converter were a fraction of that in the control converter [9]. However, the authors highlighted some practical limitations related to their design that are mainly concerned with the increased number of used active components, in addition to the requirement of an efficient high frequency transformer design for practical very high-power applications [9]. Similarly, another paper described the detailed design of a Solid-State Transformer (SST) for smart and micro grid applications supporting AC and DC

systems, including the DC-DC conversion stage [21], which also utilizes a high-frequency transformer to achieve electrical isolation and to obtain the effect of boost conversion. Nevertheless, it still introduces the challenge of requiring bulky capacitors at both input and output sides to smoothen the currents when directly connected to the output of the PV panels [21]. Another work considered using a resonant switched capacitor (RSC) DC-DC converter for high-power application [22], which also introduces soft switching to minimize the switching losses, in addition to using two output filtering capacitors that are out of phase in order to eliminate the ripple contents whilst maintaining the components count [22]. However, the original components' count includes multiple controlled switches and diodes per module and is relatively high compared to the conventional DC-DC converters [22]. Likewise, the work presented in [23] uses a similar topology that shares the advantage of minimizing the output ripples as a result of interleaving, in addition to minimizing switching losses with low overall voltage stress across them. Another RSC DC-DC is proposed in [24], where it is designed mainly for medium-voltage, high-power applications and is also advantageous in terms of minimizing the switching losses by soft switching techniques, which leads to increasing the maximum operational switching frequency thus reducing the footprint of the system [24]. A new converter topology for high-power applications is also introduced in [25], where it utilizes a resonant inductor to transfer the energy from the input side to the output side. Nevertheless, it holds the disadvantage of discontinuous input and output currents operation, which affects the PV farm performance, and necessitates bulky and expensive capacitor banks. Yet, the proposed converter also introduces soft switching mechanism to minimize switching losses with a variable switching frequency that can be

utilized with proper controllers [25]. Soft switching techniques are also employed in [25] for the same purpose. The proposed converter in [26] is composed of a combination between conventional boost and a series-parallel resonant converters. The resulting voltage stresses across the diodes and switches are thus minimized, in addition to the system modularity that allows multiple modules to be connected in different combination to achieve higher output voltages.

An interleaved converter is also proposed in [27], where its design is based on the conventional boost converter, however; with an integrated voltage multiplier module to extend the voltage gain. The proposed converter is characterized by a low input current ripple and low switching losses, which is advantageous for the renewable sources [7, 27]. The low input current ripple requires a proper design of the inductor values with respect to the switching frequency. Consequently, the concept of interleaving divides the stress between the different stages in terms of several parameters (e.g. the input power, current and the maximum voltage across the switches) [7, 27]. The problem of discontinuous output current is still present due to the lack of an output inductor, leading to the installation of bulky capacitor banks. Additionally, another proposed design in [28] replaces the rectifier diode in a conventional boost converter with a switch and introduces an auxiliary circuit that allows for an extended gain, in addition to soft switching (i.e. zero voltage switching for the controlled switches, and zero current switching for the diode). However, the diode zero current switching is utilized by operating the inductor of the auxiliary circuit at the Discontinuous Conduction Mode (DCM) [28]. The proposed design utilizes this single circuit in an interleaved fashion to increase the system's overall allowed voltage and/or

current ratings. However, the system still lacks the advantage of a continuous output current, and thus the same problem of requiring bulky capacitors at the high-voltage side persists. On the other hand, Multi-Level DC-DC converters for high-power applications have also been proposed by different works in the literature. For instance, the authors of [29] presented the analysis of a hybrid topology that combines conventional boost and switched capacitors converters. The main advantages of the proposed topology was the reduced voltage stress across the controlled switch, in addition to the high level of modularity that theoretically allows the aggregation of large number of stages to enhance the voltage gain [29]. Nonetheless, the major drawback of this topology is the large number of used capacitors, and although the rating of individual capacitors for each stage is low, adding them in series to achieve the required high output voltage for grid-connection level with minimal ripples significantly increases the capacitor banks requirements [29], whereas achieving the same ripple levels in conventional Cuk, for instance, requires less capacitance due to its inherent continuous current output. The problem of high-rated capacitors also persists for the aggregated effect of the other system capacitors [29]. A similar topology with the same conversion ratio using the transformer-less design is presented in [30]. The authors also addressed the same disadvantages of the high capacitor requirements. Also, this topology has a higher number of controlled switches than [29], where bi-directional switches are used for each stage. Having said that, the modularity and scalability advantages are evident for the Multi-Level DC-DC converters, whereas the switched capacitors large requirements impose a major constraint on the applications that it can be reliably used to. Consequently, the work presented in [3] proposes different topological variations for high gain DC-DC converters,

based on the conventional non-isolated boost and buck-boost converters. It compares the cascaded and series connections of DC-DC converters in terms of the overall efficiency and performance. Figures 2.2 and 2.3 shows the high level block diagram of both configurations based on [3]. The cascade connection point is from the output of the first converter to the input of the second, that is, the whole input power flows through both converters, on the other hand, a direct parallel-input, series-output connection shorts out the second converter as shown in Figure 2.4 (a). The author of [3] tackled this problem by inverting the second stage input using a unity-gain buck-boost as an auxiliary converter so that the output voltage becomes a summation of the individual converters' output voltages. The modified circuit is shown in Figure 2.4 (b).

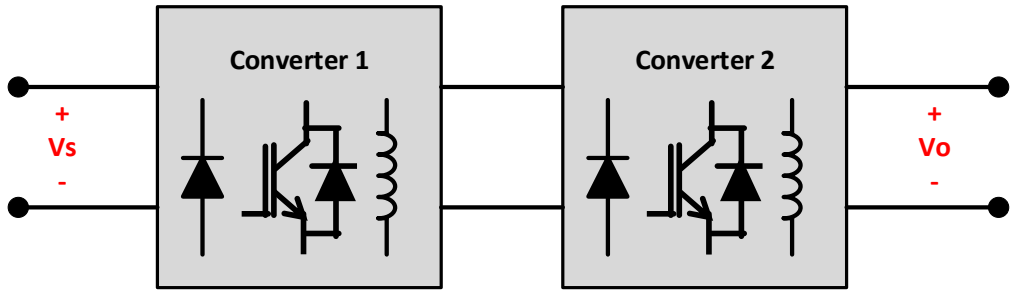


Figure 2.2: High level block diagram of a non-isolated cascaded two-stage DC-DC converter

An overall comparison between the cascaded and series connected boost-converters presented in [3] is shown in Table 2.1. The paper also provides sensitivity analysis in terms of the effects of slight variations in the internal inductors' resistances on the overall gain, and

the results showed that higher variations are present at high duty cycle (D), especially for a high nominal per-unit parasitic resistance values.

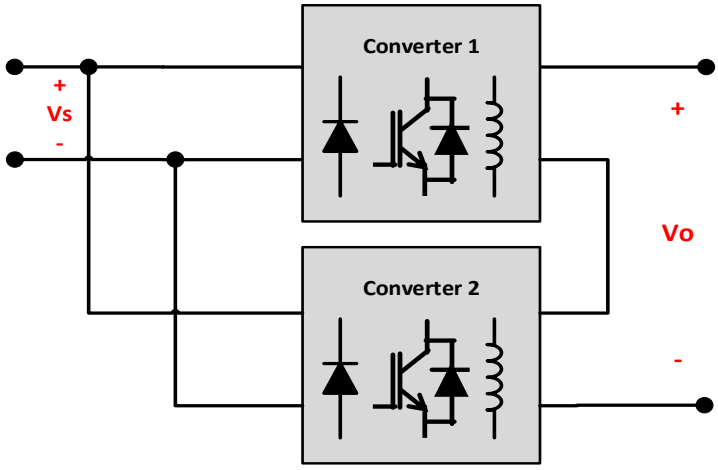
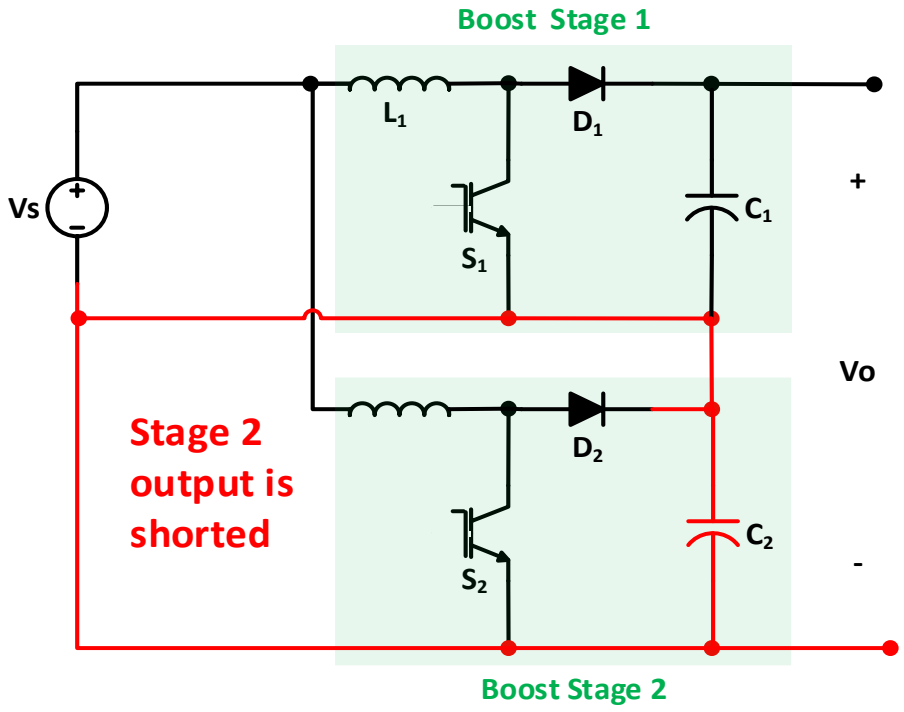


Figure 2.3: High level block diagram of a non-isolated parallel-input, series output two-stage DC-DC converters

The experimental maximum gain for the cascade converters was 29 p.u., compared to 22.5 pu for the series case [3]. Nonetheless, the used converters in [3] still also had the limitation of large filtering capacitor requirements due to the discontinuous current at the output side.

Table 2.1: General Characteristics Comparison between the types of converters presented in [3]

Converter Type	Two-stage Cascaded Boost Converter	Two-stage Series Boost Converter
Ideal Static Gain	$\frac{1}{(1-D)^2}$ (Higher)	$\frac{2}{1-D}$ (Lower)
Diode & Switch Voltage Stress	Stage 1: V_{o1} Stage 2: V_o	Stage 1: $V_o/2$ Stage 2: $V_o/2$
Continuous Input Current	Yes	Stage 1: Yes Stage 2: No
Power-Flow Paths	1 (Higher Ratings)	2 (Lower Ratings)



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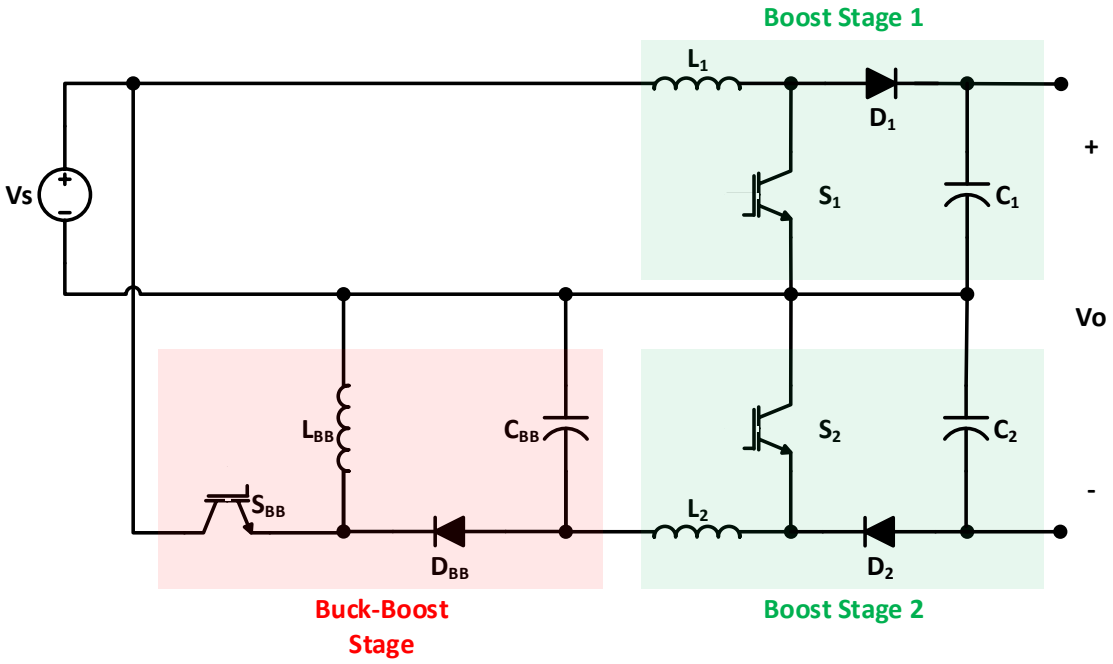


(b)

Figure 2.4: Series Boost Converter (a) direct connection, (b) practical connection

To wrap-up this literature review, the overall system to be incubated in an efficient, high-power DC-DC converter should highlight the requirements summarized in Table 2.2.

Table 2.2: High level requirements for an efficient high-gain, high-power DC-DC converter design.

Category	**Requirement**	**Justification**
Voltage Conversion Ratio	High	Achieve the required high DC levels based on low input voltages
Parasitic Resistances	Minimal	Minimizing the caused gain deterioration at high duty cycles
Total Number of Components & Their Rating	Minimum	Reduce the overall size and cost of the converter
Switches/Diodes Voltage Stress	Minimum	Minimize the switching losses
Switching Techniques	Soft Switching	Minimize the switching losses
Input/Output Current	Continuous	Minimize current ripples, with LV & HV bulky capacitors' requirements

Based on the aforementioned requirements and presented data in Table 1.1 and Table 2.2, Cuk and SEPIC converters were selected as the cores of two different designs that are to be compared at the end based on both theoretical and practical basis. The adopted topologies will be a cascade and series connection of both converters individually, with the auxiliary buck-boost converter in the series case, similar to [3].

Chapter 3 : Design Methodology:

The topologies to be studied in details throughout this thesis are divided into four main categories. Those are:

1) Cascaded Two-stage Cuk Converter
2) Cascaded Two-stage SEPIC Converter
3) Series Two-stage Cuk Buck-Boost Converter
4) Series Two-stage SEPIC Buck-Boost Converter

Figures 3.1 through 3.4 show the four different topologies with their ideal components. Nevertheless, an accurate representation would have to take the circuit non-idealities into account. Thus, a detailed modeling of each converter (Cuk, SEPIC and Buck-Boost) is presented in later chapters, where it takes the following non-idealities into account:

1) Parasitic Inductors Resistance r_L
2) Equivalent Series Resistance (ESR) of the capacitors r_C
3) On-State resistance of the controlled switches r_s
4) On-State resistance of the diodes r_d

The switching losses and forward bias voltage of both controlled switches and diodes are neglected here since it is assumed that a full-scale high-voltage, high-power practical implementation would utilize soft-switching techniques, in addition to the fact that forward bias voltages are negligible compared to the application's rated voltages.

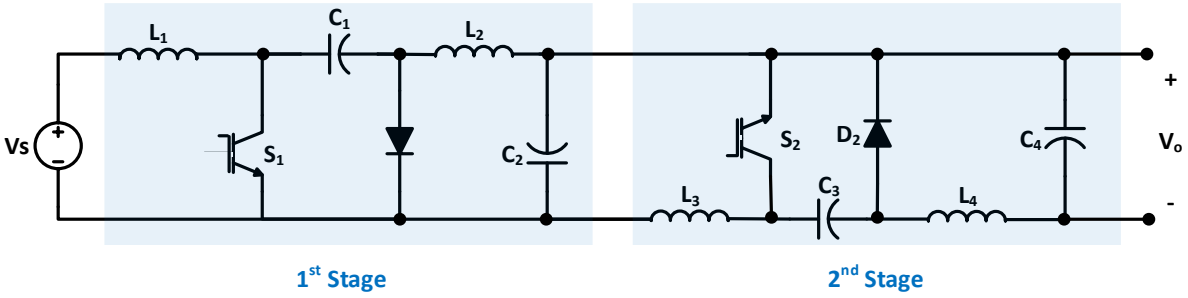


Figure 3.1: Two-Stage Cascaded Cuk DC-DC Converter

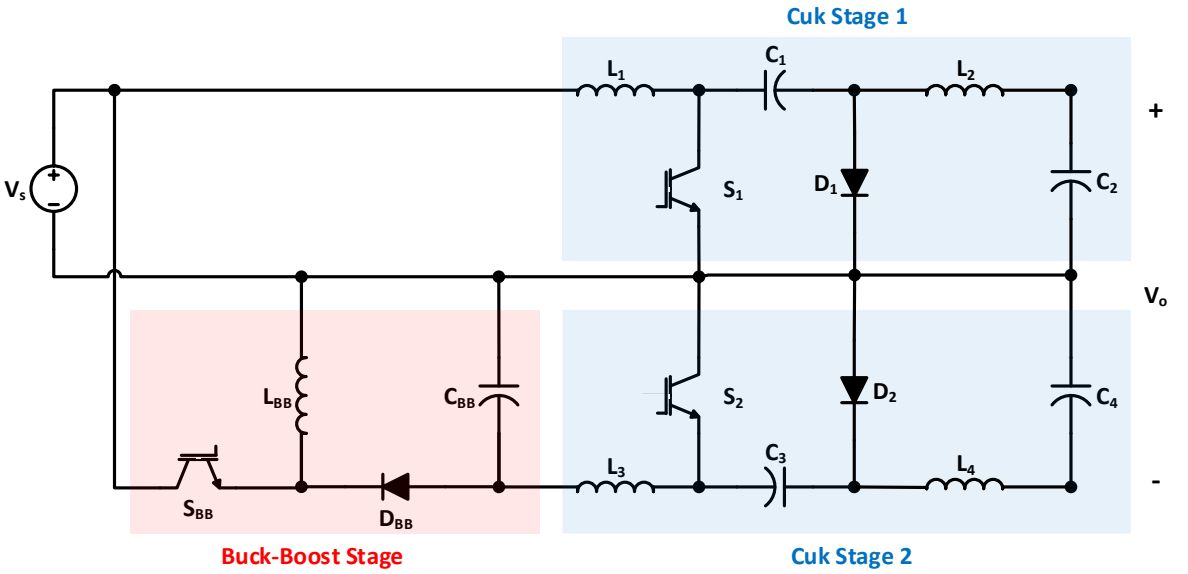


Figure 3.2: Two-Stage Series Cuk Buck-Boost DC-DC Converter

Once these models are derived, their corresponding output/input transfer relations are obtained on an individual basis, indicating the practical gain deteriorations at high duty cycles that are usually associated with the high conversion ratio applications. Additionally, small-signal models of Cuk & SEPIC are derived as well as a practical verification for their

derived transfer relations on an individual basis. This will be followed by applying the derived models on the high-gain, high-power DC-DC converter configurations shown in the Figures 3.1 to 3.4 in order to assess their theoretical efficiency and performance with the modeled non-idealities. Sensitivity analysis is also performed on the four different configurations based on slight possible operational variations in the parasitic inductor resistance r_L. Each of the four different topologies is practically implemented on a scaled-down prototype to verify its operating principle and predicted efficiencies across a wide duty-cycle operational range, followed by a projection of the coming results on the high-power real life applications.

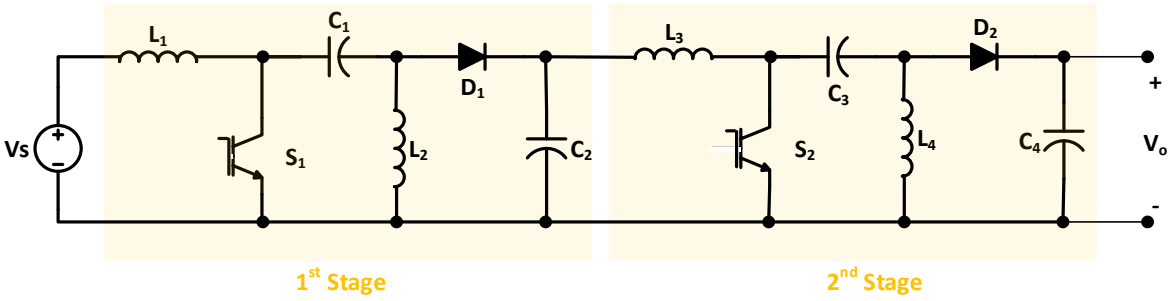


Figure 3.3: Two-Stage Cascaded SEPIC DC-DC Converter

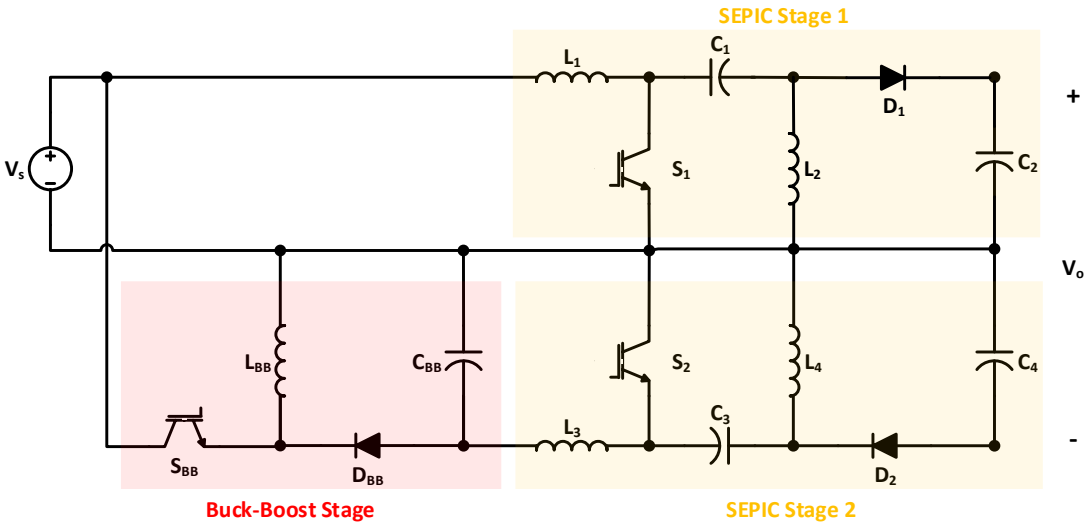


Figure 3.4: Two-Stage Series SEPIC Buck-Boost Converter

Chapter 4 : Modelling of DC-DC Converters

In this chapter, the modeling steps are first presented, then the detailed models of Cuk, SEPIC and Buck-Boost converters are derived. The simulation results of all converters are presented, followed by the practical results of both Cuk and SEPIC to practically verify the derived models and their performance. To start with, the mathematical modelling of DC-DC converters is usually done using State-Space representation, which is represented by the following equations:

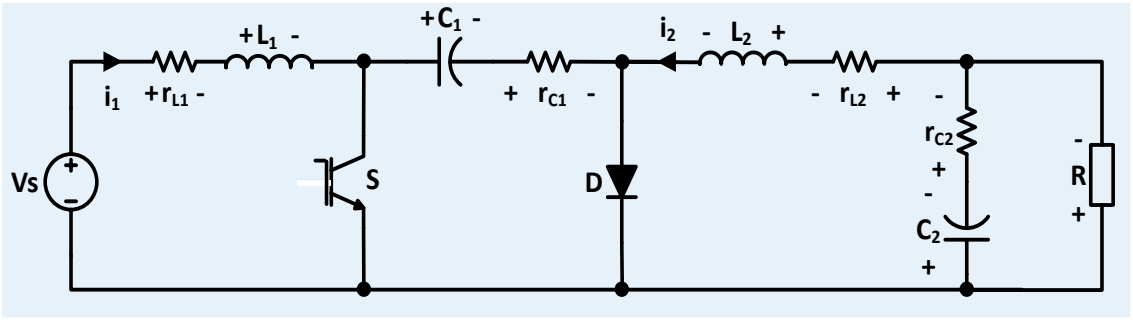
$$\dot{x} = Ax + Bu \tag{4.1a}$$

$$y = Cx + D_f u \tag{4.1b}$$

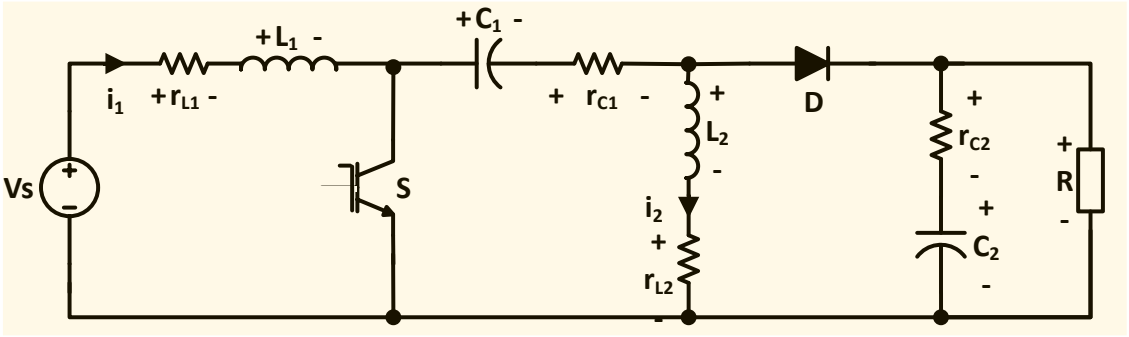
However, it is difficult to directly accomplish such representation to describe the whole system due to the switching nature of the DC-DC converters. That is, the resulting model in terms of system dynamics when the switch is on is completely different than the one resulting when it is off. Thus, an average model is achieved by first obtaining the two models separately, and then combining them using state space averaging method, which considers the weight of each mode of operation on the total duty cycle (*d*). Where *d* is defined as the ratio of the switch-on time to the switching period. This notion will be denoted as *d* throughout this chapter to include the perturbation part as shall be discussed later, whereas it is denoted as *D* otherwise to indicate steady state operation. Thus, the state space averaged model can be expressed as follows:

$$X_{avg} = dX_{on} + (1 - d)X_{off} \tag{4.2}$$

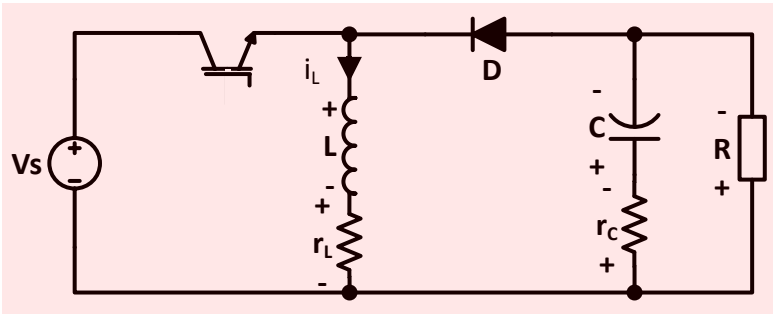
In terms of the considered circuit's non-idealities, Figure 4.1 shows the three converters with the added parasitic elements.



(a)



(b)



(c)

Figure 4.1: Converter topology considering the non-idealities: (a) Cuk, (b) SEPIC and (c) Buck-Boost

Since both Cuk and SEPIC converters are of fourth order, the number of states required to represent the system dynamics at any given switching state is also four, whereas this number is reduced to 2 for the second order Buck-Boost. In terms of the converters' gains, the ideal transfer relation between the input and output voltage for all the three converters in terms of the absolute value is given by:

$$\frac{v_o}{v_s} = \frac{d}{1-d} \tag{4.3}$$

However, this relation does not take into account the given non-idealities, meaning that a more accurate formulation should be obtained from the derived models using state space equations. That is, and under the desirable steady state operating conditions, the changes in the state variables are negligible and can be approximated to zero, and thus (4.1a) can be equated to zero as well. Consequently, and taking into account that the system input u is the input voltage v_s and its output y is the output voltage v_o, the following relations can be obtained:

$$Ax + Bu = 0 \tag{4.4a}$$

$$\frac{v_o}{v_s} = \frac{y}{u} = -CA^{-1}B \tag{4.4b}$$

Small signal models are derived for both Cuk and SEPIC in order to analyze the effects of small input perturbations on the converters overall performance and stability, and to form the basis of designing control systems that can be considered as part of this thesis's future work. The variations covered by these small signal models are usually considered for the input voltage and the duty cycle. For that, the system has to be first linearized using, for instance,

the Multivariable Taylor's Series First Order Approximation, in order to split the nonlinear terms. Consequently, all the states in addition to the input voltage and duty cycle are replaced in the state equations with a new term, including their DC operating values, denoted in capital letters, added to a perturbation term in order to develop the small signal model that mainly depends on the perturbations. Table 4.1 illustrates these substitutions.

Table 4.1: System variables with their perturbation terms

Common Parameters	**Cuk & SEPIC**	
$d = D + \delta d$	$i_1 = I_1 + \delta i_1$	$i_2 = I_2 + \delta i_2$
	$v_{C1} = V_{C1} + \delta v_{C1}$	$v_{C2} = V_{C2} + \delta v_{C2}$
	Buck-Boost	
$v_S = V_S + \delta v_s$	$i_L = I_L + \delta i_L$	$v_C = V_C + \delta v_C$

Consequently, Taylor Series multivariate 1st order approximation around the equilibrium operating point for Cuk and SEPIC is found by:

$$f(i_1, i_2, v_{C1}, v_{C2}, d, v_s) \approx f(I_1, I_2, V_{C1}, V_{C2}, D, V_S) + \frac{\partial f}{\partial i_1}|_{eqb}.\delta i_1 + \frac{\partial f}{\partial i_2}|_{eqb}.\delta i_2 + \frac{\partial f}{\partial v_{C1}}|_{eqb}.\delta v_{C1} + \frac{\partial f}{\partial v_{C2}}|_{eqb}.\delta v_{C2} + \frac{\partial f}{\partial (d)}|_{eqb}.\delta d + \frac{\partial f}{\partial v_S}|_{eqb}.\delta v_s \quad (4.5a)$$

Where $f(i_1, i_2, v_{C1}, v_{C2}, d, v_s)$ here represents the disturbance term of the differential of any state (e.g. $f_1 = \frac{\partial \delta i_1}{\partial t}$ for the input inductor current), and "eqb" denotes the equilibrium

conditions selected for the specific design. For simplicity, the Taylor approximation is denoted as follows:

$$f(i_1, i_2, v_{C1}, v_{C2}, d, v_s) \approx E + U + G + H + J + K + M \tag{4.5b}$$

Where E is zero for all the states it represents the steady state term, whereas the terms from U to J are the same terms as in the original averaged matrix, however, substituted with the steady state values multiplied by the perturbation term here instead of the state as a whole. The same also applies to M since it is the term representing the input voltage which also exists in the averaged system matrices. K, on the other hand, requires the partial differentiation of all state equations at their equilibrium points to get the split duty cycle perturbation terms that would eventually be used as a system input.

4.1. Modelling of Cuk Converter

4.1.1. Non-ideal State-Space Model:

When the switch is triggered, it is ideally replaced with a short circuit, however, it is replaced here with its internal resistance r_s. Consequently, the diode is off since the cathode potential is greater than the anode's. The state space representations can then be obtained as follows:

$$\frac{di_1}{dt} = \frac{v_{L1}}{L_1} = \frac{-\alpha_1}{L_1} i_1 - \frac{-r_s}{L_1} i_2 + \frac{1}{L_1} v_s \tag{4.6a}$$

$$\frac{di_2}{dt} = \frac{-r_s}{L_2} i_1 - \frac{(\alpha_2 + \alpha_3)}{L_2}\ i_2 + \frac{1}{L_2} v_{C1} + \frac{(\alpha_4 - 1)}{L_2} v_{C2} \tag{4.6b}$$

$$\frac{dv_{C1}}{dt} = -\frac{1}{C_1} i_2 \tag{4.6c}$$

$$\frac{dv_{C2}}{dt} = \frac{\alpha_5}{C_2} i_2 - \frac{\alpha_5}{RC_2} v_{C2} \tag{4.6d}$$

The converter's output voltage is also represented in terms of the given states, since it is considered here as the state-space system output y defined in (4.4) :

$$v_O = v_{C2} + ic_2 rc_2 = \alpha_2 i_2 + (1 - \alpha_4) v_{C2} \tag{4.6e}$$

Where α_i in this context are constants used to represent combinations of the parasitic resistance terms, and are defined as follows:

$$\alpha_1 = r_{L1} + r_s \tag{4.7a}$$

$$\alpha_2 = \frac{r_{c2} R}{R + r_{C2}} \tag{4.7b}$$

$$\alpha_3 = r_{C1} + r_{L2} + r_s \tag{4.7c}$$

$$\alpha_4 = \frac{\alpha_2}{R} \tag{4.7d}$$

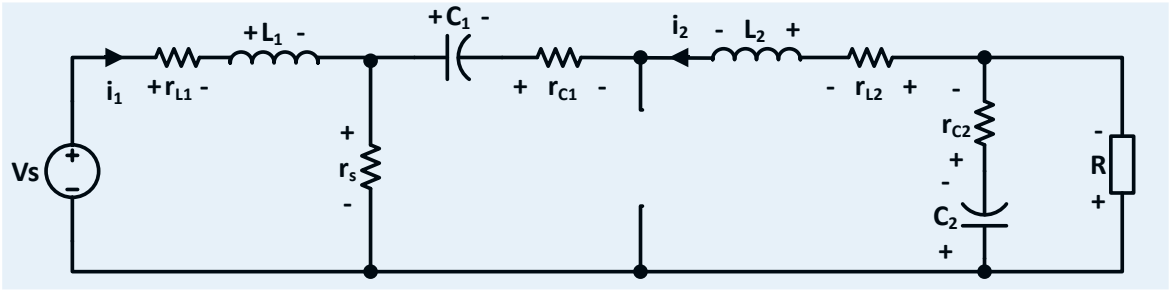
$$\alpha_5 = \frac{\alpha_2}{r_{C2}} \tag{4.7e}$$

Thus, and by using the state space representation for the on-state model, the system matrices can be defined as:

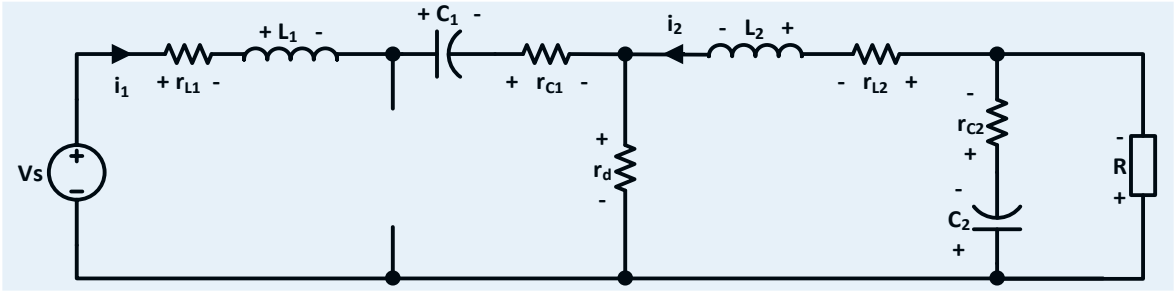
$$\begin{bmatrix} \dot{\imath}_{1on} \\ \dot{\imath}_{2on} \\ \dot{v}_{C1on} \\ \dot{v}_{C2on} \end{bmatrix} = \begin{bmatrix} \frac{-\alpha_1}{L_1} & \frac{-r_s}{L_1} & 0 & 0 \\ \frac{-r_s}{L_2} & \frac{-(\alpha_2 + \alpha_3)}{L_2} & \frac{1}{L_2} & \frac{(\alpha_4 - 1)}{L_2} \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{\alpha_5}{C_2} & 0 & \frac{-\alpha_5}{RC_2} \end{bmatrix} \begin{bmatrix} i_{1on} \\ i_{2on} \\ v_{C1on} \\ v_{C2on} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{4.8a}$$

$$v_{o_{on}} = [0 \quad \alpha_2 \quad 0 \quad (1-\alpha_4)] \begin{bmatrix} i_{1on} \\ i_{2on} \\ v_{C1on} \\ v_{C2on} \end{bmatrix} \tag{4.8b}$$

Figure 4.2 shows the non-ideal Cuk converter in both on and off states topologies.



(a)



(b)

Figure 4.2: Cuk converter topology when the switch is: (a) on, (b) off

As for the off-state model, the same steps are repeated. Here, the switch is off and thus the diode is on. This causes the system dynamics to alter resulting into the following state space equations:

$$\begin{bmatrix} \dot{\imath}_{1off} \\ \dot{\imath}_{2off} \\ \dot{v}_{C1off} \\ \dot{v}_{C2off} \end{bmatrix} = \begin{bmatrix} \frac{-\alpha_6}{L_1} & \frac{-r_d}{L1} & \frac{-1}{L_1} & 0 \\ \frac{-r_d}{L_2} & \frac{-(\alpha_2+\alpha_7)}{L_2} & 0 & \frac{(\alpha_4-1)}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{\alpha_5}{C_2} & 0 & \frac{-\alpha_5}{RC_2} \end{bmatrix} \begin{bmatrix} i_{1off} \\ i_{2off} \\ v_{C1off} \\ v_{C2off} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{4.9a}$$

$$v_{o_{off}} = [0 \quad \alpha_2 \quad 0 \quad (1-\alpha_4)] \begin{bmatrix} i_{1off} \\ i_{2off} \\ v_{C1offff} \\ v_{C2off} \end{bmatrix} \tag{4.9b}$$

Using (4.2), the averaged state space model is represented as:

$$\dot{x} = A_{avg}x + B_{avg}u \tag{4.10a}$$

$$y = C_{avg}x + D_{f_{avg}}u \tag{4.10b}$$

Where:

$$A_{avg} = \begin{bmatrix} \frac{d(\alpha_6-\alpha_1)-\alpha_6}{L1} & \frac{r_d(d-1)-r_s}{L_1} & \frac{d-1}{L_1} & 0 \\ \frac{d(r_d-r_s)-r_d}{L_2} & \frac{\alpha_8}{L_2} & \frac{d}{L_2} & \frac{-\alpha_3}{L_2} \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & 0 & 0 \\ 0 & \frac{\alpha_5}{C_2} & 0 & \frac{-\alpha_5}{RC_2} \end{bmatrix} \tag{4.10c}$$

$$B_{avg} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T \tag{4.10d}$$

$$C_{avg} = [0 \quad \alpha_1 \quad 0 \quad 1-\alpha_4] \tag{4.10e}$$

Using this derived model, the modified input/output relation is obtained from (4.4) as follows:

$$\frac{V_o}{V_s} = -\frac{R(d-d^2)}{\alpha_9 d^2 + \alpha_{10} d + \alpha_{11}} \tag{4.11}$$

The rest of $\alpha_i's$ are listed as:

$$\alpha_6 = r_{C1} + r_{L1} + r_d \tag{4.12a}$$

$$\alpha_7 = r_{L2} + r_d \tag{4.12b}$$

$$\alpha_8 = -(\alpha_2 + \alpha_3)d + (\alpha_2 + \alpha_7)(d-1) \tag{4.12c}$$

$$\alpha_9 = R + r_{L1} + r_{L2} - r_{C1} \tag{4.12d}$$

$$\alpha_{10} = r_s - r_d + r_{C1} - 2r_{L2} - 2R \tag{4.12e}$$

$$\alpha_{11} = R + \alpha_7 \tag{4.12f}$$

4.1.2. Small Signal Model

The elements U through M in (4.5b) were obtained for each of the states as well as the output voltage, and the resulting small signal model was as follows:

$$\begin{bmatrix} \dot{\delta i_1} \\ \dot{\delta i_2} \\ \dot{\delta v_{C1}} \\ \dot{\delta v_{C2}} \end{bmatrix} = \begin{bmatrix} U_1 & G_1 & H_1 & J_1 \\ U_2 & G_2 & H_2 & J_2 \\ U_3 & G_3 & H_3 & J_3 \\ U_4 & G_4 & H_4 & J_4 \end{bmatrix} \begin{bmatrix} \delta i_1 \\ \delta i_2 \\ \delta v_{C1} \\ \delta v_{C2} \end{bmatrix} + \begin{bmatrix} K_1 & M_1 \\ K_2 & M_2 \\ K_3 & M_3 \\ K_4 & M_4 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{v_s} \end{bmatrix} \tag{4.13a}$$

$$\delta v_o = [U_5 \quad G_5 \quad H_5 \quad J_5]\,[\delta i_1 \quad \delta i_2 \quad \delta v_{C1} \quad \delta v_{C2}]^T \tag{4.13b}$$

Where matrix A and C are comparable to those in (4.10), as well as the 2nd column of the B matrix. However, the terms K_1 through K_4 are found using (4.5) as:

$$K_1 = \frac{\partial f_1}{\partial d}|_{eqb}.\hat{d} = \frac{(r_d + r_{C1} - r_s)I_1 + (r_d - r_s)I_2 + V_{C1}}{L_1}\,\delta d \tag{4.14a}$$

$$K_2 = \frac{(r_d - r_s)I_1 + (r_d - r_{C1} - r_s)I_2 + V_{C1}}{L_2}\,\delta d \tag{4.14b}$$

$$K_3 = \frac{-I_1 - I_2}{C_1}\,\delta d \tag{4.14c}$$

$$K_4 = 0 \tag{4.14d}$$

The small signal model defined in (4.13) can be transformed to its transfer function equivalent with respect to any input in order to test the model response at any operating point in CCM.

4.2. Modelling of SEPIC Converter

4.2.1. Non-ideal State-Space Model

Similar to what has been done with the Cuk converter, the analysis would begin with the on-state, then the off-state followed by the averaged model. When the switch is on, the state space representations can then be obtained as follows:

$$\begin{bmatrix} \dot{\imath}_{1on} \\ \dot{\imath}_{2on} \\ \dot{v}_{C1on} \\ \dot{v}_{C2on} \end{bmatrix} = \begin{bmatrix} -\frac{\alpha_7}{L1} & -\frac{r_s}{L_1} & 0 & 0 \\ -\frac{r_s}{L_2} & -\frac{\alpha_4}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{\alpha_3}{RC_2} \end{bmatrix} \begin{bmatrix} i_{1on} \\ i_{2on} \\ v_{C1on} \\ v_{C2on} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{4.15a}$$

$$v_{o_{on}} = [0 \quad 0 \quad 0 \quad (1-\alpha_2)] \begin{bmatrix} i_{1on} \\ i_{2on} \\ v_{C1on} \\ v_{C2on} \end{bmatrix} \tag{4.15b}$$

When the switch is off, the system dynamics alter in a fashion that produces the following state equations:

$$\begin{bmatrix} \dot{\imath}_{1off} \\ \dot{\imath}_{2off} \\ \dot{v}_{C1off} \\ \dot{v}_{C2off} \end{bmatrix} = \begin{bmatrix} -\frac{\alpha_1+\alpha_4}{L1} & -\frac{\alpha_1+r_D}{L_1} & -\frac{1}{L_1} & -\frac{(1-\alpha_2)}{L_1} \\ -\frac{r_D+\alpha_1}{L_2} & -\frac{\alpha_1+\alpha_6}{L_2} & 0 & -\frac{(1-\alpha_2)}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{\alpha_3}{C2} & \frac{\alpha_3}{C2} & 0 & -\frac{\alpha_3}{RC_2} \end{bmatrix} \begin{bmatrix} i_{1off} \\ i_{2off} \\ v_{C1off} \\ v_{C2off} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{4.16a}$$

$$v_{o_{off}} = [\alpha_1 \quad \alpha_1 \quad 0 \quad (1-\alpha_2)] \, [i_{1off} \quad i_{2off} \quad v_{C1off} \quad v_{C2off}]^T \tag{4.16b}$$

Similar to what has been done with Cuk Converter, the averaged state space model is derived as follows:

$$A_{avg} = \begin{bmatrix} \frac{(\alpha_1+\alpha_4)(d-1)-(\alpha_9)d}{L_1} & \frac{\alpha_{12}}{L_1} & \frac{d-1}{L_1} & \frac{\alpha_3(d-1)}{L_1} \\ \frac{(r_D+\alpha_1)(d-1)-r_s d}{L_2} & \frac{\alpha_{13}}{L_2} & \frac{d}{L_2} & \frac{\alpha_3(d-1)}{L_2} \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & 0 & 0 \\ \frac{\alpha_3(1-d)}{C_2} & \frac{\alpha_3(1-d)}{C_2} & 0 & -\frac{\alpha_3}{RC_2} \end{bmatrix} \tag{4.17a}$$

$$B_{avg} = \left[\frac{1}{L_1} \quad 0 \quad 0 \quad 0\right]^T \tag{4.17b}$$

$$C_{avg} = [\alpha_1(1-d) \quad \alpha_1(1-d) \quad 0 \quad (1-\alpha_2)] \tag{4.17c}$$

Where α_{12} and α_{13} also represent parasitic resistance terms defined as:

$$\alpha_{12} = (\alpha_2 + \alpha_7)(d-1) - \alpha_3 d \tag{4.18a}$$

$$\alpha_{13} = (\alpha_2 + r_d)(d-1) - r_s d \tag{4.18b}$$

Similar expression to that shown in (4.11) can be derived for SEPIC converter using the same formulation.

4.2.2. Small-Signal Model

The SEPIC small signal model follows the same rules as Cuk model. Consequently, the terms K_1 through K_4 are found for SEPIC in a similar fashion as follows:

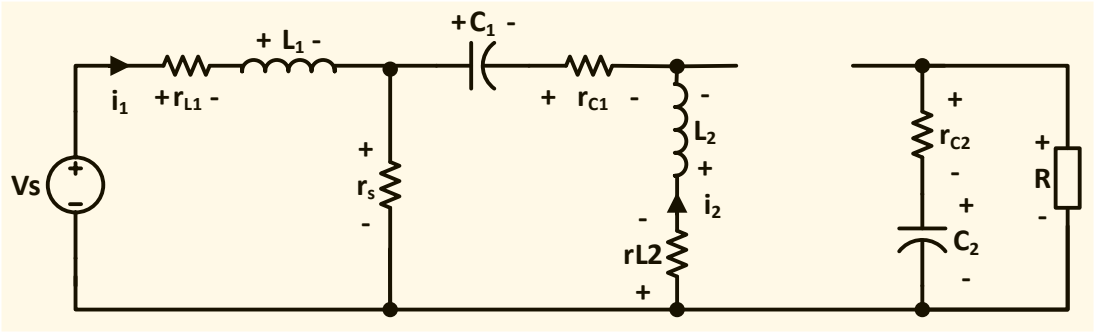
$$K_1 = \frac{(r_{C1} + r_D - r_s + \alpha_1)I_1 + (r_D - r_S + \alpha_1)I_2 + V_{C1} + (1-\alpha_2)V_{C2}}{L_1}.\delta d \tag{4.19a}$$

$$K_2 = \frac{(r_D - r_S + \alpha_1)I_1 + (r_D - r_s - r_{C1} + \alpha_1)I_2 + V_{C1} + (1-\alpha_2)V_{C2}}{L_2}.\delta d \tag{4.19b}$$

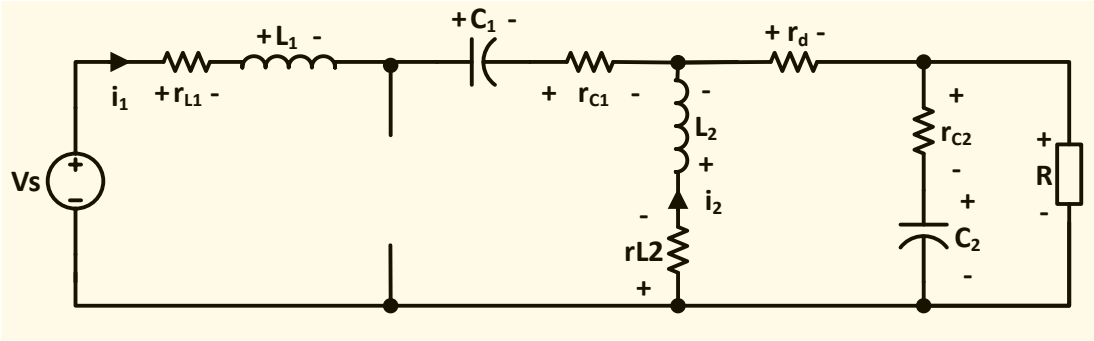
$$K_3 = \frac{-I_1 - I_2}{C_1}.\delta d \tag{4.19c}$$

$$K_4 = -\frac{\alpha_3(I_1 + I_2)}{RC_2}.\delta d \tag{4.19d}$$

Again, the obtained small signal model can then be transformed to transfer function form to test its response at different operating points. Figure 4.3 shows the topological variations in SEPIC converter when the switch is on or off.



(a)



(b)

Figure 4.3: SEPIC converter topology when the switch is: (a) on, (b) off

4.3. Modelling of Buck-Boost Converter

4.3.1. Non-Ideal State-Space Model:

As a second order converter, a state-space representation of the buck-boost converter is based on two states. Namely, inductor current and capacitor voltage. Nevertheless, the deriving methodology is very similar to what has been done with Cuk and SEPIC converter. The state space representation of the non-ideal buck-boost model is only to be derived here for the purpose of assessing its parasitic elements effect on the overall gain of the series Cuk and SEPIC configurations as an auxiliary converter. That is, a separate practical confirmation

and a small-signal model are not derived specifically for this converter as they are out of the scope of this thesis. Moving on, the on-state representation is derived as follows when the switch is on:

$$\begin{bmatrix} \dot{\imath_{Lon}} \\ \dot{v_{Con}} \end{bmatrix} = \begin{bmatrix} -\frac{r_L + r_s}{L} & 0 \\ 0 & -\frac{1}{C(R + r_C)} \end{bmatrix} \begin{bmatrix} i_{Lon} \\ v_{Con} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s \tag{4.20a}$$

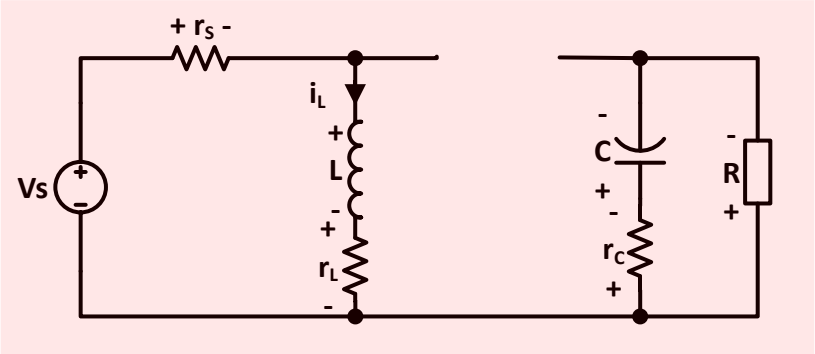
$$v_{o_{on}} = [0 \quad 1 - \alpha_2] \begin{bmatrix} i_{Lon} \\ v_{Con} \end{bmatrix} \tag{4.20b}$$

Figure 4.4 shows the difference between the on-state and off-state topologies for a non-ideal Buck-Boost converter. In terms of the off-state, the state space representation is derived as:

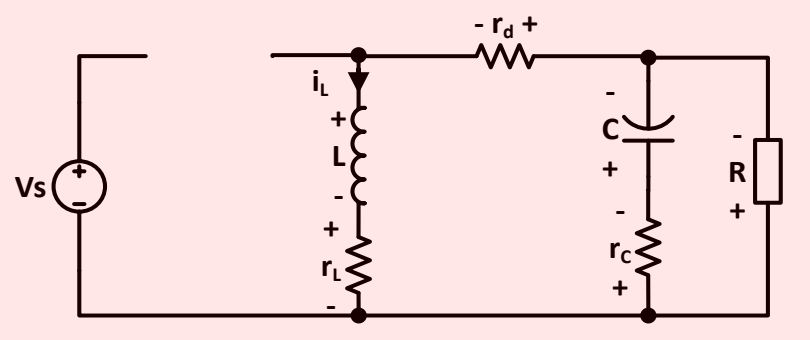
$$\begin{bmatrix} \dot{\imath_{Loff}} \\ \dot{v_{Coff}} \end{bmatrix} = \begin{bmatrix} -\frac{r_L + r_d + \alpha_2{}'}{L} & \frac{\alpha_4{}' - 1}{L} \\ \frac{\alpha_5{}'}{C} & -\frac{1}{C(R + r_C)} \end{bmatrix} \begin{bmatrix} i_{Loff} \\ v_{Coff} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s \tag{4.21a}$$

$$v_{o_{off}} = [\alpha_2{}' \quad 1 - \alpha_5{}'] \begin{bmatrix} i_{Loff} \\ v_{Coff} \end{bmatrix} \tag{4.21b}$$

Where $\alpha_i{}'$ represents the same coefficients as the ones mentioned above, however, replacing r_{C2} with r_C since buck-boost's output capacitor is the only one in this topology. Consequently, the averaged state-space matrices and the output/input transfer relation for this converter can be found in a similar manner using (4.2) and (4.4).



(a)



(b)

Figure 4.4: Buck-Boost converter topology when the switch is: (a) on, (b) off

4.4. Practical Verification of the Derived Models

The derived models' performance was compared against the ideal one for both Cuk and SEPIC converters both theoretically and practically. The maximum testing power rating was selected to be in the range of ~100W for safety considerations. However, the selected components were maintained to withstand high-power ratings in order to utilize their parasitic resistances. Nevertheless, the input/output results are expected to have similar trends. For the selected ratings, and with a combined 12V input, Table 4.2 shows the selected

components with their parasitic resistances, where the chosen values guarantee a CCM operation across the whole testing spectrum extended from a duty cycle of 0.6 to 0.85, with the PWM signals being generated through the eZDSP F28335 board. The parasitic resistance values are obtained from components datasheets throughout this thesis. Having said that, these values usually exhibit slight operational variations based on the specific operating point of the component, which introduces a source of measurement error, added to the tolerance of the used measuring devices. Collectively, these errors, even with small magnitudes, may slightly amplify the differences between theoretical predictions and practical results.

Table 4.2: Components with their corresponding parasitic resistance

Component Type	**Part Number**	**Value/Rating**	**~ Parasitic R (mΩ)**
Inductor	Hammond 195C30	1 mH	9
Capacitor	ECOS2WB221CA	$220\ \mu F$	264
Diode	APT10SCD120B	1200 V	50
IGBT	FGL60N100BNTD	1000 V	12

On the theoretical side, the derived transfer relations were compared to the ideal ones for both converters by plotting their gain vs. duty cycle. The components' values from Table 4.2 were used in this theoretical comparison, as well as their parasitic resistances, whereas load resistance R was fixed at 90 Ω, which is the same value used in the practical testing. Figure 4.5 shows the comparison results for both Cuk and SEPIC converters, where the ideal model

gain tends to infinity as the duty cycle approaches unity. However, and for the given parameters, the maximum gains obtained by Cuk and SEPIC using the derived models with the given theoretical parasitic parameters were ~18 and ~17, respectively, before falling back to zero at unity. On the other hand, the maximum gain would further deteriorate if a lower load value R was used with the same parasitic components (i.e. higher per unit parasitic resistances defined by the ratio between the Ohmic parasitic to the load resistances). This idea will be discussed in more details in later chapters. The results were also confirmed via the small signal model transfer functions by subjecting it to a step input of 2V and observing the output response, where a moderate duty cycle of 0.7 resulted of both ideal and non-ideal models converging to almost the same value, whereas the response differed at higher values of D such as 0.9.

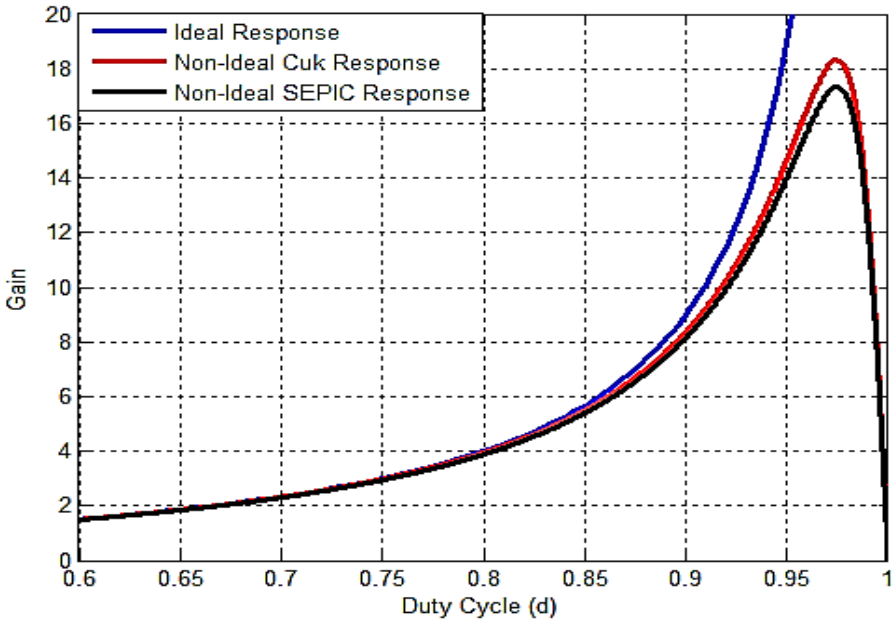
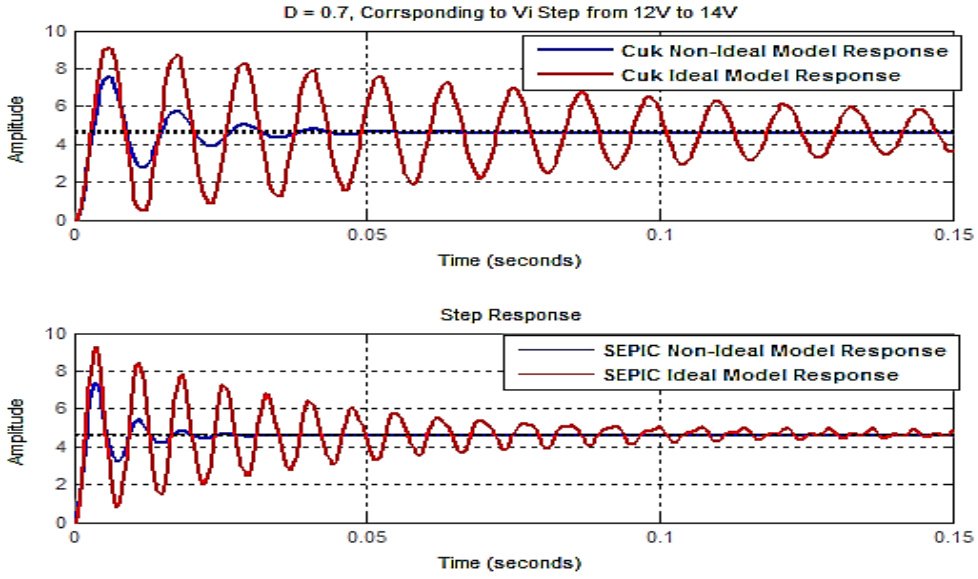
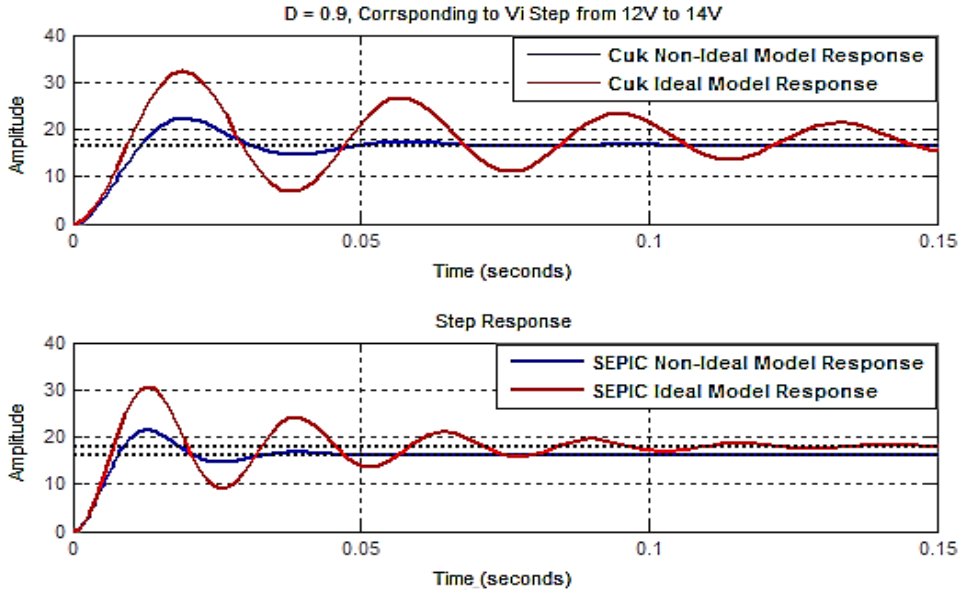


Figure 4.5: Gain Vs. Duty Cycle for both Cuk and SEPIC converters using the given parameters

Figure 4.6 illustrates this comparison, where the stability superiority for the non-ideal responses are also evident due to the damping effect of the parasitic elements consideration. On the practical implementation side, the performance of each converter is evaluated and compared to the theoretical calculations, where the output voltage is measured for multiple duty cycles to verify the trends shown in Figure 4.5. A constant switching frequency of 25 KHz was practically used and the output voltage for both converters were measured at the selected duty cycles with a constant input voltage of 12 V.



(a)



(b)

Figure 4.6: Step Response of Ideal and Theoretically Derived models for both Cuk and SEPIC responses at (a) D = 0.7, (b) = 0.9

The experimental setup is shown in Figure 4.7 whereas the practical data from the model of both converters are shown in Figure 4.8. The results show the similar trend between the practical and theoretical models, although the gain gap increases between the ideal and practical models as d increases further, which is mainly due to the differences and variations in the parasitic resistances of the practical setup compared to the derived theoretical models. In addition, accounting for the voltage drops across the used switches which were neglected in the derived model may have affected the gain practically. Also, a steady gap is attributed to the hard-switching of the IGBT with a relatively high switching frequency of 25 KHz, which also contributed to an increase in the neglected switching losses in the models based on the given assumptions in chapter 3.

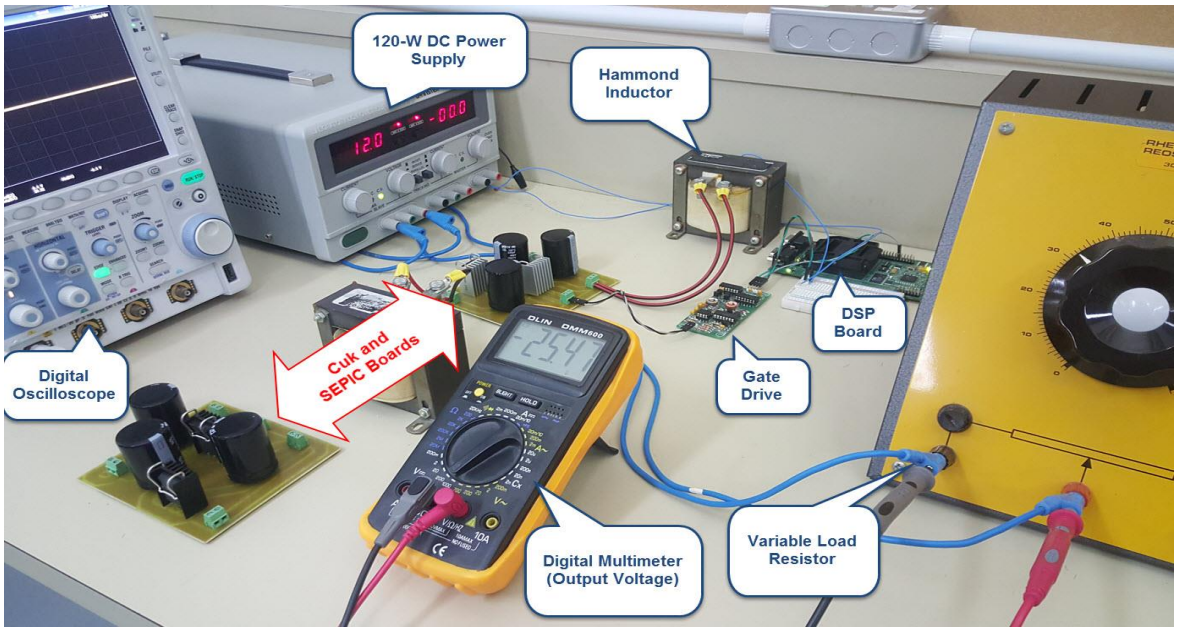


Figure 4.7: Cuk and SEPIC Experimental Testing Setup

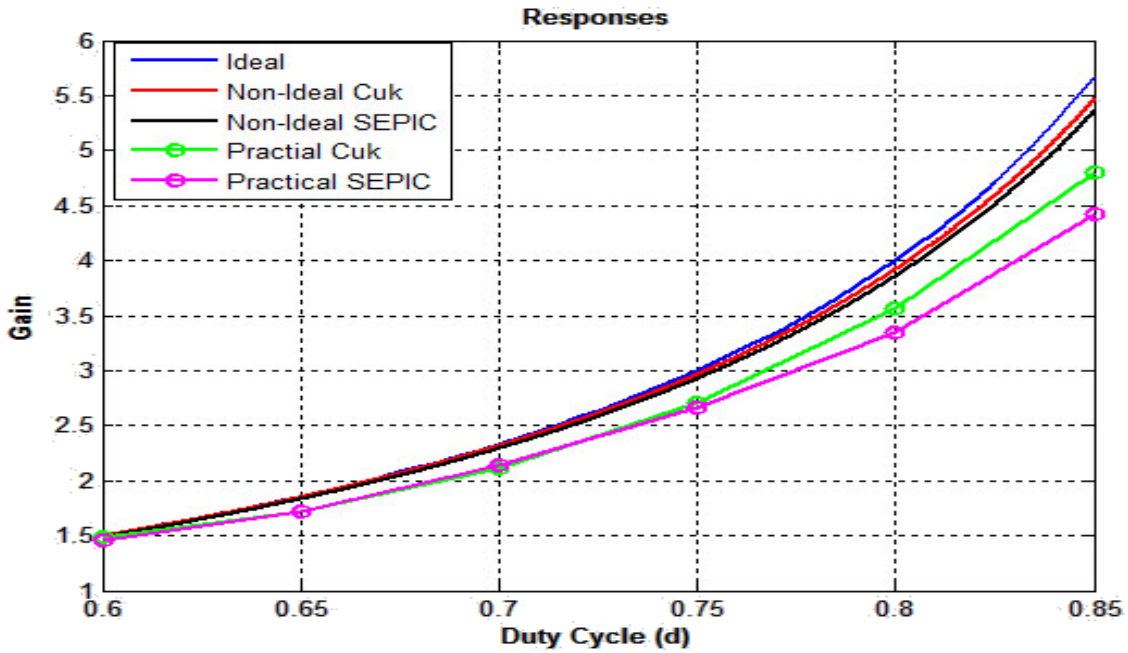


Figure 4.8: Gain Vs. Duty Cycle for the ideal, non-ideal and practical models' results for both Cuk and SEPIC converters

Chapter 5 : Gain and Efficiency Assessment of the Proposed High Gain DC-DC Converters

In this chapter, the derived models are used to assess and compare the overall efficiency of the four different proposed circuit topologies, in addition to the maximum theoretical achievable gains based on a given set of parasitic parameters. The comparison are first cover the two-stage cascaded Cuk and SEPIC topologies, followed by their series counterparts. After that, practical verification of the model trends is presented, followed by an overall assessment for a theoretical 1-MW HVDC application for PV systems.

5.1. Efficiency Derivations of the Proposed Topologies

5.1.1. Two-stage Cascade Connected Converters (Cuk or SEPIC)

As stated previously, cascade connection of DC-DC converters implies connecting the input of the second converter to the output of the first. Thus, the second converter input voltage is scaled from the first by its gain factor. That is, if both converters' switching actions are controlled by the same duty cycle, which will be the assumed case throughout this thesis, then the two-stage output is ideally the square of a single converter individual gain. Notice that for Cuk converter, the switches and capacitor polarities in Figure 3.1 are reversed for the second stage since its input is negative, and thus it shares the non-negative output property with SEPIC. Consequently, the output polarity of both configurations is positive. As for the efficiency assessment part, an ideal converter would always employ an ideal efficiency (i.e. 100%), independent of the duty cycle value. However, and using the derived output to input

voltage transfer relation shown in (10), the theoretical efficiency of a non-ideal cascaded Cuk or SEPIC converter can be obtained considering the parasitic elements of each stage. Generally, the overall gain of a non-ideal transfer relation for such converter is expressed as:

$$\frac{V_o}{V_s} = G_1 G_2 \tag{5.1}$$

Where the terms G_1 and G_2 are not identical and individually dependent on the parasitic elements of each stage separately. As for the efficiency, it can be approximated by dividing the practical gain on the ideal one, keeping in mind that such approximation may result into an over-estimated efficiency in highly lossy converters, which is assumed not to be the case for well-designed high-power applications where switching and parasitic losses are minimized. This assumption is verified by simulation results where the error is found to be minimal, particularly, in the range of ~(2-3)%.

$$\eta_{casc} = \frac{G_1 G_2}{G_{ideal}^2} \tag{5.2}$$

Similar to the case of an individual converter, it can be also shown that the overall system efficiency deteriorates as the duty cycle increases for a constant load, until eventually approaching zero as duty cycle approaches unity, where the opposite happens for the case of constant power loads. This idea will be discussed in more details in later sections.

5.1.2. Two-stage Series Converters

In contrast to the cascade converters, parallel-input series output connection of two DC-DC converter stages, both operated using the same duty ratio, results into an overall gain equal

to twice the gain of an individual converter. One of the main advantages of this connection is the power sharing between the two-stage. That is, each converter processes only half of the overall input power, in addition to the fact that a failure of any stage does not result into a complete load isolation from the source, rather, it still theoretically gets half of its rated power. This advantage is also important from the point of view of the ratings of each stage components compared to the cascade connection. These points will be thoroughly covered when comparing the performance of the four different topologies in later sections. As for the efficiency calculation, the ideal gain of a two-stage series converter operating at the same 'D' can be obtained as follows:

$$\frac{V_o}{V_s} = G_1 + G_2 = 2G_{ideal} \tag{5.3}$$

The practical gain of each converter is dependent on its parasitic elements, which are usually selected to be the same since both stages have the same ratings. Nevertheless, and taking the effect of the buck-boost auxiliary converter into account, which should practically be designed to have the minimal interference in the system operation, the efficiency equation of a practical two-stage series connected converter becomes:

$$\eta_{series} = \frac{G_1 + G_{BB}G_2}{2G_{ideal}} \tag{5.4}$$

Where G_{BB} indicates the buck-boost converter gain, which is connected in a cascade fashion to the second series converter stage.

5.2. Prototype Testing of the Cascade/Series Topologies

A practical prototype was implemented in the lab for each of the four proposed topologies under a power rating of ~ 120 W as a proof of concept in order to test the working principle of the proposed converters and to compare their performances. All the performed tests took place under the following conditions:

1) Switching Frequency: $f_s = 20\ KHz$
2) Input Voltage: $V_s = 15\ V$

The used components and their corresponding ratings were unified between the Cuk and SEPIC series topologies, as well as for the cascaded cases in order to obtain comparable results. The used components were the same as those used in Table 4.2. However, the used inductor earlier were combined with other types to obtain the desired values that would guarantee a CCM operating condition. Table 5.1 lists the newly added components, whereas Table 5.2 shows where each inductor is used, emphasizing on the similarity in used components between SEPIC and Cuk topologies.

Table 5.1: Additional components used in the practical implementation

Component Type	**Part Number**	**Value/Rating**	**~ Parasitic R (mΩ)**
Inductor	Hammond 159ZL	2.5 mH	44
Inductor	Hammond 195G10	5 mH	40

Table 5.2: The different inductors used in different stages

Stage		Casc. Stage 1		Casc. Stage 2		Series		Buck-Boost
Component		L_1	L_2	L_1	L_2	L_1	L_2	L
Hammond 159ZL		*x1*	*x2*	*x1*		*x1*	*x1*	
Hammond 195G10				*x1*	*x2*		*x1*	
Hammond 195C10						*x1*		*x1*
Total	L (mH)	*2.5*	*5*	*7.5*	*10*	*3.5*	*7.5*	*1*
	r_L (mΩ)	*44*	*88*	*84*	*80*	*53*	*84*	*9*

The practical results were then compared to the theoretical predictions for each topology, in terms of both gain and efficiency relations obtained in the previous section. The testing spectrum was carried out for two cases.

1) Constant Impedance Loads
2) Constant Power Loads

Each of these cases will be discussed in a separate section, where the validity of the overall theoretical models accuracy is assessed by the practical results, and then the models are used to extend the predictions of the models to higher duty cycles with the corresponding higher gains. The practical setup used for evaluating and testing the proposed connections is shown in Figures 5.1 and 5.2 for the cascade and series cases, respectively.

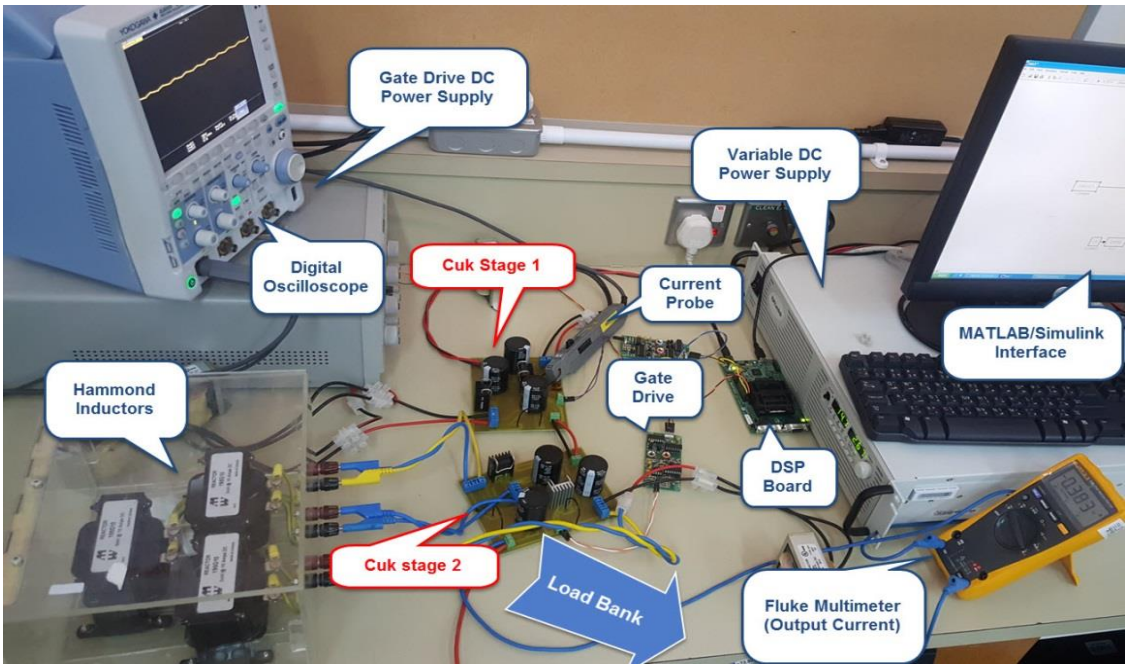


Figure 5.1: Cascaded Cuk Converter Experimental Setup

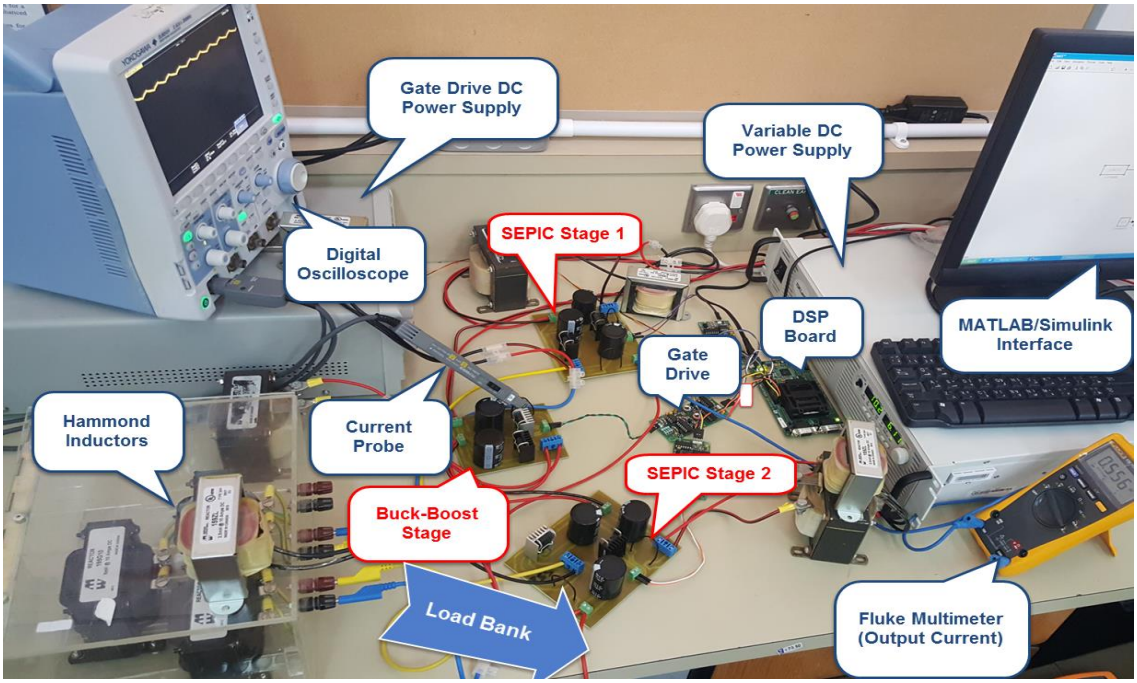


Figure 5.2: Series SEPIC converter experimental setup

5.2.1. Constant Impedance Loads

The case of practical testing with a fixed impedance for a variable duty cycle was investigated using the given parameters. The impedance value was selected as for the input power to be ~120 W around a duty cycle of 0.8 (i.e. the point of an ideal gain of 16 for the cascade connection, and 8 for the series connection). The operating D range was selected from 0.65 to 0.8 for constant impedance case, and from 0.6 to 0.8 for constant power case in order to guarantee CCM operation due to the practical limitations of the used components. For a constant impedance load, the converter's demanded power increases with D as the output voltage increases as well. The practical implementation results for both cascade and series converters are presented separately in the following subsections, followed by an overall efficiency assessment of the implemented prototypes based on the used components and the rated power.

A. Cascade Converters Gain

Both Cuk and SEPIC cascade converters were tested using the given parameters for each operating point. The gathered points were plotted against the predicted ones obtained from the theoretical model over the given operating range for comparison. The results are shown in Figure 5.3, where the similar trends between theoretical and practical results are evident in terms of the increasing gain sloping behavior. The slight gap between the results, however, can be related to several reasons similar to those discussed earlier in section 4.4 when Cuk and SEPIC models were verified individually. That is, the neglected forward bias voltage of

the used diodes and IGBTs, especially since the used diode has a relatively high forward drop of around 1.6 V, compared to the low operating voltages of the practically implemented prototype.

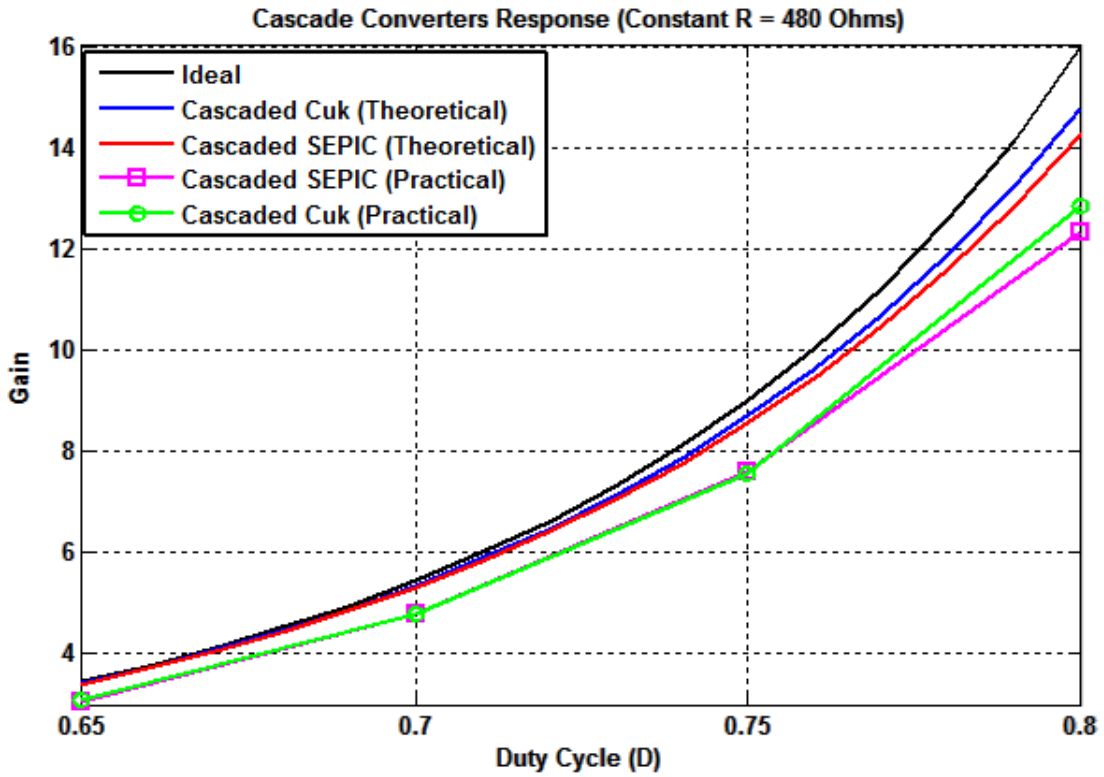


Figure 5.3: Practical Vs. Theoretical results for Cascaded Cuk & SEPIC converters (Gain Vs. Duty Cycle)

That is, such losses would appear insignificant with much higher voltage and power ratings, but would introduce a significant amount of loss here. Furthermore, the hard switching losses also contribute to the losses gap. Practically, the first stage gain was found to be considerably

less than the second cascade stage due to the mentioned factors, where the higher input to the second stage reduces the effect of such non-idealities. Nevertheless, the obtained results from the implemented prototypes successfully serve as a proof of concept for the practical operational principle for both Cuk and SEPIC cascade connected converters. Based on this conclusion, an extension to the operating range can be obtained for the theoretical model to assess the expected behavior of the implemented prototype with its ratings and parasitic elements at more extreme duty cycles, which are to be compared later to a practical high-power case with more realistic parasitic elements. Figure 5.4 shows the extended range of the theoretical models compared to the ideal response.

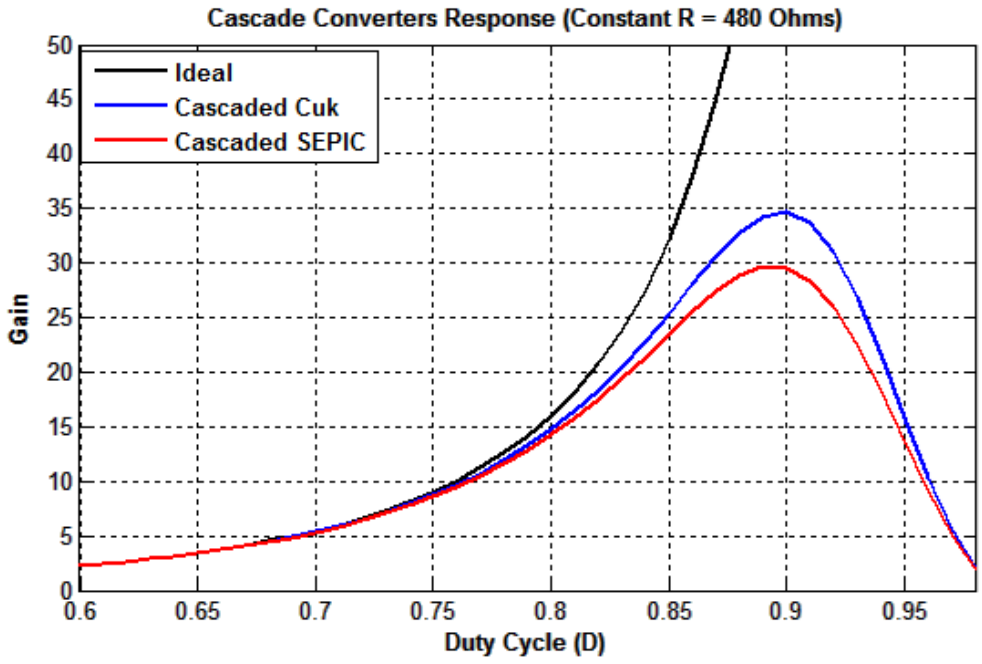


Figure 5.4: Cascaded Theoretical models response based on the prototype ratings with an extended range (Gain Vs. Duty Cycle)

B. Series Converters Gain

The practical results for the series prototypes were also obtained across the same operating range, where the ground point of the supply was common through both stages, in addition to the auxiliary buck-boost converter as shown in Figures 3.3 and 3.4 for both Cuk and SEPIC, respectively. Similar to the previous section, the Gain Vs. Duty Cycle graph was plotted between the practical and theoretical estimations, where the theoretical models included the effect of the Buck-Boost converter and accounted for its gain deterioration contributions at higher duty cycles caused by its parasitic elements, although it is not considered as a main part of the system, and is only included as a polarity reversal tool. On the other hand, it should be noted that the buck-boost effect is minimal in well-designed high power applications as will be discussed later. Figure 5.5 shows the practical results in a similar manner to that shown in Figure 5.3. Comparing the practical results to the theoretical ones, a wider gain gap to that found in Figure 5.3 is also found here mainly due to the reasons discussed in the previous subsection. However, the gap is higher here mainly due to the amplified practical effect of the Buck-Boost converter's parasitic elements and switching losses on the second stage gain while operating with such low power and voltage levels.

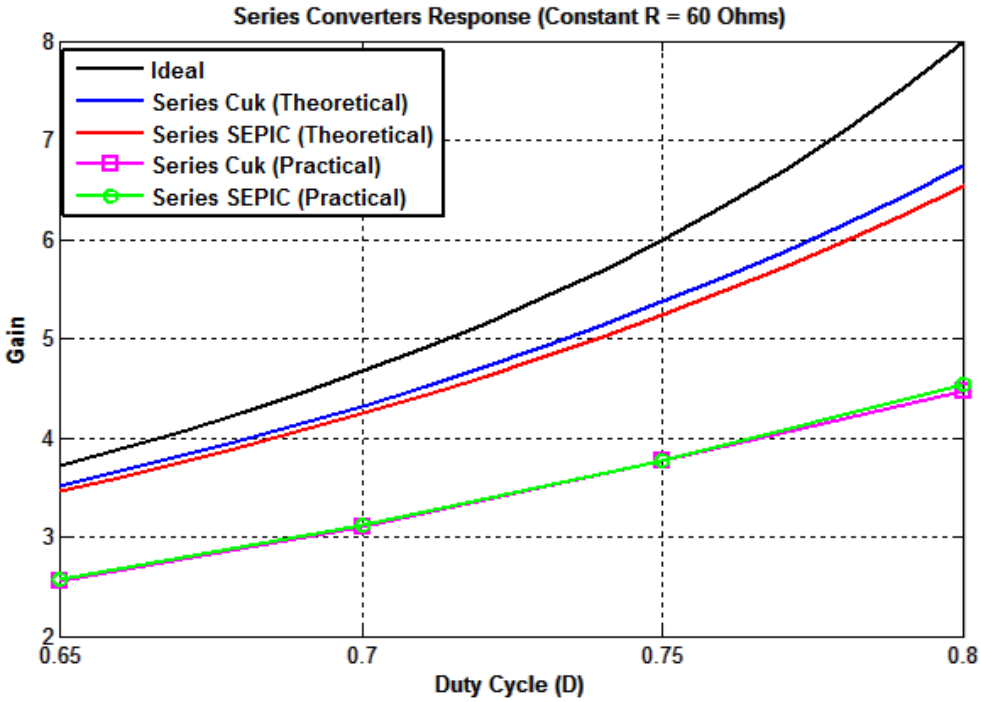


Figure 5.5: Practical Vs. Theoretical results for the series Cuk & SEPIC converters (Gain Vs. Duty Cycle)

Consequently, the first stage output was significantly higher than that of the second stage. Yet, the implemented prototypes functionality is practically confirmed, with comparable trends to the estimated ones through the theoretical model. Thus, the theoretical model predictions are extended similar to what has been done with the Cascaded case and the result is shown in Figure 5.6.

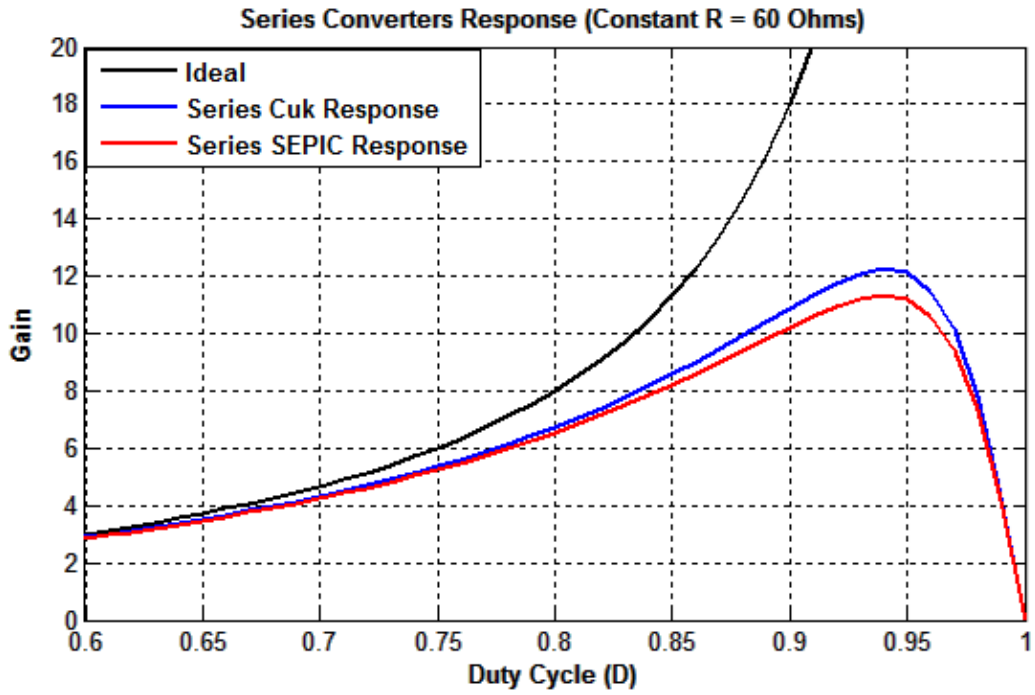


Figure 5.6: Series Theoretical models response based on the prototype ratings with an extended range (Gain Vs. Duty Cycle)

C. Practical Cascaded/Series Efficiency Comparison

The collected data for all configurations were also used to compare their practical efficiencies to the theoretical predictions over the specified operating range. The derived equations in section 5.1 were used as a basis for this comparison. Figure 5.7 summarizes the results of this comparison, where the theoretical efficiencies are higher than those obtained practically due to the aforementioned reasons, where the key effect for the wide efficiency gap of series converters is the auxiliary buck-boost converter.

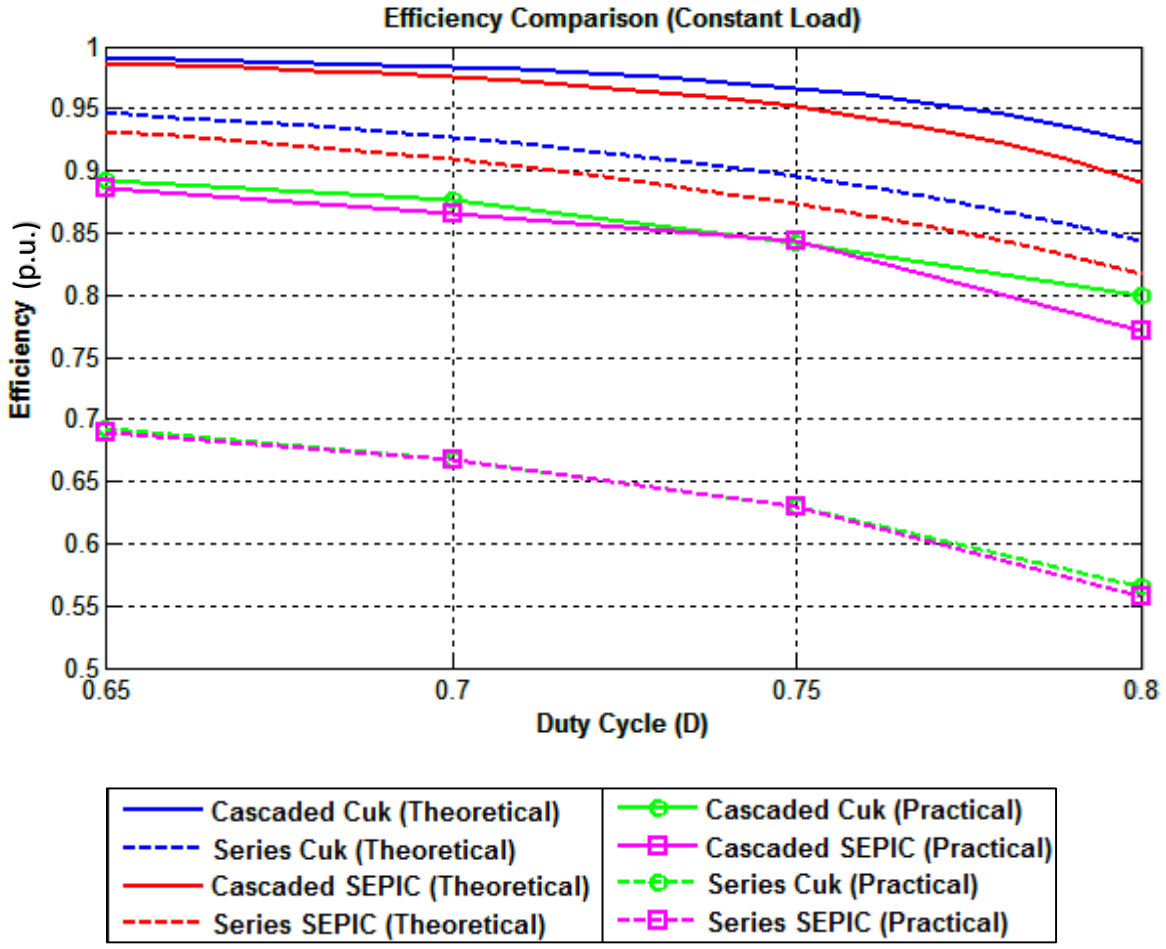


Figure 5.7: Practical Vs. Theoretical results for the efficiencies obtained for Cascaded and Series Cuk & SEPIC converters (Efficiency Vs. Duty Cycle)

That is, the prototyped cascade converters efficiencies are much closer to their theoretical counterparts compared to series converters, whereas this gap would be largely bridged if the series first stage efficiency is assumed equal to the second stage as well, which is practically the case for high-power, high conversion-ratio applications. Similar to the previously introduced results. The data presented in Figure 5.7 were extended across a wider operating

range once the model trends were verified practically. Figure 5.8 shows the efficiency comparison between the four different topologies based on the prototype ratings.

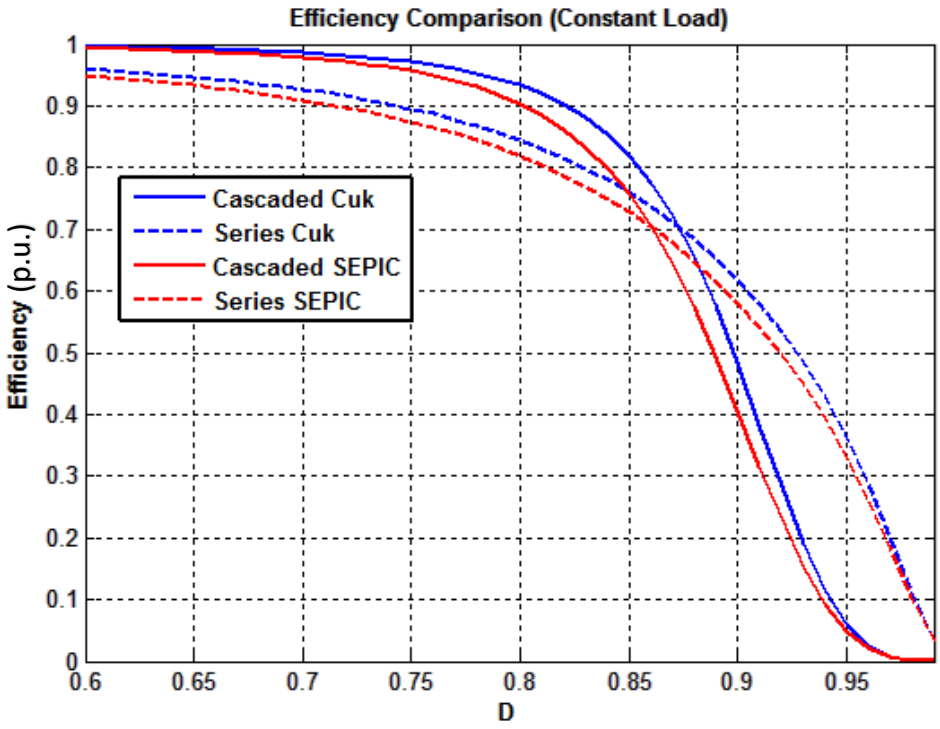


Figure 5.8: Extended range theoretical efficiency comparison between the different models based on the prototype ratings (Efficiency Vs. Duty Cycle)

It clearly shows the superiority of the cascade connections for duty ratios less than 0.85, before series converters eventually overtakes the lead, however, the theoretical efficiencies at such extreme duty cycles are largely deteriorated. Yet, it must be emphasized again that these results only represent the situation for the implemented prototype in the lab for the purpose of models verification and the validation of working principle. For instance, the

selected inductors for the prototype were based on varying operating requirements for both load and power ratings. Those requirements, on the other hand, would be considerably different at higher power applications. Thus, the effect of parasitic resistances is not accurately represented compared to real life high-power applications, where the used inductors with the corresponding parasitic resistances would be highly dependent on the inductor's current rating and it is winding cross sectional area and materials. A more detailed study of the converters gain sensitivity with respect to the inductors resistance and its operational variations is presented in Chapter 6. Also, the used electrolytic capacitors had a relatively high ESR compared to the other elements (i.e. each used capacitor had an ESR of 0.264 Ω, which is almost a triple of the maximum used $\boldsymbol{r_L}$). This scenario doesn't reflect the practical proportion between the inductors and capacitors internal resistances in real life high-power applications. Finally, such applications would utilize a higher-rating switches with much less on-state resistances. A more realistic case is to be simulated and presented in the following section as well in order to demonstrate the expected efficiency performance in such high-power applications, while maintaining the corresponding parasitic effects.

Elaborating on the auxiliary buck-boost converter effect on Figures 5.7 and 5.8 results, it should be noted that based on its low equivalent load resistance in the given prototype. As a result, its inductor parasitic resistance was relatively high. Thus, Figure 5.8 can be re-plotted without the buck-boost effect to demonstrate the more practical case in high-power applications, where the results are largely altered even on the theoretical level. The findings are summarized in Figure 5.9, where it clearly shows a significant improvement in the efficiency profile of the series-connected converters.

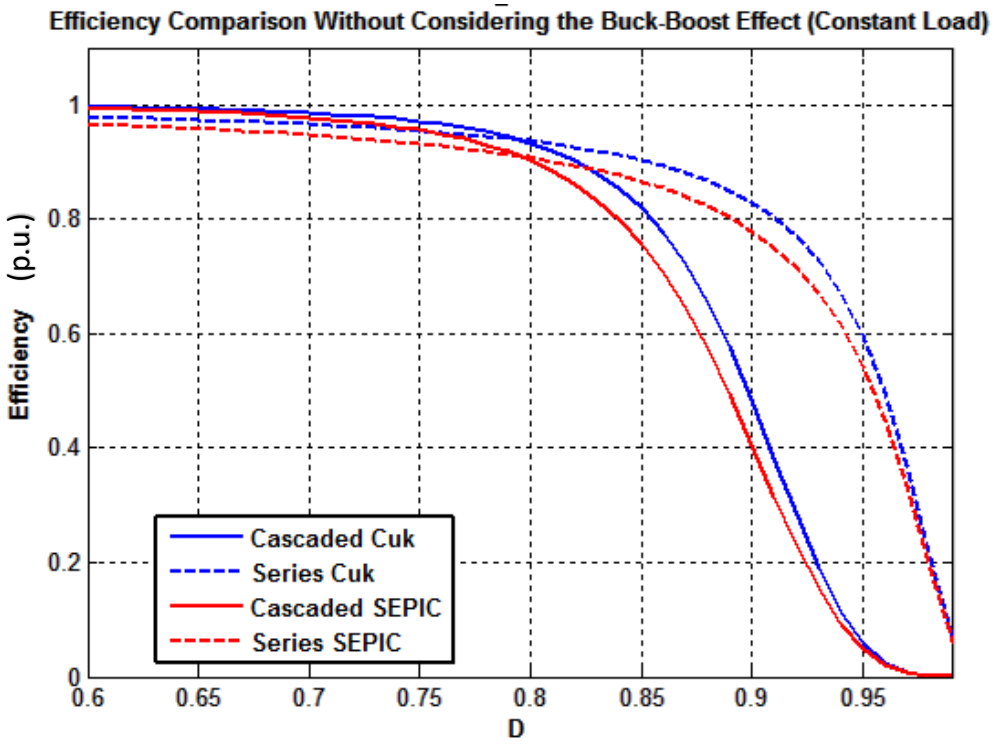


Figure 5.9: The Theoretical Efficiency Comparison results without considering the Buck-Boost effect (Efficiency Vs. Duty Cycle)

5.2.2. Constant Power Loads

On the other hand, the constant power load scenario was also considered through the practical implementation, with the load power fixed to 120 W by varying the load resistor value accordingly for each D value. As mentioned before, the practical range for duty cycle's variation here is from 0.6 to 0.8 to guarantee operating under the CCM, within the practical limitations of the used components. This section presents the results in a similar fashion to its predecessor, where the cascaded case is considered first, followed by series and finally the overall efficiency assessment.

A. Cascade Converters Gain

The cascade Cuk and SEPIC converters gain for each corresponding duty cycle within the given range was practically obtained and plotted against the theoretical predictions. The results are shown in Figure 5.10, whereas the extended graph showing the Gain Vs. Duty cycle for the wider range is shown in Figure 5.11.

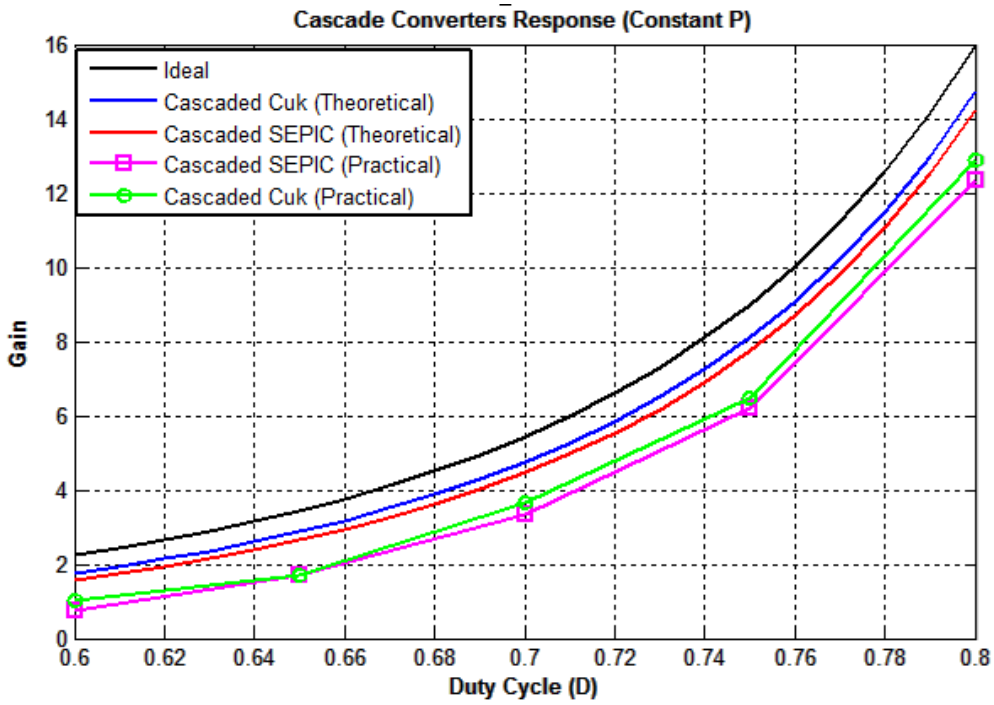


Figure 5.10: Practical Vs. Theoretical results for Cascaded Cuk & SEPIC converters for constant power load (Gain Vs. Duty Cycle)

The close similarity between the ideal and theoretical models is also clear here. This is mainly due to the fact that load resistor is variable, and increases proportionally with duty cycle,

whereas the parasitic resistances of the used practical components are assumed constant, meaning that the per-unit value of all parasitic resistances decrease significantly as the duty cycle increases, and thus their overall effect becomes continuously minimal and the theoretical models approach the ideal one as D approaches 1 and R approaches an infinite value, showing the advantage of energy transmission at higher voltages for the same power.

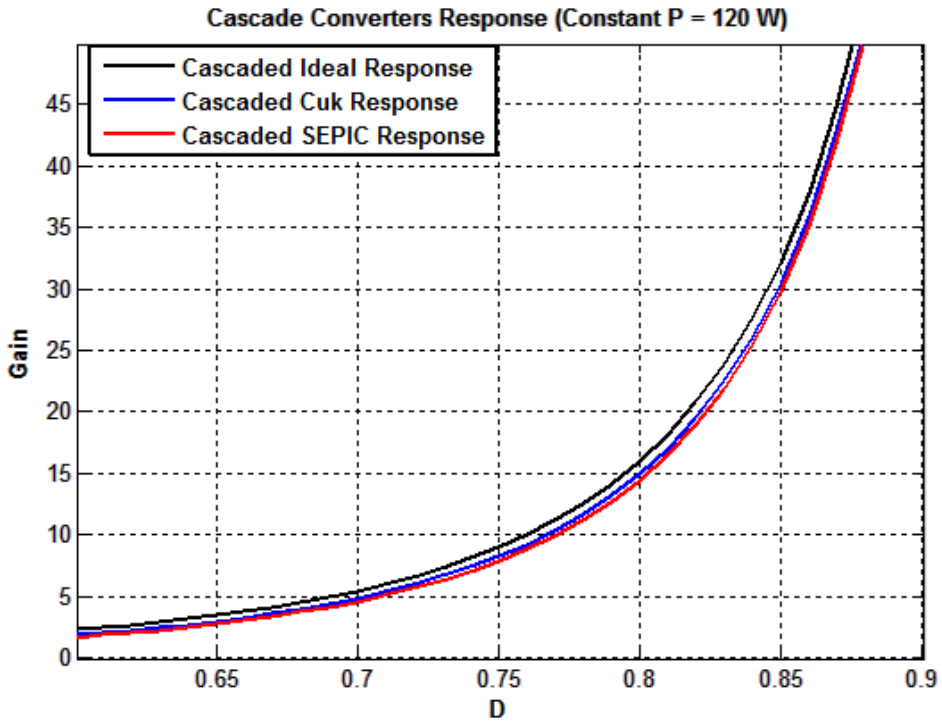


Figure 5.11: Cascaded theoretical models response based on the prototype ratings with constant P and an extended range (Gain Vs. Duty Cycle)

B. Series Converters Gain

Similarly, the series converters response with respect to a constant power load was also practically obtained for the given range, and Figure 5.12 shows the comparison between the practical and theoretical results. Again, the wider gap is closely related to the low practical over-all gain of the second stage, where it would also be greatly bridged if the first stage output is reflected on the second as well. Figure 5.13, on the other hand, shows the theoretical results for the extended range, where the presented results here also include the theoretical effect of the auxiliary buck-boost converter, resulting into the wider gap between the theoretical model predictions and the ideal response compared to the cascaded converters case shown in Figure 5.11.

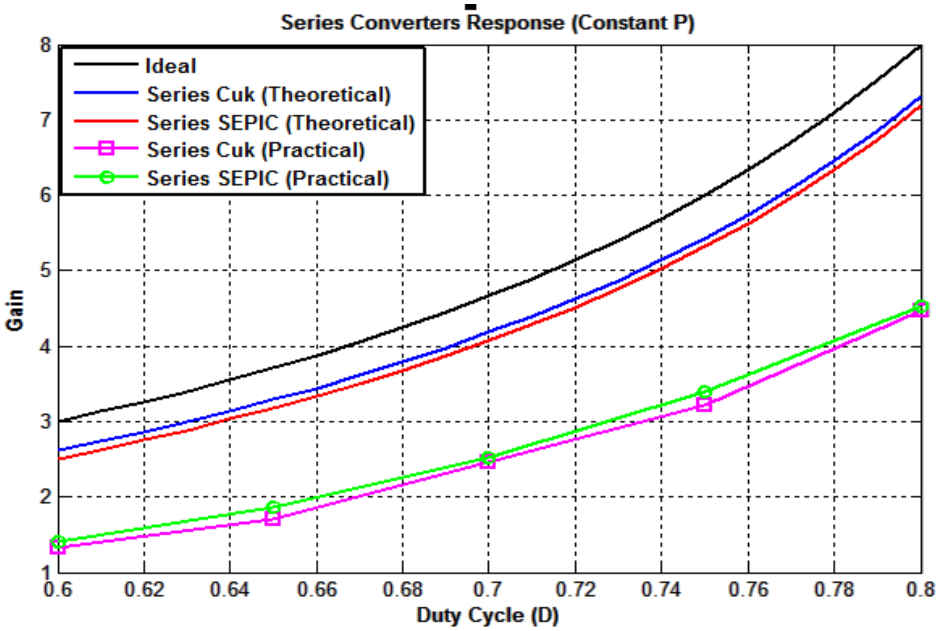


Figure 5.12: Practical Vs. Theoretical results for Series Cuk & SEPIC converters for constant power load (Gain Vs. Duty Cycle)

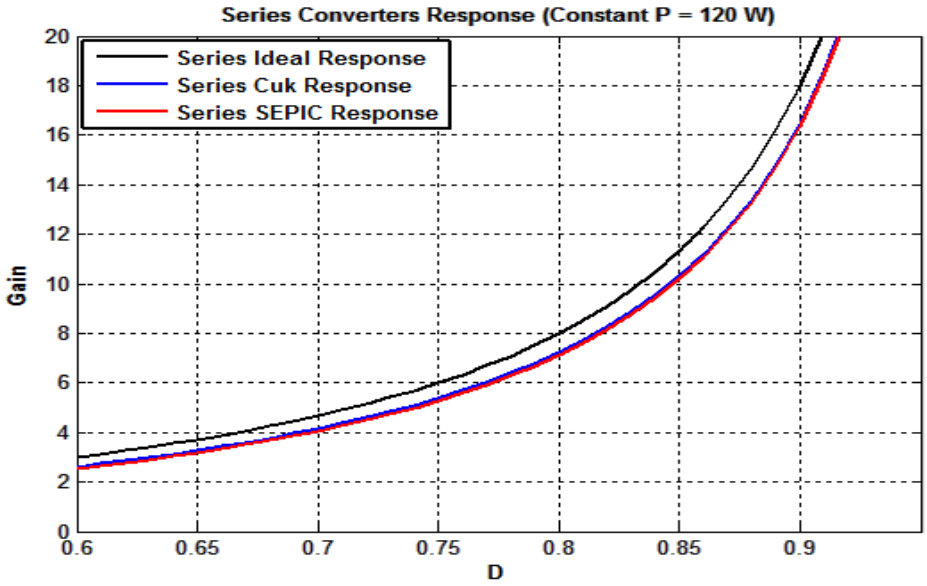


Figure 5.13: Series theoretical models response based on the prototype ratings with constant P and an extended range (Gain Vs. Duty Cycle)

C. Practical Cascaded/Series Efficiency Comparison

Similarly, the derived equations in section 5.1 were used as a basis for this efficiency comparison. The practical and theoretical comparison is shown in Figure 5.14, whereas the extended comparison is shown in Figure 5.15, where it can be noted that the efficiency of series connected converters is relatively lower than that of the cascaded converters, although both of them increase with D as expected. On the other hand, and by comparing the curves in Figure 5.14 to those in Figure 5.7, the superiority of constant-load efficiency at lower duty cycles is evident, despite of the actual power levels. This trend is mainly because for constant-power loads, maintaining the same input power at lower duty cycles requires decreasing the load resistor value, which increases the corresponding per-unit parasitic

resistances, leading to such overall decrease in efficiency, in contrast to the constant power-case where the parasitic resistances effect is minimized as the load increases proportionally to D. Consequently, the buck-boost efficiency is found here to be practically consistent for the different operating points, which is due to its relatively constant per-unit parasitic resistances while operating with a constant power. That is, the buck-boost output voltage was around 6.9 V throughout the tests, which shows the significant amount of loss it caused. Theoretically, the effect of buck-boost consideration in the efficiency calculations is a constant degradation in the second stage converter's gain by ~10% for all duty cycle values. However, this ratio is practically amplified based on the discussed reasons earlier.

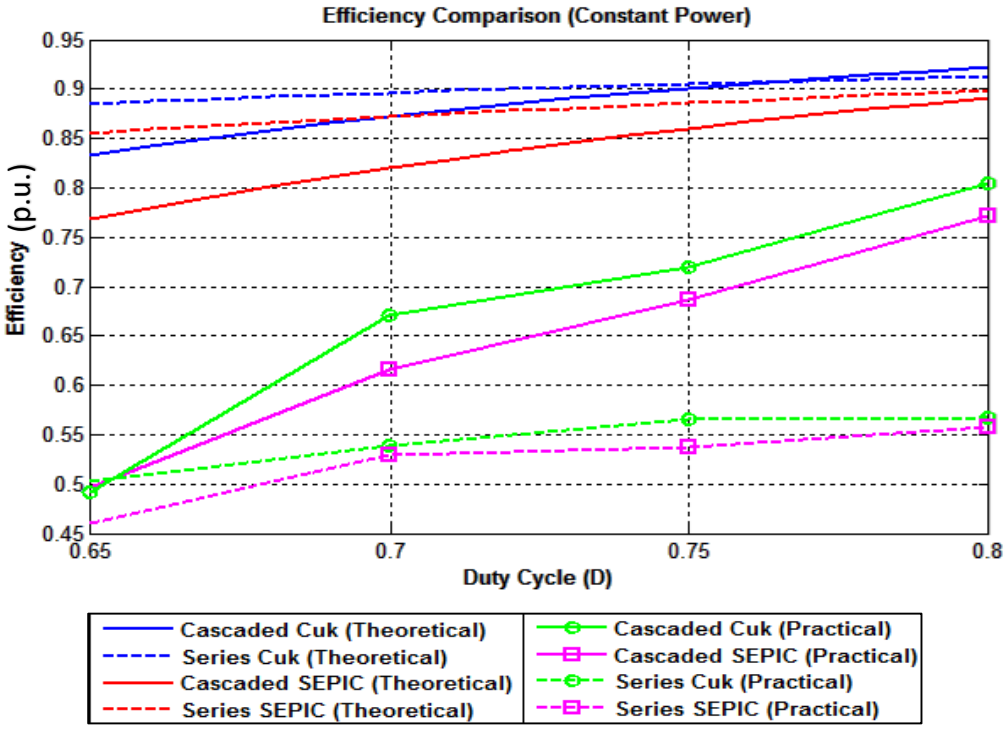


Figure 5.14: Practical Vs. Theoretical results for the efficiencies obtained for Cascaded and Series Cuk & SEPIC converters with constant P (Efficiency Vs. Duty Cycle)

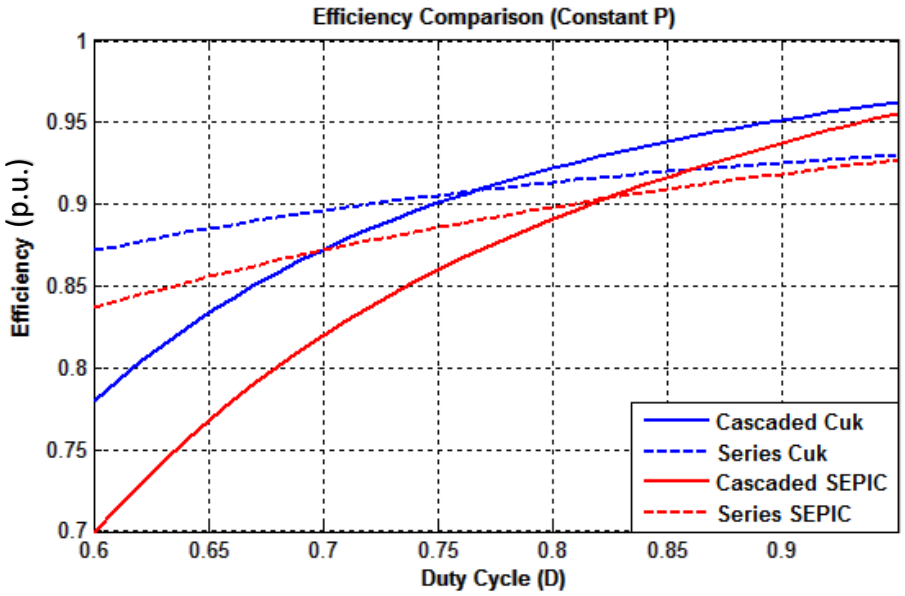


Figure 5.15: Theoretical Efficiency comparison between the different models based on the prototype ratings and constant P load (Efficiency Vs. Duty Cycle)

Therefore, neglecting the effect of buck-boost in the calculations, based on the assumptions mentioned earlier regarding the real-life high-power applications, adjusts the efficiency responses to be in the series converters favor as shown in Figure 5.16.

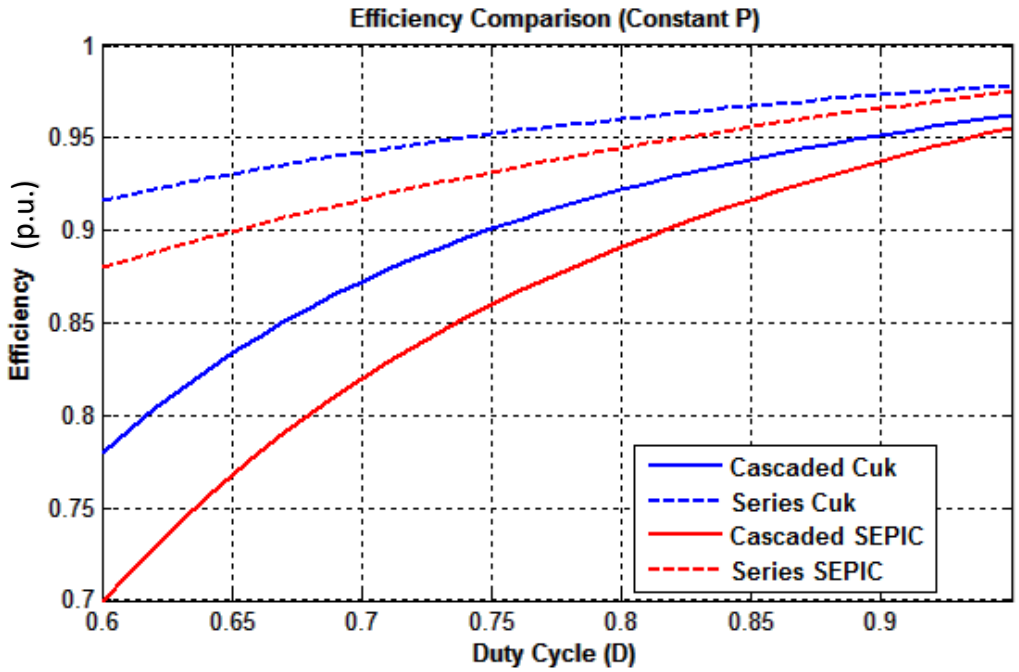


Figure 5.16: Theoretical Efficiency comparison between the different models based on the prototype ratings and constant P load without considering Buck-Boost (Efficiency Vs. Duty Cycle)

5.3. High-Power Evaluation of the Proposed Topologies

In order to test the viability and practicality of using such topologies in real life, high power applications, a testing scenario was created, where a 1.5-kV PV output is to be connected to a 132-kV HVDC line. Thus, and intermediate high-gain DC-DC conversion stage is required, similar to that shown in Figure 1.1. In this section, the component requirements for each of the four proposed topologies are presented in terms of the active switches and diodes, based on practical switches from ABB, which are summarized in Table 5.3:

Table 5.3: ABB high rating IGBT and Diode for practical evaluation

Type	Part Number	Voltage Rating (V)	Current Rating (A)
IGBT	5SNA 0750G650300	6500	750
Dual Diode	5SLD 0600J650100	6500	600 (Per Diode)

The converters are to be compared based on the number of active components they require, which is directly inferred from the switches voltage and current stresses for each configuration. Several isolated and non-isolated DC-DC converters have been introduced in different works as alternatives to achieve similar conversion-ratio requirements for high power applications, some of which were discussed in the literature survey of this thesis. Other options include the bi-directional Dual-Active-Bridge (DAB) DC-DC converters discussed in [33-35], whereas in-depth soft-switching analysis to enhance conventional DAB performance and reduce the overall losses are discussed in [36]. Consequently, similar uni-directional full-bridge DC-DC converters were also introduced in the literature, and will be included in this section to be compared with the proposed topologies in terms of the given aspects since such PV applications do not require bi-directional power flow capabilities. For simplicity, the assumption that all used devices and components are ideal is used, in addition to the availability of the required control techniques to avoid the series-connected switches mismatch. After that, efficiency analysis is performed on the four proposed topologies for the given 1 MW system parameters, while only considering the inductors parasitic resistance, as well as the IGBT on-resistance from Table 5.3, whereas the diode on-resistance is

neglected due to its minimal effects as the converters are operating at high duty cycles, indicating that its effect is present only for a fraction of duty cycle. In addition, the capacitors ESR effect is also neglected for such high power application due to its low per-unit values and minimal effect.

5.3.1. Full Bridge DC-DC Converter

Being an isolated DC-DC converter, the full bridge converter is composed of three stages as indicated previously in Figure 2.1. The PV output (1.5-kV) is first inverted into a high frequency AC waveform using the full-bridge single phase inverter, then the high-frequency transformer scales up this signal to the output side while achieving electrical isolation, and finally the full-bridge rectifier is used to convert the power signal back to DC. The total required gain to boost the input voltage from 1.5-KV to 132-kV is 88, which can be utilized through a combination of duty cycle and high-frequency transformer design as shown in the equation below:

$$\frac{V_o}{V_s} = 2D\,\frac{N_S}{N_P} \tag{5.5}$$

In this demonstration, the duty cycle is set to 0.5 in order for all the switches, sharing the same voltage and current stresses, to have an evenly distributed active time. Thus, the whole gain is attributed to the transformer's turns ratio. As for the selected rectifier, full-bridge and center-tapped full-wave rectifier were compared in terms of their total didoes Peak Inverse Voltage (PIV) requirements, where center-tapped rectifier utilizes two diodes, with twice the output voltage as the PIV of each. On the other hand, a full-bridge rectifier requires four

diodes rated for the output voltage as their PIV. Additionally, center-tapped transformers require two secondary windings, where each is utilized for only one-half cycle [37]. Thus, the full-bridge rectifier is selected as it shares a similar total PIV requirements with the center-tapped. That is, such high voltage ratings cannot be practically covered by individual diodes, so the overall number of the diodes composing the required strings is similar here. In addition to less full-bridge requirements for its transformer secondary windings. However, and although high-frequency transformers have been practically introduced in several works in the literature and showed high efficiencies for PV applications of low or moderate power levels per module/level such as the microgrid connection of residential panels and in microinverters [38-42], it should be emphasized that such high-frequency transformers are still hard to design for single-stage high power applications and are associated with lower efficiencies, whereas using low-frequency bulky transformer with such turns ratio requirement is not a practical option [3,9, 43]. Yet, the full-bridge converter will be used in this context to compare its theoretically ideal requirements with respect to the proposed topologies, the system was simulated using PSIM to verify the given predictions, where the high-frequency switches are rated for the system input voltage and current, whereas the rectifier diodes are rated for the output voltage and current. Thus, the input parameters can be utilized using a minimal number of switches, whereas the main bulk of active components comes from the output diode requirements. That is, and using the given ratings in Table 5.3, a string of 41 diodes has to be connected in series to replace each of the bridge diodes, maintaining a 100% safety margin (i.e. components are operated at a maximum of half of their rated values). Thus, a total of 164 diodes are required, in addition to 8 IGBT switches,

maintaining the same safety margin for current. That is, the switches are connected in parallel when an individual string current rating is not sufficient to withstand the input current. As a result, the total number of required active components in the circuit shown in Figure 5.17 is 172. A detailed sample calculation is carried out for series converters in order to provide the reader with detailed calculation guidance.

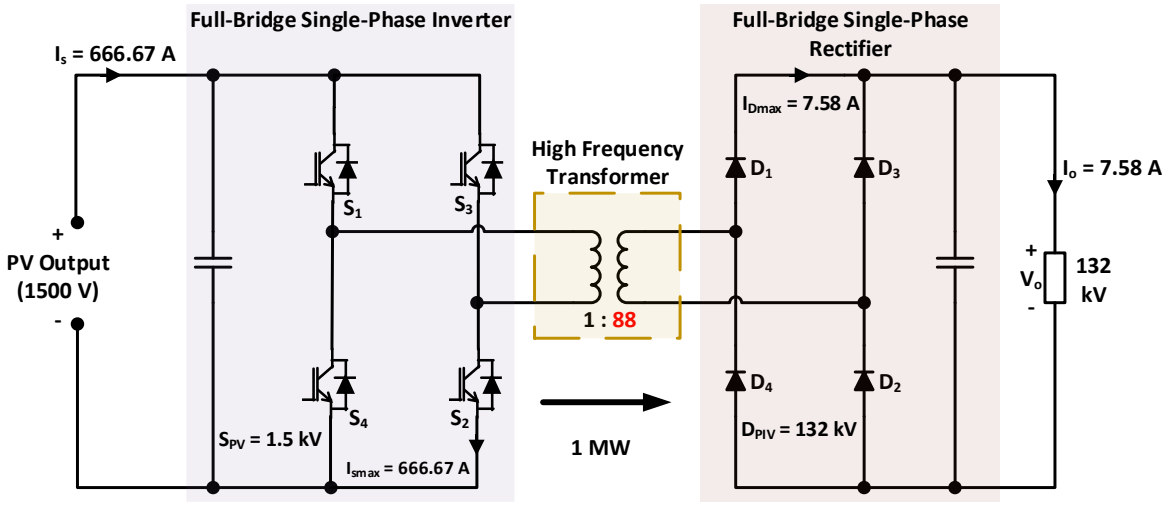


Figure 5.17: Full-Bridge Converter for the 1-MW PV application

5.3.2. Series-Connected Proposed Converters

The number of active components required for series connection of both Cuk and SEPIC converters is the same as they share similar voltage and current stresses across their active components. However, the total gain of 88 requires each stage to operate at an extreme duty cycle of 0.9778, which, even for a minimal parasitic effect, causes a reduced efficiency. Thus, a pre-series boost converter is added to the system right after the PV output, where it's

designed to operate at a moderate gain of 5 to boost the input into 7.5-kV level. That is, such a moderate gain at a duty cycle of 0.8 is associated with high efficiency, and the series-converter gain requirement is thus decreased to 17.6, shared equally between the two stages, where each of them operates at a duty cycle of 0.898. Figures 5.18 and 5.19 show the series Cuk and SEPIC configurations for the given application. As for the number of utilized switches, the boost stage active components have current stress that is equal to the converter's input current, whereas their voltage stress is equal to the output. Thus, a total of 6 IGBT switches and 9 diodes are required. Buck-boost converter, on the other hand, shares the property of having a summation of input and output current and voltages as its stress limits with both Cuk and SEPIC converters. Thus, this stage requires a total of 5 IGBTs and 5 diodes. As for the series stages, the number of active components required for each individual stage is found to be 46, distributed evenly between IGBT switches and diodes. Therefore, a total of 92 active components is required for both stages, whereas the total number of high-rated active components required for the whole system is 117. In terms of detailed calculations. Each rating, voltage or current, in Figures 5.18 and 5.19, is multiplied by 2 to account for the safety factor Then the following computations are carried out based on the active components rating given in Table 5.3

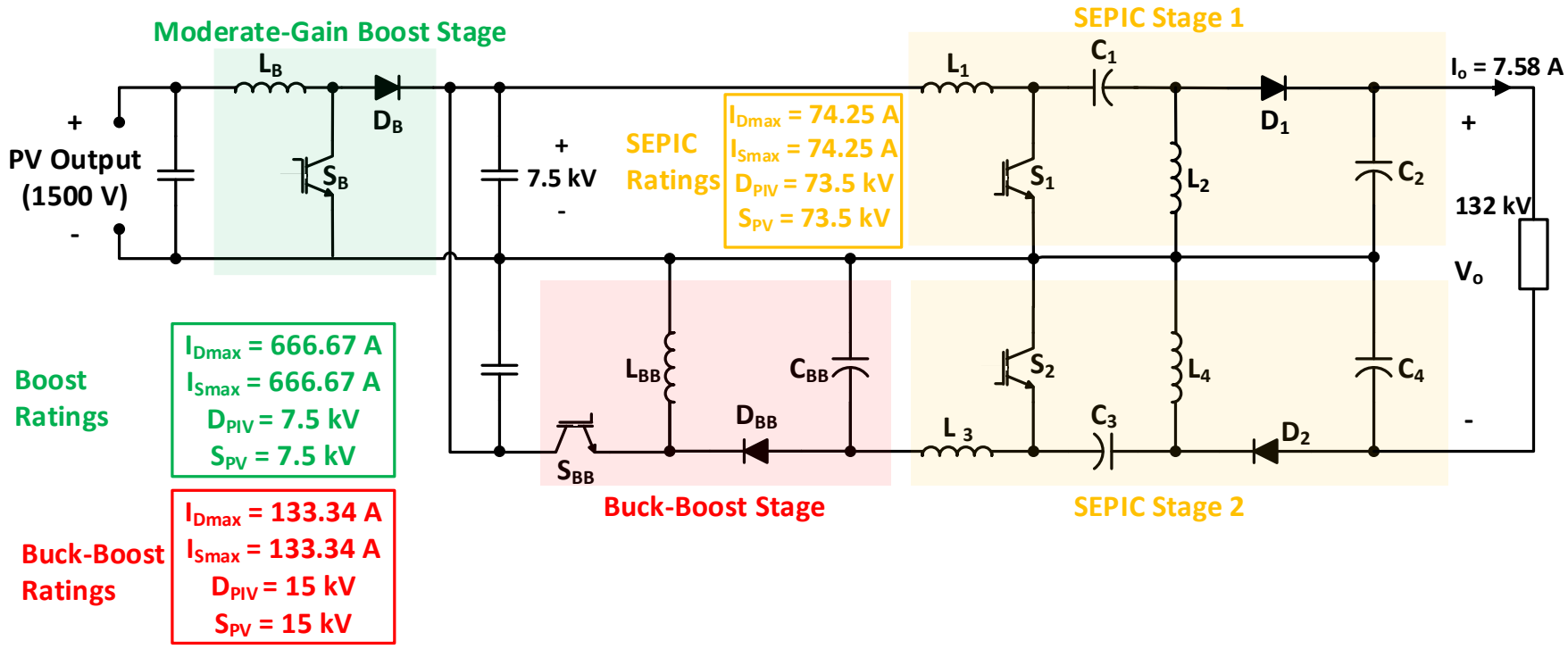


Figure 5.18: Series-Connected SEPIC converter for the 1-MW PV Application

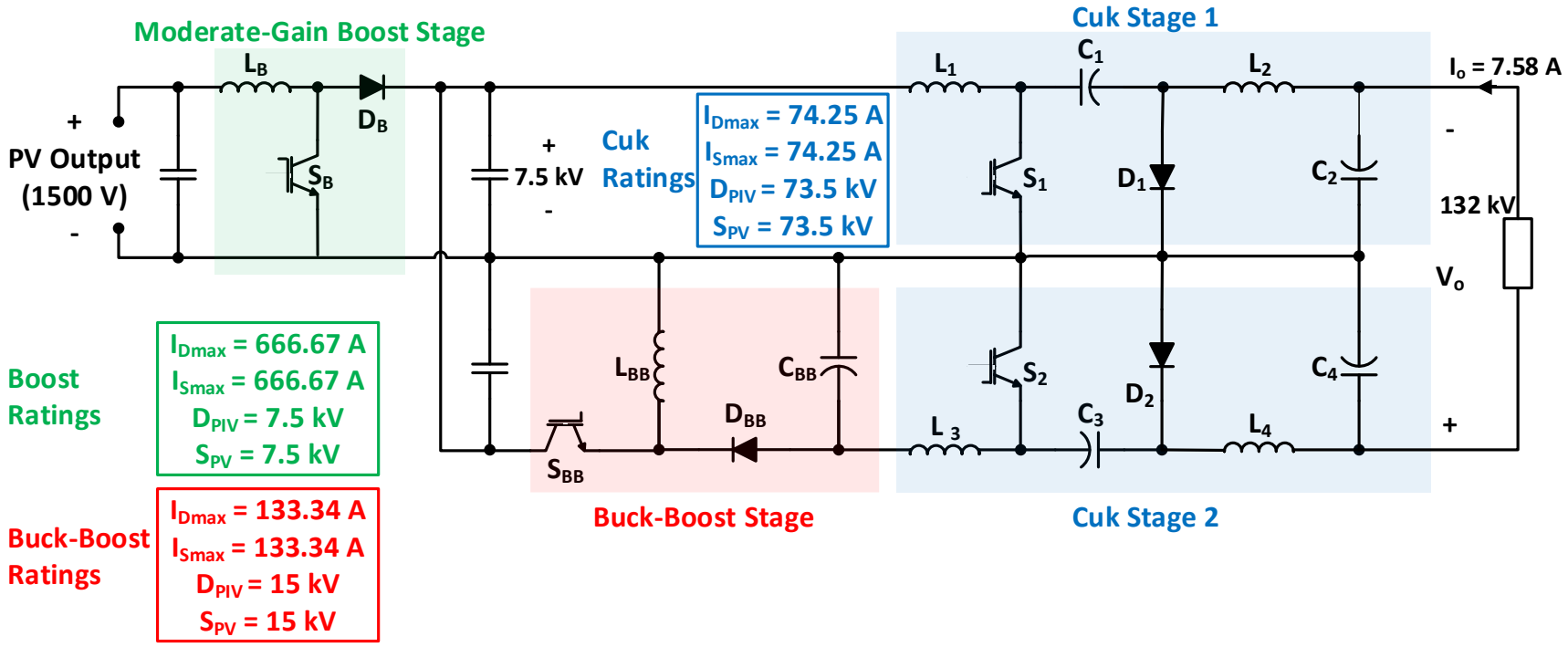


Figure 5.19: Series-Connected Cuk converter for the 1-MW PV Application

A. Boost Stage:

Table 5.4: Highly-Rated Switches for Boost Stage (Series)

	Diodes	**IGBTs**
Components Per Valve	$N_{DPV} = \frac{2 \times 7.5kV}{6.5kV} = 2.3 \rightarrow 3$	$N_{SPV} = \frac{2 \times 7.5kV}{6.5kV} = 2.3 \rightarrow 3$
Number Of Valves	$N_{DV} = \frac{2 \times 666.67\ A}{600\ A} = 2.2 \rightarrow 3$	$N_{SV} = \frac{2 \times 666.67\ A}{750\ A} = 1.8 \rightarrow 2$
Total	$\boldsymbol{N_D = N_{DPV} \times N_{DV} = 9}$	$\boldsymbol{N_S = N_{SPV} \times N_{SV} = 6}$

B. Buck-Boost Stage:

Table 5.5: Highly-Rated Switches for Buck-Boost Stage (Series)

	Diodes	**IGBTs**
Components Per Valve	$N_{DPV} = \frac{30kV}{6.5kV} \rightarrow 5$	$N_{SPV} = \frac{30kV}{6.5kV} \rightarrow 5$
Number Of Valves	$N_{DV} = \frac{266.67\ A}{600\ A} \rightarrow 1$	$N_{SV} = \frac{266.67\ A}{750\ A} \rightarrow 1$
Total	$\boldsymbol{N_D = N_{DPV} \times N_{DV} = 5}$	$\boldsymbol{N_S = N_{SPV} \times N_{SV} = 5}$

C. Cuk/SEPIC Stage:

Table 5.6: High-Rated Switches for Cuk/SEPIC Stage (Series)

	Diodes	**IGBTs**
Components Per Valve	$N_{DPV} = \frac{2 \times 73.5kV}{6.5kV} \rightarrow 23$	$N_{SPV} = \frac{2 \times 73.5kV}{6.5kV} \rightarrow 23$
Number Of Valves	$N_{DV} = \frac{2 \times 74.25\ A}{600\ A} \rightarrow 1$	$N_{SV} = \frac{2 \times 74.25\ A}{600\ A} \rightarrow 1$
Total	$\boldsymbol{N_D = N_{DPV} \times N_{DV} \times 2 = 46}$	$\boldsymbol{N_S = N_{SPV} \times N_{SV} \times 2 = 46}$

Thus, the overall count for each series configuration introduced in Figures 5.18 and 5.19 is simply obtained by adding the numbers from Tables 5.4 through 5.6 as 60 diodes and 57 IGBTs. Noting that voltage and current stresses for the different single converters are listed in Table 1.1.

5.3.3. Cascade-Connected Proposed Converters

A similar analysis was carried out for the cascade converters, where the assumption that each stage is designed to provide equal gains was maintained, where each stage is expected to boost its input by a factor of 9.38, resulting into a first stage output of around 14-kV, in addition to a moderate switches voltage stress and increased current stress. On the other

hand, the second stage input is no longer negligible with respect to the output, resulting into a significant increase in the voltage stress for the second stage. Figures 5.20 and 5.21 show the cascaded Cuk and SEPIC circuits for the given application.

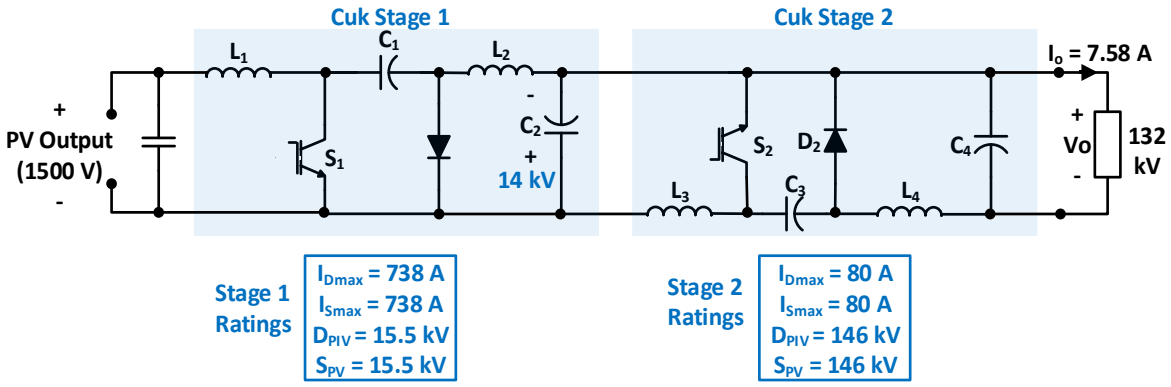


Figure 5.20: Cascade-Connected Cuk converter for the 1-MW PV Application

As for the total number of active components, the first stage utilizes a total of 10 IGBTs and 15 diodes, whereas the second stage utilizes 27 diodes and a similar number of IGBT switches, resulting into a total number of 79 active components.

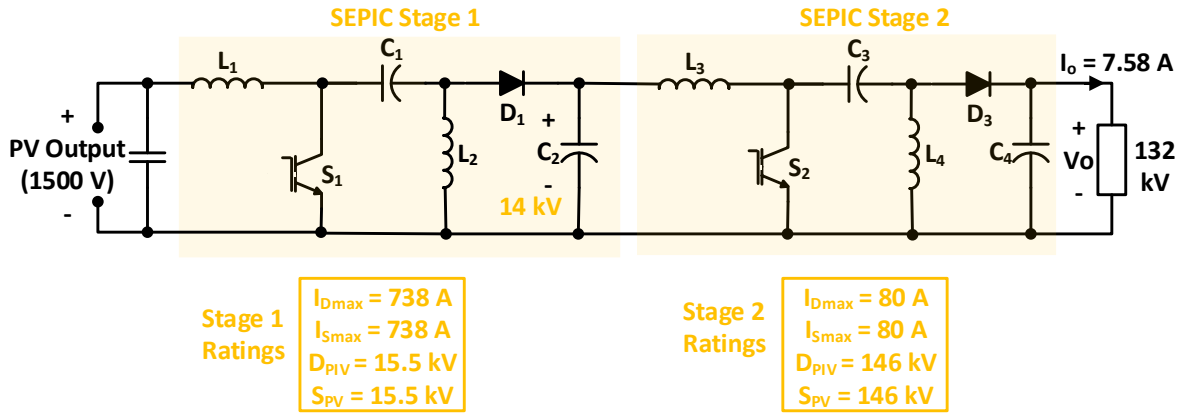


Figure 5.21: Cascade-Connected SEPIC converter for the 1-MW PV Application

5.3.4. DC-DC Converters Topological Comparison

Based on the data presented earlier, the total number of required active components for each given circuit are summarized here, where a qualitative comparison is also developed. Table 5.7 shows that among the adopted topologies in this comparison, the full-bridge converter utilizes a higher number of active switches with the same high rating, followed by the series Cuk/SEPIC converters, whereas the cascade connection required the least number of such components for the given ratings.

Table 5.7: Quantization of the number of active switches per converter for the different topologies

Converter Type	Device	Number Per Converter	Total
Full-Bridge	IGBT	8	172
	Diode	164	
Seires (Cuk/SEPIC)	IGBT	57	117
	Diode	60	
Cascade (Cuk/SEPIC)	IGBT	37	42
	Diode	42	

However, a major point that should be taken into account is that series converters circuits in this comparison were connected in a cascade fashion to a boost converter. That is, for applications requiring very high gain, utilizing the two-stages parallel-input series-output converters may not be a practical solution. Thus, a hybrid connection of different types of converters was introduced. The boost converter could have been replaced by other options, providing the same functionality (e.g. Cuk or SEPIC), however, several factors must be taken into account when making such selection, such as the operational duty cycle of the selected converter and the corresponding efficiency based on its parasitic elements. In addition, the overall number of the used components as well as their ratings. On the other hand, the results presented earlier demonstrated that when neglecting the auxiliary buck-boost converter effect, then series converters have higher efficiency compared to the

cascaded ones. Thus, selecting the appropriate combination of converters is highly dependent on the application in terms of the required conversion ratio, accepted efficiency margin, and components ratings.

Moreover, the filtering requirements are also to be taken into account when deciding on the type of converter used for a specific application. That is, Cuk converter is superior in the aspect of providing continuous input/output current. SEPIC and boost, on the other hand, provide continuous input current. However, applications with very high output voltages such as the 1-MW example, require much bulkier capacitors bank at the output side, and thus it is more important to utilize continuous output current to reduce the output filter requirements. For instance, using the same output filter with Cuk and SEPIC results into higher output ripples in SEPIC due to the aforementioned reasons.

In terms of modularity, the proposed series connection is limited to two stages only with its non-isolated topology. Yet, combinations such as the ones achieved earlier in this section are possible, whereas the cascade connected converters can be added indefinitely. However, with the drawback of very high ratings with each added stage, which limits the number of practically achievable stages, in addition to efficiency deterioration that increase while adding stages, where any loss within an earlier stage is amplified by propagating through the later stages, unlike the series connected converters where such problems are local. That is, the auxiliary buck-boost low efficiency within the practical prototype only affected the second stage output. Elaborating on the modularity point, series-connection of the proposed converters can be realized in different hybrid ways as well. For instance, the topology shown in Figure 5.22 is a result of having a SEPIC converter as the first stage,

whereas a Cuk converter is directly connected as a second stage. The need for a buck-boost converter is eliminated here as Cuk converters inherently reverses its output polarity, and thus the problem of shorting the second stage output is also eliminated. Other similar topologies can be realized using the same principle, stressing on the point that the specific selection is closely related to the given application.

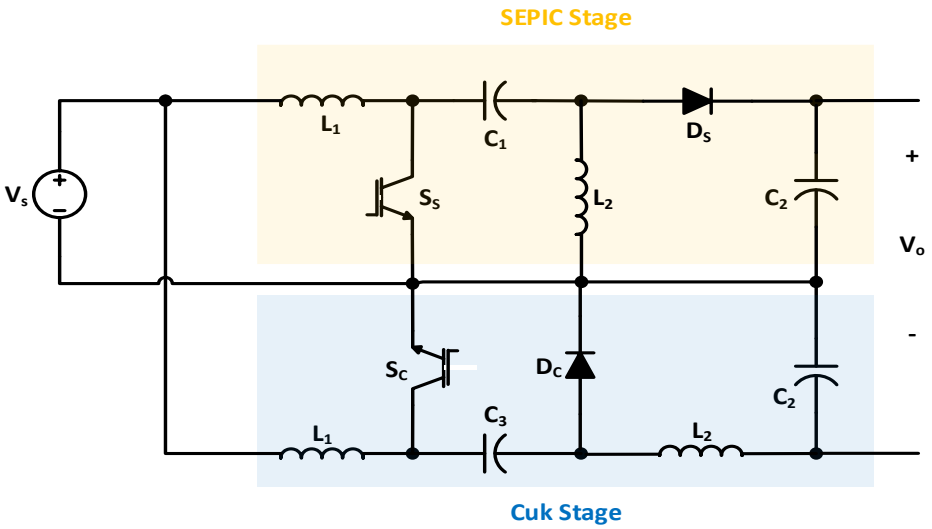


Figure 5.22: Hybrid SEPIC-Cuk Series Connected DC-DC converter

5.3.5. Efficiency Estimation in High Power Applications

In this section, the efficiency of the four proposed topologies is estimated for the given 1-MW example. As stated previously, the assumptions will be that inductors parasitic resistance r_L and the IGBT on-state resistance r_s are the components with the major effect on the overall efficiency. The given assumptions are in-line with the assumptions introduced in chapter 3 that for a real-life high power implementation, the system should be utilizing soft-switching technique and high-quality components to minimize such losses. As for the considered parasitic elements, the inductors internal resistance is assumed on per-unit basis. In other words, when Cuk or SEPIC converters are operating in the boosting mode, then the input inductor current is greater than that of the output current by a factor that is ideally equal to the conversion ratio. Thus, the coils cross-sectional area is expected to be larger for the input inductor, leading to a less per-unit resistance. Consequently, the output inductor parasitic resistance is greater. As a result, the given assumption will be that $r_{L1} = 0.0005\,pu$, whereas $r_{L2} = 0.001\,pu$ through this comparison using the different topologies. Nonetheless, the IGBT on-resistance is estimated from the "*5SNA 0750G650300"* datasheet as 1.9 $m\Omega$. This value is used to get the series/parallel equivalent on-state resistance of the IGBT strings estimated previously in this section. Moreover, the efficiency of the pre-series boost converter in Figures 5.18 and 5.19 is assumed ideal as it's operating at a moderate duty cycle and thus loses are expected to be minimal. Table 5.8 summarizes the efficiency estimation for the four different proposed topologies.

Table 5.8: Efficincy Estimation of the 1-MW example for the different topologies

Converter Type	Stage	$r_S(m\Omega)$	$r_{L1}(pu)$	$r_{L2}(pu)$	Estimated $\eta\%$
Cascaded Cuk	Stage 1	2.85	0.0005	0.001	**91.5 %**
	Stage 2	51			
Cascaded SEPIC	Stage 1	2.85	0.0005	0.001	**91.6 %**
	Stage 2	51			
Series Cuk	Stage 1 & 2	28.5	0.0005	0.001	**95.8 %**
	Buck-Boost	5.7	0.001	*N/A*	
Series SEPIC	Stage 1 & 2	28.5	0.0005	0.001	**95.9 %**
	Buck-Boost	5.7	0.001	*N/A*	

The estimated efficiencies are calculated at the specific operating points introduced earlier in this section, which are all around 0.9, indicating a potential that even for such high operational duty cycle, efficiencies beyond 90% can still be theoretically achieved. However, and although cascade converters are superior in terms of gain, Table 5.8 results highlight that the efficiency is clearly in favor of series connection for high-power applications requiring a high conversion ratio. Thus, a tradeoff between these two parameters is established for such applications. Nevertheless, a proper selection of inductors for each stage can further increase the estimated efficiency, which was based on estimated values. Consequently, the similarity between Cuk and SEPIC in terms of efficiency is evident when the key factors are r_L and r_s only, and thus it is expected for the

performance of these two converters to be comparable in high power applications, given their differences discussed earlier.

Also, the high power scenario given here can be extended to include a broader-scale implementation. For instance, a theoretical scenario that can be considered is local multiples of the 1-MW farms that are to be connected to the AC grid through DC links. Thus, the output of these farms is boosted to the DC-Link voltage through the proposed connections, and the aggregated DC power is then combined at a main station to be inverted to AC and fed to the grid. Here, the required electric isolation per standards is achieved.

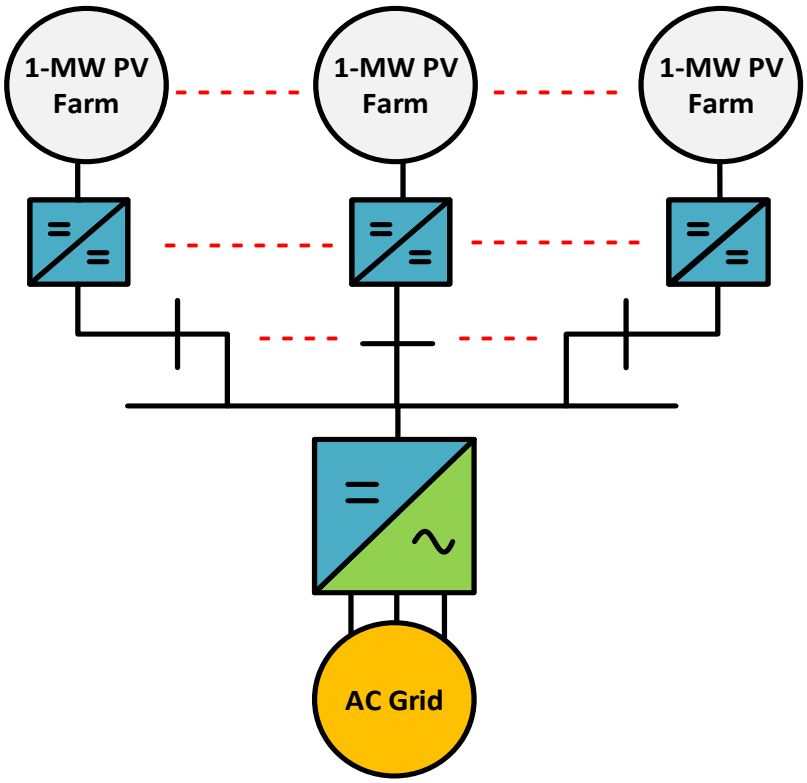


Figure 5.23: High-Power System Implementation for different local PV farm output aggregation

Chapter 6 : Sensitivity Analysis of the Proposed Topologies

This chapter investigates the effects of slight variations of the nominal inductors parasitic resistance on the overall system gain for the four proposed topologies. Since such sensitivity analysis is mainly concerned with high-power applications within the scope of this thesis, then the following assumptions are made to simplify the calculations:

1) The losses in capacitors, diodes and switches are negligible
2) The major sources of parasitic variations are the inductors
3) Each stage inductors have the same r_L value on per unit basis
4) Variations occur simultaneously in both stages
5) The buck-boost auxiliary converter is excluded from the analysis since it is not considered as a major system component in this regard

Generally, the local sensitivity of a system output Y to variations in a system input x is defined as [3, 44]:

$$S_x^Y = \frac{\delta Y/Y}{\delta x/x} = \frac{\delta Y}{\delta x}\frac{x}{y} \tag{6.1}$$

Following the given assumptions, the derived Cuk and SEPIC gain equations in chapter 4 are modified in order to maintain r_{L1} and r_{L2} only as non-idealities (i.e. x_1 & x_2). The detailed derivation for Cuk converter is presented here, where a similar derivation can be obtained for SEPIC converter by following the exact same steps. Consequently, equation (4.11) for Cuk converter can be re-written as:

$$\frac{V_o}{V_s} = \frac{D}{1-D}\,\frac{(1-D)}{(1-D)\left(r_{L2(pu)}+1\right)+r_{L1(pu)}(D^2/1-D)} \tag{6.2}$$

Where $r_{Li(pu)}$ indicates the per-unit value of the i[th] inductor parasitic resistance with respect to the converter's load resistance. Thus, and by first generalizing (6.2) to include the two stage cascade and series converters, and then applying (6.3) to the modified equations, with respect to each $r_{L(pu)}$ independently, the following results can be obtained for the two-stage cascaded Cuk converter:

$$S_{r_{L1(pu)}}^{G_{CascCuk}} = -2r_{L1}(pu)\ \frac{D^2}{(1-D)^2\left(r_{L2(pu)}+1\right)+r_{L1(pu)}D^2} \tag{6.3}$$

$$S_{r_{L2(pu)}}^{G_{CascCuk}} = -2r_{L2}(pu)\ \frac{(D-1)^2}{(1-D)^2\left(r_{L2(pu)}+1\right)+r_{L1(pu)}D^2} \tag{6.4}$$

Applying the same principle to the two-stage series connected Cuk converter for each r_L independently yields:

$$S_{r_{L1(pu)}}^{G_{SerCuk}} = 0.5\ S_{r_{L1(pu)}}^{G_{CascCuk}} \tag{6.5}$$

$$S_{r_{L2(pu)}}^{G_{SerCuk}} = 0.5\ S_{r_{L2(pu)}}^{G_{CascCuk}} \tag{6.6}$$

These results indicate that r_L variations in series connected Cuk converters contribute to as much as half the gain variations caused by the same amount of variation in a cascade connection. It follows that SEPIC converter results were found to have the same pattern. Nevertheless, a simulated scenario was constructed concerning the four different topologies in order to test the theoretical results and extend their predictions. PSIM software was used as a simulation tool for different scenarios in order to assess and compare the sensitivity at different duty cycles. Effect on the different topologies was tested through simulation and compared to the theoretical predictions for a duty cycle of 0.9. Once confirmed, the findings were expanded to project the behavior of changes in

parasitic resistances on a broader scale of duty cycles. Figures 6.1 through 6.4 present the gain sensitivity response for changes in the corresponding r_L values following the given assumptions for a D value of 0.9, and a combined nominal per unit r_{Li} value of 0.001, which is assumed throughout this chapter:

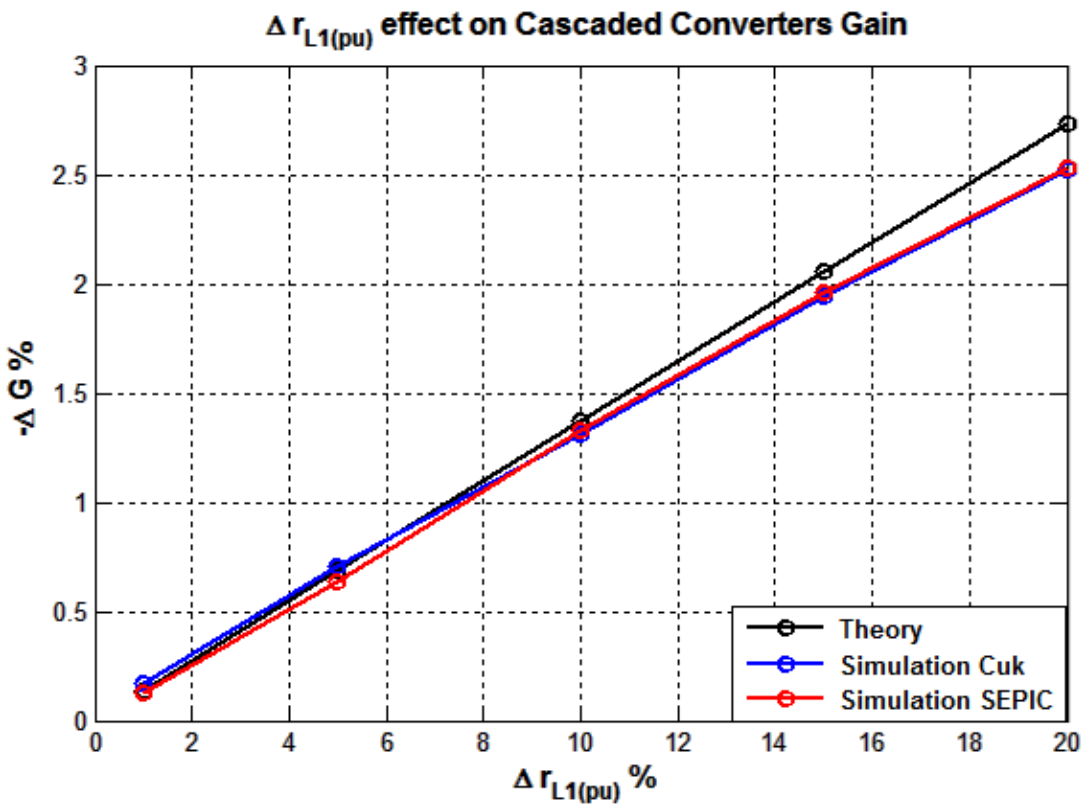


Figure 6.1: $\Delta \boldsymbol{r_{L1}}(\boldsymbol{pu})$ effect on cascaded converters gain (D = 0.9)

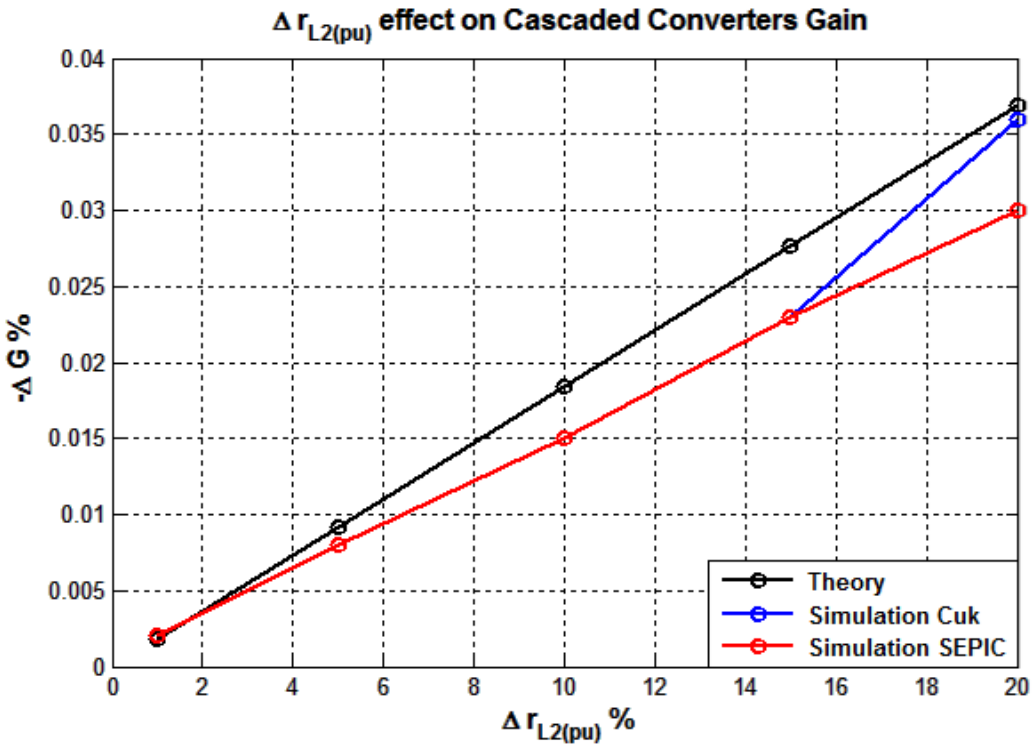


Figure 6.2: $\Delta \boldsymbol{r_{L2}}(\boldsymbol{pu})$ effect on cascaded converters gain (D = 0.9)

The results clearly show the accuracy and the validity of the derived models, where slight variations only exist between the simulations and predicted theory using (6.5) and (6.6). The main interpretations made from Figures 6.1 through 6.4 are that when only considering the parasitic r_{Li} in the models, which are the key gain deterioration factors in high gain, high-power applications, then both Cuk and SEPIC sensitivities to their variations are almost identical. Also, the variations effect in cascade connected converters on the total gain is double of that of the series connected ones for both inductors for two-stage converters.

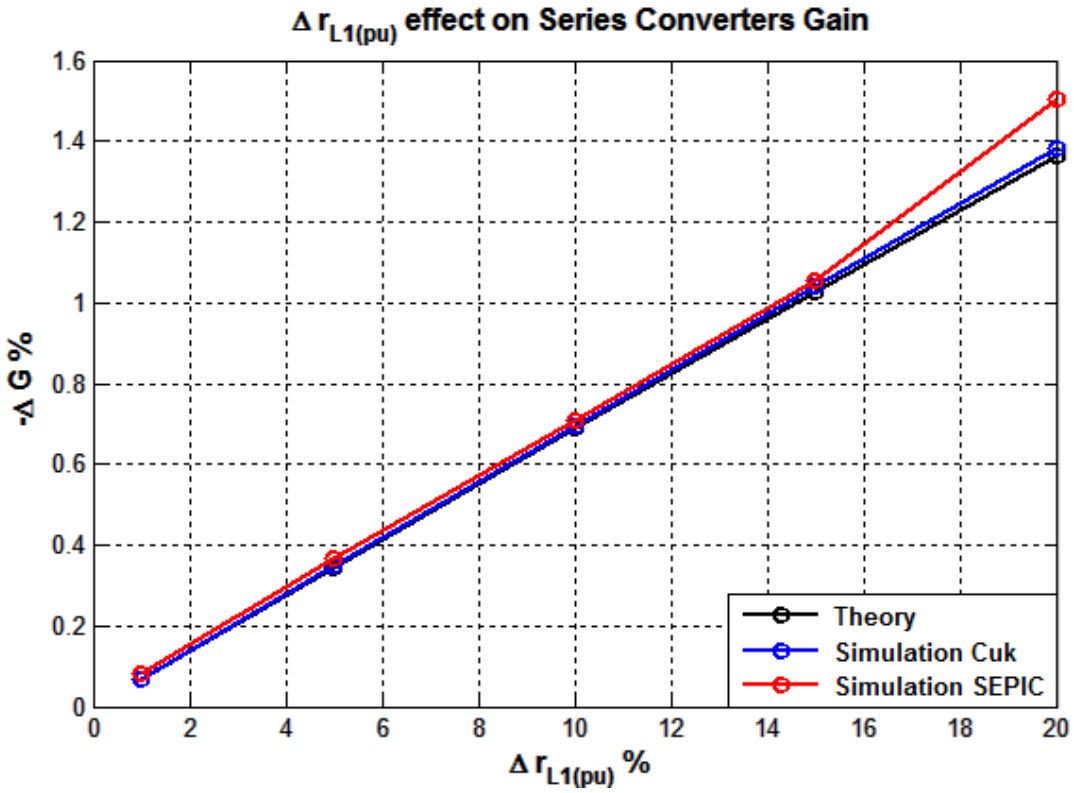


Figure 6.3: $\Delta \boldsymbol{r_{L1}(pu)}$ effect on series converters gain (D = 0.9)

Another conclusion that can be drawn is that r_{L1} variations are far more effective on the gain change than r_{L2} for the same per unit variations. That is, the gain deterioration for cascade converters in response to 10% change to the nominal r_{L1} was 1.38%, whereas this number decreased to 0.018% for the same percent change in r_{L2}. This is mainly due to the fact that in both converters, L_1 is placed in the high current side, and thus a slight increase in its resistance value contributes to a significantly larger voltage drop, compared to that of L_2 which is placed in the low current side for both Cuk and SEPIC.

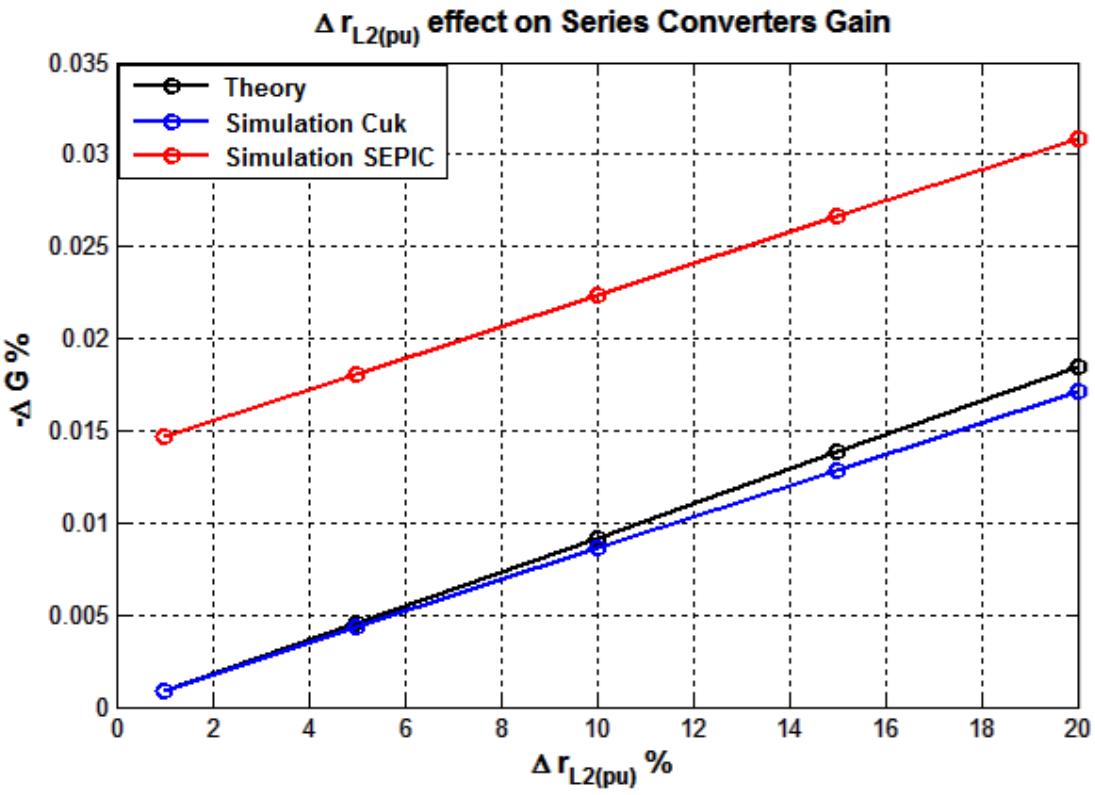


Figure 6.4: $\Delta \boldsymbol{r_{L2}(pu)}$ effect on series converters gain (D = 0.9)

Another interesting result related to the previous point is that the same per unit variation introduced to different nominal r_L values results into a lower gain change for the higher nominal r_L. Consequently, the same variations are observed to cause a greater gain loss as D approaches unity, until the variations go back to zero at D = 1 as the gain of the whole system does, which is a logical consequence of operating near the extremes. Figure 6.5 illustrates this idea by comparing the theoretical gain change with respect to changes in r_{L1} within the same given variations range of 1-20% for a wide range of D. The results were obtained the Cuk model, where cascaded SEPIC would've generated the same response as discussed earlier. Similar responses for series converters, as well as considering

$\Delta r_{L2}(pu)$ % effect, produce comparable results, respecting the -ΔG % variations for the different cases.

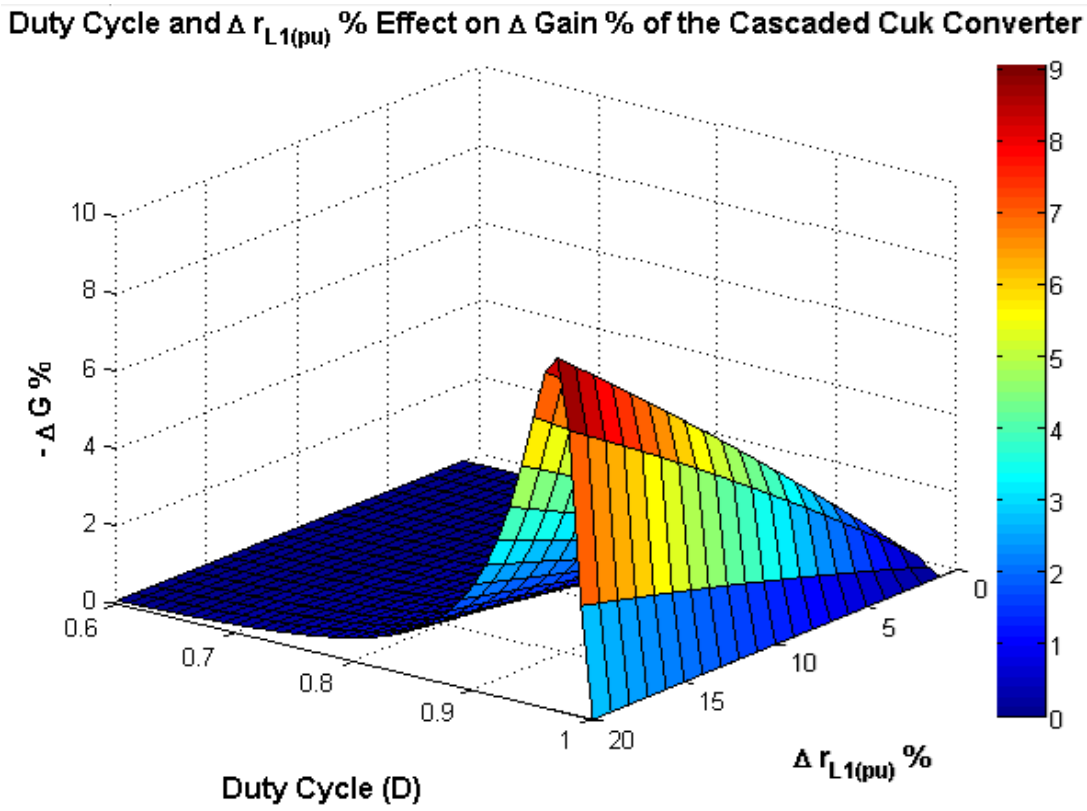


Figure 6.5: D and $\Delta \boldsymbol{r_{L1}(pu)}$ % effect on the -ΔG % for Cascaded Cuk Converter

Chapter 7 : Conclusion & Future Work

7.1. Conclusion

DC-DC converters with high conversion ratio are considered as a key aspect of PV systems integration to the AC or HVDC grids. This work has presented four different topologies based on the cascade and series connections of Cuk/SEPIC converters to achieve such requirements. Detailed theoretical models for these converters were derived and practically verified, as well as for the combined systems where a low power prototype was used to verify the expected theoretical trends gain and efficiency for both constant load and constant power scenarios. The systems were also theoretically evaluated for a high-power 1-MW PV application and showed that voltage stress levels across their active components were comparable to conventional isolated DC-DC converter systems, and thus they required less combined number of diodes/switches. In addition, the theoretical efficiency was estimated for the given high-power system and was found to be greater than 90% for all converters. Specifically, series connected converters had an efficiency above 95%, while cascaded converters efficiency was slightly above 91%, whereas cascaded stages gain is superior, indicating the tradeoff between gain and efficiency between the two different connections. Consequently, Cuk and SEPIC had an almost identical performance in high-power applications. Also, this work demonstrated the importance of continuous input/output current flow for high-power renewable-energy applications in terms of decreasing the bulky filters requirements. Finally, sensitivity analysis was performed to assess the effect of inductors r_L operational variations on the overall systems gain, where the input inductor parasitic resistance was found to have a significantly more effect on the

gain than that of the output inductor, where higher sensitivities are associated with higher duty cycles, with cascade converters having double the sensitivity of the series connected converters.

7.2. Future Work

The work presented in this thesis can be expanded and carried on from different aspects. For instance, the possible ways of implementing soft-switching techniques to minimize switching losses can be thoroughly investigated for the proposed topologies, compared to the lossy hard-switching and its associated losses. In addition, the application of different control algorithms such as sliding mode control (SMC) to both cascade and series converters can be investigated to ensure robust operation with an enhanced level of immunity to parameters variation, as well as performing MPPT, while taking the system complexity compared to single converter's topology into consideration. That is, sliding mode controllers are appropriate for DC-DC converters due to their variable space structure (VSS) nature as non-linear systems (i.e. switching action), making it easier to formulate their sliding surface. A single-stage Boost SMC with MPPT capability for PV-Grid integration application is presented in [45] and may be taken as a reference to expand this work. Also, other studies on improved topological variations may be carried out to investigate the viability of extending the proposed topologies and their combinations with other types of converters, such as isolated series-connected converter or multi-port DC-DC conversion systems, analogous to multi-secondary winding transformers.

REFERENCES

[1] S. Aljoaba, A. Cramer, B. Walcott. "Thermoelectrical Modeling of Wavelength Effects on Photovoltaic Module Performance—Part I: Model". *IEEE Journal of Photovoltaics.* vol 3, No. 3, Jul 2013.

[2] J. Lee, B. Min, T. Kim, D. Yoo, J. Yoo. "A Novel Topology for Photovoltaic DC/DC Full-Bridge Converter With Flat Efficiency Under Wide PV Module Voltage and Load Range". *IEEE Transactions on Industrial Electronics*, vol. 55, No. 7. Jul. 2008

[3] N. Denniston, A. Massoud, S. Ahmed, P. Enjeti. "Multiple-Module High-Gain High-Voltage DC–DC Transformers for Offshore Wind Energy Systems". *IEEE Transactions on Industrial Electronics*, vol. 58, No. 5, May 2011.

[4] *International Electrotechnical Commission,* IEC 61215-1:2016, 2016

[5] E. Serban, M. Ordonez, C. Pondiche. "DC-Bus Voltage Range Extension in 1500 V Photovoltaic Inverters". *IEEE Journal of Emerging & Selected Topics in Power Electronics, vol. 3, No. 4, Dec. 2015.*

[6] W. Li, X. He. "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications". *IEEE Transactions on Industrial Electronics*, vol 58, No. 4, Apr. 2011.

[7] F. Tofoli, D. Pereira, W. Paula, D. Oliveira. "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter". *IET Power Electronics*, vol. 8, No. 10, April 2015.

[8] R. Reiter, L. Michels, A. Peres, S. Oliveira. "Analysis of PV Arrays for Residential Applications Using a Three-Phase Step-Up Isolated DC-DC Converter with High-Frequency Transformer". *37th Annual Conference on IEEE Industrial Electronics Society*. Nov. 2011.

[9] K. Park, Z. Chen. "A Double Uneven Power Converter-Based DC–DC Converter for High-Power DC Grid Systems". *IEEE Transactions on Industrial Electronics*, vol. 62, No. 12, Dec. 2015.

[10] A. El Khateb, N. Abd Rahim, J. Selvaraj, B. Williams. “DC-to-DC Converter With Low Input Current Ripple for Maximum Photovoltaic Power Extraction”. *IEEE Transactions on Industrial Electronics*, vol 62, No. 4, Apr. 2015.

[11] B. Williams. “DC-to-DC Converters With Continuous Input and Output Power”. *IEEE Transactions on Power Electronics.* vol 28, No. 5. May 2013.

[12] J. Wang, W. G. Dunford and K. Mauch, “A comparison of modified boost converters with continuous inductor current mode and ripple free input current with conventional converters”. *Industry Applications Conference*. pp. 878 – 885. Oct 1996.

[13] H. Liu and F. Li, “Novel High Step-Up DC–DC Converter With an Active Coupled-Inductor Network for a Sustainable Energy System”, *IEEE Transactions on Power Electronics*, vol. 30, No. 12, Dec. 2015.

[14] Y. Wang, L. Xue, C. Wang, P. Wang, W, Lei. “Interleaved High-Conversion-Ratio Bidirectional DC–DC Converter for Distributed Energy-Storage Systems—Circuit Generation, Analysis, and Design”. *IEEE Transactions on Power Electronics.* vol. 31, No. 18. Aug 2016.

[15] Chen, Z., Liu, S., Shi, L. ‘A soft switching full bridge converter with reduced parasitic oscillation in a wide load range’, *IEEE Trans. Power Electron.*, 2014, 29, (2), pp. 801–812.

[16] A. Elasser, M. Kheraluwala, M. Ghezzo, R. Steigerwald, N. Evers, J. Kretchmer, T. Chow. “A Comparative Evaluation of New Silicon Carbide Diodes and State-of-the-Art Silicon Diodes for Power Electronic Applications”. *IEEE Transactions on Industry Applications*, vol. 39, No. 4. Jul 2003.

[17] X. Yuan, S. Walder, N. Oswald. “*EMI Generation Characteristics of SiC and Si Diodes: Influence of Reverse-Recovery Characteristics*”. *IEEE Transactions on Power Electronics.* vol. 30, No. 3. Mar 2015.

[18] J. Kim, S. Park, Y. Kim, Y. Jung, C. Won. "High-efficiency bidirectional sof switching DC-DC converter". *Power Electronics Conference (IPEC)*. Jun 2010.

[19] B. Williams. “Generation and Analysis of Canonical Switching Cell DC-to-DC Converters”. *IEEE Transactions on* Industrial *Electronics.* vol. 61, No. 1. Jan 2014.

[20] I. Gowaid, G. Adam, A. Massoud, S. Ahmed, D. Holliday, B. Williams. “Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability”. *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 30, No. 1, Jan 2015.

[21] X. She, X. Yu, F. Wang, A. Huang. “Design and Demonstration of a 3.6-kV–120-V/10-kVA Solid-State Transformer for Smart Grid Application”. *IEEE Transactions on Power Electronics.* vol. 29, No. 8. Aug 2014.

[22] A. Parastar, J. Seok. “High-Gain Resonant Switched-Capacitor Cell-Based DC/DC Converter for Offshore Wind Energy Systems”. *IEEE Transactions on Power Electronics.* vol. 30, No. 2. Feb 2015.

[23] A. Paraster, Y. Kang, J. Seok. “Multilevel Modular DC/DC Power Converter for High-Voltage DC-Connected Offshore Wind Energy Applications”. *IEEE Transactions on Industrial Electronics*. vol. 62, No. 5. May 2015.

[24] W. Chen, A. Huang, C. Li, G. Wang, W. Gu. “Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems”. *IEEE Transactions on Power Electronics*. vol 28, No. 4. Apr 2013.

[25] W. Chen, X. Wu, L. Yao. W. Jiang. “A Step-up Resonant Converter for Grid-Connected Renewable Energy Sources”. *IEEE Transactions on Power Electronics*. vol. 30, No. 6. Jun 2015.

[26] H. Athab, A.Yazdani, B. Wu. “A Transformerless DC–DC Converter With Large Voltage Ratio for MV DC Grids”. *IEEE Transactions on Power Delivery.* vol 29, No. 4. Aug 2014.

[27] K. Tseng, C. Huang. “High Step-Up High-Efficiency Interleaved Converter With Voltage Multiplier Module for Renewable Energy System”. *IEEE Transactions on Industrial Electronics*. vol. 61, No. 3. Mar 2014.

[28] H. Choi, M. Ciobotaru, M. Jang, V. Agelidis. “Performance of Medium-Voltage DC-Bus PV System Architecture Utilizing High-Gain DC–DC Converter”. *IEEE Transactions on Sustainable Energy.* vol.6, No. 2. Apr 2015.

[29] J. Rosas-Caro, J. Ramirez, F. Peng and A. Valderrabano, "A DC–DC multilevel boost converter", IET Power Electronics, vol. 3, no. 1, p. 129, 2010.

[30] X. Zhang and T. Green, "The Modular Multilevel Converter for High Step-Up Ratio DC–DC Conversion", IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4925-4936, 2015.

[31] X. Hu, C. Gong. “A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques”. *IEEE Transactions on Power Electronics*, vol. 29, No. 2. Feb 2014.

[32] L. Zhou, B.Zhu, Q. Luo, S. Chen. “Interleaved non-isolated high step-up DC/DC converter based on the diode–capacitor multiplier”. *IET Power Electron.*, vol. 7, No. 2, pp. 390–397, 2014.

[33] Y. Shi, R. Li, Y. Xue, H. Li. “Optimized Operation of Current-Fed Dual Active Brdige DC-DC Converter for PV Applications”. *IEEE Transactions on Industrial Electronics*, vol. 62. No. 11, Nov 2015.

[34] Y. Lu, H. Wu, Y. Xing, K. Sun. “A Dual-Active-Bridge Converter-Based High Step-up Converter with Voltage-Multiplier for High-Efficiency PV Application”. *2015 IEEE Applied Power Electronics Conference and Exposition (APEC).* pp.1112-1117. Mar 2015.

[35] M. Cacciato, A.Consoli, R. Attanasio, Fr. Gennaro. “Sof-Switching Converter With HF Transformer for Grid-Connected Photovoltaic Systems”. *IEEE Transactions on Industrial Electronics.* vol. 57, No.5, May 2015.

[36] G. Ortiz, H. Uemura, D. Bortis, J. Kolar, O. Apeldroon. “Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters”. *IEEE Transactions On Electron Devices*. vol. 60, No. 2. Feb 2013.

[37] M. Rashid. *Power Electronics: Devices, Circuits and Applications 4th Edition*. Pearson, England, 2014. pp: 103-157.

[38] G. Franceschini, E. Lorenzani, G. Buticchi. “Saturation Compensation Strategy for Grid Connected Converters Based on Line Frequency Transformers”. *IEEE Transactions on Energy Conversion.* vol. 27, No. 2. Jun 2012.

[39] W. Cha, Y. Cho, J. Kwon, B. Kwon. “Highly Efficient Microinverter With Soft-Switching Step-Up Converter and Single-Switch-Modulation Inverter”. *IEEE Transactions on Industrial Electronics.* vol 62, No.6. Jun 2015.

[40] H. Keyhani, H. Toliyat. “Single-Stage Multistring PV Inverter With an Isolated High-Frequency Link and Soft-Switching Operation”. *IEEE Transactions on Power Electronics.* vol. 29, No. 8, Aug 2014.

[41] H. Fan, H. Li. “High-Frequency Transformer Isolated Bidirectional DC–DC Converter Modules With High Efficiency Over Wide Load Range for 20 kVA Solid-State Transformer. “IEEE Transactions on Power Electronics”. vol. 62, No. 12, Dec 2011.

[42] H. Hu, S. Harb, N. Kutkut, Z. Shen, I. Batarseh. “A Single-Stage Microinverter Without Using Eletrolytic Capacitors”. *IEEE Transactions on Power Electronics*. vol. 28, No. 6, Jun 2013.

[43] M. Uslu. “Analysis, Design, and Implementation of a 5 KW Zero Voltage Switching Phase-Shifted Full-Bridge DC/DC Converter Based Power Supply For Arc Welding Machines”. M.A. Thesis, Middle-East Technical University, Turkey, 2006.

[44] A. Saltelli, S. Tarantola, F. Campolongo, M. Ratto, "Sensitivity Analysis In Practice: A Guide to Assessing Scientific Models", Ispra, Italy: John Wiley & Sons, Ltd, England. pp. 5-10.

[45] P. Valencia and C. Ramos-Paja, "Sliding-Mode Controller for Maximum Power Point Tracking in Grid-Connected Photovoltaic Systems", Energies, vol. 8, no. 11, pp. 12363-12387, 2015.

APPENDIX

The practical prototypes for the proposed connections where carried out using a combined switching frequency of 20-kHz, and a fixed input of 15-V throughout. The PWM signals were generated using the eZDSP F28335 board, with the appropriate gate drive circuitry to provide the required Gate-to-Emitter voltage of ~15 V_{DC}. Figure A.1 shows a sample PWM signal generated for a duty cycle of 0.75:

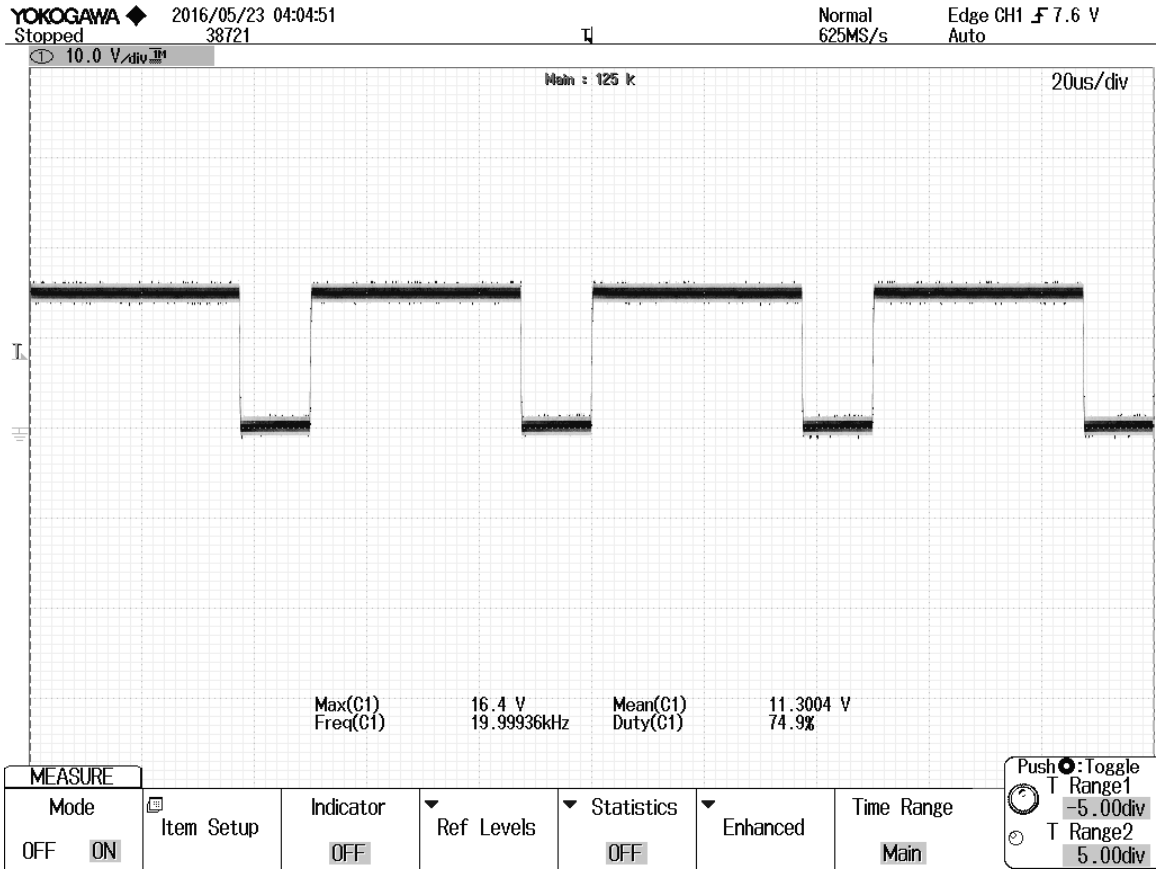


Figure A.1: Generated PWM signal for D = 0.75

The current continuity through inductors was assured by the proper design of their values in CCM. Table A.1 summarizes the inductors design formulas for the used converters:

Table A.1: CCM Limits for inductor values

Converter Type	L_1 **Design Equation**	L_2 **Design Equation**
Cuk **SEPIC**	$L_1 > \frac{(1-D)^2 R}{2Df}$	$L_2 > \frac{(1-D)R}{2f}$
Buck-Boost	$L > \frac{(1-D)^2 R}{2f}$	*N/A*

These equations, on the other hand, do not take the limited requirements of the current ripple into account. Thus, the inductors may be re-designed for a maximum allowable ripples, where *L* values must be above the CCM limits to ensure continuity. Figures A.2 and A.3 show the current continuity of a single operating point for the implemented Cascaded Cuk prototype in terms of the input current for both first and second stages for D = 0.75, where the mean values appearing in mV can be converted to amperes through division by 100, which is the scalability factor of the used current probes.

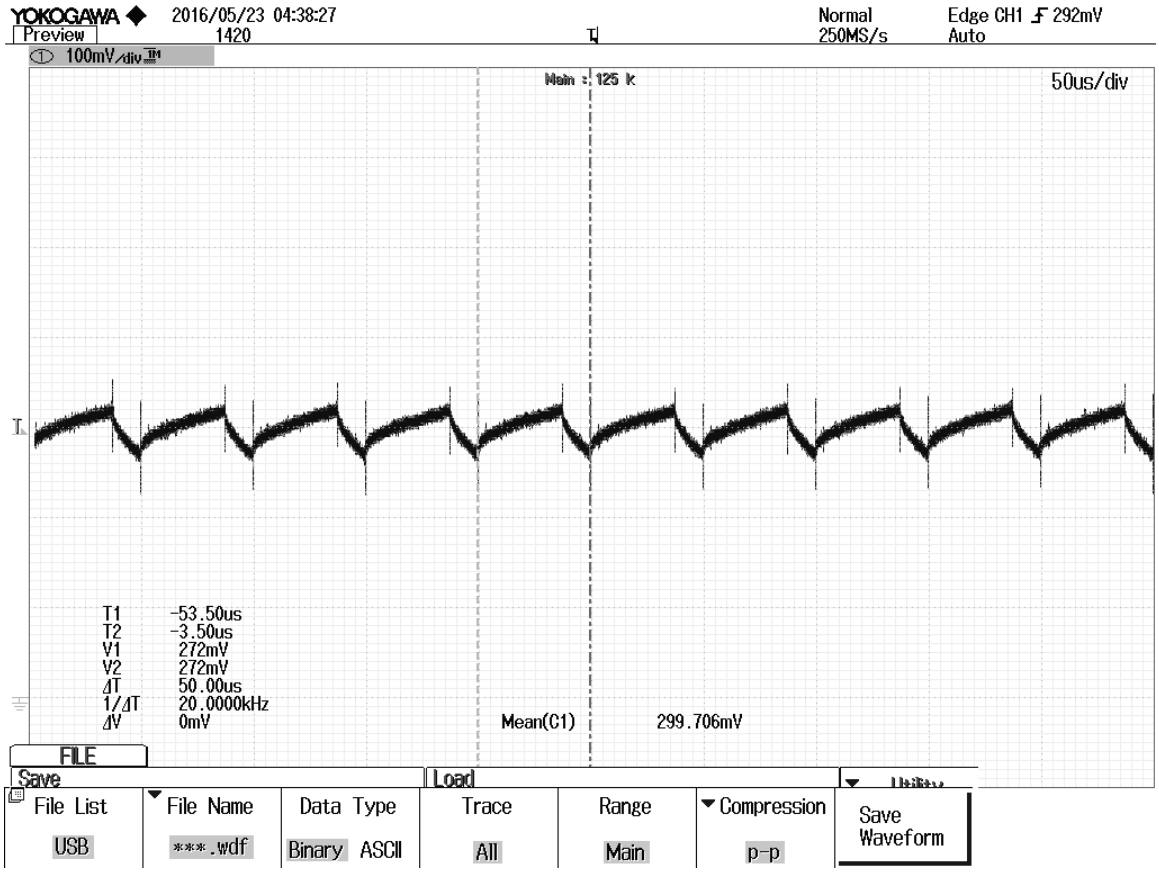


Figure A.2: Input current at D = 0.75 for the Cascaded Cuk first stage (Constant Impedance Case)

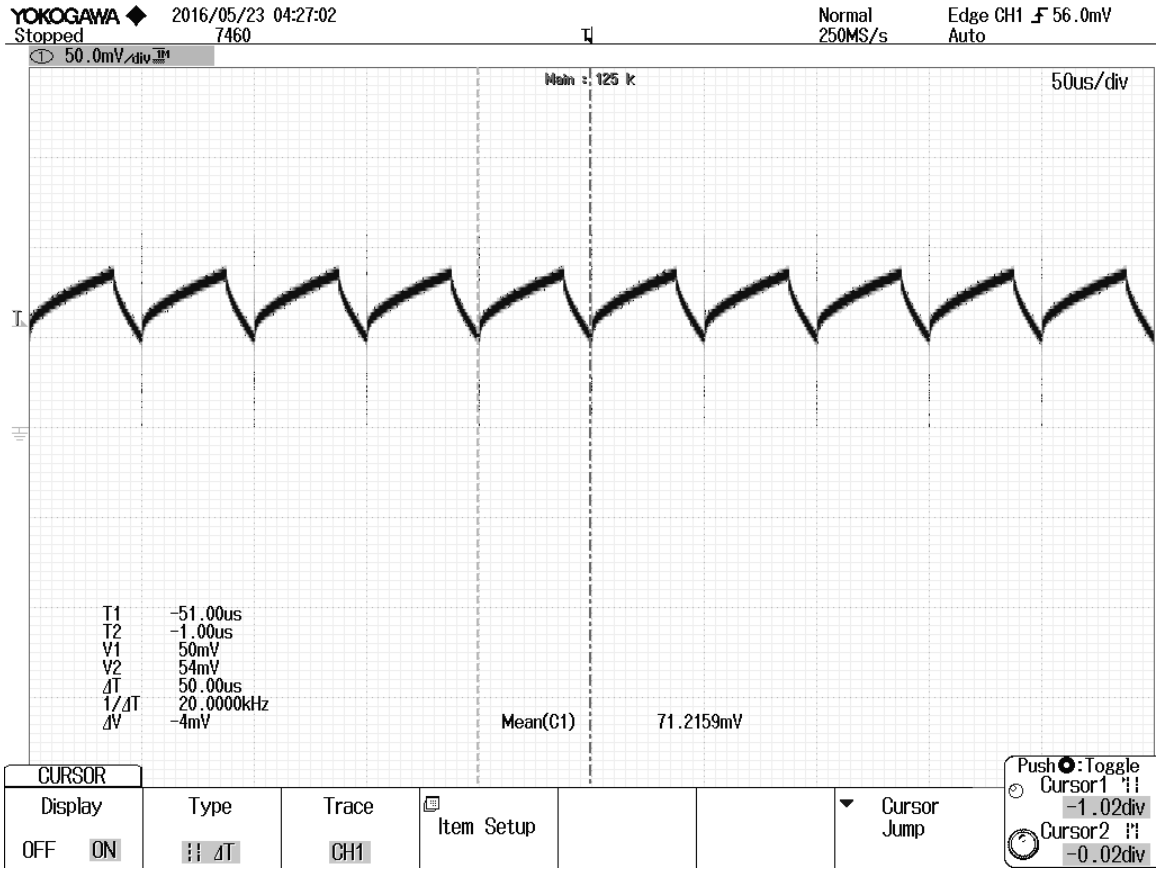


Figure 0A.3: Input current at D = 0.75 for the Cascaded Cuk second stage (Constant Impedance Case)

Also, the output voltage waveforms for each stage for the given operating point are given in Figures A.4 and A.5, where the first stage output is averaged around 38.17 V, yielding a gain of 2.54 vs. an ideal gain of 3 for D = 0.75. On the other hand, second stage average output is 113.14 V, with a gain of 2.96. This difference in gain between both stages is attributed to the higher losses of the first stage compared to its low input voltage, whereas

the second stage input is already amplified and thus its gain is closer to the ideal case at the moderate duty cycle of 0.75.

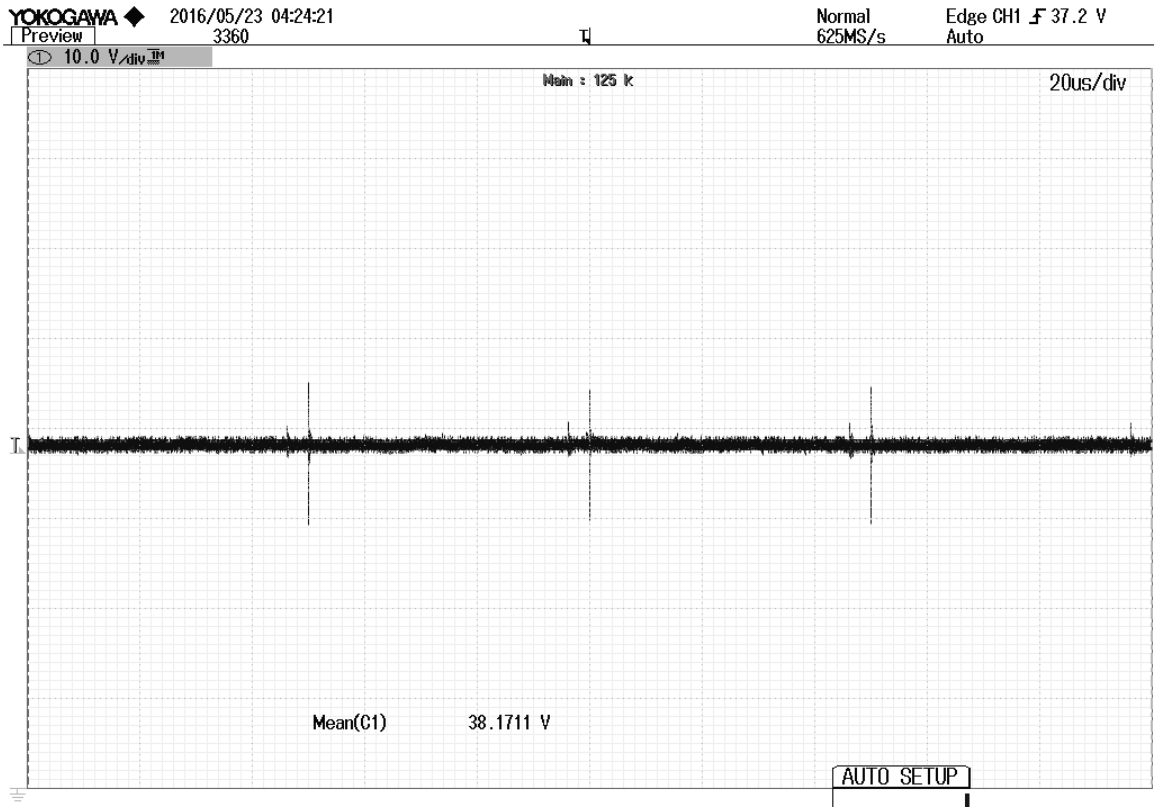


Figure A.4: First stage output voltage for the Cascaded Cuk Converter (D = 0.75, Constant Impedance Load)

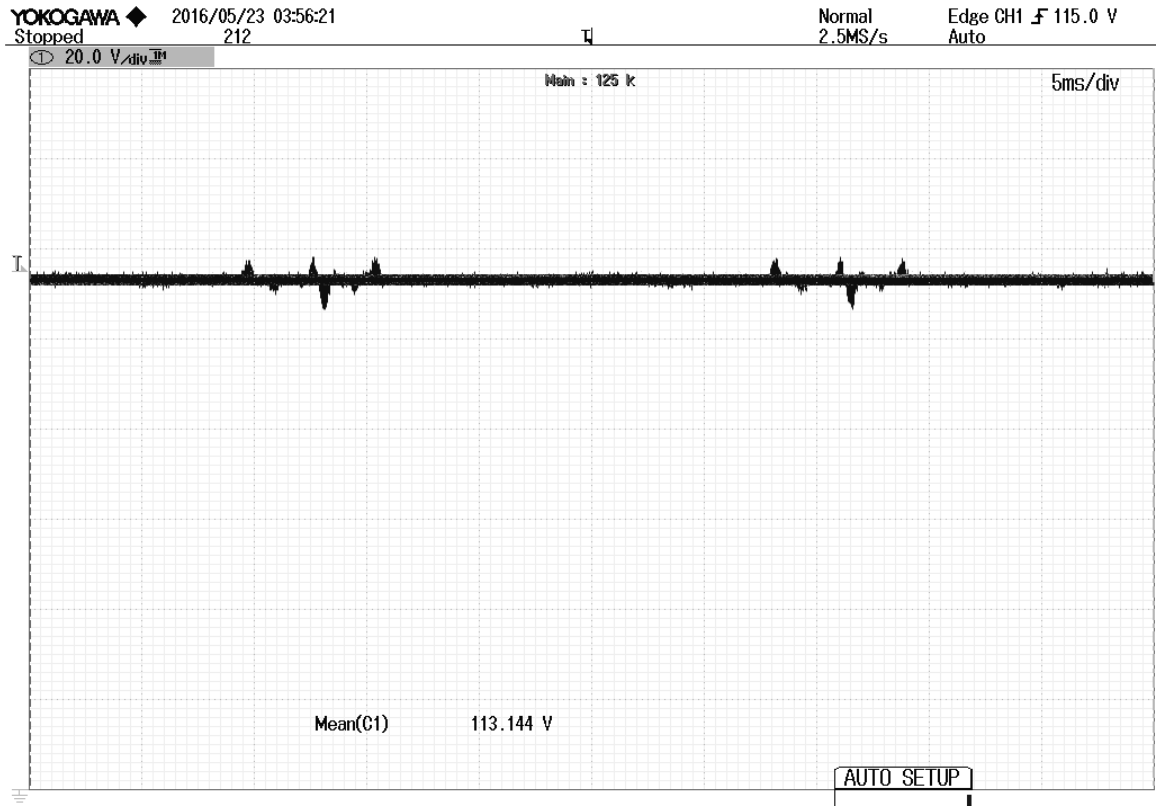


Figure A.5: First stage output voltage for the Cascaded Cuk Converter (D = 0.75, Constant Impedance Load)