ORIGINAL RESEARCH

An ultra-high voltage gain interleaved converter based on three-winding coupled inductor with reduced input current ripple for renewable energy applications

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Abstract
This article proposes an interleaved high step-up DC–DC converter topology designed for renewable energy applications, featuring an ultra-high voltage conversion ratio. The converter employs an interleaved structure, resulting in a low peak-to-peak ripple in the input source current, which is particularly advantageous for solar PV sources. To enhance the output voltage, the topology utilizes voltage multiplier cells (VMC) and coupled inductor techniques. Two coupled inductors with three windings are integrated into the proposed topology, with the secondary and tertiary windings combined with VMC. This combination effectively reduces the maximum voltage stress across power switches, enabling the use of low-rated and cost-effective power switches for implementation. The article offers comprehensive operation modes and steady-state analyses to demonstrate the converter's performance. A comparison is made between the suggested structure and other similar converter topologies. To validate the mathematical analysis, a 200-W prototype is constructed, operating at a frequency of 25 kHz and achieving a voltage conversion range of 20 to 409 V. The experimental results are presented to support the findings.

1 | INTRODUCTION

The immense potential of renewable energy sources to revolutionize the global energy landscape and contribute to a more sustainable future is emphasized [1]. They are recognized as a cleaner alternative to conventional fossil fuels, leading to reduced greenhouse gas emissions and fostering energy independence [2, 3]. Across the world, governments, businesses, and individuals are increasingly adopting renewable energy as a crucial part of their energy mix, driving significant innovation and investment in this rapidly evolving sector [2, 3]. However, renewable energy sources do have limitations, such as their inherent low voltage levels [5]. To address this issue and establish a satisfactory connectivity of these sources, as well as a high-voltage DC link, a high step-up DC–DC converter with a high-voltage gain is deemed necessary [6]. By coupling

a high-voltage DC-bus to high-voltage loads, DC/AC inverters, and DC microgrids, it becomes feasible to overcome the challenges associated with renewable energy sources [7]. One possible approach to tackle these challenges is the utilization of a conventional PWM high step-up topology. This topology is advantageous due to its simplicity in design, modelling, and implementation, as well as its cost-effectiveness, reduced volume, and number of components [8]. However, it should be noted that these converters suffer from a poor voltage gain and experience sustained high-voltage stress [9]. Increasing the duty cycle of the power switch is one approach to raise the output voltage; however, this leads to higher conduction losses and a decrease in power efficiency [10]. To tackle this issue, various high-voltage gain converters have been proposed, including approaches such as voltage multiplier cells (VMC), switched capacitors and inductors, magnetically coupled components like

coupled inductors and high-frequency transformers, as well as multi-stage topologies [11]. Additionally, high step-up converters come in several varieties, such as galvanically isolated/non-isolated, current-fed/voltage-fed, unidirectional/bidirectional, soft or hard switching, and multi-port/single-port designs [11]. For photovoltaic systems, interleaved converters using coupled inductors and a built-in transformer have been suggested in previous studies [12, 13]. These topologies offer advantages like high output voltage, low blocking voltage over power switches, and input current with low ripple. However, it is worth noting that these configurations generally require a higher number of elements compared to other converter types. Non-isolated high step-up configurations designed for renewable energy applications using VMCs and coupled inductors are presented in other research works [14, 15]. Advantages such as sustained input current with low ripple, reduced voltage stress on semiconductors, a lower element count, and improved efficiency are associated with these converters. However, their primary drawback lies in achieving a higher voltage conversion ratio, which necessitates adjusting the turn ratio of the coupled inductors and the duty cycle of the switch to significant values. References [16–18] propose DC–DC converter topologies based on three-winding coupled inductors, offering an elevated voltage conversion ratio and low peak voltage over switches. Nonetheless, these topologies lack a common ground between the output and input ports, and the input current ripple is considerable. Reference [19] suggests a dual input port topology with high-voltage gain, suitable for PV arrays, and capable of supplying the load from various input sources. However, it cannot handle two distinct voltage levels as input sources, and the voltage stress on the switch is considerable. In [20], a VMC-based MIMO structure of a high step-up converter is described. Although it allows for multiple input ports, it requires an additional inductor and power switch for each input port, which can be a disadvantage. For high-voltage applications, a multiport topology with a wider voltage range is presented in [21]. However, this design suffers from significant input current ripple, necessitating the use of filters for each input port, especially in the context of renewable power generation systems. Reference [22] proposes an interleaved high step-up converter that utilizes VMCs and one coupled inductor to couple PV sources to a high-voltage DC bus. Nevertheless, achieving a higher voltage gain in this converter requires the use of a large number of VMCs. In [23], a zero-input current ripple DC–DC converter is introduced with high step-up and soft-switching characteristics, presenting a novel and efficient approach to power conversion. The converter's ability to achieve zero input current ripple, along with its high step-up capability and soft-switching operation, makes it a promising solution for various power electronics applications. Reference [24] introduces the design and implementation of an interleaved converter with a focus on achieving high efficiency and high-voltage gain for seamless integration of renewable energy sources. The proposed converter features a minimum switch count, contributing to reduced cost and improved reliability. The study demonstrates the converter's effectiveness in efficiently harnessing renewable energy and highlights its potential significance in enhancing sustainable energy systems.
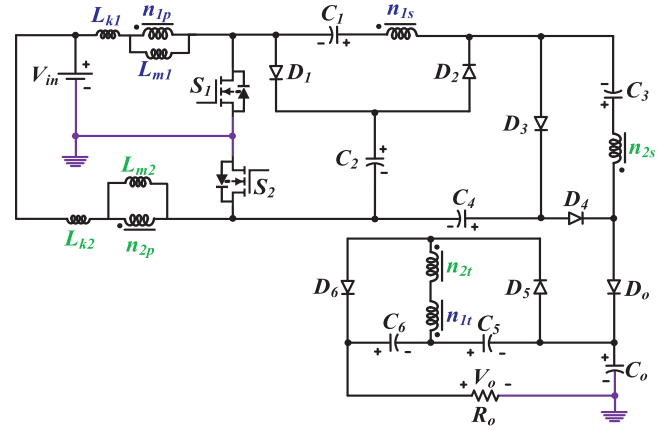

FIGURE 1 The proposed interleaved DC–DC converter.

A multicell non-isolated resonant modular multilevel DC–DC converter is proposed in [25], which incorporates self-voltage balancing and step-up conversion capabilities. The proposed converter offers improved efficiency and enhanced voltage gain, making it well suited for various applications in renewable energy integration. The study highlights the converter's self-voltage balancing feature, ensuring stable and efficient power transfer in multi-cell configurations, thereby contributing to the advancement of sustainable energy systems.

This article proposes an interleaved high step-up DC–DC converter topology with ultra-high voltage conversion ratio for renewable energy applications such as solar power generation systems. Because of the interleaved structure, the input current has a low ripple, which is appropriate for solar PV sources. VMC and coupled inductor approaches are utilized to improve the output voltage. Two coupled inductors with three windings are used in the suggested topology. The coupled inductors' secondary and tertiary windings are combined with voltage multipliers. The highest voltage stress over power switches is decreased because of this combination. As a result, low-rated and low-cost power switches can be used to implement the recommended converter. To demonstrate the proficiency of the suggested topology, operation modes and steady-state analyses are shown. In addition, the presented high step-up topology is contrasted with other interleaved converters of a similar design. Finally, to verify the calculated mathematical equations, a 200-W prototype with a frequency of 25 kHz, an input voltage of 20 V, and an output voltage of 409 V has been built and testing results are reported.

2 | PRESENTED TOPOLOGY AND MODES ANALYSIS

Figure 1 depicts an illustration of the presented converter. This topology comprises two power switches (S_1 and S_2), six power diodes (D_1, D_2, D_3, D_4, D_5, and D_6), two coupled inductors with three windings, and seven capacitors (C_1, C_2, C_3, C_4, C_5, C_6, and C_o). L_{m1} and L_{m2} present the magnetizing, and L_{k1} and L_{k2} are the leakage inductances. Because of the interlaced
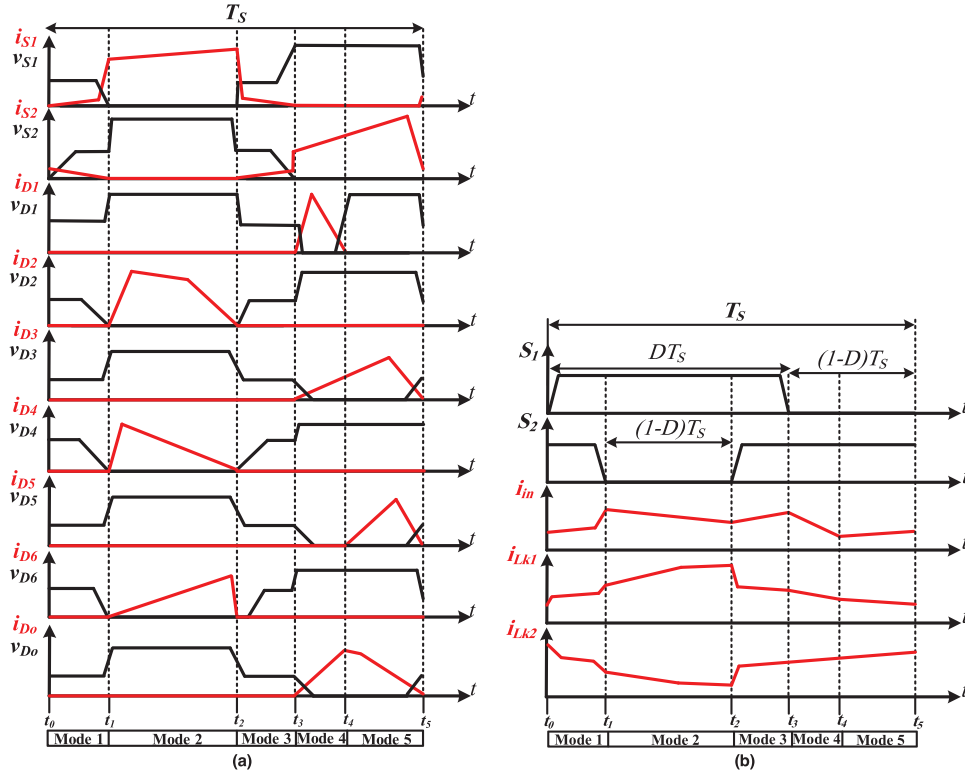
FIGURE 2   The key steady-state waveforms of the presented topology.

design, the input current is divided between L_{k1} and L_{k2}. Also, the switches are derived with 180-degree phase shift. As a result, the peak-to-peak value of the input current is minimized. The turns ratio numbers of the used coupled inductors are defined as $N_1 = n_{1t}/n_{1p} = n_{1s} = n_{1p}$, and $N_2 = n_{2t}/n_{2p} = n_{2s} = n_{2p}$. To consider the leakage influence of the coupled inductors, coupling coefficient (k) is also specified as $k = L_m/(L_m+L_k)$. Based on Figure 1, the secondary and tertiary coupled inductors' windings are merged with VMCs. These combinations lead to an ultra-high voltage gain. C_1 and D_1, C_2 and D_2, C_3 and D_3, C_4 and D_4, C_5 and D_5, and C_6 and D_6 are the used VMCs. Another benefit of the VMCs is acting like a voltage clamp and reducing the maximum blocking voltage over power switches. The waveforms of the semiconductors and inductors are shown in Figure 2. According to this figure, there are five operation mode in each switching period ($T_s = 1/f_s$). These modes have been analyzed throughout the rest of this subsection.

It should be noticed that all of voltage and current equations of Sections 2 and 3 are obtained using the KVL and KCL principles over equivalent circuit of the operational modes which are presented in Figure 3.

Modes 1 and 3 [$t_0 < t < t_1$] & [$t_2 < t < t_3$]: According to Figure 2, modes 1 and 3 operate in the same way. Power switches S_1 and S_2 are turned on during these states. The primary side of the coupled inductors became parallel with input voltage. Therefore, their magnetizing and leakage inductances are charged by V_{in}; all of diodes are reverse biased and are turned OFF. The equivalent circuits of modes 1 and 3 are shown in Figure 3a. Considering the state of diodes, C_1, C_3, and C_6

are charged, and other capacitors are released. The following equations are obtained in modes 1 and 3.

$$V_{L_{k1}} + V_{L_{m1}} = V_{in} \tag{1}$$

$$V_{L_{k2}} + V_{L_{m2}} = V_{in} \tag{2}$$

$$V_o = V_{C_5} + V_{C_6} + V_{C_o} \tag{3}$$

$$i_{in} = i_{L_{k1}} + i_{L_{k2}} = i_{S_1} + i_{S_2} \tag{4}$$

Considering the coupling coefficient (k), the voltage over magnetizing inductances can be presented as (5) and (6).

$$\begin{cases} V_{L_{m1}} = k_1 V_{in} \\ V_{L_{k1}} = (1 - k_1) V_{in} \end{cases} \tag{5}$$

$$\begin{cases} V_{L_{m2}} = k_2 V_{in} \\ V_{L_{k2}} = (1 - k_2) V_{in} \end{cases} \tag{6}$$

Mode 2 [$t_1 < t < t_2$]: Power switch S_2 is switched off at the start of mode 2; however, power switch S_1 remains turned on. The voltage over L_{m2} and L_{k2} became negative, and these inductances are discharged. Stored energy of windings n_{1s} and n_{2s} and capacitors C_2 and C_4 are transferred to capacitors C_1 and C_3. The scheme of this mode is given in Figure 3b, and Equations (7) to (9) are derived.

$$V_{L_{m2}} = k_2 (1 + N_1) V_{in} + k_2 \left(V_{C_2} - V_{C_1} \right) \tag{7}$$
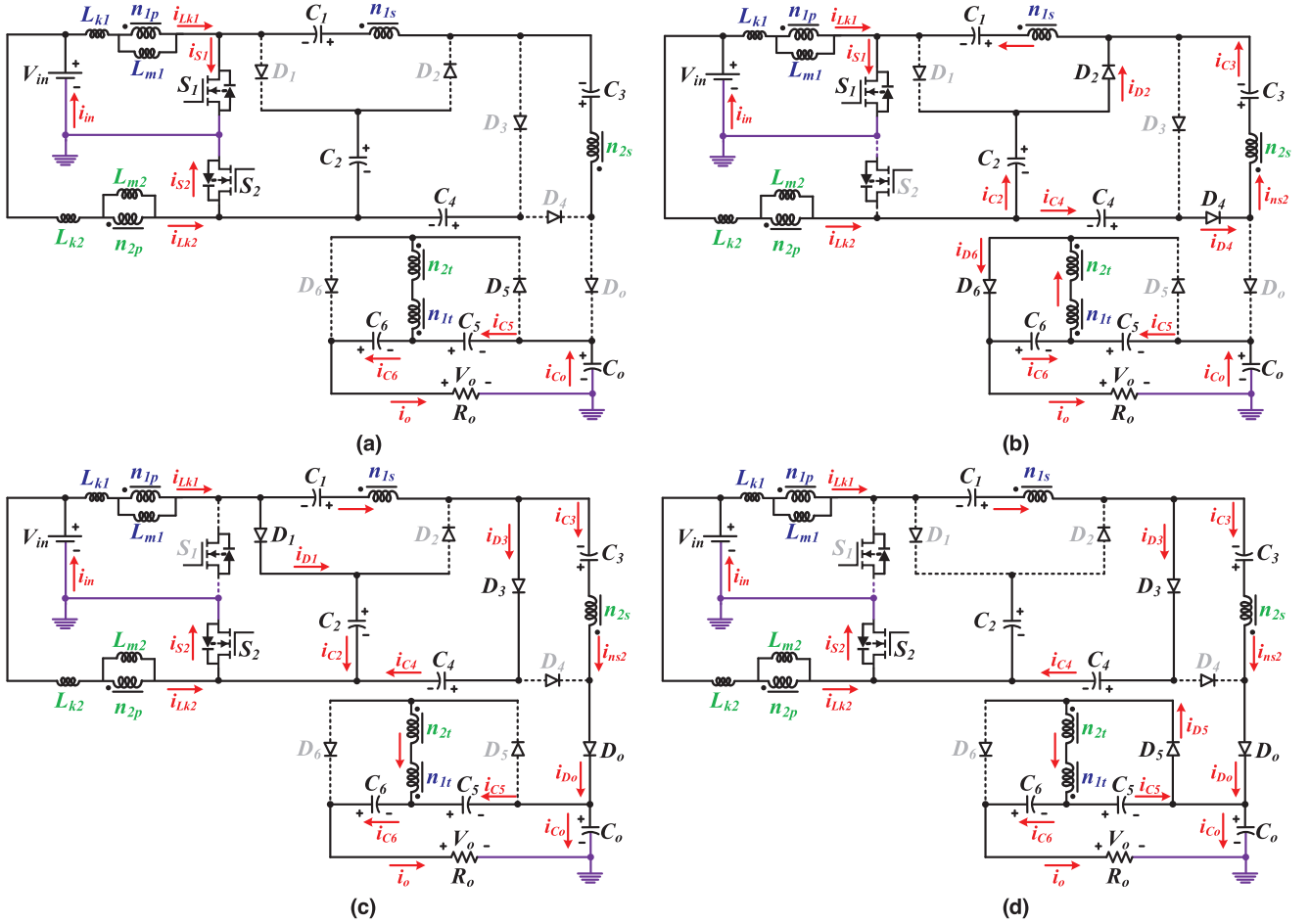
FIGURE 3 The operation modes: (a) 1 and 3, (b) 2, (c) 4, (d) 5.

$$V_{C_6} = N_2 V_{L_{m2}} - N_1 V_{L_{m1}} \tag{8}$$

$$i_{S_1} = i_{in} = i_{L_{k1}} + i_{L_{k2}} \tag{9}$$

Mode 4 [$t_3 < t < t_4$]: This mode starts when switch S_1 is turned OFF, while power switch S_2 is turned ON. During mode 4, inductances L_{k1} and L_{m2} are charged by V_{in}. However, the voltages over L_{k1} and L_{m1} are negative and their currents are reduced. The stored energy in primary winding n_{1p} is transferred to capacitor C_2. Also, stored energy in windings n_{1s} and n_{2s} is transferred to output port through diode D_o. The corresponding circuit of mode 4 is shown in Figure 3c. This mode ends when diode D_1 is turned OFF.

$$V_{L_{m1}} = k_1 \left(V_{in} - V_{C_2} \right) \tag{10}$$

$$N_1 V_{L_{m1}} = V_{C_1} + V_{C_2} - V_{C_4} \tag{11}$$

$$i_{S_2} = i_{in} = i_{L_{k1}} + i_{L_{k2}} \tag{12}$$

$$i_{C_2} = i_{D_1} \tag{13}$$

$$i_{C_3} = -i_{D_o} \tag{14}$$

$$i_{C_6} = -i_o \tag{15}$$

$$i_{D_5} = i_o + i_{C_5} \tag{16}$$

Mode 5 [$t_4 < t < t_5$]: During this mode, diode D_1 is reverse biased, and this is the only difference between mode 5 and mode 4. Figure 3d depicts the identical circuit for this mode.

$$(1 + N_1) V_{L_{m1}} = V_{in} + V_{C_1} - V_{C_4} - V_{L_{k1}} \tag{17}$$

3 | ANAYLSIS OF STEADY-STATE OPERATION

The steady-state analysis of the presented topology is provided in this part. Output voltage, semiconductor and capacitor voltage, and element current are computed for this study. In addition, to facilitate the computation simpler, N_1 and N_2 are considered equal to N, and $k_1 = k_2 = 1$.

3.1 | Voltage calculation

The following equation is determined using the volt-sec balancing principle on L_{m2}:

$$\left\langle V_{L_{m2}} \right\rangle_{T_S} = (2D - 1)V_{in} + (1 - D)[(1 + N)V_{in} + (V_{C_2} - V_{C_1})]$$
$$+ (1 - D)V_{in} = 0 \tag{18}$$

By simplifying (18), the voltage of capacitor C_1 is as (19).

$$V_{C_1} = \frac{2 + N(1 - D)}{1 - D} V_{in} \tag{19}$$

Also, applying volt-sec balance on L_{m1}, the voltage of C_2 is calculated:

$$\left\langle V_{L_{m1}} \right\rangle_{T_S} = (2D - 1)V_{in} + (1 - D)V_{in}$$
$$+ (1 - D)(V_{in} - V_{C_2}) = 0 \tag{20}$$

$$V_{C_2} = \frac{V_{in}}{1 - D} \tag{21}$$

Using (10) and (11), V_{C4} is obtained as follows:

$$V_{C_4} = V_{C_1} + (1 + N)V_{C_2} - NV_{in} = \frac{N + 3}{1 - D} V_{in} \tag{22}$$

Voltage of capacitor C_3 can be calculated using the configuration of the proposed converter at mode 4:

$$V_{C_3} = V_{C_4} - V_{C_2} - N(1 + N)V_{in} + N\left(V_{C_2} - V_{C_1}\right) \tag{23}$$

$$V_{C_3} = \frac{2 + N(1 + N(1 - D))}{1 - D} V_{in} \tag{24}$$

Furthermore, the voltages of capacitors C_6 and C_o are calculated as (25) and (26)

$$V_{C_6} = V_{C_5} = NV_{in} - N(1 + N)V_{in}$$
$$+ N(V_{C_2} - V_{C_1}) = \frac{N}{1 - D} V_{in} \tag{25}$$

$$V_{C_o} = V_{C_4} + V_{C_3} + NV_{in} = \frac{5 + N(3 + N - 2D)}{1 - D} V_{in} \tag{26}$$

Finally, the output voltage can be obtained using (3):

$$V_o = V_{C_6} + V_{C_5} + V_{C_o} = \frac{(5 + 5N) + N(N - 2D)}{1 - D} V_{in}$$
$$M = \frac{V_o}{V_{in}} = \frac{(5 + 5N) + N(N - 2D)}{1 - D} \tag{27}$$

The blocking voltages over power switches S_1 and S_2 are equal to V_{C2}:

$$V_{S_1} = V_{S_2} = \frac{1}{1 - D} V_{in} \tag{28}$$

The blocking voltages over diodes D_1, D_6, and D_o can be obtained at operation mode 2:

$$V_{D_1} = V_{C_1} - NV_{in} = \frac{2}{1 - D} V_{in} \tag{29}$$

$$V_{D_6} = V_{n_{1t}} + V_{n_{2t}} - V_{C_6} = \frac{2N}{1 - D} V_{in} \tag{30}$$

$$V_{D_o} = V_{C_o} - V_{C_4} + V_{L_{m2}} - V_{in}$$
$$\frac{(1 + 2N) + N(N - 2D)}{1 - D} V_{in} \tag{31}$$

The blocking voltage over diode D_3 is equal to V_{D2} and $V_{D5} = V_{D6}$. V_{D2} and V_{D4} are calculated based on operation mode 2. Also, $V_{D3} = V_{D2}$.

$$V_{D_2} = V_{C_4} - V_{C_2} = \frac{N + 2}{1 - D} V_{in} \tag{32}$$

$$V_{D_4} = V_{C_o} - V_{C_4} = \frac{(2 + 2N) + N(N - 2D)}{1 - D} V_{in} \tag{33}$$

The normalized blocking voltages over semiconductors are summarized as follows:

$$\frac{V_{S_1}}{V_o} = \frac{V_{S_2}}{V_o} = \frac{1}{(5 + 5N) + N(N - 2D)} \tag{34}$$

$$\frac{V_{D_1}}{V_o} = \frac{2}{(5 + 5N) + N(N - 2D)} \tag{35}$$

$$\frac{V_{D_2}}{V_o} = \frac{V_{D_3}}{V_o} = \frac{N + 2}{(5 + 5N) + N(N - 2D)} \tag{36}$$

$$\frac{V_{D_4}}{V_o} = \frac{(2N + 2) + N(N - 2D)}{(5 + 5N) + N(N - 2D)} \tag{37}$$

$$\frac{V_{D_5}}{V_o} = \frac{V_{D_6}}{V_o} = \frac{2N}{(5 + 5N) + N(N - 2D)} \tag{38}$$

$$V_{D_o} = \frac{(2N + 1) + N(N - 2D)}{(5 + 5N) + N(N - 2D)} \tag{39}$$

Figures 4a and 4b illustrate the change of output voltage and voltage stresses for different duty cycle (D) and turns ratio number (N) values.

4 | CURRENT CALCULAION

The average value of input current can be expressed versus output current and voltage gain relation:

$$I_{in} = MI_o = \frac{(5 + 5N) + N(N - 2D)}{1 - D} I_o \tag{40}$$

Based on the configuration, and place of capacitors, the average currents of diodes are equal to output current ($I_{D1 \sim Do} = I_o$). Considering the average currents and operation modes of the proposed topology, diodes current stress has been estimated as

$$i_{D_1} = \frac{2(N + 2)}{1 - D} I_o \tag{41}$$

$$i_{D_2} = i_{D_4} = i_{D_5} = i_{D_6} = i_{D_o} = \frac{2}{1 - D} I_o \tag{42}$$
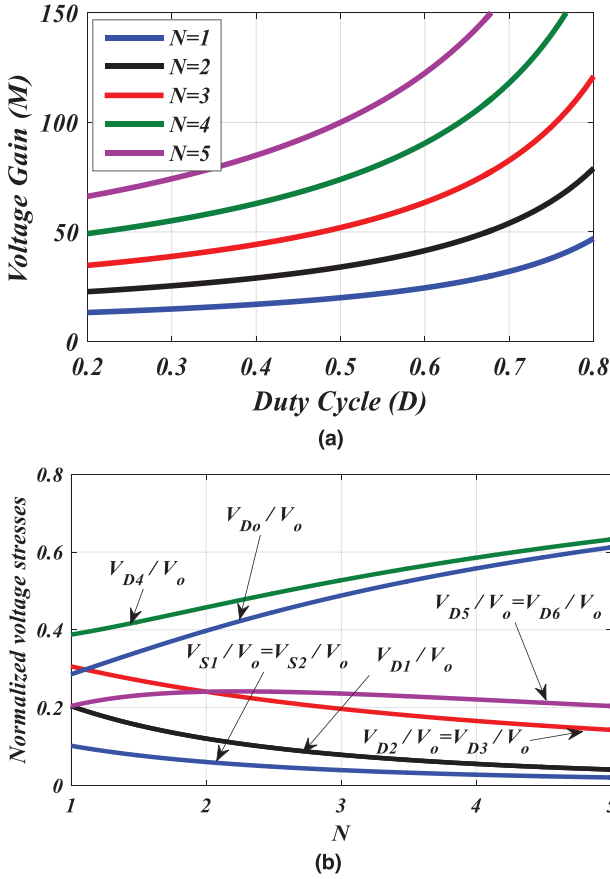
FIGURE 4 (a) Voltage conversion ratio and (b) normalized blocking voltages versus duty cycle (D) and N.

$$i_{D_3} = \frac{1}{1-D}I_o \tag{43}$$

The average currents of power switch S_1 are equal to L_{m1}, and this current can be obtained using currents of diodes D_2 and D_4.

$$I_{S_1}^{avg} = I_{L_{m1}} = i_{D_2} + i_{D_4} = \frac{4}{1-D}I_o \tag{44}$$

The average currents of switch S_2 in L_{m2} are calculated as

$$I_{S_2}^{avg} = I_{L_{m2}} = I_{in} - I_{L_{m1}} = \frac{(1+5N)+N(N-2D)}{1-D}I_o \tag{45}$$

Using average currents, the current stress pathing from power switches S_1 and S_2 is presented as follows:

$$i_{S_1} = \frac{4}{D(1-D)}I_o \tag{46}$$

$$i_{S_2} = \frac{(1+5N)+N(N-2D)}{D(1-D)}I_o \tag{47}$$

Finally, the current of C_1–C_o in each mode is calculated versus diodes and output currents:

$$\begin{cases} i_{C_1}^{S_1:on} = i_{D_2} + i_{D_4} \\ i_{C_1}^{S_1:off} = -(i_{D_3} + i_{D_o}) \end{cases} \tag{48}$$

$$\begin{cases} i_{C_2}^{S_1:on} = -i_{D_2} \\ i_{C_2}^{S_1:off} = i_{D_1} \end{cases} \tag{49}$$

$$\begin{cases} i_{C_3}^{S_1:on} = i_{D_4} \\ i_{C_3}^{S_1:off} = -i_{D_o} \end{cases} \tag{50}$$

$$\begin{cases} i_{C_4}^{S_1:on} = -i_{D_4} \\ i_{C_4}^{S_1:off} = i_{D_3} \end{cases} \tag{51}$$

$$\begin{cases} i_{C_5}^{S_1:on} = i_{C_6}^{S_1:on} = i_{C_o}^{S_1:on} = -I_o \\ i_{C_5}^{S_1:off} = i_{C_5}^{S_1:off} = i_{C_o}^{S_1:off} = \frac{1+D}{1-D}I_o \end{cases} \tag{52}$$

5 | DESIGN CONSIDERATION

The power switches and diodes are selected based on their maximum blocking voltages and pathing current stress, which is calculated in Section 3.

5.1 | Coupled inductors

To design the magnetizing inductances L_{m1} and L_{m2}, the mean current of these inductances is considered higher than half of their current ripples. With this assumption, continuous conduction mode can be obtained. Using calculated standing voltages and average currents, the minimum values of L_{m1} and L_{m2} are as (53) and (54):

$$L_{m_1} \geq \frac{DV_{L_{m1}}}{2f_s I_{L_{m1}}} = \frac{D(1-D)V_{in}}{8f_s I_o} \tag{53}$$

$$L_{m_2} \geq \frac{DV_{L_{m2}}}{2f_s I_{L_{m2}}} = \frac{D(1-D)V_{in}}{2f_s[(1+5N)+N(N-2D)]I_o} \tag{54}$$

5.2 | Capacitors

To reduce the voltage ripple over capacitors, the presented assumption in (55) is used:

$$\Delta V_{C_{1\sim o}} \leq 2\% V_{C_{1\sim o}} \tag{55}$$

The minimum capacitors (C_1–C_o) values are determined using computed standing voltages and pathing currents:

$$C_1 \geq \frac{2DI_o}{1\% f_s[2+N(1-D)]V_{in}} \tag{56}$$

$$C_2 \geq \frac{D(2N+1)I_o}{1\% f_s V_{in}} \tag{57}$$

$$C_3 \geq \frac{DI_o}{1\% f_s[2+N(1+N(1-D))]V_{in}} \tag{58}$$

TABLE 1 Comparison results.

Topologies	Number of elements					Voltage gain	Max volt. switches	Max volt. diodes	Common ground	Method
	Cores	C*	S*	D*	Total					
[1]	3	6	3	10	22	$\frac{1+3N}{1-D}$ $= 10$	$\frac{1}{1+3N}$ $= 0.25$	$\frac{1+4N}{1+3N}$ $= 1.25$	Yes	VMC + CL*
[4]	6	8	6	14	34	$\frac{3+D}{1-D}$ $= 9$	$\frac{1}{3+D}$ $= 0.27$	$\frac{2}{3+D}$ $= 0.55$	No	VMC
[6]	4	7	4	6	21	$\frac{2(1+N)}{1-D}$ $= 10$	$\frac{1}{2(1+N)}$ $= 0.25$	$\frac{1+2N}{2(1+N)}$ $= 0.75$	Yes	VMC + CL
[7]	3	7	4	6	20	$\frac{2+4N}{1-D}$ $= 15$	$\frac{1}{2+4N}$ $= 0.16$	$\frac{1}{2}$	Yes	VMC + BT + CL
[8]	3	5	2	6	16	$\frac{2(1+N)}{1-D}$ $= 10$	$\frac{1}{2(1+N)}$ $= 0.25$	$\frac{1+2N}{2(1+N)}$ $= 0.75$	Yes	VMC + BT
[9]	2	7	2	8	19	$\frac{1+3N}{1-D}$ $= 10$	$\frac{1}{1+3N}$ $= 0.25$	$\frac{2N}{1+3N}$ $= 0.5$	Yes	VMC + CL
[13]	3	5	2	6	16	$\frac{2+3N}{1-D}$ $= 12.5$	$\frac{1}{2+3N}$ $= 0.2$	$\frac{1+3N}{2+3N}$ $= 0.8$	Yes	VMC + BT*+ CL
[22]	2	7	2	7	18	$\frac{2(1+N)}{1-D}$ $= 10$	$\frac{1}{2(1+N)}$ $= 0.25$	$\frac{1}{(1+N)}$ $= 0.5$	No	VMC + CL
Proposed	2	7	2	7	18	$\frac{(5+5N)+N(N-2D)}{1-D}$ $= 24.5$	$\frac{1}{(5+5N)+N(N-2D)}$ $= 0.1$	$\frac{(2N+2)+N(N-2D)}{(5+5N)+N(N-2D)}$ $= 0.38$	Yes	VMC + CL

C, capacitors; S, power switches; D, diodes; CL, coupled inductor; BT, built in transformer, D = 0.6, N = 1.

$$C_4 \geq \frac{DI_o}{1\% f_s (N+3) V_{in}} \tag{59}$$

$$C_5 = C_6 \geq \frac{(1+D) I_o}{2\% f_s N V_{in}} \tag{60}$$

$$C_o \geq \frac{(1+D) I_o}{2\% f_s [5 + N (3 + N - 2D)] V_{in}} \tag{61}$$

6 | COMPARISON WITH OTHER TOPOLOGIES

This section compares the presented topology to the other interleaved converter topologies. Table 1 provides an overview of comparison. The technique utilized to propagate the output voltage, maximum blocking voltage across switches and diodes, voltage gain, common ground, and component count is all considered. Based on Table 1, the number of magnetic cores in [4] is higher than others, where six magnetic cores are used. Thus, the cost and volume of this converter are not suitable. Also, in [4] and [6, 7], six and four power switches are used, which are more than other converters. Furthermore, the total number of used components in [8] and [13] is lowest. However, in both topologies, three magnetic cores are utilized, which is more than the recommended structure. The comparison of voltage gain versus diverse duty cycle values and constant N ($N = 1$) are shown in Figure 5a. The proposed converter offers an ultra-voltage gain, which is higher than others. For one case ($N = 1$, $D = 0.6$), the value of proposed converter's voltage gain is equal to 24.5. The nearest value of the voltage gain among the converters men-

tioned in Table 1 is related to the converter [7]. The voltage gain of this topology for $N = 1$, $D = 0.6$ is obtained as 15. The comparison of maximum blocking voltages over semiconductors vs various turns ratio values of numbers and $D = 0.6$ are depicted in Figures 5b and 5c. The maximum blocking voltage on switches in the converter [4] is constant versus turns ratio number, and is higher than other topologies. Also, the suggested topology offers lowest V_S/V_o. Due to low blocking voltage over power switches, low rated switches are utilized for implementing the suggested topology. This benefit can reduce the total cost. Based on Figure 5c, for $N < 2$, the maximum blocking voltage of the recommended topology is lower than others. But, for $N > 2$, V_D/V_o of converters in [7] and [22] is reduced. The suggested converter, on the other hand, has a higher voltage conversion ratio than [7] and [22]. Also, operating with high value of turns ratio can increase the conduction loss and reduce the efficiency.

7 | EXPERIMENTAL RESULTS

A hardware prototype with 200-W power has been developed in the laboratory to confirm the theoretical and computational calculations. The experimental setup is shown in Figure 6. Also, the components' requirements used in the prototype are given in Table 2. The duty cycle of S_1 and S_2 is equal to 0.55, which is constant during the test. A STM32H743Vit6 microcontroller board is used to generate PWM pulses of the switches. The obtained waveforms from the prototype test are presented in the rest of this section. The primary side currents of the two coupled inductors are depicted in Figure 7. The input DC
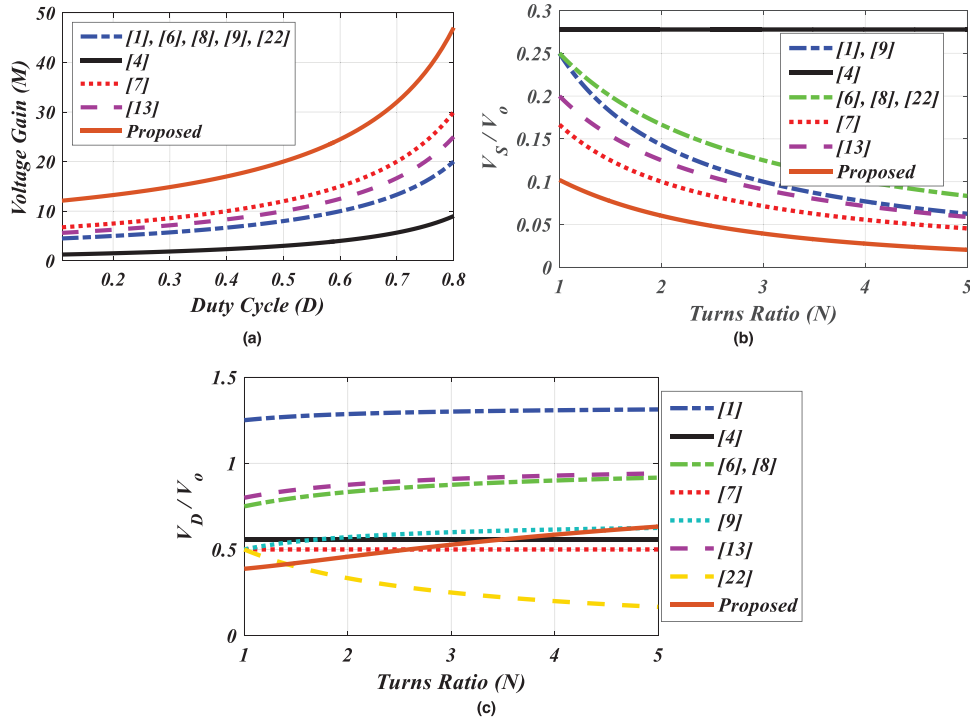
FIGURE 5 Comparison results: (a) voltage gain for $N = 1$, (b) maximum V_S/V_o for $D = 0.6$, (c) maximum V_D/V_o for $D = 0.6$.
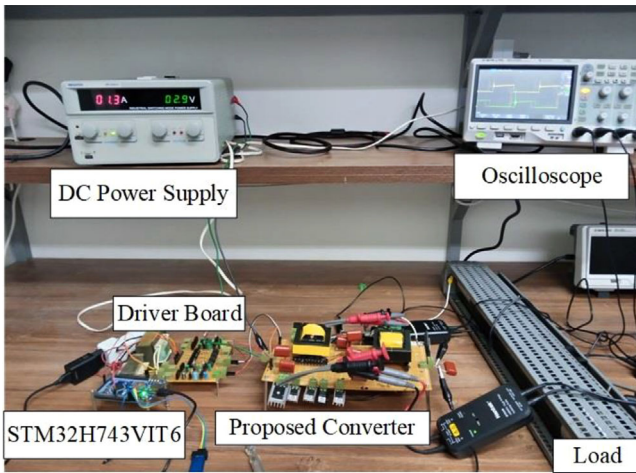

FIGURE 6 The experimental setup.

FIGURE 7 Current waveforms (i_{in}, i_{Lk1}, and i_{Lk2}).
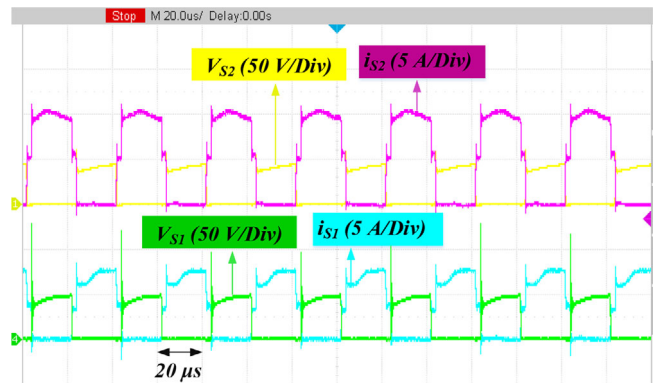
FIGURE 8 Current and voltage waveforms of switches.

source current is the sum of the two mentioned currents, which can be seen in this figure. The average value of i_{in} is 10 A, and approximately equal to theoretical value. Figure 8 demonstrates the voltage and current of power switches. The gate pulses of the switches have 180 degrees phase difference, and their duty cycle is 0.55. Thus, these switches are turned OFF for 45% of the switching period. Based on this figure, the maximum blocking voltages across the switches S_1 and S_2 are 49 and 44 V, respectively. Also, the current stress for switches S_1 and S_2 is 8 and 10.5 A, respectively. Figure 9 represents the voltage of diodes. The voltage over the diode D_1 is 83 V. This value con-
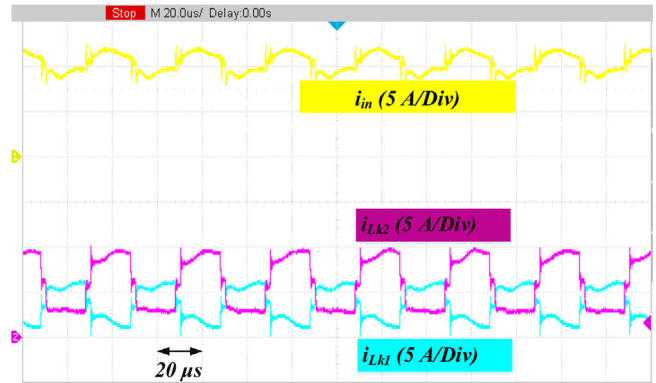
TABLE 2 Components and specification of the laboratory prototype.

Element	Specification
S_1 and S_2	IRFP260
D_1, D_2, D_3, D_4, D_5, D_6, and D_o	MUR1560
C_1 and C_4	Polyester (250 Volt/2*2.2μF)
C_2, C_3, C_5, C_6, and C_o	Polyester (250 Volt/2.2μF)
Coupled inductors	EE55 Ferrite Core, $N_1{:}N_2$ = 1:1, $L_m = 243 \mu$H

Parameter	Value
P_o	200 W
V_{in}	20 V
V_o	409 V
f_s	25 kHz
Duty cycles	$D_1 = D_2 = D = 0.55$

FIGURE 10 Diodes voltage waveforms (V_{D5}, V_{D6}, and V_{Do}).

FIGURE 9 Diodes voltage waveforms (V_{D1}, V_{D2}, V_{D3}, and V_{D4}).

FIGURE 11 Capacitors voltage waveforms (V_{C1}, V_{C2}, V_{C3}, and V_{C4}).
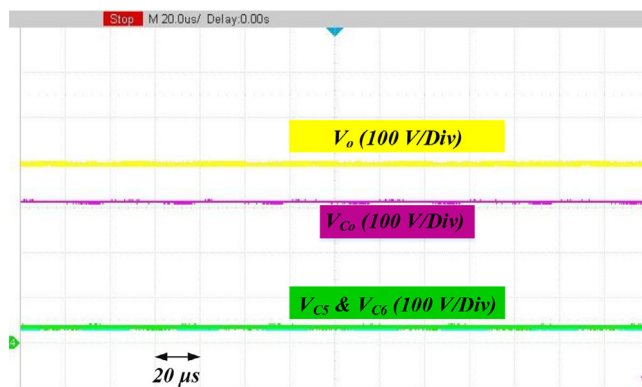
FIGURE 12 Voltages waveforms (V_o, V_{Co}, V_{C5}, and V_{C6}).

firms Equation (29). The voltage over diodes D_2 and D_3 is almost equal and about 122 V. Therefore, Equations (32) and (36) are verified. The voltage of output diode D_o is obtained as almost 123 V, and V_{D4} is measured as 163 V. These values also confirm Equations (31) and (33), respectively. The voltage waveforms of diodes D_5 and D_6 are complementary, and their maximum value is 88 V. These waveforms are shown in Figure 10. Among the used diodes in the proposed converter, D_4 suffers from highest blocking voltage (about 163 V), and the experimental normalized voltage stress of this diode is equal to 0.4. The voltage of C_1, C_2, C_3, and C_4 are measured using isolated probes, which are 100, 40, 145, and 165 V, respectively. These waveforms are shown in Figure 11. The voltage waveforms of capacitors C_5, C_6, and C_o are shown in Figure 12, and their values are 40, 40, and 329 V. According to theoretical calculations (Equation (25)) and experimental results, the voltages over capacitors C_5 and C_6 are equal. The value of the output voltage is equal to the sum of the voltages of capacitors, C_5, C_6, and C_o which is also shown in Figure 12. The output voltage is 409 V, indicating that the experimental voltage gain of the proposed converter is 20.45. The voltage waveform of the capacitors demonstrates that, despite the use of low-capacity capacitors in this converter, the voltage ripples of the capaci-
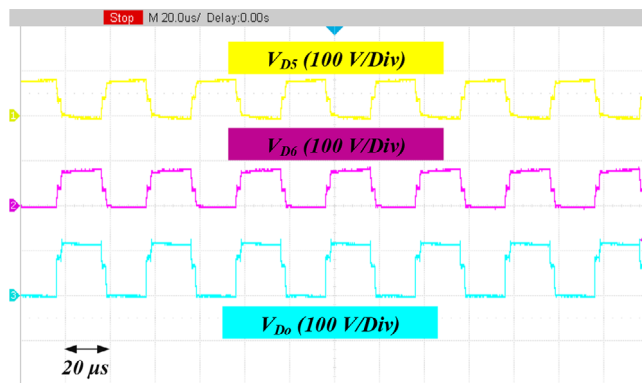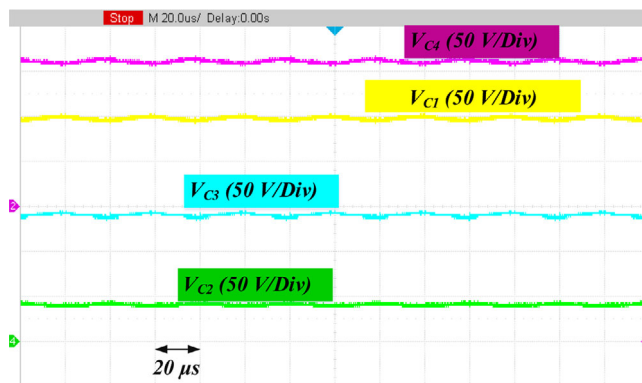
tors are measured at low values. Furthermore, because of the minimal input current ripple and ultra-high voltage gain, the proposed design could be an appropriate solution for integrating renewable energies like PV panels with a high-voltage DC connection. The measured efficiency of the presented topology is shown in Figure 13. This curve shows the variation of efficiency versus output power. The power range is set from 50 W to rated power (200 W). The efficiency at rated power is measured 93.38%. The highest efficiency is 94.65 %. For P_o = 50 to 200 W, the efficiency is higher than 93%.
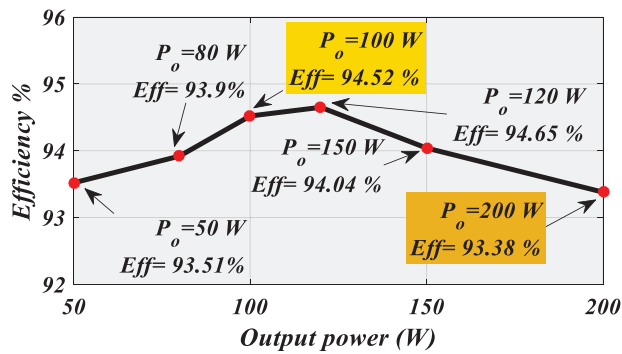
FIGURE 13   Efficiency versus output power.

8 | CONCLUSION

A topology of interleaved high step-up topology with an ultra-high voltage gain is presented in this article for applications involving renewable energies systems. The input current has a low ripple due to the interleaved design, making it suitable for PV sources. To enhance the output voltage, VMC and coupled inductor techniques are used. In the proposed topology, two coupled inductors with three windings are employed. Secondary and tertiary windings are paired with VMC. This combination reduces the maximum voltage stress across power switches. As a consequence, low-rated and low-cost power switches can be used to set up the presented topology. To show the effectiveness of the designed topology, operating modes and steady-state analyses are provided, as well as comparisons with other similar interleaved topologies. Finally, a 200-W prototype with $f_s = 25$ kHz, voltage conversion of 20 to 409 V, and 93.38 % efficiency at rate power is built for the purpose of validating mathematical computations, and experimental findings are provided. The maximum efficiency is obtained 94.52% at $P_o = 120$ W.

AUTHOR CONTRIBUTIONS
Seyed Majid Hashemzadeh: Conceptualization; data curation; formal analysis; software; writing—original draft; writing—review & editing. **Hadi Aghaei**: Conceptualization; data curation; resources; software; validation; visualization; writing—original draft; writing—review & editing. **Vafa Marzang**: Formal analysis; writing—original draft; writing—review & editing. **Atif Iqbal**: Project administration; supervision; validation; writing—original draft; writing—review & editing. **Ebrahim Babaei**: Supervision; validation; writing—review & editing. **Seyed Hossein Hosseini**: Project administration; supervision; writing—review & editing. **Shirazul Islam**: Data curation; formal analysis; writing—review & editing.

CONFLICT OF INTEREST STATEMENT
The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT
The data that support the findings of this study are available from the corresponding author upon reasonable request.

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