Received: 9 April 2023 | Revised: 20 June 2023 | Accepted: 15 July 2023

IET Power Electronics

DOI: 10.1049/pel2.12561

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

Triple boost switched capacitor multilevel inverter (TB-SCMLI) with reduced components and self-voltage balance

Md. Reyaz Hussan[1] | **Mohammed A. Al-Hitmi**[2] | **Marif Daula Siddique**[3] | **Shirazul Islam**[2] | **Atif Iqbal**[2]

[1]Department of Electrical Engineering, Zakir Husain College of Engineering and Technology, Aligarh Muslim University, Aligarh, Uttar Pradesh, India

[2]Department of Electrical Engineering, Qatar University, Doha, Qatar

[3]Department of Electrical Engineering, National University of Singapore (NUS), Singapore, Singapore

Correspondence
Mohammed A. Al-Hitmi, Department of Electrical Engineering, Qatar University, Doha, Qatar.
Email: m.a.alhitmi@qu.edu.qa

Funding information
Qatar University, Grant/Award Number: QUCP-CENG-2022-571

Abstract

Multi-level inverter (MLIs) designs with switched-capacitor (SC) are on the rise due to their applicability in sustainable energy systems and high voltage applications. In this light, this paper presents a compact triple-boost switched-capacitor multilevel inverter (TB-SCMLI) topology with fewer switches and self-voltage balancing capacitors. Large spikes appear in the source current and charging currents of switched-capacitors as a result of the charging and discharging actions of the switched capacitors. In order to suppress the spikes in the source and charging currents of switched-capacitors, the proposed converter incorporates a soft switching circuit. The soft charging circuit consists of an inductor and a diode in the charging path of the proposed converter to ensure soft charging of the switched-capacitors. By inserting a small value of inductance in the soft charging circuit, the proposed converter can significantly suppress source current spikes. The proposed TB-SCMLI is able to provide seven levels of output voltage by balancing the voltage of two capacitors with the given control logic. The various SCMLIs are evaluated to determine the contribution of the suggested TB-SCMLI topology's merits and downsides. To validate the performance of the proposed TB-SCMLI, comprehensive experimental findings under various laboratory test settings have been given.

1 | INTRODUCTION

The multilevel inverters (MLIs) are responsible for the conversion of direct current (dc) to alternating current (ac), which is involved in the photovoltaic (PV) cells and fuel cell types of renewable energy system (RES) [1–3]. MLIs have developed into critical power devices, with widespread use in distributed generation systems, electric vehicles, uninterruptible power supplies, and motor drives. MLIs have a number of advantages, the most important of which are their higher voltage operation with a lower voltage stress on switches, lower switching losses, reduced dv/dt, and enhanced harmonic profile of the output voltage. Over the course of the past few decades, several different models of conventional MLIs, including the cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC), have been presented [4, 5].

The increase in output levels is due to a cumulative effect brought on by increasing the number of isolated dc sources in CHB, clamping diodes in FC, and capacitors in NPC. NPC needs a lot of clamp diodes and power switches to be able to make more output levels. Also, there is a problem with the way the voltage of NPC's capacitors is not balanced. In the same way, FC needs a lot of capacitors, so it will be expensive if it generates higher levels. In low-frequency applications, capacitors also need to have a lot of storage space. In this situation, NPC is better than FC. CHB is different from NPC and FC in that it does not use clamping diodes and has a low voltage stress. But CHB needs a number of separate power sources. When using RES, the voltage must be increased in order to support the applications that require a higher voltage. On the load side, either a dc-dc boost converter is needed after the input or a transformer in order to produce a greater magnitude or a boosted output voltage. All of these factors result in inverter systems that are intricate, cumbersome, and prohibitively expensive [6, 7]. For the generation of higher voltage levels, two half-bridges are utilized to adjust the polarity of a single-phase load for ac voltage

generation [8–10]. As a result, this sort of multilevel inverter is only appropriate for cascaded systems with at least three separate DC sources for three-phase operation. Moreover, it is not viable for grid-connected solar PV applications since the ac output neutral is linked to a half-bridge, which produces leakage current in the PV cell due to common mode voltage [11].

Several initiatives are currently underway to generate high voltage levels with reduced components, fewer dc sources, self-voltage balancing features, and boosting capabilities. As a device that produces intermediate levels, capacitors have attracted significant interest. Flying capacitors (FCs) are necessary for creating intermediate voltage levels in the hybrid MLI. To maintain the requisite capacitor voltages, however, complex control circuitry is required. In addition, only 50% of the source voltage is produced at the load terminals. Consequently, subsequent efforts are undertaken to increase the output voltage without using inductors or transformers across the output terminals. Switched capacitor-based voltage boost structures are recommended for creating the proper voltage for low- or medium-voltage applications, as these power sources often provide low voltage. In these configurations, a parallel connection of the capacitor to the isolated DC voltage source will charge the capacitor, while a series connection will discharge it. When coupled in series, switched-capacitor sub-modules enhance the magnitude of the output voltage [12–14]. In 1989, Ronald Marusarz [15] introduced the idea of the switched-capacitor. Since then, other switched-capacitor-based MLIs have been proposed in the scientific literature, each with its own merits and shortcomings.

Novel multilevel inverters based on the switched-capacitor concept have been published in the literature as a means of addressing these problems. Using the capacitors as a virtual power supply instead of the isolated sources in the inverters is a smart option. The capacitor in switched-capacitors (SCs) is charged in parallel with the power source. The high voltage gain is achieved by connecting the capacitor and power supply in series, which eliminates the need for bulky inductance components. In addition to boosting the voltage at the input, the switched-capacitor MLI (SCMLI) has the ability to effectively raise the levels of voltage at the output [16–18]. A quadruple boost SCMLI has been presented in [19], which requires 12 switches, 3 capacitors, and 2 diodes to generate 17-levels at the output. Switching losses are reduced here as more than 50% of the switches operate at low frequencies. A quintuple voltage boosting 11-level SCMLI topology has been presented in [20]. The suggested basic design has one DC source, nine switches, nine gate-driver circuits, four capacitors, and five diodes. A grid-tied single-phase single-stage PV system interfaced with a novel 17-level MLI is presented in [21]. In order to generate higher voltage levels, an SCMLI with extending ability and a reduced number of switches in comparison to other same level topologies is presented in [22].

Depending upon the gain of SCMLI, the topologies used to generate 7-level single phase ac output voltage are broadly classified into two categories. The SCMLIs having a voltage gain of 1.5 are reported in [7, 23–28] while converters having a voltage gain of 3 are reported in [6, 29–32]. The converters suggested in [6, 7] require more than one input source which may not be a viable option in certain applications. Further, the requirement for multiple sources increases the cost of the converter. A cascaded H-bridge arrangement is used in [26] to generate a 7-level output ac voltage. However, the presented converter requires an auxiliary circuit or complex control strategies to maintain voltage balancing across the capacitor. To maintain the self-voltage balancing across the capacitors, an improved 7-level triple boost SCMLI (TB-SCMLI) configuration is proposed in this paper. The proposed converter is able to maintain self-voltage balancing across the capacitors even at low values of modulation index and during variations in operating frequency of the converter. It utilizes a single DC source, 9 unidirectional switches, 2 capacitors and a diode. Four pair of switches, (S_1, S_2), (S_3, S_4), (S_6, S_7), (S_8, S_9), are complementary in nature, which eases the control complexity. The per unit total standing voltage of the TB-SCMLI is quite low in comparison to most of the topologies present in literature. The proposed converter is considered as a suitable candidate for the applications requiring voltage boost action. To validate the viability of the proposed converter, a comparative analysis of the proposed converter with state-of-the-art converters reported in the literature with reference to various parameters is discussed in the subsequent section of this paper.

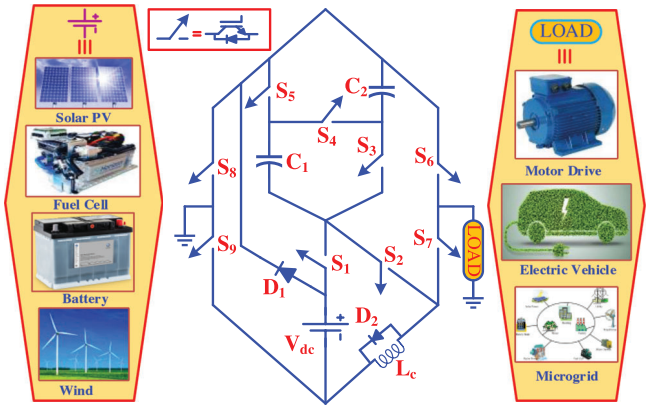

FIGURE 1 Topology configuration of the proposed TB-SCMLI.

2 | PROPOSED 13L SCMLI TOPOLOGY

2.1 | Description of the proposed 7L topology

Figure 1 shows the proposed single-phase 7-level triple-boost SCMLI (TB-SCMLI), which employs a single input source (V_{dc}), 9 switches (S_1–S_9), a single diode (D), and two capacitors (C_1 and C_2). All the nine switches are unidirectional switches with antiparallel diodes. The concept of switched-capacitors is implemented into the architecture to charge and discharge each capacitor when linked in parallel and series to the DC voltage source, respectively. Regardless of the single voltage source, the proposed topology yields a peak voltage amplitude of $3V_{dc}$ by utilizing the charging of capacitors C_1 and C_2 to V_{dc} (V_{dc} being

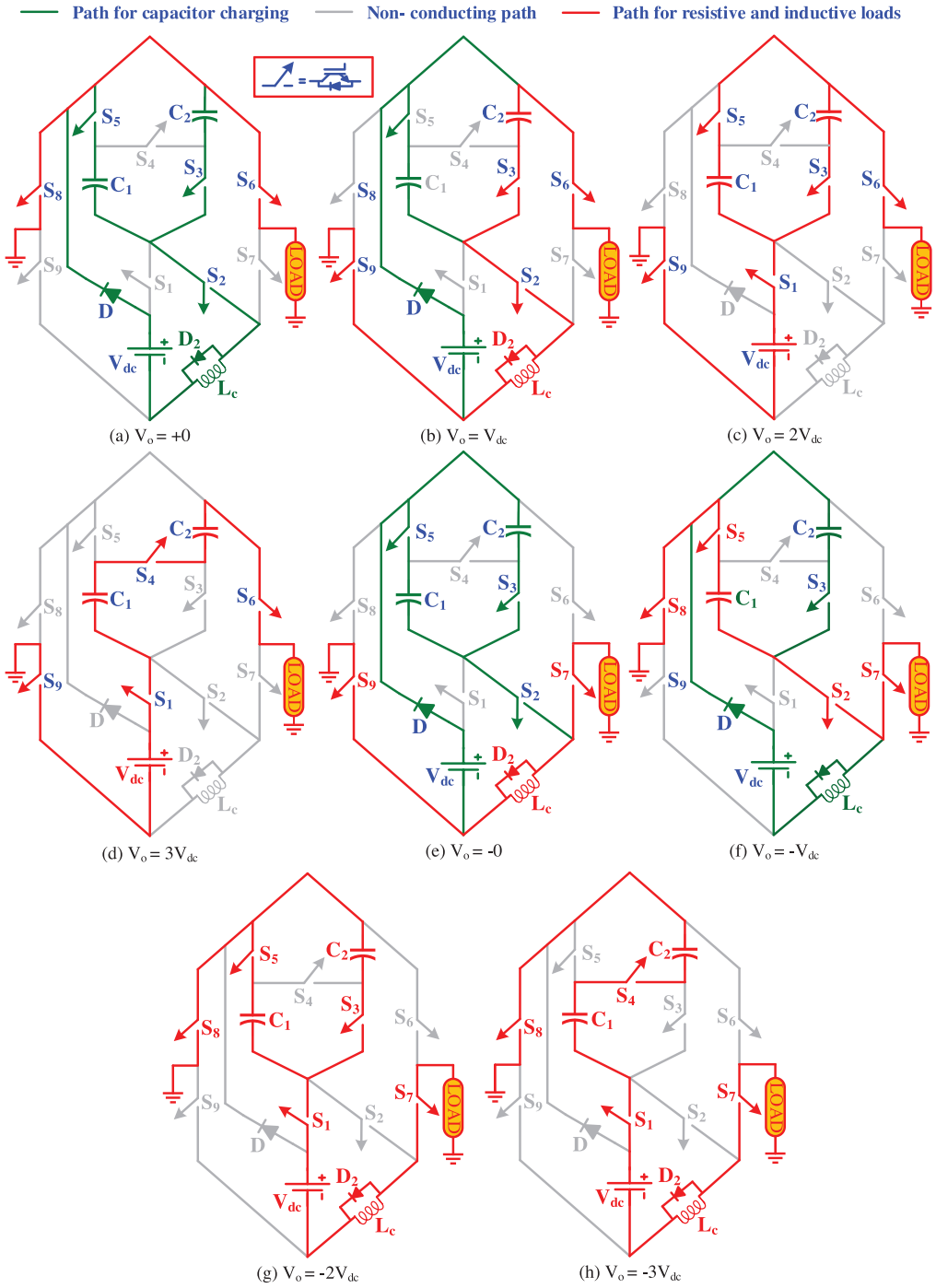

FIGURE 2 Operating states of the proposed 7L TB-SCMLI at the positive levels.

the source voltage), which is a noteworthy aspect of the proposed work. Switches S_1–S_5 block the voltage of V_{dc}, while the switches S_6–S_9 need to block the voltage of $3V_{dc}$. As shown in Figure 1, the proposed inverter can be a viable option for solar PV, electric vehicles, fuel cells, battery power applications, wind energy, motor drives, and other applications. Detailed circuit analysis showing the positive states of the proposed topology is illustrated in Figure 2. All other states can be easily visualized using the switching logic presented in Table 1. Table 2 indicates the voltage stress across switches during each voltage level.

2.2 | Analysis of self-voltage balancing of capacitors

Self-voltage balance is one of the most desirable qualities of SC-based converters as the voltage/current sensor(s) are not being

TABLE 1 Switching states for the proposed 7L TB-SCMLI.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	C_1	C_2	V_{out} ($\times V_{dc}$)
1	0	0	1	0	1	0	0	1	D	D	+3
1	0	1	0	1	1	0	0	1	D	D	+2
0	1	1	0	1	1	0	0	1	C	C	+1
0	1	1	0	1	1	0	1	0	C	C	0
0	1	1	0	1	0	1	0	1			
0	1	1	0	1	0	1	1	0	C	C	−1
1	0	1	0	1	0	1	1	0	D	D	−2
1	0	0	1	0	0	1	1	0	D	D	−3

Note: 1, ON state of the switch; 0, OFF state of the switch; C/D, charging/discharging of the capacitor.

TABLE 2 Voltage stress across switches during each voltage level.

	[0]	[+1]	[+2]	[+3]	[−1]	[−2]	[−3]
S_1	V_{dc}	V_{dc}	0	0	V_{dc}	0	0
S_2	0	0	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}
S_3	0	0	0	V_{dc}	0	0	V_{dc}
S_4	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}	0
S_5	0	0	0	V_{dc}	0	0	V_{dc}
S_6	0	V_{dc}	$2V_{dc}$	$3V_{dc}$	0	0	0
S_7	V_{dc}	0	V_{dc}	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
S_8	0	0	0	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
S_9	V_{dc}	V_{dc}	$2V_{dc}$	$3V_{dc}$	0	0	0

used. Capacitors C_1 and C_2 are self-balanced in the proposed triple-boost SCMLI utilizing a mechanism based on their series-parallel connection with the dc source. Capacitors C_1 and C_2 are in parallel to the dc source at the output levels of zero, and $\pm V_{dc}$ as given in Table 1. For the $\pm 2V_{dc}$ output voltage, either C_1 or C_2 is in series with the dc source. Finally both C_1 and C_2 are discharged in series with the dc source to generate $\pm 3V_{dc}$ output voltage. The charging and discharging cycles of capacitors C_1 and C_2 for a complete cycle are depicted in Figure 3. Fast charging of capacitors C_1 and C_2 is ensured by the fact that the total charge path time constant caused by parasitic elements is smaller than the time interval between each voltage level. From the discharge pattern of capacitors, C_1 and C_2 shown in Figure 4, the capacitors, C_1 and C_2 are discharged during the time interval t_2 to t_2'. The magnitude of ripple voltage, Δv_{c1} and Δv_{c2} appearing across the charge supplied by the capacitor, C_1 during this period is,

$$\Delta v_{c1} = \Delta v_{c2} = \frac{\Delta Q_{c1}}{C_1} = \frac{\Delta Q_{c2}}{C_2} = \frac{1}{C_1}\int_{t_2}^{t'_2} i_o dt = \frac{1}{C_2}\int_{t_2}^{t'_2} i_o dt \quad (1)$$

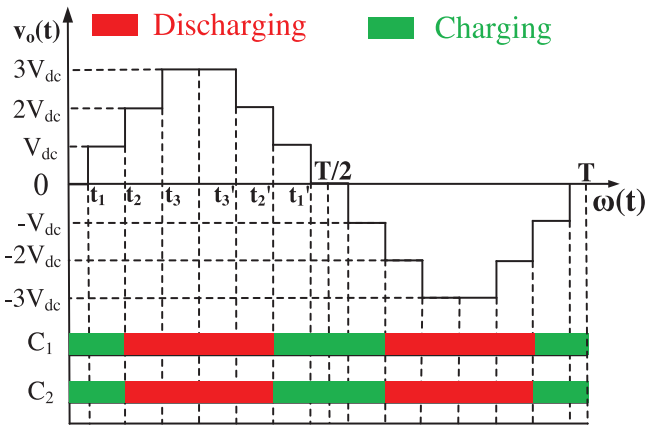

FIGURE 3 Operating states of the proposed 7L TB-SCMLI at the positive levels.

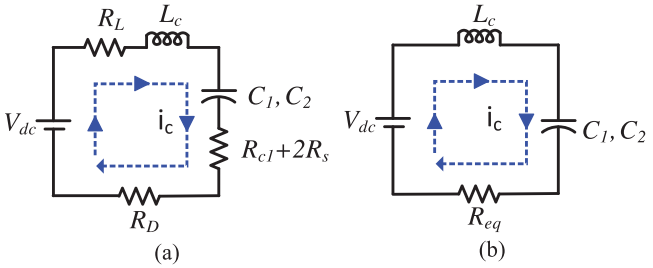

FIGURE 4 (a) Charging path of the capacitors, C_1 and C_2 (b) Equivalent circuit of charging path of capacitors, C_1 and C_2.

Corresponding to t_2 to t_2', θ_2 to $\pi-\theta_2$ is the discharge period of capacitor, the value of C_1 to be selected for a given value of ripple voltage, Δv_{c1} using (1) is given by,

$$C_1, C_2 > \frac{1}{2\pi f \Delta v_{c1}} \int_{\theta_2}^{\pi-\theta_2} I_o \sin(\omega t - \phi) d(\omega t)$$

$$= \frac{I_o \cos\theta_2 2\cos\phi}{\pi f \Delta v_{c1}} \quad (2)$$

where ϕ is the phase angle, I_o is the peak value of fundamental component of load current and f_s is the frequency of output voltage of MLI. As per the standards discussed in literature, the recommended value of voltage ripple in case of MLI is 5–10% of the nominal voltage appearing across the capacitor.

2.2.1 | Selection of soft charging inductor, L_c

After including the soft charging inductor L_c, the capacitor is charged during each half cycle of ac output voltage [33]. The equivalent circuit formed by the source, V_{dc} and inductor, L_c during charging of switched-capacitors, C_1 and C_2 is shown in Figure 4. Both the capacitors have two switches and a diode in their charging path. The charging current in its path encounters

the parasitic elements shown by equivalent series resistance of inductor (R_L), ON-state resistance of the switch (R_s), internal resistance of the diode (R_D), forward voltage drop (V_d) of diode and internal resistance (R_c) of the capacitor [34]. If R_{eq} is the equivalent resistance, the first order differential equations describing the states of capacitor voltage v_{ceq} and inductor current, i_{Lc} are

$$i_{LC} = C_{eq} \frac{dv_{ceq}}{dt} \tag{3}$$

$$V_{dc} = L_c \frac{di_{LC}}{dt} + v_{veq} \tag{4}$$

From Figure 3, it is evident that the capacitors are discharged to the load between t_2 and t_2', or θ_2 to $\pi-\theta_2$. Assuming that a resistive load, R_o, is connected across the output of the proposed converter, integrating both sides of (3) and (4) for the discharging period θ_2 to $\pi-\theta_2$ yields the following result:

$$\Delta i_{LC} = \frac{\omega_r V_{dc}}{\omega R_o} (\theta_2 - \theta_1) \sin(\omega t - \theta_2) \tag{5}$$

$$\Delta v_{ceq} = V_{dc} - \frac{{\omega_r}^2 L_c V_{dc}}{\omega R_o} (\theta_2 - \theta_1) \cos(\omega t - \theta_3) \tag{6}$$

where $\omega_r = \frac{1}{\sqrt{L_c C_{eq}}}$ is the resonant frequency of equivalent circuit shown in Figure 4b. Substituting the ω_r in (6) and simplifying, the desired value of L_c required to limit the spikes in source and capacitor current is given by

$$L_c = \left(\frac{V_{dc}}{\omega R_o \Delta I_{LC} \sqrt{C_{eq}}} (\theta_2 - \theta_1) \right)^2 \tag{7}$$

The magnitude of ripple in charging current is inversely proportional to the value of soft charging inductance, L_c, according to (7). Incorporating L_c into the proposed converter reduces ripples in the charging current. The reduction in ΔI_{LC} results in a decrease in transient losses in capacitors.

2.3 | Modulation strategy

Figure 5 depicts the level-shifted multicarrier sinusoidal pulse width modulation technique used to generate the 7-level single-phase ac output voltage. In this method, a sinusoidal wave signal is compared to a triangular carrier signal with a level shift. In the proposed converter, a sinusoidal wave signal with a peak amplitude of 3 is compared with six carrier signals with peak values distributed between −3 and +3. Each carrier signal has a maximum amplitude of 1. Figure 5a depicts the switching scheme used by the converter to generate various switching states (A_0–A_3, B_0–B_3). Now, the OR logic combines these switching states to generate the gate pulses required by the switches (S_1–S_9) to generate 7-level ac output voltage. Figure 5b depicts the gating operation of transitioning phases.

3 | COMPARISON OF THE PROPOSED TOPOLOGY WITH STATE-OF-THE-ART TOPOLOGIES

In this section, the comparison of the proposed 7-level TB-SCMLI topology with the state-of-the-art topologies reported in literature is carried out [35]. This comparison is done with reference to various features of the converters as mentioned in Table 3. The proposed topology requires 9 switches, 1 auxiliary diode, 1 input source and 2 capacitors for production of 7-level single phase ac output voltage. The topologies reported in [6, 7] require more than one source for generation of 7-level output and hence make these SC-MLI less attractive. However, the rest of the SC-MLI topologies require only one input source. The voltage gain of the proposed and the topologies reported in [6, 29–32] is 3 while the rest of the topologies have voltage gain of 1.5. The topologies proposed in [29] require 16 switches while the topology suggested in [7, 25] require 7 switches, although [7] uses 2 dc sources. The power density of the SC-MLI listed in last of Table 3 is evaluated on the basis of requirement of gate drivers used to provide gating pulses to switches. Therefore, the power density, D of the topologies suggested in [29, 32] is lowest while for [7, 25], its value is highest. However, the proposed SC-MLI configuration requires only 9 switches. Therefore, its power density is moderate.

The SC-MLI configuration suggested in [2], and [6, 12] require only 1 capacitor having voltage ratings V_{dc} and $0.5V_{dc}$, respectively. The SC-MLI topologies suggested in [23, 24] and [27] require 3 capacitors having voltage ratings of $0.5V_{dc}$ and V_{dc}. The proposed 7-level SC-MLI require only 2 capacitors each of voltage rating of V_{dc}. The 7-level SC-MLI suggested in [7, 23, 25] and the proposed converter require auxiliary diode. For fair evaluation of TSV, it is divided by the voltage gain. From Table 3, it is observed that TSV_{pu} of the topology suggested in [25] is lowest at 5, and highest at 9.3 for [7], while it is fairly good at 5.7 for the proposed topology.

The efficiencies of various converters suggested in [6, 7, 31, 32, 23–30] are also included in Table 3. The highest efficiency of the converter having voltage gain of 1.5 is reported in [26] at 98%. The value of highest efficiency for the converters having voltage 3 is reported in [6] which has efficiency of 97.5%. From Figure 6, it can be observed that the efficiency of the converter at full load equal to 1 kW and half load of 500 W are 92.4% and 97.06%, respectively. The high efficiency at low load validates viability of the proposed converter. The abovementioned comparison of the proposed converter with state-of-the-art converters reported in literature validates the viability of the proposed converter.

4 | POWER LOSS AND EFFICIENCY ANALYSIS

Switches, diodes, and capacitors are all components of the proposed design that contribute to the overall power loss. Switching loss and conduction loss are two significant types of losses [27, 33],

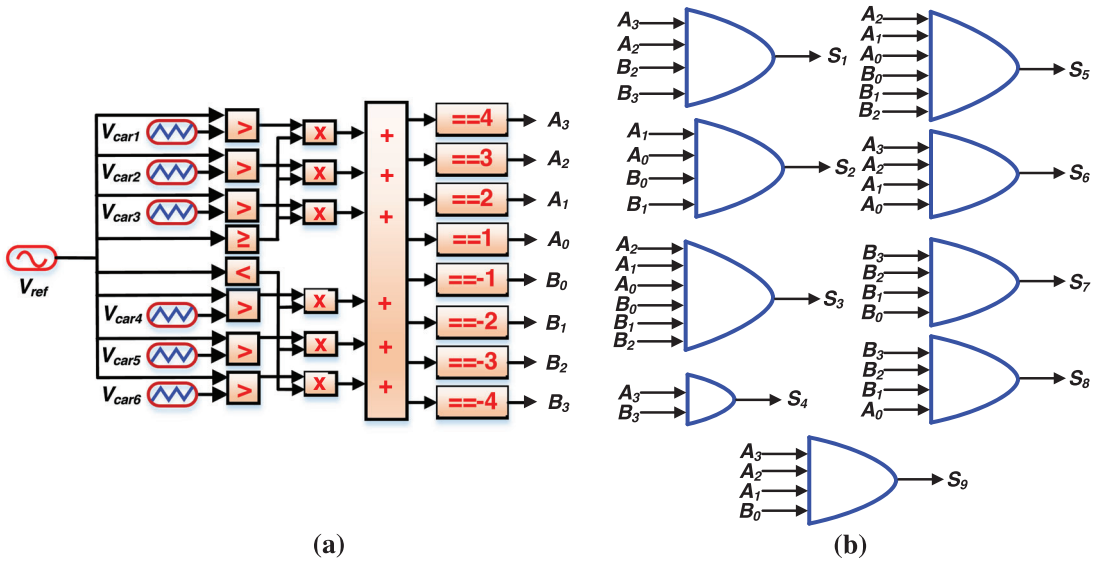

FIGURE 5 (a) Switching scheme of the proposed 7L TB-SCMLI (b) OR logic used to generate gating pulses to switches.

TABLE 3 Comparison table for different 7L SC-based topologies with proposed topology.

References	N_L	G	N_{IS}	N_{Sw}	N_d	N_{ad}	N_{gd}	N_c	PIV	N_m	TSV_{pu}	VRC		η (%)	D
												$0.5V_{dc}$	V_{dc}		
[6]	7	3	3	10	10	0	10	0	3	6	8	0	0	97.5	M
[7]	7	1.5	2	7	7	2	7	1	1	3	9.3	0	1	90	H
[23]	7	1.5	1	9	9	1	9	3	1	6	6.7	2	1	97	M
[24]	7	1.5	1	10	10	0	10	3	1	4	5.3	2	1	95	M
[25]	7	1.5	1	7	7	2	7	2	1.5	2	5	2	0	96.1	H
[26]	7	1.5	1	10	10	0	10	1	1	8	6	1	0	98	M
[27]	7	1.5	1	9	9	0	9	3	1	7	5.3	2	1	96.7	M
[28]	7	1.5	1	8	8	0	8	1	1.5	4	8	1	0	96	H
[32]	7	3	1	14	14	0	14	2	2	6	6.3	0	2	94.7	L
[29]	7	3	1	16	12	0	14	2	2	6	5.3	0	2	93	L
[30]	7	3	1	12	12	0	11	2	2	4	5.3	0	2	93	M
[31]	7	3	1	10	10	0	10	2	3	4	6	0	2	91	M
[P]	7	3	1	9	9	1	9	2	3	4	5.7	0	2	97.06	M

Note: N_L, number of levels; G, voltage gain; N_{IS}, number of input dc sources; N_{sw}, number of switches; N_d, number of diodes in parallel with switches; N_{ad}, number of auxiliary diodes; N_{gd}, number of gate driver circuit; N_c, number of capacitor; TSV_{pu}, total standing voltage in per unit; PIV, peak inverse voltage in per unit; N_m, number of switches tolerating maximum output voltage; VRC, voltage rating of capacitors; η, efficiency; f_s, switching frequency; D, power density; L, low; M, medium; H, high.

$$P_{loss} = P_{sw} + P_{con} \tag{8}$$

where P_{loss} is the total power loss associated with the proposed MLI, P_{sw} is the switching loss and P_{con} is the conduction loss. Switching losses are caused by the switch's non-ideal behaviour, which may be computed by approximately considering the voltage and current to be linear during the turn-on and turn-off phases. The inherent switching delays of semiconductor devices cause overlapping between the voltage and current at each switching transition, which results in switching losses. Using Equation (9), we can determine how much power is lost during the switching process:

$$P_{sw} = f_o \left[\sum_{\text{all switches within } 1/f_o} \sum \frac{V_{ON}\, I_{ON}\, T_{ON}}{6} + \frac{V_{OFF}\, I_{OFF}\, T_{OFF}}{6} \right] \tag{9}$$

where V_{ON} is the voltage across the power switch just before turn-ON, I_{ON} is the current flowing through power switch

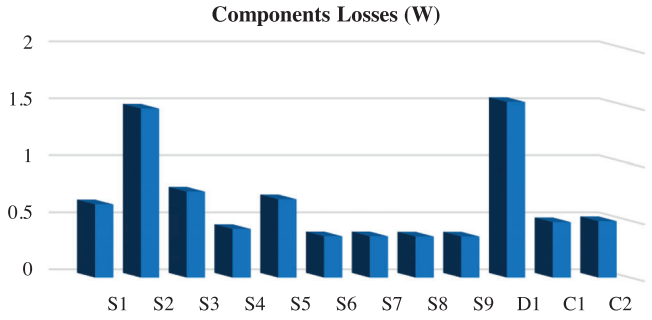

FIGURE 6 Power loss distribution for the input voltage of 100 V and at an output power of 200 W.

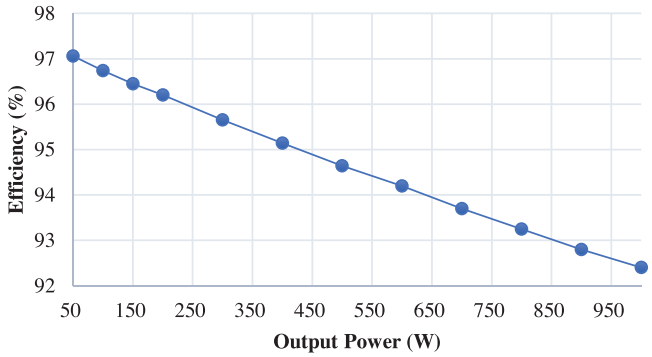

FIGURE 7 Efficiency curve of the proposed TB-SCMLI topology.

TABLE 4 Calculation of losses and efficiency at an output power of 200 W.

Parameters	Simulation
Switching and conduction losses of switches (W)	5.443
Diode, D (W)	1.54
Capacitor, C_1 (W)	0.487
Capacitor, C_2 (W)	0.496
Total losses (W)	7.966
Efficiency (%)	96.02

after turn-ON, T_{ON} is the ON transition period, V_{OFF} is the voltage across power switch after turn-OFF, I_{OFF} is the current flowing through power switch before turn-OFF, T_{OFF} is the OFF transition period, and f_o is the fundamental frequency of ac output. Conduction losses are power lost as a result of the internal resistance of conducting power switches.

$$P_{con} = \sum_{all\ switches} I^2{}_{RMS}\, R_{ON} \tag{10}$$

where I_{RMS} is the RMS current flowing through the switch and R_{ON} is the ON-state resistance of the switch. Utilising Plecs software, the power loss across the various components of the converter has been determined. The thermal modelling part of the software is used for the calculation of different losses in the switches, capacitors, and diodes. The switch used for this study is IGA30N60H3_IGBT and the diode is IGB30N60H3_Diode.

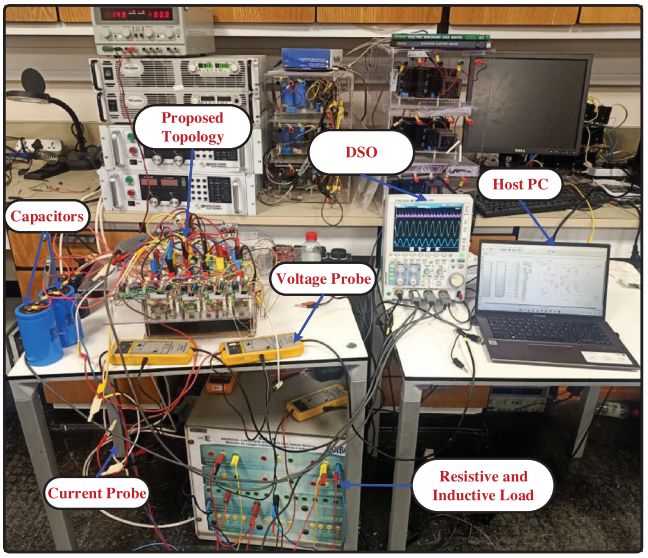

FIGURE 8 Experimental setup for the proposed TB-SCMLI topology.

TABLE 5 Parameters for experimental validation.

Parameters	Specifications
DC voltage sources (TDK-Lambda)	100 V
Capacitors (PG-6DI)	4700 μF, 450 V
R, L load	RL load bank
Output frequency	50 Hz, 100 Hz
Switching frequency	5 kHz
Voltage THD	19.95%
Output power	0.5–1 kW

Internal resistance of both the capacitors is taken as 0.1 ohm. Forward voltage drop and ON-state resistance of diode is taken as 1.3 V and 0.001 ohms. Figure 7 depicts the distribution of power loss for various components for the input voltage of 100 V and at an output power of 200 W. Table 4 provides the calculation of losses and efficiency at 200 W output power. The same method is used to calculate efficiency at various output powers.

5 | RESULTS AND DISCUSSION

To validate the operation of the suggested triple-boost SCMLI topology, a 1 kW experimental setup was developed as shown in Figure 8 and the hardware results are taken by utilizing the well-known level-shifted PWM technique. Nine IGBT switches (SKM75GB128D:1200 V), 2 capacitors (PG-6DI, 4700F), and a diode are designed in the lab to ascertain the technical feasibility of the proposed 7-level SCMLI topology. For pulse generation, a gate driver circuit GDX-4A2S1 based on Texas Instruments' high performance gate driver IC UCC21520 is used. A digital signal processor (DSP) TMS320F28379D is utilised in order to transmit gating signals to the switches. A dc source

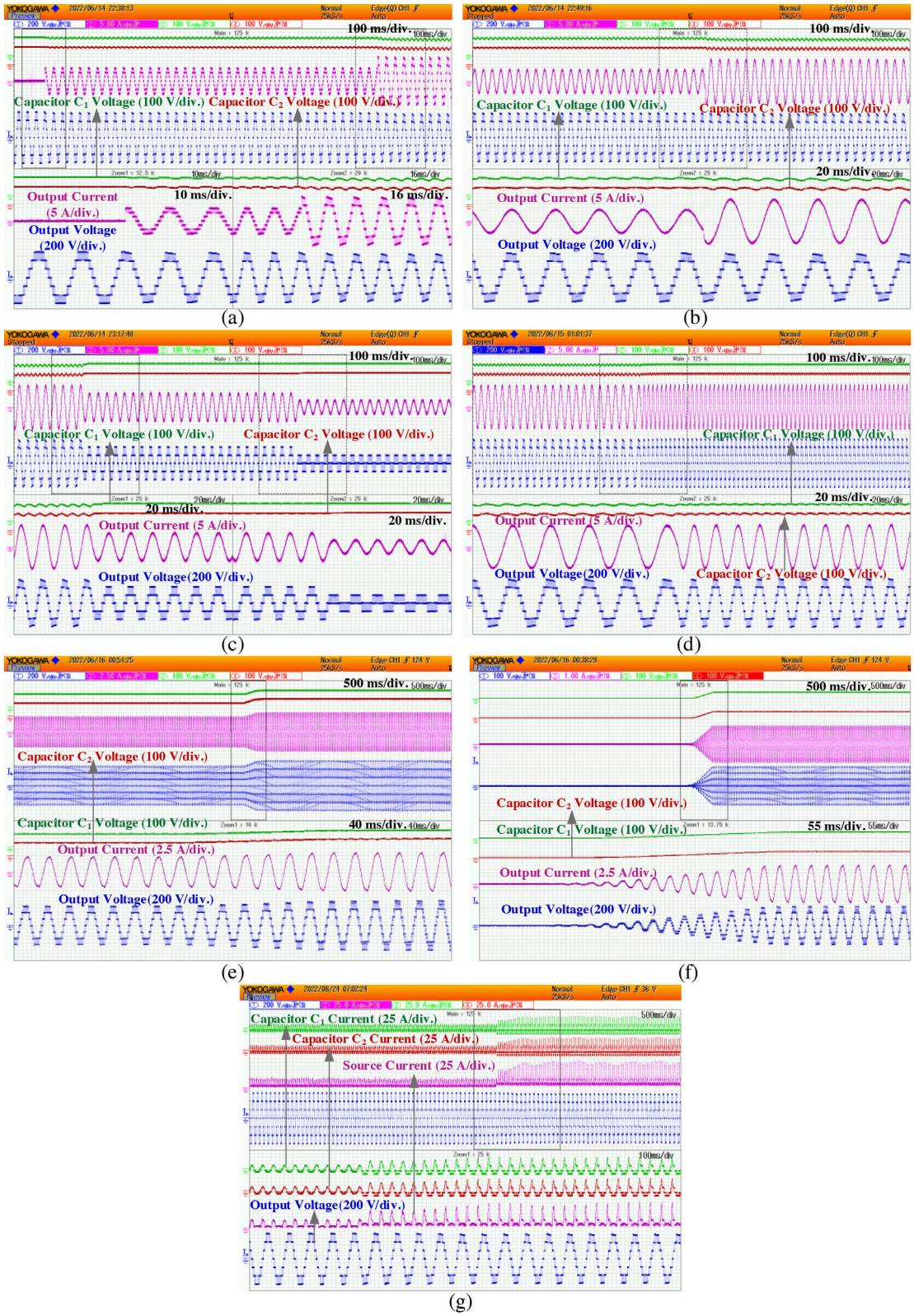

FIGURE 9 Output voltage, output current, capacitor voltages for (a) dynamic resistive load change, (b) inductive load change, (c) modulation index change, (d) change in frequency of the reference sinusoidal signal, (e) change in input supply voltage, (f) starting of the inverter, (g) capacitor currents, source current and output voltage.

(TDK-Lambda) is utilised. Other parameters taken for experimental validation are given in Table 5. The waveforms for the different conditions are shown in Figure 9. The measured output voltage formed seven voltage levels, with the magnitude of each level being equal to the dc voltage input (100 V). The highest voltage level of 300 V conformed to a boosting gain of 3. These findings are consistent with the theoretical analysis. Figures 9a and 9b show the output waveforms for dynamic load change from no load to 100–50 Ω, and $Z = 100\ \Omega + 100$ mH to $Z = 50\ \Omega + 50$ mH, respectively. Capacitor voltages are maintained at about 100 V. Output waveforms for modulation index change from 1 to 0.6 to 0.3, and frequency change of reference wave from 50 to 100 Hz is shown in Figures 9c and 9d, respectively. Figure 9e depicts the output waveforms for step change in input voltage from 80 to 100 V. Finally, starting of the inverter is shown in Figure 9f. As indicated in Figure 1, an inductor (L_c) has been placed in the charging loop of C_1 and C_2 in order to charge the capacitors smoothly. In addition, a power diode is connected in parallel with the inductor to ensure that currents flowing in the opposite direction can flow freely. As a result, the suggested topology can restrict the amount of charging current that travels through the capacitors which is verified by Figure 9g, which shows the capacitor currents and the input source current with the output voltage. Overall, the waveforms of the experiment confirm the analysis. All capacitors can self-balance, and the steady-state output voltage has seven levels. In addition, the proposed topology offers good transient performance.

6 | CONCLUSION

Here, a circuitry improvement for a single dc source-based switched-capacitor multilevel inverter topology is given in order to achieve a high voltage gain. The proposed TB-SCMLI consists of fewer switching components with reduced voltage ratings. Four of the switch pairs are complementary in nature which reduces the control complexity. TSV_{pu} of the proposed inverter is also lower compared to most of the 7L topologies. The proposed TB-SCMLI provides a three times increase in output voltage by utilizing two capacitors and one DC source. Capacitors are automatically balanced according to the switching logic of the proposed MLI. The proposed converter contains a soft switching circuit to supress source and capacitor charging current spikes in switched capacitors. In terms of component count, TSV_{pu}, and efficiency, the comparison research demonstrates the superiority of the proposed TB-SCMLI over other SC-based MLIs. The experimental test outcomes under many operating situations illustrate the effectiveness of the suggested circuit's operation.

AUTHOR CONTRIBUTIONS

Md Reyaz Hussan: Conceptualization, Formal analysis, Writing—original draft; Mohammed Al-Hitmi: Funding acquisition, Supervision, Writing—review and editing; Marif Siddique: Data curation, Investigation; Shirazul Islam: Methodology, Writing—review and editing; Atif Iqbal: Supervision, Validation, Writing—review and editing.

FUNDING INFORMATION

This work was supported in part by Qatar univsersity Research Grant from Qatar University, Doha, Qatar, Under Grant: QUCP-CENG-2022-571. The statement made herein are solely the responsibility of the authors. The APC for this manuscript is funded by the Qatar National Library, Doha, Qatar.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

ORCID

Md. Reyaz Hussan https://orcid.org/0000-0002-3245-9495
Shirazul Islam https://orcid.org/0000-0002-1689-8279
Atif Iqbal https://orcid.org/0000-0002-6932-4367

REFERENCES

1. Mohsenzadeh, M., Rezanejad, M., Adabi, J.: Marxiplier: An innovative Marx-based single-source multilevel inverter with voltage multiplying capability. IEEE Trans. Ind. Electron. 69(1), 357–364 (2022)
2. Tran, T., Nguyen, M., Duong, T., Lim, Y., Choi, J.: A switched-capacitor-based six-level inverter. IEEE Trans. Power Electron. 37(4), 4804–4816 (2022)
3. Roy, T., Sadhu, P.K., Dasgupta, A.: Cross-switched multilevel inverter using novel switched capacitor converters. IEEE Trans. Ind. Electron. 66(11), 8521–8532 (2019)
4. Salem, A., Huynh, K.G., Robbersmyr, K., Norambuena, M., Rodriguez, J.: Voltage source multilevel inverters with reduced device count: Topological review and novel comparative factor. IEEE Trans. Power Electron. 36(3), 2720–2747 (2021)
5. Liu, J., Lin, W., Wu, J., Zeng, J.: A novel nine-level quadruple boost inverter with inductive-load ability. IEEE Trans. Power Electron. 34(5), 4014–4018 (2019)
6. Lee, S.S., Sidorov, M., Idris, N.R.N., Heng, Y.E.: A symmetrical cascaded compact-module multilevel inverter (CCM-MLI) with pulsewidth modulation. IEEE Trans. Ind. Electron. 65(6), 4631–4639
7. Raman, S.R., Cheng, K.W.E., Ye, Y.: Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution. IEEE Trans. Power Electron. 33(7), 5937–5948 (2018)
8. Tsunoda, A., Hinago, Y., Koizumi, H.: Level- and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion. IEEE Trans. Ind. Electron. 61(8), 4011–4021 (2014)
9. Shalchi Alishah, R., Hosseini, S.H., Babaei, E., Sabahi, M., Gharehpetian, G.B.: New high step-up multilevel converter topology with self-voltage balancing ability and its optimization analysis. IEEE Trans. Ind. Electron. 64(9), 7060–7070 (2017)
10. Raman, S.R., Fong, Y.C., Ye, Y., Eric Cheng, K.W.: Family of multiport switched-capacitor multilevel inverters for high-frequency AC power distribution. IEEE Trans. Power Electron. 34(5), 4407–4422 (2019)
11. Guo, X.: A novel CH5 inverter for single-phase transformerless photovoltaic system applications. IEEE Trans. Circuits Syst. II Express Briefs 64(10), 1197–1201 (2017)
12. Sandeep, N.: A 13-level switched-capacitor-based boosting inverter. IEEE Trans. Circuits Syst. II Express Briefs 68(3), 998–1002 (2021)
13. Ye, Y., Zhang, G., Wang, X., Yi, Y., Cheng, K.W.E.: Self-balanced switched-capacitor thirteen-level inverters with reduced capacitors count. IEEE Trans. Ind. Electron. 69(1), 1070–1076 (2022)

14. Hussan, M.R., Sarwar, A., Siddique, M.D., Iqbal, A., Alamri, B.: A cross connected asymmetrical switched-capacitor multilevel inverter. IEEE Access 9, 96416–96429 (2021)
15. Marusarz, R.: A switched capacitor, inductorless DC to AC voltage step-up power converter. In: 20th Annual IEEE Power Electronics Specialists Conference. Milwaukee, WI, USA. pp. 99–103 (1989)
16. Khan, M.N.H., Forouzesh, M., Siwakoti, Y.P., Li, L., Blaabjerg, F.: Switched capacitor integrated (2n + 1)-level step-up single-phase inverter. IEEE Trans. Power Electron. 35(8), 8248–8260 (2020)
17. Hussan, M.R., Sarwar, A., Siddique, M.D., et al.: A novel switched-capacitor multilevel inverter topology for energy storage and smart grid applications. Electronics 9(10), 1703 (2020)
18. Hussan, M.R., Sarwar, A., Tayyab, M., Tariq, M., Bakhsh, F.I., Ahmad, A.: A single-source switched-capacitor based 13-level sextuple boost inverter with reduced component count and low THD. IET Gener. Transm. Distrib. 17(11), 2587–2599 (2023)
19. Panda, K., Bana, P., Kiselychnyk, O., Wang, J., Panda, G.: A single-source switched-capacitor-based step-up multilevel inverter with reduced components. IEEE Trans. Ind. Appl. 57(4), 3801–3811 (2021)
20. Deliri, S., Varesi, K., Padmanaban, S.: An extendable single-input reduced-switch 11-level switched-capacitor inverter with quintuple boosting factor. IET Gener. Transm. Distrib. 17(3), 621–631 (2022)
21. Bana, P.R., Panda, K.P., Padmanaban, S., Mihet-Popa, L., Panda, G., Wu, J.: Closed-loop control and performance evaluation of reduced part count multilevel inverter interfacing grid-connected PV system. IEEE Access 8, 75691–75701 (2020)
22. Panda, K.P., Bana, P.R., Naayagi, R.T., Panda, G.: A dual-source self-balanced switched-capacitor reduced switch multilevel inverter with extending ability. IEEE Access 10, 61441–61450 (2022)
23. Liu, J., Wu, J., Zeng, J.: Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques. IEEE J. Emerging Sel. Top. Power Electron. 6(3), 1616–1626 (2018)
24. Liu, J., Zhu, X., Zeng, J.: A seven-level inverter with self-balancing and low-voltage stress. IEEE J. Emerging Sel. Top. Power Electron. 8(1), 685–696 (2020)
25. Lin, W., Zeng, J., Fu, B., Yan, Z., Member, S., Liu, J.: Switched-capacitor based seven-level boost inverter with reduced devices. CSEE J. Power Energy Syst. (2021)
26. Sathik, M.J., Sandeep, N., Blaabjerg, F.: High gain active neutral point clamped seven-level self-voltage balancing inverter. IEEE Trans. Circuits Syst. II Express Briefs 67(11), 2567–2571 (2020)
27. Lee, S.S., Lim, C.S., Siwakoti, Y.P., Lee, K.: Hybrid 7-level boost active-neutral-point-clamped (H-7L-BANPC) inverter. IEEE Trans. Circuits Syst. II Express Briefs 67(10), 2044–2048 (2020)
28. Ren, L., Zhang, L., Wang, L., Dai, S.: Capacitor voltage regulation strategy for 7-level single DC source hybrid cascaded inverter. IEEE J. Emerging Sel. Top. Power Electron. 6777(c), 1 (2022)
29. Lee, S.S.: A single-phase single-source 7-level inverter with triple voltage boosting gain. IEEE Access 6, 30005–30011 (2018)
30. Siddique, M.D., Mekhilef, S., Mekhilef, S., Shah, N.M., Ali, J.S.M., Blaabjerg, F.: A new switched capacitor 7L inverter with triple voltage gain and low voltage stress. IEEE Trans. Circuits Syst. II Express Briefs 67(7), 1294–1298 (2020)
31. Siddique, M.D., Ali, J.S.M., Mekhilef, S., Mustafa, A., Sandeep, N., Almakhles, D.: Reduced switch count based single source 7L boost inverter topology. IEEE Trans. Circuits Syst. II Express Briefs 67(12), 3252–3256 (2020)
32. Wang, Y., Wang, C., Guo, Y., Wang, K., Liang, J.: An X-type boost multilevel inverter based on switched capacitor cells with low voltage stress and high frequency applications. IEEE J. Emerging Sel. Top. Power Electron. 6777 (2021)
33. Varesi, K., Esmaeili, F., Deliri, S., Tarzamni, H.: Single-input quadruple-boosting switched-capacitor nine-level inverter with self-balanced capacitors. IEEE Access 10, 70350–70361 (2022)
34. Karimi, M., Kargar, P., Varesi, K.: An extendable asymmetric boost multilevel inverter with self-balanced capacitors. Int. J. Circuit Theory Appl. 50(4), 1297–1316 (2022)
35. Tarzamni, H., Gohari, H.S., Sabahi, M., Kyyra, J.: Non-isolated high step-up DC-DC converters: Comparative review and metrics applicability. IEEE Trans. Power Electron. (2023)

How to cite this article: Hussan, M.R., Al-Hitmi, M.A., Siddique, M.D., Islam, S., Iqbal, A.: Triple boost switched capacitor multilevel inverter (TB-SCMLI) with reduced components and self-voltage balance. IET Power Electron. 1–10 (2023).
https://doi.org/10.1049/pel2.12561