IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 27, 2021, accepted June 10, 2021, date of publication June 14, 2021, date of current version June 21, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3088957

Voltage Lift Switched Inductor Double Leg Converter With Extended Duty Ratio for DC Microgrid Application

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This work was supported by Qatar University-Marubeni Concept to Prototype Development Research under Grant M-CTP-CENG-2020-2 from the Qatar University.

ABSTRACT In a DC microgrid, while integrating the low voltage sources such as Fuel cells and photovoltaics, an efficient DC-DC converter is crucially needed. Contributing to a high voltage whilst being operated on a low duty ratio is among the demanded features of the converter. For high voltage applications, the conventional converters are to be operated beyond the prescribed range of the duty ratio which may result in various detrimental effects such as voltage spikes, increased current ripples, and reduced efficiency. In this paper, a voltage lift switched inductor double leg converter (VLSIDL) has been proposed. This novel converter has the feature of attaining a very high voltage without using any complex circuitry such as transformer, multiple voltage lift circuits, cascaded or parallel structure, etc. This particular converter has three switches that are operated in three modes with two different duty ratios. Double duty control offers flexibility in the selection of duty ratio for a particular output voltage and a significantly high gain is easily attained. The double duty ratio not only provides an extended range but also improves the efficiency and performance of the converter. The steady-state analysis of the proposed converter is done analytically and the same is verified through the hardware prototype.

INDEX TERMS DC-DC converter, voltage lift, switched inductor, double duty, high voltage gain, and wide duty range.

I. INTRODUCTION

Increased population and environmental concerns have raised the demand for clean energy sources. Enormous efforts have been put down to explore renewable sources of energy, such as photovoltaics, wind, and fuel cells. However, these generating units have low terminal voltage, which urgently calls for high gain DC-DC converters for their proper integration in DC microgrid as can be seen from Fig. 1 [1]. To achieve such a high gain, a conventional boost or buck-boost converter would have to be operated at an extremely large duty ratio. However, as the duty ratio crosses the prescribed limit, the effect of parasitic elements starts dominating and the converter efficiency gets reduced [2], [3]. Moreover, switching losses and current ripples are increased at a higher duty ratio in conventional boost converter [4]. Consequently, the transient response is negatively affected and the output side diode experiences a severe reverse recovery issue which ultimately adds up to the loss and voltage/current stress on the devices [5]–[7]. Therefore, coming up with some converter topologies, which would be able to impart high voltage gain at a lower duty ratio and having a wider control range of duty ratio are the main concerns of this paper.

In literature, many boost converters with different features have been reported. They are either with proper isolation using transformers/coupled inductors or imply direct connection if applications do not require a magnetic coupling and involve only switching devices along with the passive elements [8], [9]. This simplifies the structure and design of the converter for low and medium-power applications [10]. These non-isolated types of converters rarely use a built-in transformer for voltage boosting rather they involve one

The associate editor coordinating the review of this manuscript and approving it for publication was Kan Liu.

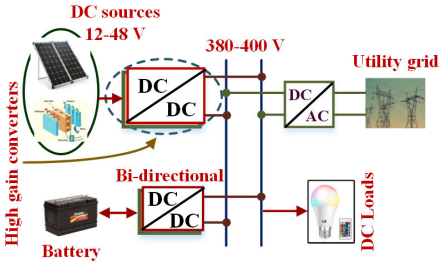

FIGURE 1. DC microgrid brief layout.

or more voltage boosting networks to achieve the required voltage at the output. Sometimes to get the high voltage, they are either cascaded or interleaved with another unit of the same or different type of networks [11]. In addition, there are few multi-level or multi-modular type of non-isolated converters which are justified for some high voltage and high power applications in industry or academia [12]. However, involving multiple networks in cascade, parallel or modular form not only increases the size and bulkiness but also drops off the efficiency.

The most commonly reported non-isolated converters available in the literature include the different design of switched inductors, switched capacitors, coupled inductors, or combined structure type of converters [13]. Switched-capacitor based converters not only raise the voltage gain but also possess more immunity against EMI owed to its inductor-free structure [5]. However, these converters suffer from input current ripples and weak voltage regulation during large load variations. Topologies based on coupled inductors can easily uplift the voltage gain in consort with lowering voltage stress across switches but endure reduced efficiency due to more losses in leakage inductance. Moreover, the leakage inductance of coupled inductor sometimes resonates with the parasitic capacitance of the output diode causing voltage ringing in the diode circuit [14]. Mitigation of this resonance is achieved by a suitable snubber circuit which increases the complexity and cost of the converter. Combining different basic converters to get a modified one is a simple approach to enhance the gain of the converter. Cascaded converters presented in [15] own high voltage gains but have limited practical applications owing to their size and intricate control. To reduce the circuit complexity, the two switches of the cascaded converter are integrated into one, to form a quadratic boost converter. A straightforward shortcoming of the quadratic boost converter is that the duty ratio of the two converters can no longer be independently controlled [16]. Moreover, the voltage gain is highly non-linear and switch voltage stress is significant. Further to improve efficiency, a quasi-resonant quadratic boost converter is presented in [17]. Since the input current level in boost converters is higher than the output, interleaving seems to be a promising solution for reducing input current ripples and achieving high gain in these converters. Numerous topologies are reported with different combinations of interleaving.

However, interleaved converters are slightly complex with more active and passive elements, causing the converter to be less efficient [18]. Moreover, the gain factor is not sufficiently high in these converters owing to their limited duty ratio ($D \leq 0.5$). Voltage lifting can easily be achieved by using the switched-inductor network in the circuit. The plausible feature of charging in parallels and discharging in series of a switched-inductor cell makes the converter easy to accomplish high gain [4]. However, in these converters too, the gain factor is limited, and balanced inductor circuit design is problematic. In all the aforementioned converters, there is single duty cycle control to manage the voltage gain. In [19]–[21], the proposed converter can attain high gain by operating the converter in three different modes. Further, the extended version of the same is presented in [22] where a diode-capacitor circuit is used additionally to enhance the gain and efficiency of the converter. However, there is no substantial improvement in the gain is observed even after including one more switch and additional circuitry. In this paper, a novel high gain Voltage Lift Switched-Inductor-Double-Leg (VLSIDL) boost converter is proposed which is highly suitable for high voltage applications owing to its higher gain at low duty ratio. In particular, this converter appears as a suitable interface to integrate low voltage solar PV, battery, or fuel cell to high voltage DC bus in a DC microgrid as can be seen from Fig.1. Moreover, the double duty control widens its application area for hybrid and multiport outputs with suitable control in electric vehicles and similar applications. In the last decade, 380-V dc distribution systems have begun to supplant conventional 48-V dc distribution systems. As a result, there is increasing demand for high step-up dc–dc converters in network server and data center applications. In addition, UPS and avionic standards also call for such high gain converter.

II. VOLTAGE LIFT SWITCHED-INDUCTOR-DOUBLE-LEG BOOST CONVERTER

A. THE POWER CIRCUIT

The power circuit of the proposed converter is shown in Fig. 2. The circuit is realized by using four identical inductors L_{11}, L_{12}, L_{21}, and L_{22}, diodes D_1-D_7, switches S_1-S_3, capacitors C_1, C_2, C_3, and C_o across the load R. Inductors L_{11} and L_{12} together with diodes D_1, D_2, and capacitor C_1 set up the voltage lift switched inductor network in the first leg. Similarly, inductors L_{21} and L_{22} along with diodes D_3, D_4, and capacitor C_2 constitute the voltage lift switched inductor network in another leg. Switches S_1 and S_2 are operated simultaneously by the same gate pulse with duty cycle δ_1, while switch S_3 is separately operated with another gate pulse having a duty cycle δ_2 with a phase shift of $\delta_2 T_S$, where T_S is the period of one complete cycle. The generalized extended version of the proposed topology is shown in Fig. 3 where the proposed converter can be seen with its multiple voltage lift cells in different legs. However, the converter characteristics will resemble the parent converter as proposed and analyzed

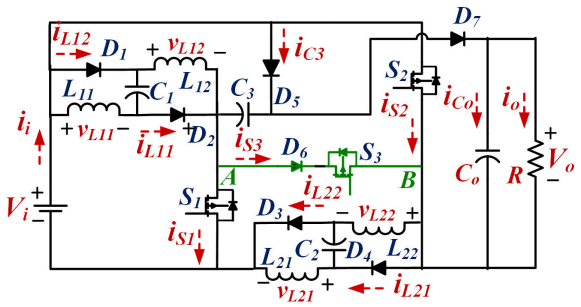

FIGURE 2. Power circuit layout of the proposed converter.

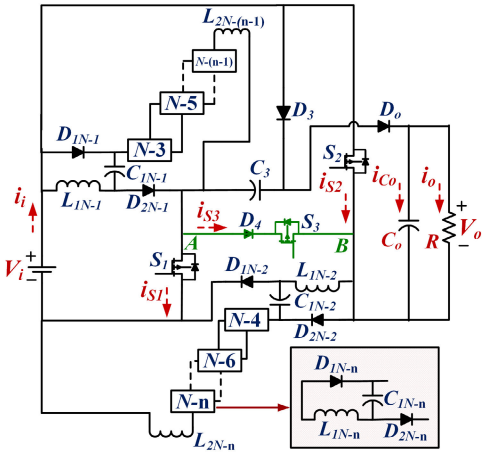

FIGURE 3. The generalized extended version of the proposed converter.

in the later sections. Few assumptions are made erstwhile to the analysis of the proposed circuit in CCM and DCM: the elements used in the circuit are presumed as ideal ones such that the switches are supposed to be lossless with negligible ON-state resistance, forward voltage drops across diodes are insignificant enough to affect the performance of the circuit, and trivial ESR of inductances and capacitances are assumed. Moreover, all the inductors are chosen identical with equal values.

B. CCM OPERATION AND ANALYSIS

The power circuitry of the proposed converter in CCM is shown in Fig. 4. The CCM operation of the converter is described in three modes.

1) MODE-I [t_0 TO t_1]

During this interval, the switches S_1 and S_2 are turned on while S_3 is kept OFF. Current follows the path as shown by a highlighted part of the equivalent power circuit in Fig. 4(a). In this mode, all the inductors L_{11}, L_{12}, L_{21}, and L_{22} are being magnetized in parallel by the source voltage $V_{\rm I}$. Meanwhile, all the capacitors are also charged by the input supply. In the same duration, the stored energy in the capacitor $C_{\rm O}$ is released to the load R to maintain ripplesfree constant output. Throughout this mode, diode D_1 and D_2 remain forward biased in leg-1. Fig. 5 represents the typical characteristics of inductors during CCM and it is observed that the current through inductors remains continuous throughout the entire cycle. The corresponding voltages across the inductors are also depicted in the same figure.

$$\begin{cases} V^I_{L11} = V^I_{L12} = V^I_{L21} = V^I_{L22} = V_i \\ V^I_{C1} = V^I_{C2} = V^I_{C3} = V_i; \quad V^I_{Co} = V_o \\ I^I_i = I^I_{L11} + I^I_{L12} + I^I_{L21} + I^I_{L22} + I^I_{C1} + I^I_{C2} + I^I_{C3} \end{cases} \tag{1}$$

The superscript "I" denotes that the converter is operating in mode- I. It is noteworthy that the current in all the four inductors L_{11}, L_{12}, L_{21}, *and* L_{22} are linearly increasing with slopes *tan* (α^I_{11}), *tan* (α^I_{12}), *tan* (α^I_{21}), and *tan* (α^I_{22}) respectively as shown in Fig. 5. The characteristics waveform of each components during this mode is shown in Fig. 6(a). The magnetizing angles of the inductors are expressed as follows.

$$\begin{cases} \alpha^I_{11} = \tan^{-1}\left[\left(I^{(Max1)}_{L11} - I^{(Min)}_{L11}\right)(\delta_1 T_s)^{-1}\right] \\ \quad = \tan^{-1}\left(L^{-1}_{11} V_i\right) \\ \alpha^I_{12} = \tan^{-1}\left[\left(I^{(Max1)}_{L12} - I^{(Min)}_{L12}\right)(\delta_1 T_s)^{-1}\right] \\ \quad = \tan^{-1}\left(L^{-1}_{12} V_i\right) \\ \alpha^I_{21} = \tan^{-1}\left[\left(I^{(Max1)}_{L21} - I^{(Min)}_{L21}\right)(\delta_1 T_s)^{-1}\right] \\ \quad = \tan^{-1}\left(L^{-1}_{21} V_i\right) \\ \alpha^I_{22} = \tan^{-1}\left[\left(I^{(Max1)}_{L22} - I^{(Min)}_{L22}\right)(\delta_1 T_s)^{-1}\right] \\ \quad = \tan^{-1}\left(L^{-1}_{22} V_i\right) \\ \alpha^I = \alpha^I_{11} = \alpha^I_{12} = \alpha^I_{21} = \alpha^I_{22} \end{cases} \tag{2}$$

2) MODE-II [t_1 TO t_2]

In Fig. 4(b), the power circuitry of the proposed converter during mode II is shown. In this mode, switches S_1 and S_2 are turned OFF while the third switch S_3 is turned ON. During this mode, the inductor of both VLSI networks is magnetized in series by a combination of input voltage V_i and respective capacitors $C_{1/2}$. Diodes $D_{1/2}$ and $D_{3/4}$ remain reverse biased because of capacitor voltages. Throughout this mode, the capacitor C_o is discharged through load R. The voltages across the inductors are given as,

$$\begin{cases} V^{II}_{L11} = V^{II}_{L12} = V^{II}_{L21} = V^{II}_{L22} = 0.25(V_i + V^{II}_{C1} + V^{II}_{C2}) \\ and, \; V^{II}_{C1} = V^{II}_{C2} = V^{II}_{C3} = V_i; \quad V^{II}_{Co} = V_o \\ therefore, \; V^{II}_{L11} = V^{II}_{L12} = V^{II}_{L21} = V^{II}_{L22} = 0.75 V_i \end{cases} \tag{3}$$

The superscript "II" denotes that the converter is operating in mode- II. It is noteworthy that the current in all the four inductors L_{11}, L_{12}, L_{21}, and L_{22} are again increasing linearly with slopes $tan(\alpha^{II}_{11})$, $tan(\alpha^{II}_{12})$, $tan(\alpha^{II}_{21})$, and $tan(\alpha^{II}_{22})$ respectively. The magnetizing angles of the inductors are the same

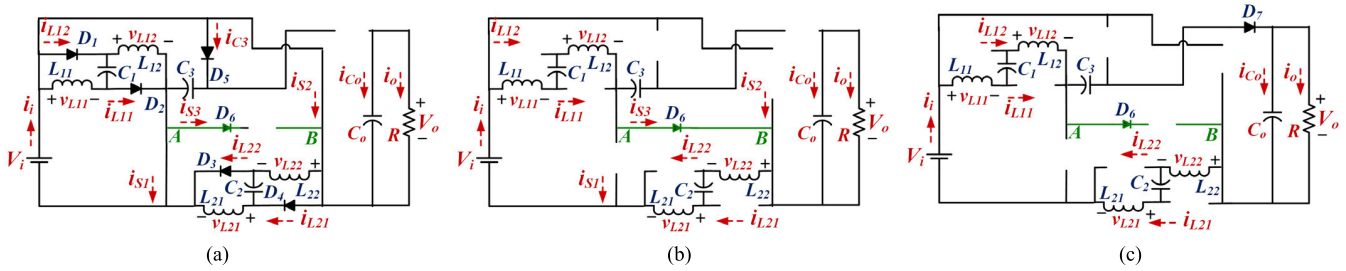

FIGURE 4. power circuitry of proposed converter in CCM (a) mode-I, (b) mode-II and (c) mode III.

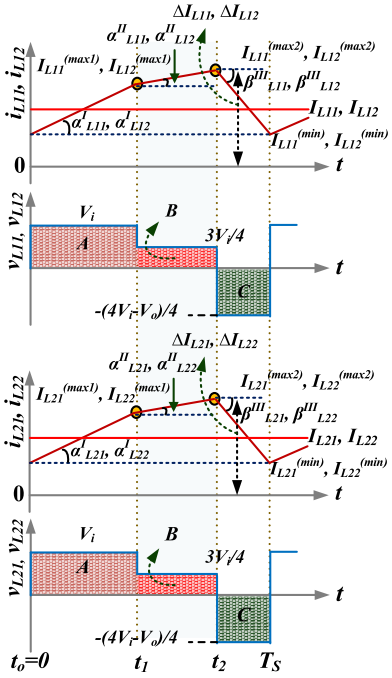

FIGURE 5. Inductors current and voltage characteristics in CCM.

and expressed as

$$\begin{cases} \alpha_{11}^{II} = \tan^{-1}\left(L_{11}^{-1}V_i\right) \\ \quad = \tan^{-1}\left(\left(I_{L11}^{(Max2)} - I_{L11}^{(Max1)}\right)(\delta_2 T_s)^{-1}\right) \\ \alpha_{12}^{II} = \tan^{-1}\left(L_{12}^{-1}V_i\right) \\ \quad = \tan^{-1}\left(\left(I_{L12}^{(Max2)} - I_{L12}^{(Max1)}\right)(\delta_2 T_s)^{-1}\right) \\ \alpha_{21}^{II} = \tan^{-1}\left(L_{21}^{-1}V_i\right) \\ \quad = \tan^{-1}\left(\left(I_{L21}^{(Max2)} - I_{L21}^{(Max1)}\right)(\delta_2 T_s)^{-1}\right) \\ \alpha_{22}^{II} = \tan^{-1}\left(L_{22}^{-1}V_i\right) \\ \quad = \tan^{-1}\left(\left(I_{L22}^{(Max2)} - I_{L22}^{(Max1)}\right)(\delta_2 T_s)^{-1}\right) \\ \alpha^{II} = \alpha_{11}^{II} = \alpha_{12}^{II} = \alpha_{21}^{II} = \alpha_{22}^{II} \end{cases} \tag{4}$$

3) MODE-III [t_2 TO t_3]

Fig. 4(c) represents the equivalent power circuit of the converter during mode III in which all the switches S_1, S_2, and S_3 are turned OFF. In this mode, the series connection of input voltage V_i all inductors and all the capacitors together supply power to the load R and capacitor C. Throughout this mode, diodes $D_{1/2}$ and $D_{3/4}$ remain reverse biased because of capacitor voltages. The voltages across the inductors and capacitors are given as,

$$\begin{cases} V_L^{III} = 0.25\left(V_i - V_o + V_{C1}^{III} + V_{C2}^{III} + V_{C3}^{III}\right) \\ \quad = 0.25\left(4V_i - Vo\right), \\ such\ that, \\ V_L^{III} = V_{L11}^{III} = V_{L12}^{III} = V_{L21}^{III} = V_{L22}^{III} \end{cases} \tag{5}$$

The "III" is expressed as the superscript to represent the mode III operation. It is noteworthy that the inductor currents are linearly decreasing with slopes $tan(\beta_{11}^{III})$, $tan(\beta_{12}^{III})$, $tan(\beta_{21}^{III}.)$, and $tan(\beta_{22}^{III})$ respectively i_{L11}, i_{L12}, i_{L21}, and i_{L22}. Moreover, the demagnetizing angles of L_{11}, L_{12}, L_{21}, and L_{22} current are the same and expressed as follows,

$$\begin{cases} \beta_{11}^{III} = \tan^{-1}\left(\dfrac{4V_i - V_o}{4L_{11}}\right) = \tan^{-1}\left(\dfrac{I_{L11}^{(Min)} - I_{L11}^{(Max2)}}{1 - \delta_1 T_s - \delta_2 T_s}\right) \\ \beta_{12}^{III} = \tan^{-1}\left(\dfrac{4V_i - V_o}{4L_{12}}\right) = \tan^{-1}\left(\dfrac{I_{L12}^{(Min)} - I_{L12}^{(Max2)}}{1 - \delta_1 T_s - \delta_2 T_s}\right) \\ \beta_{21}^{III} = \tan^{-1}\left(\dfrac{4V_i - V_o}{4L_{21}}\right) = \tan^{-1}\left(\dfrac{I_{L21}^{(Min)} - I_{L21}^{(Max2)}}{1 - \delta_1 T_s - \delta_2 T_s}\right) \\ \beta_{22}^{III} = \tan^{-1}\left(\dfrac{4V_i - V_o}{4L_{22}}\right) = \tan^{-1}\left(\dfrac{I_{L22}^{(Min)} - I_{L22}^{(Max2)}}{1 - \delta_1 T_s - \delta_2 T_s}\right) \\ we\ have\ L = L_{11} = L_{12} = L_{21} = L_{22}, \\ \text{and } \beta^{III} = \beta_{11}^{III} = \beta_{12}^{III} = \beta_{21}^{III} = \beta_{22}^{III} \end{cases} \tag{6}$$

From Fig. 5, the area covered by the inductor L (i.e. L_{11}, L_{12}, L_{21}, *and* L_{22}) voltage waveform in Mode I, II, III are related as presented below,

$$\int_0^{\delta_1 T_s} V_L^I dt + \int_{\delta_1 T_s}^{\delta_2 T_s} V_L^{II} dt + \int_{\delta_2 T_s}^{(1-\delta_1-\delta_2)Ts} V_L^{III} dt = 0 \tag{7}$$

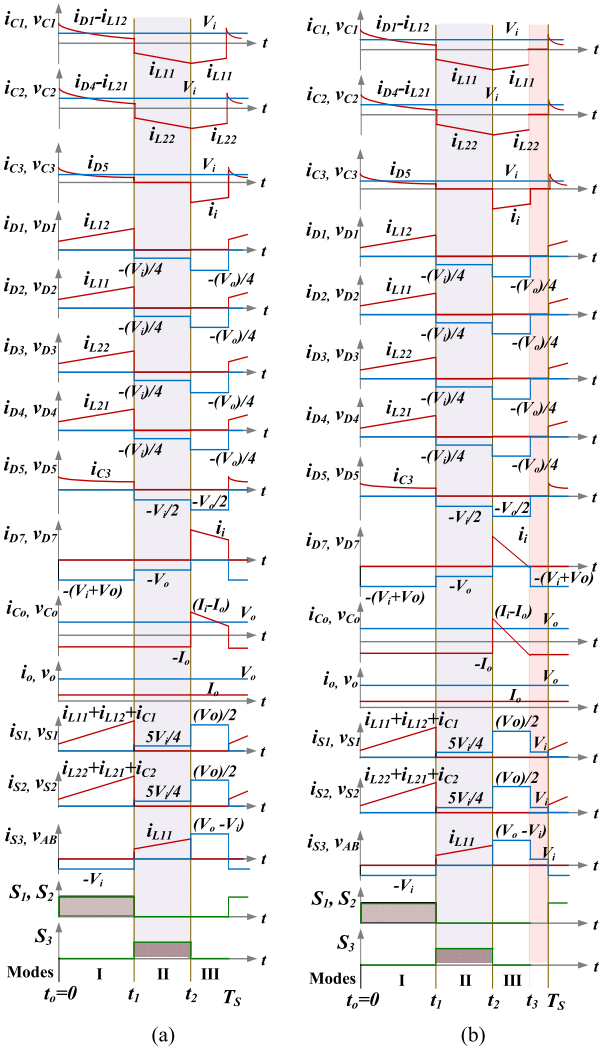

FIGURE 6. Characteristics waveforms during (a) CCM and (b) DCM of the converter.

By substituting (1), (3), and (5) in (7), the voltage gain for CCM is obtained as follows,

$$\begin{cases} G_{CCM} = \dfrac{V_o}{V_i} = \dfrac{(4-\delta_2)}{1-\delta_1-\delta_2} \end{cases} \tag{8}$$

C. DCM OPERATION AND ANALYSIS

The DCM operation of the proposed VLSIDL converter is analyzed in four different modes of operation. Fig. 6(b) shows the typical characteristics of the converter for DCM, where it is assumed that the inductor currents reached zero levels at time t_3. Let's consider 'θ' as the magnetizing angle which is having subscript and superscript to represent a particular inductor and mode of operation respectively. Similarly, 'γ' represents the demagnetizing angle of inductor current which is also having subscript and superscript to represent certain inductor and mode of operation as shown in Fig. 7. Since the inductors behave identically, a single waveform for current

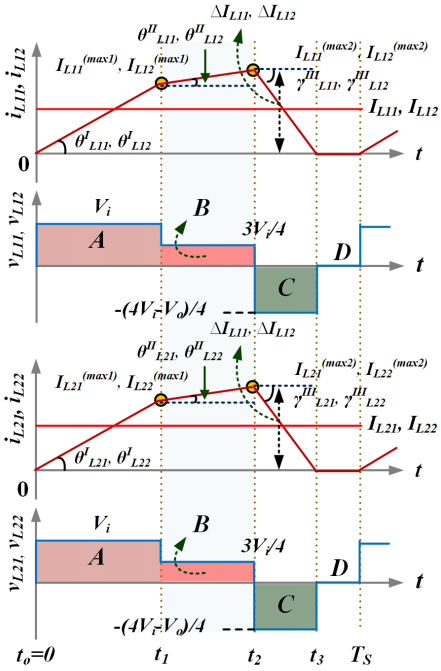

FIGURE 7. Inductors current and voltage characteristics in DCM.

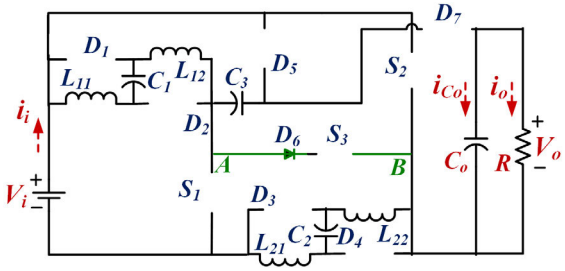

FIGURE 8. DCM layout of the converter circuit.

and voltage for all the inductors is presented. The modes of operation in DCM are explained below.

1) MODE-I [t_0 TO t_1]

The equivalent power circuit during this mode is the same as the Mode -I of CCM operation. Switches S_1 and S_2 are gated by the same pulse for turning ON them simultaneously while switch S_3 is kept OFF. Diode D_1 is forward biased and D_2 is reverse biased. The maximum values of inductor currents are expressed as follows,

$$\begin{cases} I_L^{(max1)} = L^{-1} V_i \delta_1 T_s = \delta_1 T_s \tan(\theta^I) \\ As\ we\ have\ L = L_{11} = L_{12} = L_{21} = L_{22}, \\ \text{and } \theta^I = \theta^I_{11} = \theta^I_{12} = \theta^I_{21} = \theta^I_{22} \\ \therefore\ I_{L^{(max1)}} = I_{L1^{(max1)}} = I_{L12^{(max1)}} = I_{L21^{(max1)}} = I_{L22^{(max1)}} \end{cases} \tag{9}$$

2) MODE-II [t_1 TO t_2]

The operation of the converter during this mode is similar to that of mode -II of CCM and the equivalent power circuit is

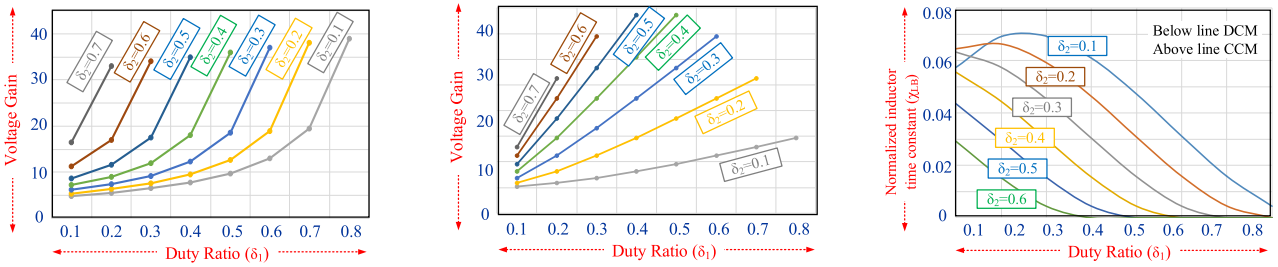

FIGURE 9. Voltage gain curve of proposed converter in (a) CCM and (b) DCM, and (c) boundary condition between CCM and DCM w.r.t. duty ratio (δ_1).

shown in Fig. 4(b). Switches S_1 and S_2 are turned OFF and S_3 is put ON. The maximum values of inductor currents are calculated as follows,

$$\begin{cases} I_L^{(Max2)} \begin{cases} = I_L^{(Max1)} + \left(0.75L^{-1}V_i\right)\delta_2 T_S \\ = \left(L^{-1}V_i\right)(0.75\delta_2 + \delta_1)\, T_S \\ = \delta_1 T_S \tan(\theta^I) + \delta_2 T_S \tan(\theta^{II}) \end{cases} \\ I_L^{(Max1)} = I_{L11}^{(Max1)} = I_{L12}^{(Max1)} = I_{L21}^{(Max1)} = I_{L22}^{(Max1)} \\ \Rightarrow 4\theta^{II} = 3\theta^I \end{cases} \tag{10}$$

3) MODE-III [t_2 TO t_3]

Similar to mode III of CCM, all the switches S_1, S_2 and S_3 are turned OFF. The equivalent circuit for this mode is the same as mode III of CCM. During this mode, all the inductors L_{11}, L_{12}, L_{21}, and L_{22} are in series with input voltage source V_i and the Capacitors C_1 C_2 and C_3 along with the load. At the end of this mode, inductors completely demagnetize to zero value at $t = t_3$. For this mode, the maximum amplitude of the current through inductors L_{11}, L_{12}, L_{21}, and L_{22} can be expressed as follows. The current values are expressed in terms of demagnetizing angles and duty ratio.

$$\begin{cases} I_L^{(Max2)} \begin{cases} = 0.25\,(V_o - V_{C1} - V_{C2} - V_{C3} - V_i)\, L^{-1}\delta_3 T_s \\ = 0.25\,(V_o - 4V_i)\, L^{-1}\delta_3 T_s = \delta_3 T_s(\gamma^{III}) \end{cases} \\ \Rightarrow \gamma^{III} = \gamma_{11}^{III} = \gamma_{12}^{III} = \gamma_{21}^{III} = \gamma_{22}^{III} \\ \therefore\ I_L^{(Max2)} = I_{L11}^{(Max2)} = I_{L12}^{(Max2)} = I_{L21}^{(Max2)} = I_{L22}^{(Max2)} \end{cases} \tag{11}$$

4) MODE-IV [t_3 TO t_4]

In this mode, all the switches S_1, S_2, and S_3 are turned OFF and inductor L_{11}, L_{12}, L_{21}, and L_{22} currents remain at zero. The equivalent circuitry for this DCM mode is shown in Fig. 8. Throughout this mode, the inductor L_{11}, L_{12}, L_{21}, and L_{22} energies are zero, and capacitor C_o discharges through the load. Using (10) and (11), the value of δ_3 can be obtained as follows,

$$\delta_3 = \left(\frac{V_i(4\delta_1 + 3\delta_2)}{Vo - 4V_i}\right) \tag{12}$$

$$\begin{cases} I_{Co} = \dfrac{I_L^{(\max 2)}\delta_3 T_s - 2I_o T_s}{2T} = \dfrac{I_L^{(\max 2)}\delta_3}{2} - I_o \\ I_{Co} = \dfrac{(V_i)^2\,(4\delta_1 + 3\delta_2)^2\, T_s}{8L\,(V_o - 4V_i)} - \dfrac{V_o}{R} \end{cases} \tag{13}$$

Since, under steady-state conditions, the value of the current I_{CO} is zero.

$$\frac{(V_i)^2\,(4\delta_1 + 3\delta_2)^2\, T_s}{8L\,(V_o - 4V_i)} = \frac{V_o}{R}$$

Using (12)-(13), voltage gain in DCM is obtained as follows,

$$\begin{cases} G_{DCM} = \dfrac{V_o}{V_i} = 2 + \sqrt{4 + \dfrac{(4\delta_1 + 3\delta_2)^2}{8\chi}}, \quad \chi = Lf_s/R \end{cases} \tag{14}$$

where, χ and f_S is normalized inductor time constant and switching frequency respectively. Fig. 9(a) and (b) show the voltage gain curve of the proposed converter in CCM and DCM mode w.r.t. duty ratio resp. From (8) and (14), the CCM and DCM boundary normalized inductor time constant χ_{LB} is calculated as follows,

$$\chi_{LB} = \frac{(1 - \delta_1 - \delta_2)^2\,(4\delta_1 + 3\delta_2)}{8(4 - \delta_2)} \tag{15}$$

The plot of χ_{LB} versus duty cycle duty ratio D_1 and D_2 is shown in Fig. 9(c) along with CCM and DCM boundaries. It is noted that the CCM and DCM boundary dependent on both duty ratios D_1 and D_2. The condition to operate SIDL converter in DCM is given as follows,

$$\chi_{LB} > \chi \Rightarrow \frac{(1 - \delta_1 - \delta_2)^2\,(4\delta_1 + 3\delta_2)}{2(4 - \delta_2)} > Lf_s/R$$

Therefore, the VLSIDL converter operates in DCM when the value χ_{LB} is higher than χ.

D. EFFICIENCY ANALYSIS

Non-idealities are taken care of while investigating the efficiency of the converter. Fig. 10 depicts the equivalent power circuit of the converter with non-ideal components used to develop the circuit model. However, few simple assumptions are made before the analysis such as inductors being identical in nature have the same inductive and inherent series resistive values (i.e. $L_{11} = L_{12} = L_{21} = L_{22} = L$ and $r_{L11} = r_{L12} = r_{L21} = r_{L22} = r_L$). Also, it is assumed that all the diodes D_1-D_7 are identical and have forward voltage drop V_{FD} and forward resistance r_{FD}. All the switches are identical and have ON state resistance r_s.

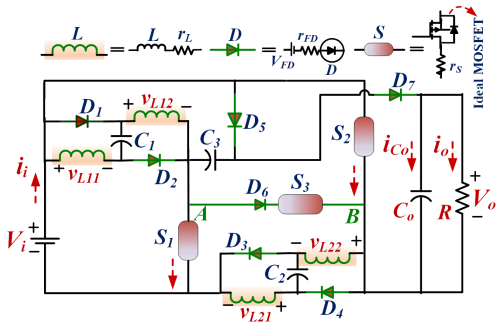

FIGURE 10. The converter layout with non-ideal components.

1) MODE-I [t_0 TO t_1]

The average current through the capacitor C_o and average voltage across the inductors are given by,

$$I_{Co}^{I} = -V_o/R, \quad V_{L11}^{I} = V_i - I_{L11}(r_{L1} + r_{FD} + 2r_S) - V_{FD} \tag{16}$$

Similar equations can be written for other inductor voltages which can be generalized with $V_L = V_{L11} = V_{L12} = V_{L21} = V_{L22}$ owing to identical elements and symmetrical circuit. Moreover, the average Inductor current is also assumed as $i_L = i_{L11} = i_{L12} = i_{L21} = i_{L22}$. Therefore, a simplified equation for the inductor voltage is written as follows,

$$V_L^I = V_i - I_L(r_L + r_{FD} + r_S) - V_{FD}$$

2) MODE-II [t_1 TO t_2]

The average current through the capacitor C_o and average voltage across the inductors are given by,

$$I_{Co}^{II} = -\frac{V_o}{R} V_L^{II} = \frac{3V_i - I_L\,(4r_L + r_S + r_{FD}) - V_{FD}}{4} \tag{17}$$

3) MODE-III [t_2 TO t_3]

The average current through the capacitor C_o and average voltage across the inductors are given by,

$$\begin{aligned} I_{Co}^{II} &= -(I_i - I_0), \\ V_L^{III} &= \frac{4V_i - V_o - I_L\,(4r_L + 2r_{FD}) - 2V_{FD}}{4} \end{aligned} \tag{18}$$

Again, by volt-second balance principle,

$$\int_0^{\delta_1 T_s} V_L^I dt + \int_{\delta_1 T_s}^{\delta_2 T_s} V_L^{II} dt + \int_{\delta_2 T_s}^{(1-\delta_1-\delta_2)T_s} V_L^{III} dt = 0$$

From (16)-(18), the voltage gain obtained as,

$$\begin{aligned} \frac{V_o}{V_i} &= \frac{(4-\delta_2) - A}{(1-\delta_1-\delta_2) + B + C + D} \\ A &= \frac{V_{FD}(2+2\delta_1-\delta_2)}{V_i}, \quad B = \frac{4r_L}{(1-\delta_1-\delta_2)} \\ C &= \frac{r_S(4\delta_1+\delta_2)}{(1-\delta_1-\delta_2)}, \quad D = \frac{r_{FD}(2+2\delta_1-\delta_2)}{(1-\delta_1-\delta_2)} \end{aligned} \tag{19}$$

The total input and output power can be calculated as,

$$\eta = \frac{1 - (V_{FD}/V_i)}{1 + \frac{4r_L}{(1-\delta_1-\delta_2)^2} + \frac{r_S(4\delta_1+\delta_2)}{(1-\delta_1-\delta_2)^2} + \frac{r_{FD}(2+2\delta_1-\delta_2)}{(1-\delta_1-\delta_2)^2}} \tag{20}$$

Therefore,

$$P_{loss} = \left(1 - \frac{1 - (V_{FD}/V_i)}{1 + \frac{4r_L}{(1-\delta_1-\delta_2)^2} + \frac{r_S(4\delta_1+\delta_2)}{(1-\delta_1-\delta_2)^2} + \frac{r_{FD}(2+2\delta_1-\delta_2)}{(1-\delta_1-\delta_2)^2}}\right) \times V_i I_i \tag{21}$$

The aforementioned equation gives the theoretical efficiency of the VLSIDL converter. Moreover, it justifies the inverse relation of parasitic elements in components and duo duty cycles with efficiency. Therefore an optimized duty cycle is chosen for low losses and enhanced converter performance.

III. EFFECT OF UNBALANCED LEGS ON THE CONVERTER

A. IF $L_{11} > L_{12}$ AND $L_{21} > L_{22}$

The unbalanced leg behavior can be realized with many possible relative differences in the inductance values and consequently, the modes of operation will vary. It is assumed that in leg-1, the value of inductance L_{11} is larger than the value of inductance L_{12} (therefore, $L_{11} > L_{12}$), and in leg-2, the value of inductance L_{21} is larger than the value of inductance L_{22} (therefore, $L_{21} > L_{22}$). Predominantly, the inductor's currents depend on the inductance values. The typical waveforms of current through inductors are shown in Fig. 11. Under this condition, the converter operates in four modes as follows,

1) MODE I [t_o TO t_1]

During this mode, the inductors are magnetized parallelly and behave the same way as the mode I of CCM and DCM. Its equivalent circuit model is shown in Fig. 4(a). S_1 and S_2 are ON while S_3 is OFF in this mode and the output capacitor maintains a constant voltage across the load. However, the current in different inductors is not the same owing to its value difference. The slope of inductor current can be calculated as:

$$\left.\begin{aligned} Leg-1: \ \frac{di_{L11}}{dt} &= \frac{V_i}{L_{11}}, \quad \frac{di_{L12}}{dt} = \frac{V_i}{L_{12}} \\ Leg-2: \ \frac{di_{L12}}{dt} &= \frac{V_i}{L_{12}}, \quad \frac{di_{L22}}{dt} = \frac{V_i}{L_{22}} \end{aligned}\right\} \tag{22}$$

During this mode, the current through inductor L_{12} and L_{22} is higher than the current through inductor L_{11} and L_{21} since $L_{11} > L_{12}$ and $L_{21} > L_{22}$, respectively. The magnitude of current through inductors of leg-1 and leg-2 at $t_1 = \delta_1 T_S$ can be obtained as follows,

$$\left.\begin{aligned} Leg-1: \ I_{L11}^{(\max 1)} &= I_{L11}^{(\min)} + \frac{V_i}{L_{11}}\delta_1 T_S; \\ I_{L12}^{(\max 1)} &= I_{L12}^{(\min)} + \frac{V_i}{L_{12}}\delta_1 T_S \\ Leg-2: \ I_{L21}^{(\max 1)} &= I_{L21}^{(\min)} + \frac{V_i}{L_{21}}\delta_1 T_S; \\ I_{L22}^{(\max 1)} &= I_{L22}^{(\min)} + \frac{V_i}{L_{22}}\delta_1 T_S \end{aligned}\right\} \tag{23}$$

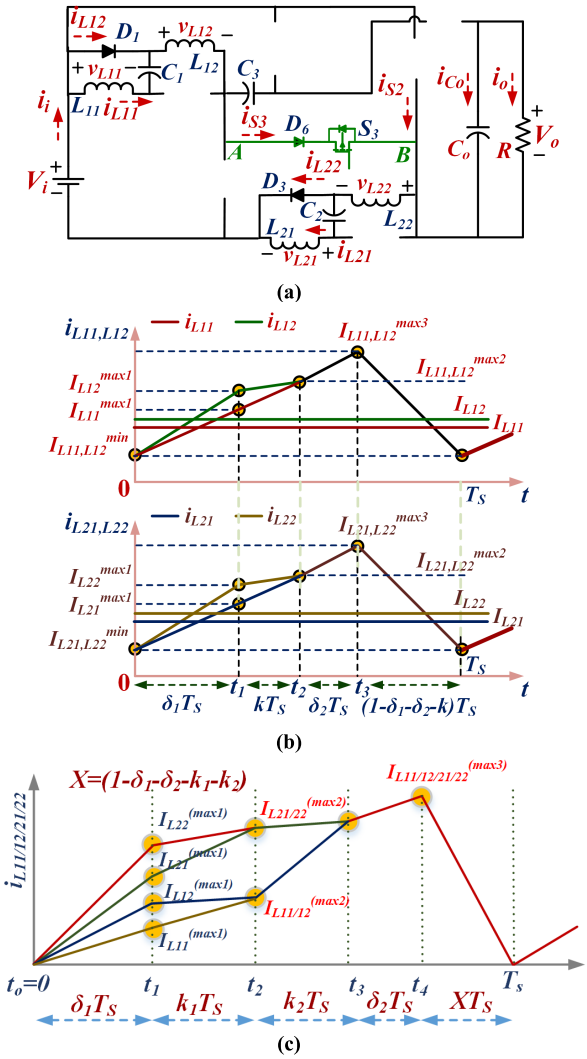

FIGURE 11. (a) Proposed converter structure when $L_{11} > L_{12}$ and $L_{21} > L_{22}$ (modified Mode II), (b) respective inductor current waveforms and (c) Current characteristics of the inductors when their values are unequal.

At the end of this mode ($t_1 = \delta_1 T_S$),

$$I_{L11}^{(\max 1)} < I_{L12}^{(\max 1)}; \quad I_{L21}^{(\max 1)} < I_{L22}^{(\max 1)} \tag{24}$$

2) MODE II [t_1 TO t_2]

This mode of operation is an addition to the operation in CCM with the same value inductance and this mode exists for a short period say kT_S. When S_1 and S_2 are turned OFF and putting S_3 ON, Initially the converter attains the circuit structure as shown in Fig. 4(b). Diode D_1 is still forward biased and provides a path for capacitor C_1 to charge inductor L_{11} and a local path is created. This happens until the current i_{L11} reaches up to the current flowing through the inductor L_{12} i.e. i_{L12} as can be seen from Fig. 10. Similar conditions will rise for the currents in Leg-2. The mathematical governing equations during this mode are:

The slopes of the inductor currents are given as:

$$\left.\begin{aligned} Leg-1: \frac{di_{L11}}{dt} &= \frac{V_{C1}}{L_{11}} \simeq \frac{V_i}{L_{11}}, \quad \frac{di_{L12}}{dt} = \frac{V_i}{2L_{12}} \\ Leg-2: \frac{di_{L21}}{dt} &= \frac{V_{C2}}{L_{21}} \simeq \frac{V_i}{L_{21}}, \quad \frac{di_{L22}}{dt} = \frac{V_i}{2L_{22}} \end{aligned}\right\} \tag{25}$$

And the magnitude of current through the two legs are given as:

$$\left.\begin{aligned} Leg-1: I_{L11}^{(\max 2)} &= I_{L11}^{(\max 1)} + \frac{V_i}{L_{11}} kT_S; \\ I_{L12}^{(\max 2)} &= I_{L12}^{(\max 1)} + \frac{V_i}{2L_{12}} kT_S \\ Leg-2: I_{L21}^{(\max 2)} &= I_{L21}^{(\max 1)} + \frac{V_i}{L_{21}} kT_S; \\ I_{L22}^{(\max 2)} &= I_{L22}^{(\max 1)} + \frac{V_i}{2L_{22}} kT_S \end{aligned}\right\} \tag{26}$$

At the end of this mode ($t_2 = \delta_1 T_S + kT_S$),

$$I_{L11}^{(\max 2)} = I_{L12}^{(\max 2)} = I_{L21}^{(\max 2)} = I_{L22}^{(\max 2)} \tag{27}$$

3) MODE III [t_2 TO t_3]

This mode occurs for a period of $\delta_2 T_S$. The converter behaves the same way as Mode II of CCM and the circuit configuration during this mode can be viewed in Fig. 4(b). The slope of the currents will be:

$$\left.\begin{aligned} Leg-1: \frac{di_{L11}}{dt} &= \frac{di_{L12}}{dt} = \frac{3V_i}{2(L_{11}+L_{12})} \\ Leg-2: \frac{di_{L21}}{dt} &= \frac{di_{L22}}{dt} = \frac{3V_i}{2(L_{21}+L_{22})} \end{aligned}\right\} \tag{28}$$

The current in the inductors will attain the following values:

$$\left.\begin{aligned} Leg-1: I_{L11}^{(\max 3)} &= I_{L11}^{(\max 2)} + \frac{3V_i}{2(L_{11}+L_{12})}\delta_2 T_S; \\ I_{L12}^{(\max 3)} &= I_{L12}^{(\max 2)} + \frac{V_i}{2(L_{11}+L_{12})}\delta_2 T_S \end{aligned}\right\} \tag{29}$$

$$\left.\begin{aligned} Leg-2: I_{L21}^{(\max 3)} &= I_{L21}^{(\max 2)} + \frac{3V_i}{2(L_{21}+L_{22})}\delta_2 T_S; \\ I_{L22}^{(\max 3)} &= I_{L22}^{(\max 2)} + \frac{V_i}{2(L_{21}+L_{22})}\delta_2 T_S \end{aligned}\right\} \tag{30}$$

4) MODE IV [t_3 TO t_S]

The converter operation in this mode resembles the Mode III of CCM with balanced legs. Fig. 4(C) illustrates its conducting path followed by the currents.

$$\left.\begin{aligned} Leg-1: \frac{di_{L11}}{dt} &= \frac{di_{L12}}{dt} = \frac{4V_i - V_o}{2(L_{11}+L_{12})} \\ Leg-2: \frac{di_{L21}}{dt} &= \frac{di_{L22}}{dt} = \frac{4V_i - V_o}{2(L_{21}+L_{22})} \end{aligned}\right\} \tag{31}$$

Using voltage division rule, the voltage across inductor can be obtained as follows,

$$\left.\begin{aligned} V_{L11} &= \frac{4V_i - V_o}{2(L_{11}+L_{12})} \times L_{11}, V_{L12} = \frac{4V_i - V_o}{2(L_{11}+L_{12})} \times L_{12} \\ V_{L21} &= \frac{4V_i - V_o}{2(L_{21}+L_{22})} \times L_{21}, V_{L22} = \frac{4V_i - V_o}{2(L_{21}+L_{22})} \times L_{22} \end{aligned}\right\} \tag{32}$$

With the available voltage of inductors in different modes, the volt-sec principle can be applied on them and the voltage relation obtained is:

$$G_{CCM} = \frac{V_o}{V_i} = \frac{(4-\delta_2)}{1-\delta_1-\delta_2} \tag{33}$$

Therefore, as a conclusion, it can be said that the converter will be having the same voltage conversion ratio even when the values of inductances are different. The behavior of the current is altered with the different modes of operation, nevertheless, the converter as a whole performs well for voltage conversion which it has been designed for.

B. If $L_{11} > L_{12} > L_{21} > L_{22}$ CONDITION

Extending the analysis made in above section, when all the four inductors are having different values is considered. Although there may rise many possible cases such as $L_{11} > L_{12} > L_{21} > L_{22}$ or $L_{11} < L_{12} < L_{21} < L_{22}$ and any more similar to this. For the analysis with different inductors, we have taken the case of $L_{11} > L_{12} > L_{21} > L_{22}$ such that the earlier made discussion can be utilized and a suitable analysis can be made. The above discussion can be extended to the case of $L_{12} > L_{21}$. The current characteristics then will acquire the shape as drawn in Fig. 11(c). As far as modes of conduction are concerned, there will be an additional mode before the current starts to decrease when the inductors are coupled in series to supply the load in the last mode of operation. So all the discussion can be summed up in five modes of operation, the earlier discussed four mode with an additional mode before mode II (CCM) of the inductors in series. The duration of this additional mode can be assumed as k_2T_S.

1) MODE I [t_o TO t_1]

During this mode, the inductors are magnetized parallelly and behaves the same way as the mode I of CCM and DCM. Its equivalent circuit model is shown in Fig. 4(a). S_1 and S_2 are ON while S_3 is OFF in this mode and the output capacitor maintains a constant voltage across the load. However, the current in different inductors are not same owing to its value difference. The slope of inductor current can be calculated as:

$$\left.\begin{aligned} Leg-1: \frac{di_{L11}}{dt} &= \frac{V_i}{L_{11}}, \quad \frac{di_{L12}}{dt} = \frac{V_i}{L_{12}} \\ Leg-2: \frac{di_{L12}}{dt} &= \frac{V_i}{L_{12}}, \quad \frac{di_{L22}}{dt} = \frac{V_i}{L_{22}} \end{aligned}\right\} \tag{34}$$

During this mode, the current through inductor L_{12} and L_{22} is higher than the current through inductor L_{11} and L_{21} since $L_{11} > L_{12}$ and $L_{21} > L_{22}$, respectively. The magnitude of current through inductors of leg-1 and leg-2 at $t_1 = \delta_1 T_S$ can be obtained as follows,

$$\begin{aligned} Leg-1: &\begin{cases} I_{L11}^{(\max 1)} = I_{L11}^{(\min)} + \dfrac{V_i}{L_{11}}\delta_1 T_S; \\ I_{L12}^{(\max 1)} = I_{L12}^{(\min)} + \dfrac{V_i}{L_{12}}\delta_1 T_S \end{cases} \\ Leg-2: &\begin{cases} I_{L21}^{(\max 1)} = I_{L21}^{(\min)} + \dfrac{V_i}{L_{21}}\delta_1 T_S; \\ I_{L22}^{(\max 1)} = I_{L22}^{(\min)} + \dfrac{V_i}{L_{22}}\delta_1 T_S \end{cases} \end{aligned} \tag{35}$$

At the end of this mode ($t_1 = \delta_1 T_S$),

$$I_{L11}^{(\max 1)} < I_{L12}^{(\max 1)}; \quad I_{L21}^{(\max 1)} < I_{L22}^{(\max 1)} \tag{36}$$

2) MODE II [t_1 TO t_2]

This mode of operation is an addition to the operation in CCM with same value inductance and this mode exists for a short period say $k1T_S$. Actually, when S_1 and S_2 are turned OFF and S_3 ON, initially the converter attains the circuit structure as shown in the Fig. 4(b). Diode D_1 is still forward biased and provides a path for capacitor C_1 to charge inductor L_{11} and a local path is created. This happens until the current i_{L11} reaches up to the current flowing through the inductor L_{12} i.e. i_{L12} as can be seen from Fig. 4(a). Similar condition can be noticed for the currents in Leg-2. The mathematical governing equations during this mode are:

The slopes of the inductor currents are given as:

$$\left.\begin{aligned} Leg-1: \frac{di_{L11}}{dt} &= \frac{V_{C1}}{L_{11}} \simeq \frac{V_i}{L_{11}}, \quad \frac{di_{L12}}{dt} = \frac{V_i}{2L_{12}} \\ Leg-2: \frac{di_{L21}}{dt} &= \frac{V_{C2}}{L_{21}} \simeq \frac{V_i}{L_{21}}, \quad \frac{di_{L22}}{dt} = \frac{V_i}{2L_{22}} \end{aligned}\right\} \tag{37}$$

And the magnitude of current through the two legs are given as:

$$\begin{aligned} Leg-1: &\begin{cases} I_{L11}^{(\max 2)} = I_{L11}^{(\max 1)} + \dfrac{V_i}{L_{11}}kT_S; \\ I_{L12}^{(\max 2)} = I_{L12}^{(\max 1)} + \dfrac{V_i}{2L_{12}}kT_S \end{cases} \\ Leg-2: &\begin{cases} I_{L21}^{(\max 2)} = I_{L21}^{(\max 1)} + \dfrac{V_i}{L_{21}}kT_S; \\ I_{L22}^{(\max 2)} = I_{L22}^{(\max 1)} + \dfrac{V_i}{2L_{22}}kT_S \end{cases} \end{aligned} \tag{38}$$

At the end of this mode ($t_2 = \delta_1 T_S + k1T_S$),

$$I_{L11}^{(\max 2)} = I_{L12}^{(\max 2)}, \quad I_{L21}^{(\max 2)} = I_{L22}^{(\max 2)} \tag{39}$$

3) MODE III [t_2 TO t_3]

This mode also occurs for short period k_2T_S. In this mode, switches S_1, S_2 and switch S_3 are still turned OFF. During this mode, the currents through the inductors L_1 and L_2 in leg-1 increase with very small positive slope (approximately zero slope) and the currents through inductors L_3 and L_4 decrease

with a large negative slope in the leg-2 of the converter. The current equations are,

$$\left.\begin{aligned} &Leg-1:\ I_{L11}^{(\max 3)} \simeq I_{L11}^{(\max 2)};\quad I_{L12}^{(\max 3)} \simeq I_{L12}^{(\max 2)} \\ &Leg-2:\ I_{L21}^{(\max 3)} = I_{L21}^{(\max 2)} + \frac{Vo - V_i}{2L_{21}} \\ &\qquad \times (\delta_1+\delta_2+k_1+k_2)T_S; \\ &I_{L22}^{(\max 3)} = I_{L22}^{(\max 2)} + \frac{Vo - V_i}{2L_{22}}(\delta_1+\delta_2+k_1+k_2)T_S \end{aligned}\right\} \tag{40}$$

At the end of this mode ($t_3 = \delta_1 T_S + \delta_2 T_S + k_1 T_S + k_2 T_S$),

$$I_{L11}^{(\max 3)} = I_{L12}^{(\max 3)} = I_{L21}^{(\max 3)} = I_{L22}^{(\max 3)} \tag{41}$$

4) MODE IV [t_3 TO t_4]

This mode occurs for a period of $\delta_2 T_S$. The converter behaves exactly the same way as Mode II of CCM and the circuit configuration during this mode can be viewed in the Fig. 3(b). The slope of the currents will be:

$$\left.\begin{aligned} &Leg-1:\ \frac{di_{L11}}{dt} = \frac{di_{L12}}{dt} = \frac{3V_i}{2(L_{11}+L_{12})} \\ &Leg-2:\ \frac{di_{L21}}{dt} = \frac{di_{L22}}{dt} = \frac{3V_i}{2(L_{21}+L_{22})} \end{aligned}\right\} \tag{42}$$

The current in the inductors will attain the following values:

$$\left.\begin{aligned} &Leg-1:\ \begin{cases} I_{L11}^{(\max 3)} = I_{L11}^{(\max 2)} + \dfrac{3V_i}{2(L_{11}+L_{12})}\delta_2 T_S; \\ I_{L12}^{(\max 3)} = I_{L12}^{(\max 2)} + \dfrac{V_i}{2(L_{11}+L_{12})}\delta_2 T_S \end{cases} \\ &Leg-2:\ \begin{cases} I_{L21}^{(\max 3)} = I_{L21}^{(\max 2)} + \dfrac{3V_i}{2(L_{21}+L_{22})}\delta_2 T_S; \\ I_{L22}^{(\max 3)} = I_{L22}^{(\max 2)} + \dfrac{V_i}{2(L_{21}+L_{22})}\delta_2 T_S \end{cases} \end{aligned}\right\} \tag{43}$$

5) MODE V [t_4 TO t_5]

The converter operation in this mode resembles the Mode III of CCM with balanced legs. Fig. 3(C) illustrates its conducting path followed by the currents.

$$\left.\begin{aligned} &Leg-1:\ \frac{di_{L11}}{dt} = \frac{di_{L12}}{dt} = \frac{4V_i - V_o}{2(L_{11}+L_{12})} \\ &Leg-2:\ \frac{di_{L21}}{dt} = \frac{di_{L22}}{dt} = \frac{4V_i - V_o}{2(L_{21}+L_{22})} \end{aligned}\right\} \tag{44}$$

Using voltage division rule, the voltage across inductor can be obtained as follows,

$$\left.\begin{aligned} &V_{L11} = \frac{4V_i - V_o}{2(L_{11}+L_{12})} \times L_{11},\ V_{L12} = \frac{4V_i - V_o}{2(L_{11}+L_{12})} \times L_{12} \\ &V_{L21} = \frac{4V_i - V_o}{2(L_{21}+L_{22})} \times L_{21},\ V_{L22} = \frac{4V_i - V_o}{2(L_{21}+L_{22})} \times L_{22} \end{aligned}\right\} \tag{45}$$

With the available voltage of inductors in different modes, the volt-sec principle can be applied on them and the voltage gain relation is obtained as:

$$G_{CCM} = \frac{V_o}{V_i} = \frac{(4-\delta_2)}{1-\delta_1-\delta_2} \tag{46}$$

Therefore, as a conclusion it can be said that the converter will be having same voltage conversion ratio even when the values of inductances are different. Obviously the behavior of the current is altered with the different modes of operation but the converter as a whole performs well for voltage conversion which it has been designed for.

IV. CLOSED-LOOP CONTROL

Control objective in this converter is to control the output voltage during perturbations in input voltage, output resistance and duty ratio. Unlike other DC-DC converters consisting of only one switch, the proposed converter consists of three switches (S_1, S_2 and S_3). As, switches S_1 and S_2 are switched simultaneously, the number of switches to be controlled are reduced to two. Conditions governing the control algorithm are given below:

a) Duty cycle of the two switches must follow the inequality ($S_{1/2} + S_3 \leq 1$).

As power stored in the charged inductors is supplied to the load only when all the switches are open. Thus, the sum of two duty cycles must never be greater than 1.0.

b) Depending upon the operating mode i.e., $S_{1/2} < S_3$ or $S_{1/2} > S_3$ saturation limits of the two duty cycles must be appropriately selected.

c) There are three states in a switching cycle operation. Switch S_3 must be turned ON just before switches S_1 and S_2 has been turned OFF.

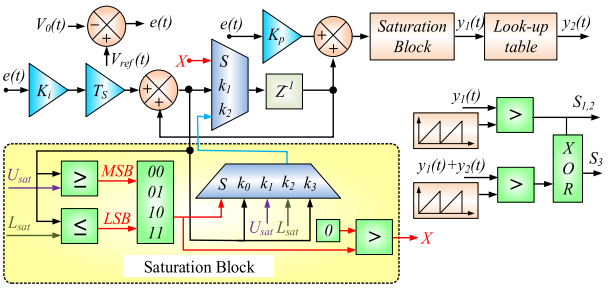

FIGURE 12. Closed controller logic of the proposed converter.

Considering these constraints, the two duty cycles are dependent upon each other. Thus, only one control loop is required to achieve closed-loop performance of the converter. The other duty cycle can be determined by using the lookup table based on the recorded steady state performance of the converter. With the above discussed strategy, the control algorithm is shown in Fig. 12. Error obtained by subtracting output voltage reference with actual output voltage is represented by *e(t)*. This error is passed through PI controller block to generate a $y_1(t)$ and which will passed through lookup table to generate a signal of $y_2(t)$. Both the constant value signal $y_1(t)$ and $y_1(t) + y_2(t)$ are compared with carrier signal of 100 kHz frequency to generate the duty cycles. The respective duty

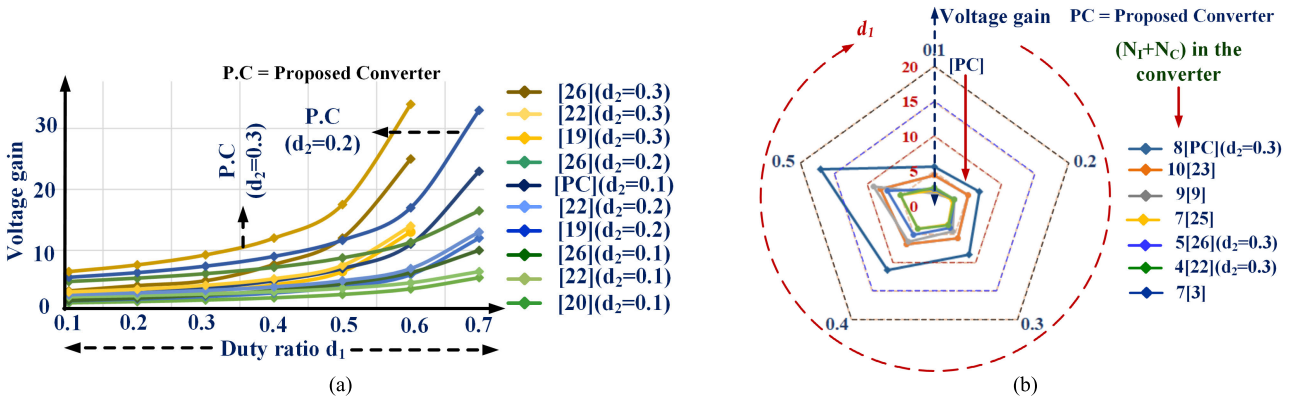

FIGURE 13. (a) Graph of voltage gain comparison and (b) plot for different converters having different numbers of energy storing elements.

pulse of both switches are obtained by doing the XOR logic operation as shown in Fig. 12.

V. COMPARISON OF CONVERTERS

Table- 1 presents the packed in detail comparison of the proposed converter with recently introduced high gain DC-DC converters. In [14], the proposed topology contributes high gain with reduced voltage spikes across the switches but possesses a complex and bulky structure with too many components particularly the coupled inductors in the converter circuit. The converter in [23] has the voltage gain four times the gain of the conventional boost converter. However, this converter has increased reverse recovery losses and poor efficiency along with a bulky structure. In [24], the converter has many important features, such as high gain, low stress, and common ground. However, the converter is very sensitive to ESR owing to the more number of different value capacitors which ultimately needs a proper voltage regulation. Asymmetrical switched inductor (A-SL) and symmetrical SL-based converter have been proposed in [4]. This converter has gained an increase in voltage ratio on account of additional inductors and diodes. However, a very high voltage appears across the output diode and an accurate design is needed to make the leg of the inductor balanced. The converter in [9] can be used for very high voltage applications but it has an excessive number of passive and active components making the circuit bulky and costlier. In [25], a dc-dc converter with higher voltage gain is presented which has features of low input ripples, low losses, and high efficiency. However, the converters mentioned so far are single duty type which lacks a widened range of duty ratio and can't be operated beyond a certain level of high duty ratio (around 0.8). An additional switch-diode pair is used in [19], [22], [26] to operate the converter in three modes of CCM to achieve the desired voltage at the output. The converters in [19], [22] constitute a high voltage across the diode and therefore a higher PIV rating diode is the prime requirement. The converter in [20] has a generalized extension for triple mode operation. However, there has been always a compromise of the performance with increasing number of cells involving switches and inductors. The total number count of the proposed converter and converter mentioned in [27] is same but the proposed converter operate with only three controlled switches and providing the flexibility in duty ratio selection which is not possible in the mentioned converter. As compared to the converter [20], the total number of the components is more and both converter providing the flexibility in duty ratio selection. Nevertheless, the voltage gain of the proposed converter is high and having lower voltage stress on the diodes as compared to the converter mentioned in [20]. The proposed converter has a double duty characteristic being operated in three modes of CCM and holds most of the aforementioned features including a precise control over the output voltage and a wide range of duty ratio. As far as voltage gain is concerned, the proposed converter provides the highest gain when an appropriate combination of duty ratio is chosen. Moreover, double duty feature of this proposed converter can be utilized for different applications e.g. controlling MPPT while being used with Photovoltaic. Voltage gain comparison with different topologies has been done and plotted in Fig. 13(a) and (b). In Fig. 13(a), flexible duty converters involving three switches are compared for their voltage gains at low duty ratio and Fig 13(b) shows the plot for different converters having different numbers of energy storing elements. It can be concluded in terms of voltage gain that the proposed converter offers the highest gain compared to all extended duty ratio converters on the cost of the mere increase in passive elements in the circuit.

VI. DESIGN OF COMPONENTS

In order to achieve the desired performance of the converter, it must be designed properly with suitable components.

A. INDUCTOR DESIGN

Same value identical inductors are chosen owing to their similar behavior and current characteristics in the circuit. For the required ripples in inductor current (ΔI_L), the value of

TABLE 1. Comparision of high gain converters.

	$G_{CCM}=V_2/V_1$	Maximum stress on diodes	Switch voltage stress	Normalized switch voltage	Number of			
					N_S	N_C	N_I	N_D
[3]	$4/(1-\delta)$ for $n=1$	$3\,V_o/4$	$S_1=S_2=V_o/4$	$S_1=S_2=1/4$	2	5	2	4
[23]	$4/(1-\delta)$	$V_o/2$	$S_1=S_2=V_o/4$	$S_1=S_2=1/4$	2	8	2	4
[9]	$(1+7\delta)/(1-\delta)[n=2]$	$(V_o+V_i)/V_o$	$S_1=S_2=(3V_i+V_o)/(4V_o)$, $S_3=S_4=(3V_o+V_i)/(4V_o)$	$S_1=S_2=(3+G_{CCM})/(4G_{CCM})$, $S_3=S_4=(1+3G_{CCM})/(4G_{CCM})$	4	1	8	17
[25]	$(2+\delta)/(1-\delta)$	$(V_o+V_i)/3V_o$	$(V_o+V_i)/3V_o$	$(1+G_{CCM})/(3G_{CCM})$	1	5	2	4
[22]	$(3+\delta_1-\delta_2)/(1-\delta_1-\delta_2)$	$(V_o+V_i)/2V_o$	$S_1=S_2=(V_o+V_i)/4V_o$, $S_3=(V_o-V_i)/2V_o$	$S_1=S_2=(1+G_{CCM})/(4G_{CCM})$ $S_3=(G_{CCM}-1)/(2G_{CCM})$	3	3	2	4
[11]	$(3-\delta_1-2\delta_2)/(1-\delta_1-\delta_2)$	(V_o-V_i)	$(V_o-V_i)/2V_o$, $(V_o-2V_i)/V_o$	$(G_{CCM}-1)/(2G_{CCM})$, $(G_{CCM}-2)/(G_{CCM})$	3	3	2	4
[19]	$(1+\delta_1)/(1-\delta_1-\delta_2)$	V_i+V_o	$S_1=S_2=(V_o+V_i)/2$, $S_3=V_o$	$S_1=S_2=(G_{CCM}+1)/2G_{CCM}$, $S_3=1$	3	1	2	2
[26]	$(1+3\delta_1+\delta_2)/(1-\delta_1-\delta_2)$	V_i+V_o	$S_1=S_2=(V_o+V_i)/2$, $S_3=V_o$	$S_1=S_2=(G_{CCM}+1)/2G_{CCM}$, $S_3=1$	3	1	4	8
[22]	$(2-\delta_2)/(1-\delta_1-\delta_2)$	V_o+V_i	$S_1=S_2=V_o/2$, $S_3=V_o-V_i$	$S_1=S_2=1/2$, $S_3=(G_{CCM}-1)/G_{CCM}$	3	2	2	3
[27]	$(5\delta+3)/(1-\delta)$	$(V_o+V_i)/2$	$S_1=S_3=V_o/4$, $S_2=S_4=(V_o+4V_i)/8$	$S_1=S_2=1/4$, $S_3=(G_{CCM}+4)/8G_{CCM}$	4	3	4	7
[20]	$3/(1-\delta_1-\delta_2)$ for $n=2$	V_o	$S_1=S_2=V_o/3$, $S_2=2V_o/3$ $S_3=V_o$	$S_1=S_2=1/3$, $S_2=1/3$ $S_3=1$	4	3	3	4
Proposed Conv.	$(4-\delta_2)/(1-\delta_1-\delta_2)$	V_o-V_i	$S_1=S_2=V_o/2$ $S_3=(V_0-V_{in})/2$	$S_1=S_2=1/2$ $S_3=(G_{CCM}-1)/2G_{CCM}$	3	4	4	7

N_S: switches, N_C: capacitors, N_I: inductors, N_D: diodes.

inductance must satisfy the following constraint,

$$L \geq \frac{V_i(\delta_1 + 0.75\delta_2)}{\Delta I_L f_S} \tag{47}$$

B. CAPACITOR DESIGN

The capacitors $C_{1/2}$, C_3, and C_0 are used in the circuit which also needs a careful design. Their values are chosen according to the following equations,

$$\begin{cases} C_{1/2} \geq \dfrac{(4-\delta_2)^2(1-\delta_1)}{R(1-\delta_1-\delta_2)^2(\Delta V_{C1/2}/V_{C1/2})f_S} \\ C_3 \geq \dfrac{(4-\delta_2)^2}{R(1-\delta_1-\delta_2)(\Delta V_{C3}/V_{C3})f_S} \\ C_0 \geq \dfrac{(\delta_2+\delta_1)}{R(\Delta V_{C0}/V_{C0})f_S} \end{cases} \tag{48}$$

C. VOLTAGE STRESS ACROSS SWITCHES

$$V_{S1} = V_{S2} = \begin{cases} = 0 \\ = 0.5V_i \\ = 0.5V_0, \end{cases} \qquad V_{S3} = \begin{cases} = V_i \\ = 0 \\ = (V_o - V_i) \end{cases} \tag{49}$$

Therefore, the voltage ratings of the switches must be chosen appropriately so that they can bear the aforementioned voltages across them

D. VOLTAGE STRESS ACROSS DIODES

Diode selection is done such that its voltage rating must be higher than PIV across it. Voltage ratings of diodes are calculated as follows,

$$V_{D1/2/3/4} = \begin{cases} = 0 \\ = -0.25V_0 \\ = -0.25V_0, \end{cases} \qquad V_{D5} = \begin{cases} = 0 \\ = -0.5V_i \\ = -0.5V_0, \end{cases}$$

$$V_{D0} = \begin{cases} = -V_0 \\ = -(V_i - V_0) \\ = 0 \end{cases} \tag{50}$$

Therefore, the diodes ratings must be the following,

$$V_{D1/2/3/4} \geq 0.25V_o, \quad V_{D5} \geq 0.5V_o, \; V_{D0} \geq (V_0 - V_i) \tag{51}$$

VII. EXPERIMENTAL INVESTIGATION

The proposed converter functionality is validated by the prototype model with specifications as tabulated in Table 2. The two gate pulses are generated through Virtex-5 FPGA with a 50% duty cycle (δ_1) to control switches S_1 and S_2. Also, the gate pulse with a 30% duty cycle (δ_2) is generated to control switch S_3 with a delay of ON period of switch $S_{1/2}$.

The experimental waveform of output voltage (V_0), output current (i_0), input voltage (V_i), and input current (i_i), is shown in Fig. 14 and Fig. 15 with $\delta_1 = 0.5$ and $\delta_2 = 0.3$. It is observed that the proposed converter developed the 400V at the load from the 23V input supply. It is noted that the input current is the addition of inductors ($L_{11} - L_{22}$) current and capacitors ($C_1 - C_3$) current and reaches its peak amplitude

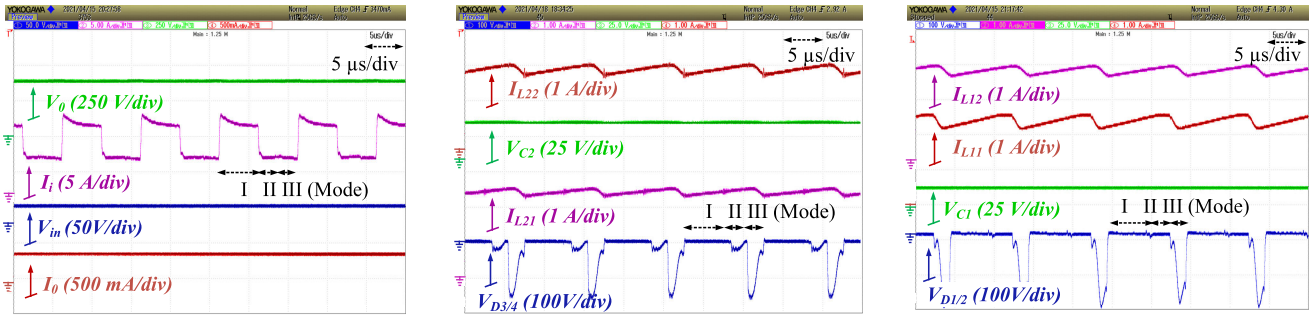

FIGURE 14. Waveform of (a) Input-output voltage and current; (b) inductor L_{21} current (i_{L21}), inductor L_{22} current (i_{L22}) and capacitor C_2 voltage (V_{C2}), PIV of diode $D_{3/4}$ ($V_{D3/4}$); (c) inductor L_{12} current (i_{L12}), inductor L_{11} current (i_{L11}), and capacitor C_1 voltage (V_{C1}), PIV of diode $D_{1/2}$ ($V_{D1/2}$) at $\delta_1 = 0.6$, $\delta_2 = 0.2$.

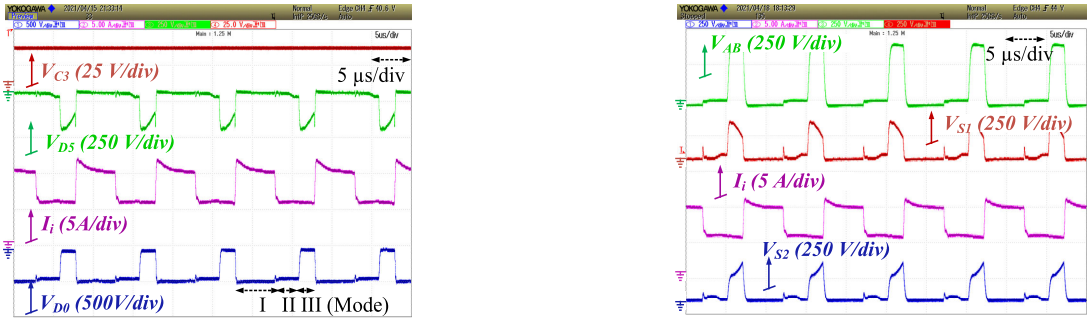

FIGURE 15. Waveform of (a) PIV of diode D_0 (V_{D0}), PIV of diode D_5 (V_{D5}), voltage across capacitor C_3 (V_{C3}), input current (i_{in}); and (b) voltage across switch S_1 (V_{DS1}), switch S_2 (V_{DS2}), voltage combination of switch S_3 and diode D_6 (V_{AB}) and input current (i_{in}) at $\delta_1 = 0.5$, $\delta_2 = 0.3$.

in mode-I. Whereas, the input current is equal to the inductor current in mode-II and with the same positive slope as in mode-I. In mode-III, the input current starts decreasing with a negative current slope as discussed in the working principle. From Fig. 14(a) the observed that the average output voltage is 400 V, the input voltage is 23 V, and the output current is 0.48 A. From Fig. 14(a), it was noticed that the proposed converter work with 94% efficiency at 200W power.

Fig. 14(b) depicts the waveform of voltage across the capacitor C_2 (V_{C2}), peak inverse voltage of diode D_3 (V_{D3}) and D_4 (V_{D4}), and inductors L_{21} and L_{22} current. It is observed that the capacitor C_2 is charged up to an input voltage of 23V. Inductors L_{22} and L_{21} are magnetizing in mode-I, II, and demagnetize in mode-III with an average current of 2.4 A. The diodes D_3 and D_4 having the PIV of 100V in mode-III only. The voltage fluctuation was observed across the diodes voltage waveform due to the inductor mismatching. Fig. 14(c) depicts the waveform of inductors L_{11} and L_{12} current, peak inverse voltage of diode $D_{1/2}$ ($V_{D1/2}$), and the voltage across the capacitor C_1 (V_{C1}). It is observed that in mode-I and II inductors L_{11} and L_{12} is magnetizing, and demagnetize in mode-III with an average current of 2.3 A. The capacitor C_1 is charged up to an input voltage of 23V. The diodes $D_{1/2}$ having the PIV of 100V in mode-III. Fig. 15(a) depicts the waveform of PIV of diode D_0 (V_{D0}) and D_5 (V_{D5}), capacitor C_3 (V_{C3}), and input current. In mode-I, the PIV

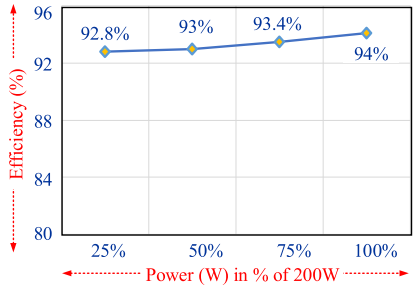

FIGURE 16. Efficiency Vs Power curve.

across the diode D_0 is 400V and 377V in mode-II as discussed in section II. Whereas, PIV across diode D_5 is 200V in mode-III. The capacitor C_3 is charged up to input voltage (23V). Fig. 15(b) depicts the waveform of input current, voltage across switch S_1 and S_2 (drain to source), and voltage combination of switch S_3 and diode D_6 (V_{AB}). It is observed that the maximum voltage stress across switch S_1 and S_2 is equal to half of the output voltage (200V) in mode-III only. Whereas, maximum voltage stress across a combination of switch S_3 and diode D_6 (V_{AB}) is 370V which is equal to the voltage difference of output voltage and input voltage. As far as efficiency is concerned it calculated for 200W prototype and achieved 94% as this power range. However, the efficiency in terms of power variation have also been calculated for a certain range of power as shown in the Fig. 16.

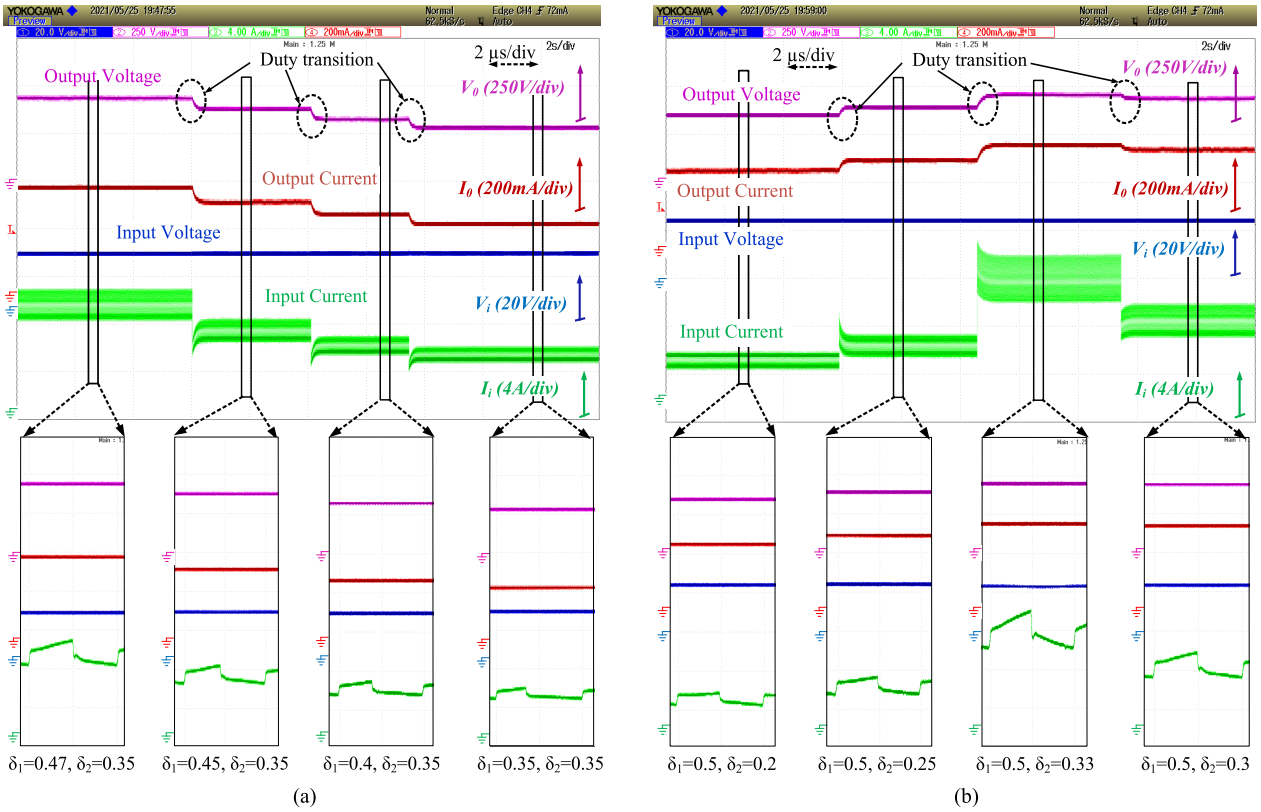

FIGURE 17. Experimental results of the proposed converter under (a) Change in δ_1 and fixed δ_2 and (b) change in δ_2 and fixed δ_1.

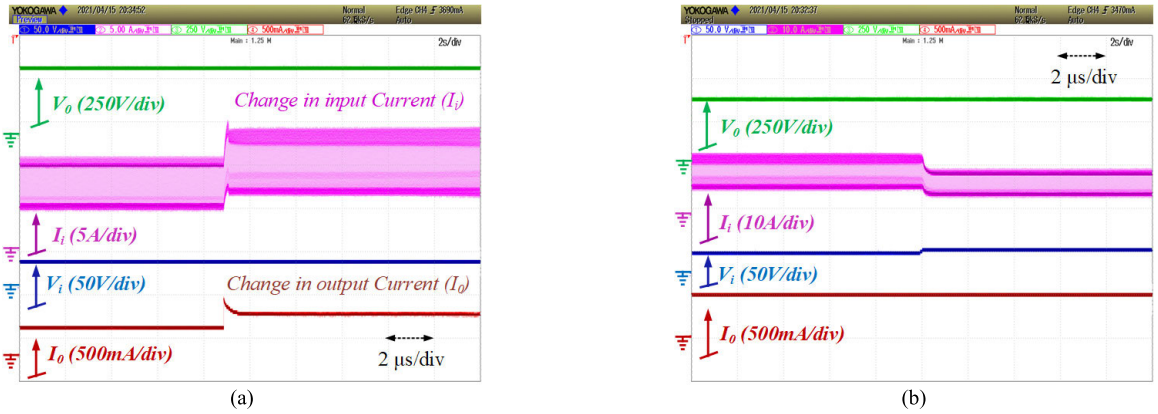

FIGURE 18. Dynamic behaviour of the proposed converter under change in (a) resistive load in open loop and (b) change in input voltage in closed-loop control.

The dynamic behavior of the proposed converter is experimentally tested with change in the duty ratio at constant input voltage and load resistance. The capacitor is connected at the input terminal which is acting as an input filter. Firstly, the proposed converter is experimented with fixed δ_2 duty ratio at 0.35 and variable δ_1 duty ratio (0.47, 0.45, 0.4, and 0.35) and the obtained results are shown in Fig. 17(a). Fig. 17(b) shows the dynamic behavior of the proposed converter with fixed δ_1 duty ratio at 0.5 and variable δ_2 duty ratio (0.2, 0.25, 0.3 and 0.33). The highest peak voltage achieved by the proposed converter is nearly 435V at combination of ($\delta_1 = 0.5$ and $\delta_2 = 0.33$) and ($\delta_1 = 0.47$ and $\delta_2 = 0.35$). From these results it can be conclude that the proposed converter is working satisfactorily at the different combination of the duty ratio.

The dynamic response of proposed converter under change in input voltage (V_i), and load resistance or power (P_0) is examined to validate its functionality.

Test I (Response Under Perturbation of Load Resistance or Power in Open-Loop): Fig. 18(a) depicted the output voltage (V_0), input voltage (V_i), output current (i_0) and input current (i_i) waveforms when load resistance or power (P_0) change. It is observed that the constant output voltage 400 V is achieved from constant 23 V even load resistance or power changed.

TABLE 2. Designing parameters of the proposed converter.

Parameters	Prototype
Power	200 W
Input Voltage (V_{in})	23 V
Duty ratio	δ_1=0.5, δ_2=0.3
Output voltage (V_0)	400 V
Load	800 Ω
Switching freq.	100 kHz
Inductors (L_{11}-L_{22})	≈1 mH, 20A (shell type,)
Capacitor $C_{1/2/3}$	≈220 μF, 100 V (film)
Capacitor C_0	≈220 μF, 450 V (film)
Switches S_1, S_2, S_3	V_{DS}=900 V, i_D=36 A, R_{ON}=65 mΩ (C3M0065090)
Diode D_0	V_{RRM}=600 V, i_F=30 A, R_{ON}=0.01Ω, V_F=0.8 V (STTH30R04/6)

Also there is spike observed in the both current waveform due to the hard manual changing the load resistance value instead of electronics load. The input and output current changed accordingly to satisfy the power balance at input and output side.

Test II (Response Under Input Voltage (V_i) Perturbation): To observe the dynamic performance of proposed converter with perturbation in input voltage, the input voltage with perturbation of 20% increment in input voltage i.e. (23V to 28V) is applied to system and reference output voltage set to +400 V at constant power or fixed load resistance. The experimental results obtained under test-II is shown in Fig. 18(b) which shows the input voltage (V_i), input current (i_i), output voltage (V_0) and output current (I_0) waveform with perturbed input voltage. It is observed that a constant 400 V is achieve at the output even though input voltage is increased by 20%. Moreover, to support the investigation, input current (i_i) and output current (i_0) is also shown. From the input current waveform, it is noticed that, the mean value of input current is decreased in corresponding to increase in input voltage to maintain the power equality at input and output side. To maintain the constant output voltage with respective change in input voltage, the duty cycle (δ_1 and δ_2) need to be adjust by PI controller according to the error signal.

The experimental results under perturbation of two test always match with theoretically analysis as expected and support the theoretical background developed.

VIII. CONCLUSION

A novel high gain Voltage Lift Switched Inductor-Double-Leg (VLSIDL) boost converter having extended duty range has been proposed for 400 V DC microgrid application. With the fine adjustment of two different duty ratio and three different operating modes, the high voltage gain has been achieved at a very reasonable duty ratio. The impact of varying the duty ratios in different combinations is also discussed. The double duty provides flexibility in choosing the best possible combination to attain a certain high voltage. The CCM, DCM characteristics waveform has been analyzed and CCM-DCM boundary, efficiency analysis have been explained in detail. It is observed from the mathematical analysis that, the maximum voltage gain can be achieved with a low (δ_2) duty pulse. From the experimental results, it concludes that the proposed converter work with 94% efficiency at $\delta_1 = 0.5$ $\delta_2 = 0.3$ for power 200 W. The experimental results confirm the theoretical analysis, feasibility, and performance of the proposed converter.

ACKNOWLEDGMENT

The statements made herein are solely the responsibility of the authors. The open access charges are paid by the Qatar National Library.

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