Mitigation of voltage imbalance in power distribution system using MPC-controlled packed-U-cells converter

Ibrahim Ahmed | **Nasser Al-Emadi** | **Adel Gastli** | **Lazhar Ben-Brahim**

Department of Electrical
Engineering, Qatar University, Doha, Qatar

Correspondence
Ibrahim Ahmed, Department of Electrical
Engineering, Qatar University, Doha, Qatar.
Email: ia1306439@qu.edu.qa

Abstract

Delivering high power quality in single-phase distribution has witnessed more challenges especially with the increased penetration of single-phase distributed generation (DG). This paper proposes a smart solid-state-based transformer, which aims to replace traditional ones, for single-phase distribution laterals, and provide load balancing and protection to the three-phase main feeders, that is based on connecting the single-phase lateral to the three-phase main feeder through a power electronics converter. This converter transfers balanced power from and to the three-phase feeder while automatically regulating the lateral single-phase voltage, hence, assuring high power quality without requiring any transformer on-load tap changer. A 7-level packed-U-cells (PUC) single-phase inverter topology was used to deliver single-phase regulated sinusoidal voltage to the AC loads, and at the same time, it is able to deliver DC power to DC loads. The simulation and hardware-in-the-loop (HIL) results have shown that the proposed topology delivers high power quality for both AC and DC loads under different operating scenarios. Moreover, the converter can play the role of a solid-state protection device coordinated with other up- and downstream protective devices. Finally, this system can be integrated within the smart grid allowing more flexibility for automation and efficient control of the grid.

KEYWORDS
distributed generation, PUC inverter, smart grid, solid-state transformer, voltage imbalance

1 | INTRODUCTION

Radial power distribution systems provide power to customers with three, two or single phases depending on the loads' requirements (see Figure 1). Most residential loads are single-phase types and are connected to single-phase distribution systems. The single-phase power distribution creates serious load balancing and power quality challenges on the three-phase main feeders and transformers including over-currents relay action, over-loads, in addition to the reduced performance of induction motors.[1] This problem has worsened with the increasing penetration of distributed generation (DG) such as rooftop PV and vehicle-to-grid (V2G) installations. Indeed, the number of small-scale distributed generators installed in the distribution network has dramatically grown, especially in low-voltage networks.[2,3] In these systems, the unevenly distributed power flow through the three phases may even worsen due to single-phase connected DGs, causing voltage deviations and unbalance. In other words, good balancing is very difficult with such new and very complex distribution system configurations.[4]

The three pillars of smart grid distribution as described in Ref. [5] are remote control and automation, decentralized energy management, and smart metering. These features require advanced metering, management, and protection systems in distribution networks. In conventional systems, the protection on the laterals is assured by cutoff fuses. However, these fuses have to be replaced manually after any fault and in most of the cases cannot be remotely controlled.[6] Moreover, automation with such a system configuration and devices is quite difficult if not impossible. Additionally, voltage regulation on the radial system is also challenging when many and different types of long laterals are used. In most of the conventional cases, voltage regulation is performed at the substation level instead of at individual loads on laterals and sub-laterals.[7]

To address these challenges, this paper proposes a novel single-phase distribution approach for distribution system laterals that incorporates smart grid features. The proposed approach ensures load balance on the three-phase main feeders by converting single-phase loads into balanced three-phase loads and provides smart protection and regulation of the voltage and current on individual single-phase laterals. Furthermore, smart power metering is also possible on each lateral since the voltage and current are sensed for control of the power electronic converters. These data could be utilized by adding a communication link between the power electronic converter and the smart grid control system to be part of the advanced metering infrastructure (AMI). The inverter design is based on the recently developed packed-U-cells (PUC) multilevel inverter which implements additional levels with the least number of switches while allowing for additional features.

The paper is organized into five sections in addition to the introduction: section II presents a literature review of the problem of power distribution system voltage balancing; section III describes the proposed voltage balancing topology; section IV discusses the simulation and its results; section V shows the hardware-in-the-loop simulation; and section VI concludes the paper.

2 | LITERATURE REVIEW

Due to the nonuniform power distribution on the three phases, the resulting currents flowing through the three-phase distribution transformer in the secondary substation are generally not balanced (with significant negative and zero sequence components), leading to different voltage drops on the three phases. This affects all loads connected to the same point of common coupling (PCC). Several approaches were proposed in the literature to mitigate the effect of single-phase loads and DG on the distribution systems. Most of them concentrate on compensating for the negative

and zero sequence components of the currents upstream the PCC using different methods. Authors in Ref. [8] proposed a controller that can mitigate the voltage unbalance at the PCC of a low-voltage network, intended as the busbar placed at the secondary side of the MV/LV transformer. This method is mainly based on compensating for the current sequences' components to pursue the relative currents balance, leading to the voltage unbalance mitigation. An important aspect associated to this regulation strategy is that the low-voltage network controller, operating at the PCC, could be considered as an interface to the main distribution grid, exchanging signals for the provision of ancillary services to the MV grid by the LV network considered as a whole.

Assuming a mature smart grid operation scenario, some kind of mechanism is expected to involve the distributed energy resources (DER) in the network management through a communication infrastructure to maintain power exchange with the upstream HV grid by a local market for ancillary services.[9] Furthermore, the ability to communicate signals across the distribution network to reach even the small DG units connected to the LV network can allow the coordination of the DG units in the entire system. In this way, both users connected to the MV network and secondary substations can participate in the network management replying to request signals coming from the main system.[10,11] The low-voltage network controller (LVNC), installed at the PCC, has the aim of elaborating the power request signals for the unbalance control, but it represents also a suitable interface to the MV grid, enabling the LV network to participate in the MV distribution system regulation by replying to the ΔP and ΔQ request signals communicated by the MV Distribution Management System (DMS). In this work, the focus is on the LV grid management, where the coordinated control involves both three-phase and single-phase inverters as shown in Figure 2.[10] This control strategy is able to mitigate the power quality issues within the low-voltage networks and, at the same time, provide network services for the regulation of the upstream medium-voltage network. However, it can be applied inside distribution substations only and cannot solve
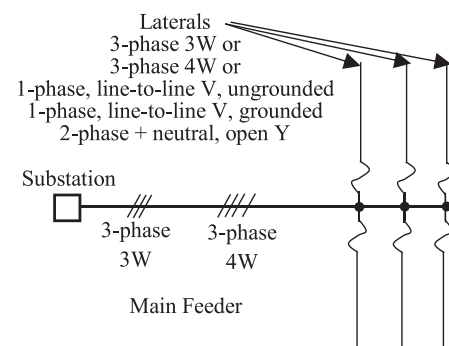
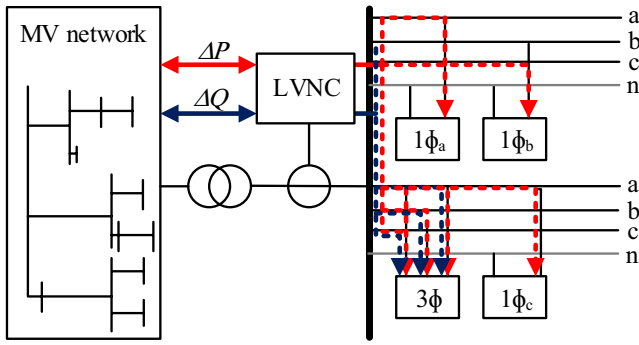

FIGURE 1 Typical power distribution system configuration

FIGURE 2 Conceptual scheme of the coordinated control for voltage balancing

FIGURE 3 Mixed three-phase and single-phase distribution system. A, Conventional unbalanced distribution approach. B, Proposed distribution approach using SSTs

the problem of mixed three-phase and single-phase distribution through a lateral and sub-laterals on the main feeder. An example is shown in Figure 3A, where the voltage regulation is conducted on the substation busbar while the three-phase customers far from the substation, even if they are fed by the same main feeder, will still witness voltage unbalance and hence power quality issue.

Other more recent and advanced methods use solid-state transformers (SSTs), which employ power electronics in the MV/LV conversion, with current compensation or modular self-balancing topologies that ensure the phases are balanced. These methods either offer a limited range such as separate phase connection (SPC) and cross phase connection (CPC) or rely on a large number of components such as the modular self-balancing topologies. A review and comparison between these methods is presented in Ref. [12].

3 | PROPOSED DISTRIBUTION SYSTEM BALANCING TOPOLOGY

The proposed approach is illustrated in Figure 3B and the topology of the SST is shown in Figure 4. It consists of placing a three-phase to single-phase bidirectional power electronics converter for any single-phase distribution system. The bidirectional three-phase controlled rectifier converts the three-phase AC power from the main feeder into a regulated DC power that is fed to a multilevel single-phase inverter and a filter to produce regulated pure sine voltage waveform. Since the rectifier is a balanced three-phase load,[13] the system will be inherently balanced. The multilevel inverter also produces DC voltage that could be used to feed small DC loads and/or integrate renewable sources such as PV panels as illustrated in the figure. In this paper, we will concentrate on the system application to low-voltage power distribution such as residential single-phase distribution system which can integrate rooftop PV as DER. The proposed system can integrate the smart meter conventional functions in addition to load balancing and power quality control features.
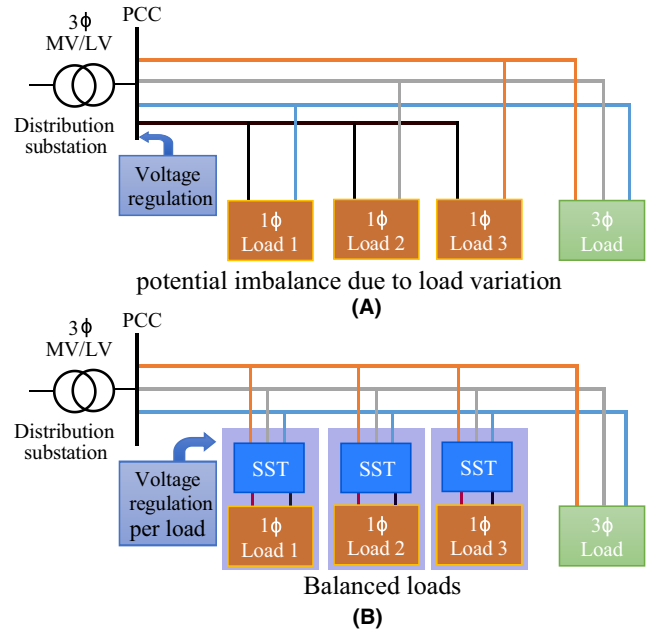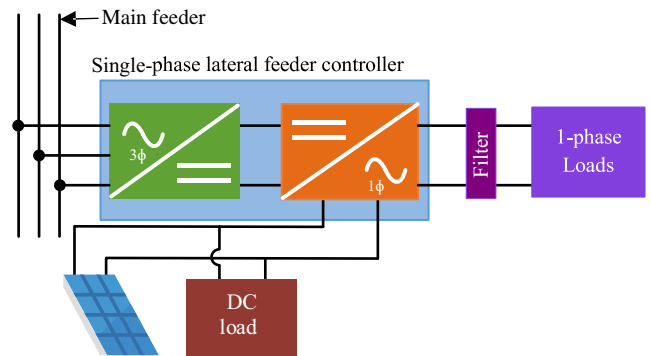

FIGURE 4 Proposed solid-state transformer-based topology

3.1 | Rectifier design

The rectifier needs to ensure the balance of the three-phase system and provide power factor correction and input current harmonics mitigation. A topology such as the four-switch three-phase (FSTP) presented in Ref. [14-16] can be used. Readers can refer to these references which show the rectifier topology in detail operated with balanced and unbalanced grids and using new methods to reduce the ripples in the DC link. This paper will focus on the design of the inverter; therefore, a diode rectifier with inductive filter is used for simplicity and to demonstrate the principle. However, the idea works well with active rectifiers that regulate the voltage, improve the power factor, and reduce current harmonics, and this has already been well addressed in the literature.
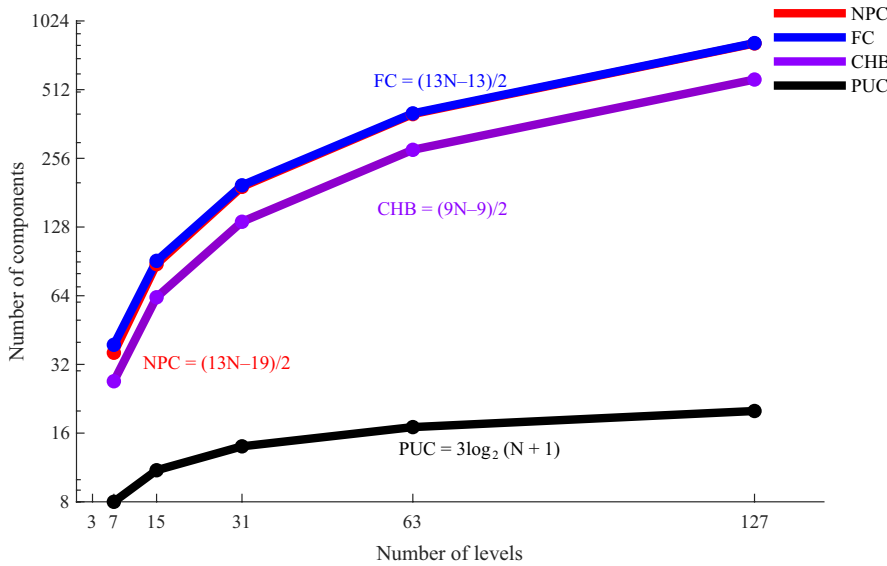
FIGURE 5 Number of components to implement additional levels for each inverter topology

3.2 | Single-phase inverter design

The selected single-phase inverter must deliver high power quality to households while satisfying the following constraints:

1. The output voltage should be purely sinusoidal with a total harmonic distortion (THD) less than 5% for residential loads (complying with the IEEE-519 standards[17]).
2. The output voltage drop should not exceed 10% of the standard nominal distribution voltage.
3. The final product should be compact enough to fit into a typical household meter compartment.

There are several ways to achieve the first constraint. First, a large filter could be employed to mitigate the harmonics and produce a low THD signal. However, this would make the final product bulky and might violate the third constraint. Another solution is to increase the switching frequency of the inverter so that the switching harmonics would fall into the high-frequency spectrum and require a smaller filter. Nonetheless, higher switching frequency increases the switching losses. Therefore, the best approach to minimize the filter size while using a medium switching frequency is to use multilevel inverter topologies.

Several single-phase multilevel inverter topologies were proposed in the literature, and among them, the most famous ones are as follows: flying capacitor (FC),[18] cascaded H-bridge (CHB),[19] neutral point clamped (NPC),[20] and packed U cells (PUC).[21] The main differences between them lie in the number of components for additional levels and their optimal control strategies. Using,[22] the relationship between the number of levels and the number of components required to implement them is shown in Figure 5 for each topology. Note that the PUC converter implements more levels with the
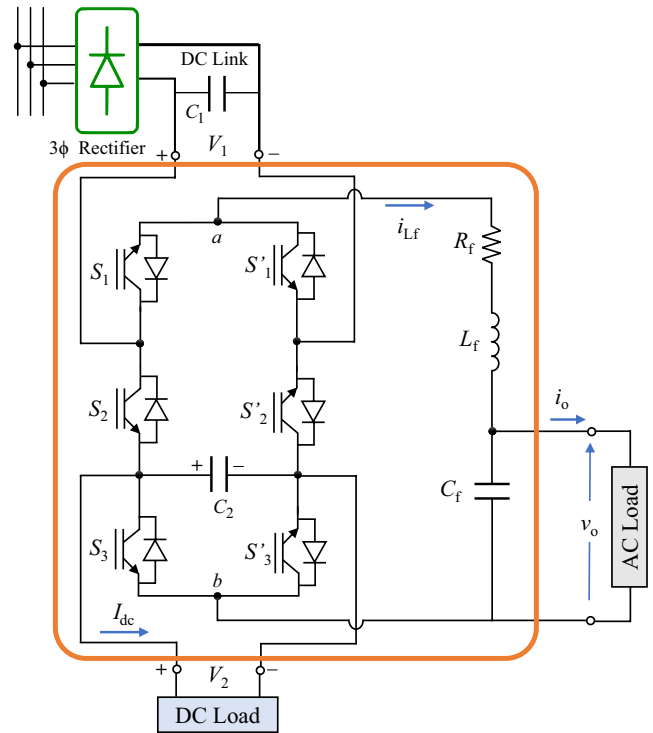

FIGURE 6 7L PUC inverter topology circuit

minimum number, which makes it a better choice for such an application.

For simplicity, a seven-level (7L) PUC inverter is considered for this application. The circuit of the 7L PUC single-phase inverter topology is shown in Figure 6. Each pair of switches (S_1, S_1'), (S_2, S_2') and (S_3, S_3') is complementary. The switching states are shown in Table 1, and the seven levels are depicted in Figure 7. To achieve the seven levels, the voltage across the capacitor V_2 should be kept at one third of the DC link voltage V_1. The switching control strategy is described

TABLE 1 Switching states for 7-level PUC inverter

State	S_1	S_2	S_3	V_i
1	0	0	0	0
2	0	0	1	$-V_2$
3	0	1	0	V_2-V_1
4	0	1	1	$-V_1$
5	1	0	0	V_1
6	1	0	1	V_1-V_2
7	1	1	0	V_2
8	1	1	1	0

hereafter. Let $S_i = \{0,1\}(i=1,2,3)$ be the switching function defined by

$$S_i = \begin{cases} 0, & \text{if } S_i \text{ is OFF} \\ 1, & \text{if } S_i \text{ is ON} \end{cases} \tag{1}$$

3.3 | Theory and model derivation

First, Let us define V_1: DC link voltage, V_2: capacitor voltage, v_i: inverter voltage across terminals a and b, v_o: output voltage, C_1: DC link capacitance, C_2: Capacitance in the inverter, L_f: filter inductance, R_f: filter resistance, C_f: filter capacitance, i_{L_f}: current through L_f, i_o: AC load current, and I_{dc}: DC load current.

Using Kirchhoff's voltage and current laws, the following differential equations can be extracted from the circuit in Figure 6.

$$\frac{dv_o}{dt} = \frac{i_{L_f} - i_o}{C_f} \tag{2}$$

$$\frac{dV_2}{dt} = \frac{(S_2 - S_3)i_{L_f} - I_{dc}}{C_2} \tag{3}$$

$$\frac{di_{L_f}}{dt} = \frac{v_i - v_o - i_{L_f}R_f}{L_f} \tag{4}$$

Given (1), v_i can be written in terms of the switching sequence S_i as follows

$$v_i = (S_1 - S_2)V_1 + (S_2 - S_3)V_2 \tag{5}$$

3.4 | Control strategy

The control objectives for the proposed inverter topology are as follows:

- Keep the output Voltage V_o follow a reference AC voltage of 240 V (V_{rms}).
- Maintain the capacitor voltage (V_2) constant at one third the DC link voltage (V_1).

To achieve these objectives, finite set model predictive control (FSMPC) is utilized. FSMPC provides several advantages including multivariable nonlinear control and excellent performance without the need for modulation.[23] Standard FSMPC incorporates three stages: (a) prediction model, (b) cost function, and (c) optimization algorithm. A normalization of the cost function has been found to yield better results[24]; therefore, a normalized cost function is used.

Prediction model: Let the output voltage v_o and the capacitor voltage V_2 be the control variables. The equations (2), (3), and (4) can be approximated with Euler method by

$$x^{k+1} = x^k + T_s x(t) \tag{6}$$

where T_s is the sampling period. Then, the prediction of the $(k + 1)$ sample of the control variables can be written as[25]

$$i_{L_f}^{k+1} = i_{L_f}^k + \frac{T_s}{L_f}(v_i^k - v_o^k - i_{L_f}^k R_f) \tag{7}$$

$$v_o^{k+1} = v_o^k + \frac{T_s}{C_f}(i_{L_f}^{k+1} - i_{dc}^k) \tag{8}$$

$$V_2^{k+1} = V_2^k + \frac{T_s}{C_2}((S_2 - S_3)i_{L_f}^k - I_{dc}^k) \tag{9}$$

Cost function: Using the equations above and considering the reference values for $v_o^* = 240\sqrt{2}sin(100\pi t)$ and $V_2^* = \frac{V_1}{3}$ (i_{L_f} is incorporated in the equation for v_o; therefore, it does not need to be controlled separately), the cost function could be written as

$$F = \lambda \left| \frac{V_2^* - V_2^{k+1}}{\Delta V_{2max}} \right| + \left| \frac{v_o^* - v_o^{k+1}}{\Delta v_{omax}} \right| \tag{10}$$

where λ is the weighting factor that will control the relative importance of the control variables and shall be determined experimentally, $\Delta V_{2max} = V_2^*$ and $\Delta v_{omax} = 2V_{omax}^*$

Prediction algorithm consists of measuring the variables for each sample k, iterating through all the 8 switching sequences, calculating the prediction and the cost function for each corresponding sequence and then selecting the sequence with the minimum cost function. Let j represent the switching sequence, where $j = [0,7]$. The flowchart of the prediction algorithm is given in Figure 8.

4 | SIMULATION

Computer simulation of the 7L PUC single-phase inverter has been carried out using MATLAB/Simulink. The simulation parameters are listed in Table 2.
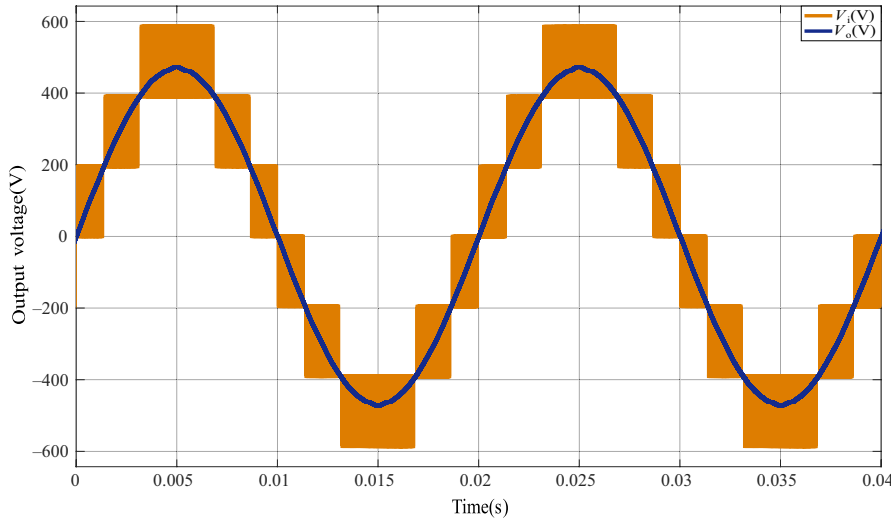
4.1 | Selection of the weighting factor λ

The weighting factor λ is selected experimentally based on the desired performance. The selection is a trade-off between the error in the capacitor voltage (ΔV_2) and output voltage THD. The average error in the capacitor voltage and the %THD were measured for different values of λ and plotted in Figure 9. Note that, taking both into account, the selected value is λ=0.55 since it will minimize the ripple voltage without severely increasing the THD. This will be the value used to carry out the rest of the simulation.

4.2 | Simulation results

The simulation has been carried out with a full load at steady state and with load steps with both AC and DC loads. Figure 11A shows the results for full load at steady state. It is clear that the capacitor voltage is well regulated and fluctuates around the reference value. The output voltage also closely matches the reference value with a small percentage of THD (around 0.65%). The input currents are inherently balanced as shown in Figure 10.

When the load changes from 10% to full load at 40 milliseconds as shown in Figure 11B, the output voltage is not affected and no voltage sag or swell appears in transient.

A DC load of 845W was applied to the capacitor terminals (applied on C_2), and the DC voltage shows some periodic 5% drops particularly near the zero crossings of the AC output voltage as illustrated in Figure 11C. This is because the DC current is considered a disturbance to the system, and it becomes significant when the AC current tends to zero (near the zero crossing). The controller is still able to maintain the DC voltage at an acceptable level, and no significant distortion appears on the AC voltage output.

The system was also simulated with a nonlinear load (through a rectifier circuit), and the results were also satisfactory as shown in Figure 11D. Therefore, we can conclude that
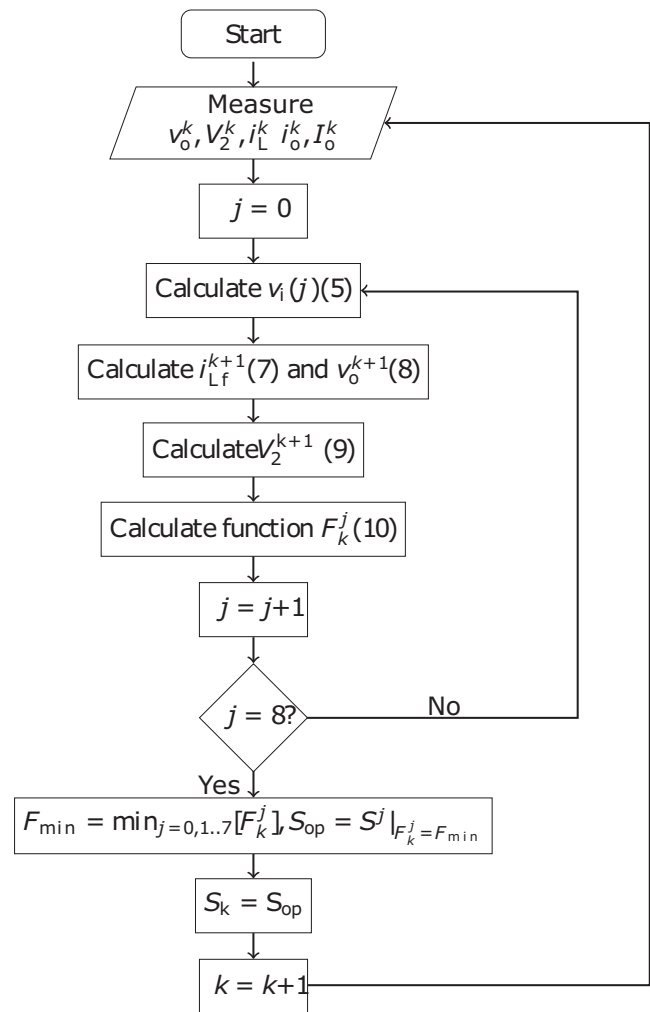

FIGURE 8 Flowchart of the prediction algorithm

the system is quite stable and delivers high-quality power to the load under different loading conditions. It is anticipated that the system performance will be improved when a PV system is connected at V_2 in parallel with the inverter capacitor C_2, because it will help stabilize the capacitor voltage.

TABLE 2 Simulation parameters

Parameters	Values
Output power P_{out}	3 kW
Load power factor PF	0.85
DC link voltage V_1	586 V
DC link capacitance C_1	10 mF
Filtering inductor L_f	600 μH
Inductor resistance R_f	30 mΩ
Filtering capacitor C_f	200 μF
Inverter capacitor C_2	330 μF
Fundamental frequency f	50 Hz
Sampling frequency f_s	24 kHz
Weighting factor λ	0.55

5 | HARDWARE-IN-THE-LOOP IMPLEMENTATION

Real-time simulation of the proposed converter has been carried out using Typhoon HIL system with DSpace DS1103 platform as a controller. The 24kHz switching frequency was selected based on the limitation of DSpace DS1103 to implement MPC in real-time above 25kHz. The LC filter was designed based on a resonance frequency that is 50 times smaller than f_s or about 480Hz. A deadtime of 250ns has been introduced between each complementary switches using Altera Cyclone V FPGA. The simulation parameters were the same as in Table 2, and the same cases of full load, step load, and nonlinear load were tested. A snapshot of the setup is shown in Figure 12

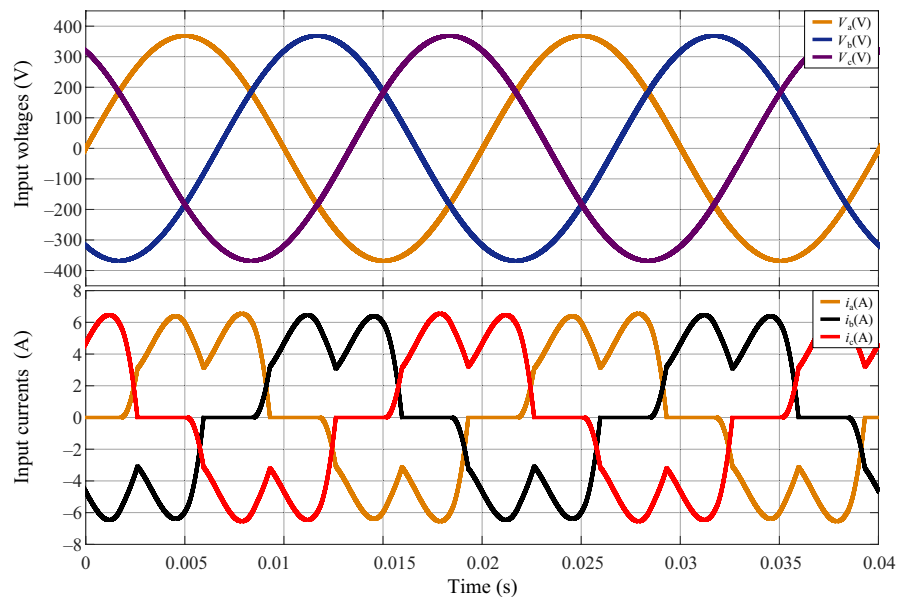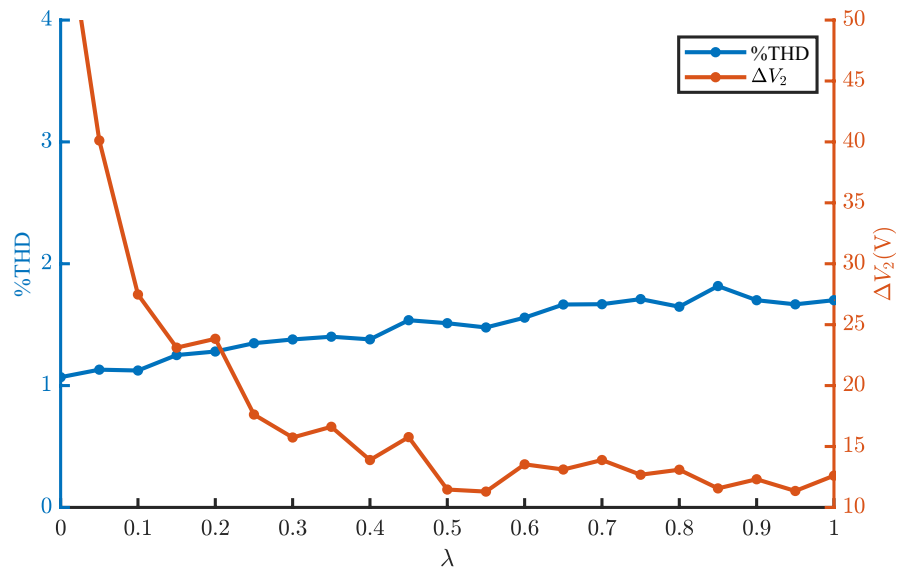**FIGURE 9** Effect of weighting factor λ on THD and ΔV_2

FIGURE 10 Input voltages and currents at full load

(A)

(B)
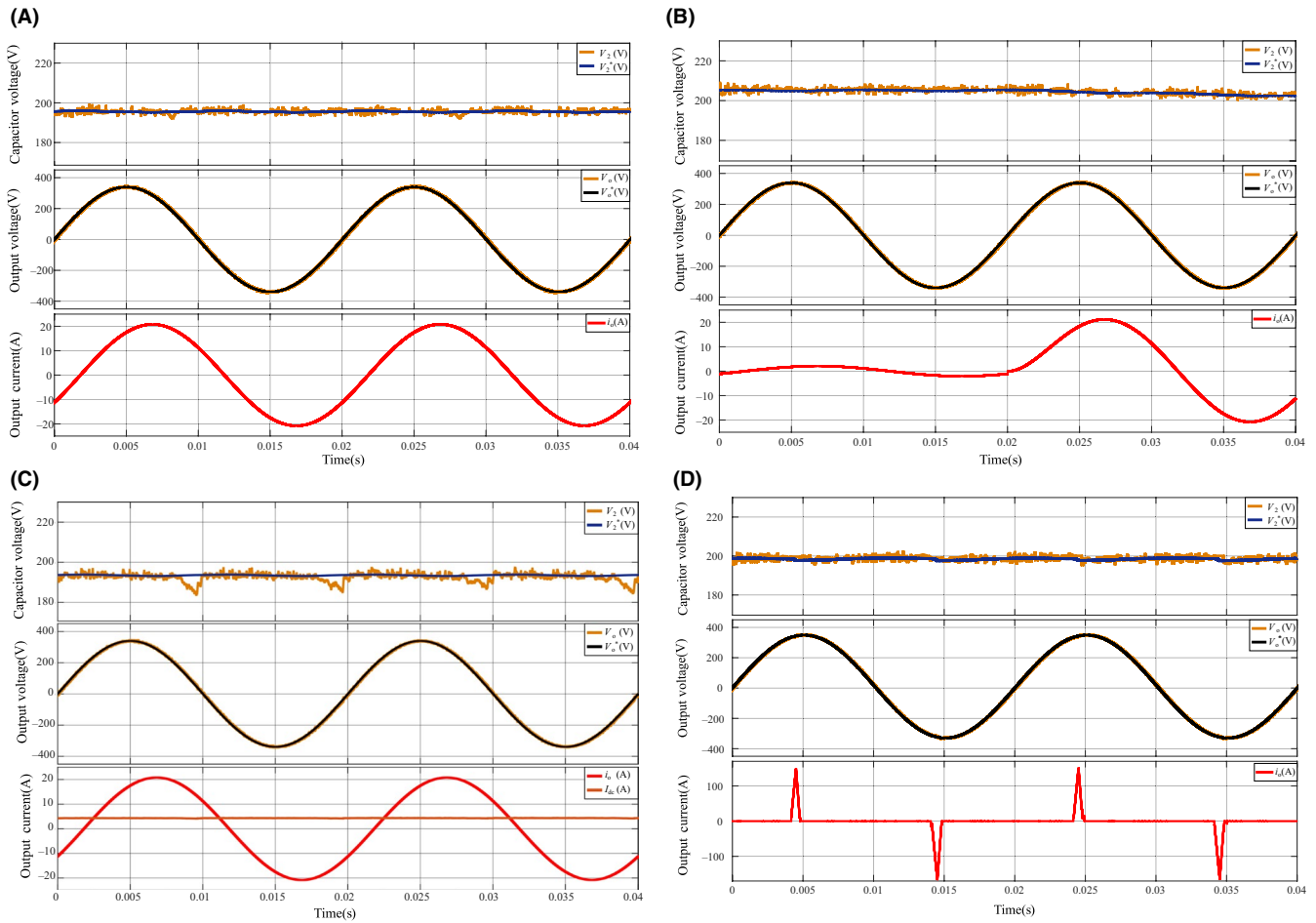

(C)

(D)

FIGURE 11 MATLAB/Simulink simulation results under different loads. A, Results at full load (THD = 0.65%). B, Results with a step from 10% to full load at 20ms (THD = 0.63%). C, Results with a DC load (THD = 0.74%). D, Results with a non-linear load (THD = 0.7%)
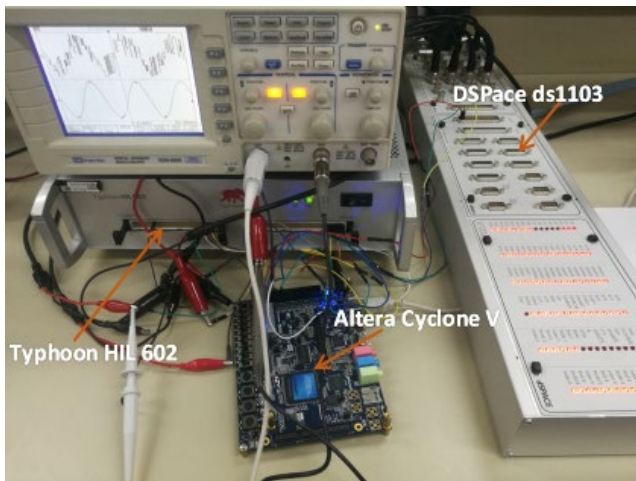

FIGURE 12 A snapshot of the hardware-in-the-loop setup

The behavior of the converter in a steady state using a 3kW load is shown in Figure 14A. The results show similar behavior to that of the MATLAB/Simulink simulation. There is a slight increase in THD percentage, which is thought to be due to the distortion caused by including

deadtime. The input currents also appear to be balanced as shown in Figure 13.

The behaviors during step load and nonlinear load are shown in Figure 14B and D, respectively. The controller is successfully able to regulate both the output and capacitor voltages, and no significant fluctuations appear during the load step or at the peaks of the current in the nonlinear load case. The DC load results shown in Figure 14C are similar to the simulation with periodic 5% drops near the zero crossing of the AC voltage. This is the same phenomenon that appeared in the simulation.

6 | CONCLUSION

The proposed three-phase to single-phase converter topology can completely mitigate the effect of voltage imbalance at the three-phase system because of its inherent 3 to 1 phase conversion. The proposed topology resembles the uninterruptible power supply (UPS) configuration and inherits all its features. It can be also used as a solid-state electronic transformer if an additional DC buck/boost converter is inserted

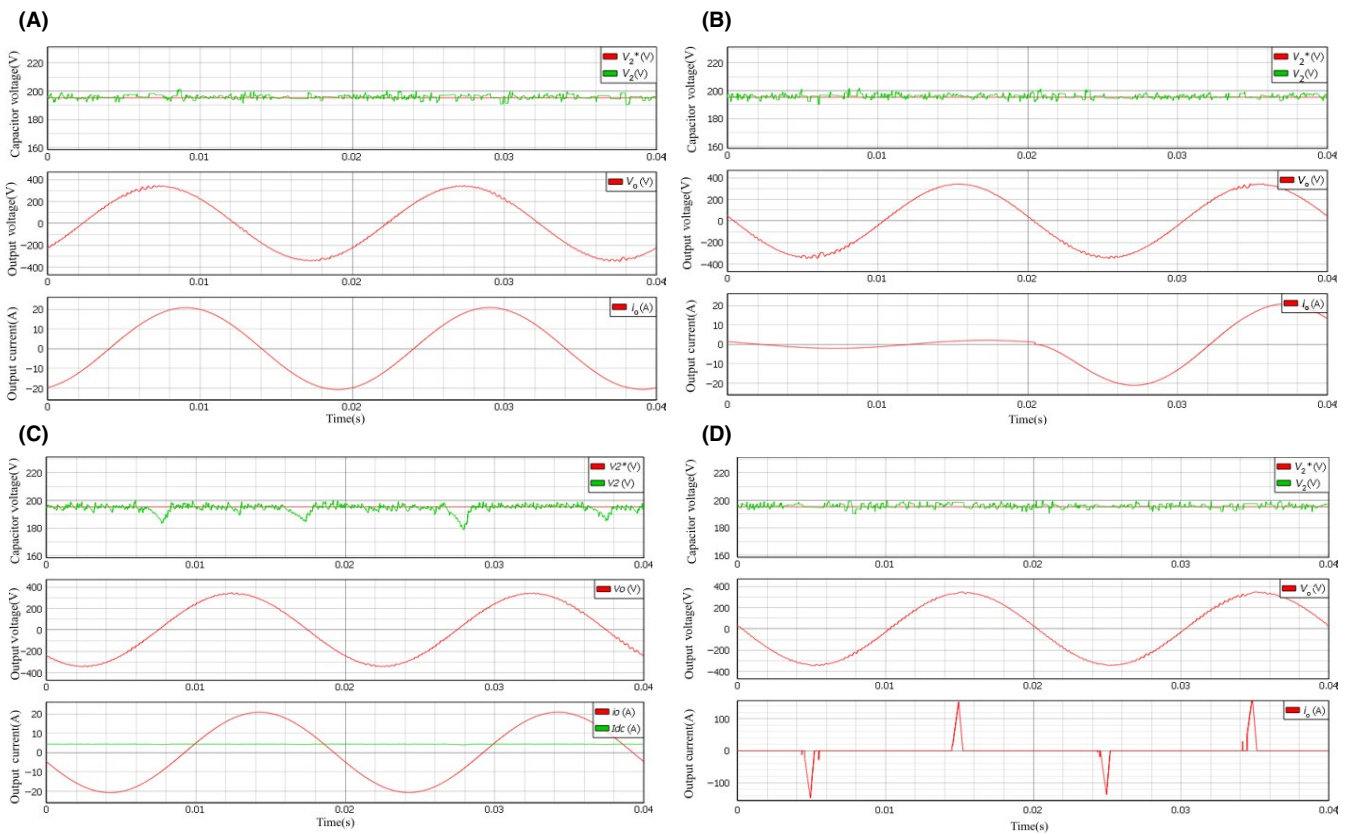**FIGURE 13** Real-time simulation input voltages and currents at full load
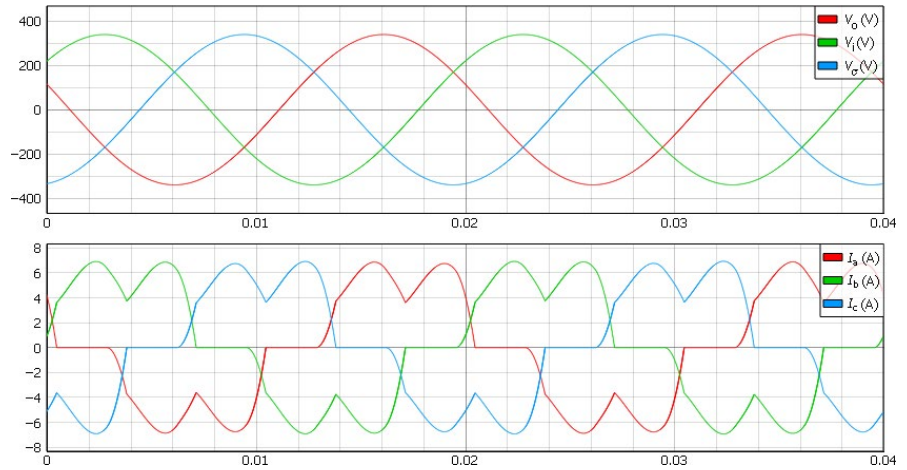

FIGURE 14 Hardware-in-the-loop results under different loads. A, Real-time simulation results at full load (THD = 1.58%). B, Real-time simulation results with a step from 10% to full load at 20 ms (THD = 1.29%). C, Real-time simulation results with a DC load (THD = 1.59%). D, Real-time simulation results with a nonlinear load (THD = 2.06%)

before the DC voltage V_1. A 7L PUC single-phase inverter topology was selected and used because of its multilevel output voltage, high performance, and cost-effectiveness. The proposed system was modeled and tested using simulations for a typical residential power distribution system integrating both DC and AC loads as well as DER. The results showed

high performance under different operating scenarios. Other smart grid features could easily be integrated into the proposed distribution approach such as voltage and current balancing, frequency regulation, power factor correction, phasor measurement unit (PMU) with real-time data communication, fault protection, and automatic or remote-controlled

feeder operation. In the grand scheme of power management, the proposed solution is a step forward to mitigate power quality complications for large-scale distribution networks.

ACKNOWLEDGMENTS

REFERENCES

1. Soltani S, Rashidinejad M, Abdollahi A. Dynamic phase balancing in the smart distribution networks. *Int J Electr Power Energy Syst*. 2017;93:374-383.
2. Shafiullah GM, Oo AMT, Ali ABMS, Wolfs P, Arif MT. Renewable energy integration: opportunities and challenges. In: Ali ABMS, ed. *Smart Grids: Opportunities, Developments, and Trends*. London: Springer, London; 2013:45-76.
3. Lopes JP, Hatziargyriou N, Mutale J, Djapic P, Jenkins N. Integrating distributed generation into electric power systems: a review of drivers, challenges and opportunities. *Electric Power Syst Res*. 2007;77(9):1189-1203.
4. Hanif A, Choudhry MA. Dynamic voltage regulation and power export in a distribution system using distributed generation. *J Zhejiang Univ-Science A*. 2009;10(10):1523-1531.
5. Buchholz BM, Styczynski Z. The three pillars of smart distribution. In: *Smart Grids – Fundamentals and Technologies in Electricity Networks*. Berlin, Heidelberg: Springer Berlin Heidelberg; 2014:225-275.
6. Haider R, Kim C-H. Chapter 7 - protection of DERs. In: Funabashi T, ed. *Integration of Distributed Energy Resources in Power Systems*, Academic Press; 2016:157-192.
7. Corsi S. Voltage control on distribution smart grids. In: *Voltage Control and Protection in Electrical Power Systems: From System Components to Wide-Area Control*. London: Springer London; 2015: 465-495.
8. Caldon R, Coppo M, Turri R. Distributed voltage control strategy for LV networks with inverterinterfaced generators. *Elect Power Syst Res*. 2014;107:85-92.
9. Madureira A, Peças Lopes J. Ancillary services market framework for voltage control in distribution networks with microgrids. *Elect Power Syst Res*. 2012;86:1-7.
10. Caldon R, Coppo M, Turri R. Coordinated voltage control in MV and LV distribution networks with inverter-interfaced users. *IEEE*. 2013;1-5.
11. Coppo M, Raciti A, Caldon R, Turri R. Exploiting inverter-interfaced DG for Voltage unbalance mitigation and ancillary services in distribution systems. *IEEE*. 2015; 371-376.
12. Ouyang S, Liu J, Wang X, Song S, Hou X. Comparison of four power electronic transformer topologies on unbalanced load correction capacity. In: *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015:3702-3709.
13. Bayliss C, Hardy B. Chapter 24 – power quality – harmonics in power systems. In: Bayliss C, Hardy B, eds. *Transmission and Distribution Electrical Engineering (Fourth Edition)*. Oxford: Newnes, 2012:987-1012[Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780080969121000241.
14. Jin N, Hu S, Gan C, Ling Z. Finite states model predictive control for fault-tolerant operation of a three-phase bidirectional AC/DC converter under unbalanced grid voltages. *IEEE Trans Industr Electron*. 2018; 65(1): 819-829.
15. Liu Y-C, Ge X, Tang Q, Deng Z, Gou B. Model predictive current control for four-switch three-phase rectifiers in balanced grids. *Electron Lett*. 2016;53(1):44-46.
16. Zhou D, Li X, Tang Y. Multiple-vector model predictive power control of three-phase four-switch rectifiers with capacitor voltage balancing. *IEEE Trans Power Elect*. 2017;33(7):5824-5835.
17. IEEE recommended practice and requirements for harmonic control in electric power systems. IEEE Std 519–2014 (Revision of IEEE Std 519–1992). 2014:1-29.
18. Moritz RMB, Batschauer AL. Capacitor voltage balancing in a 5-l full-bridge flying capacitor inverter. In: *2017 Brazilian Power Electronics Conference (COBEP)*; 2017; 1-6.
19. Kumar BJ, Chandramouli A. Modeling and simulation of nine-level cascaded H-bridge inverter based shunt active power filter for single-phase distribution system. In: International Conference on Inventive Computing and Informatics (ICICI); 2017: 675-680.
20. Wu X, Tan G, Ye Z, Yao G, Liu Z, Liu G. Virtual-space-vector PWM for a three-level neutral-point-clamped inverter with unbalanced DC-links. *IEEE Trans Power Elect*. 2018; 33(3): 2630-2642.
21. Vahedi H, Kanaan HY, Al-Haddad K. PUC converter review: topology, control and applications. In IECON 2015 – 41st Annual Conference of the IEEE Industrial Electronics Society, Nov. 2015:004 334-004 339.
22. Vijeh M, Samadaei E, Rezanejad A, Vahedi H, Al-Haddad K. New multilevel inverter with three extendable units. In: *Industrial Electronics Society, IECON 2017-43rd Annual Conference of the IEEE*, IEEE, 2017:6407-6412.
23. Bordons C, Montero C. Basic principles of MPC for power converters: Bridging the gap between theory and practice. *IEEE Ind Electron Mag*. 2015;9(3):31-43.
24. Trabelsi M, Bayhan S, Ghazi KA, Abu-Rub H, Ben-Brahim L. Finite-control-set model predictive control for grid-connected packed-U-cells multilevel inverter. *IEEE Trans Industr Elect*. 2016;63(11):7286-7295.
25. Ben-Brahim L, Gastli A, Trabelsi M, Ghazi KA, Houchati M, Abu-Rub H. Modular multilevel converter circulating current reduction using model predictive control. *IEEE Trans Industr Elect*. 2016;63(6):3857-3866.