QATAR UNIVERSITY

COLLEGE OF ENGINEERING

MODELING, DESIGN, AND IMPLEMENTATION OF HIGH GAIN POWER

ELECTRONIC DC-DC CONVERTERS FOR NANOGRID APPLICATIONS

BY

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# ABSTRACT

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Title: Modeling, Design, and Implementation of High Gain Power Electronic DC-DC Converters for Nanogrid Applications

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Nanogrids are nothing but power distribution systems that are based on renewable energy sources and are apt for low-power home applications. Nanogrids are considered to be the building cells of a Microgrid. Nanogrid is intended for feeding domestic loads (of the order of 100 W to 5 kW) from renewable energy sources such as wind farms, roof-top solar photovoltaic, biomass, and fuel cell, etc. Nonetheless, the voltages produced by these renewable energy sources are small and not sufficient enough to be utilized in all the applications. Hence, it is necessary to include high gain and high-efficiency DC-DC converters in the system. To interface the generators and the loads, power electronic converters are employed within a Nanogrid. The power system grid is also linked to the Nanogrid using these converters. The most fundamental characteristics of the high-gain DC-DC converters are high efficiency, high-voltage gain, and low voltage/current stress on switching components.

A comprehensive literature review of various boosting methods is disseminated in this research work. After a detailed investigation, five new DC-DC power converter topologies have been designed and developed to achieve high gain factors with reduced switch ratings and low cost for use in Nanogrids. The proposed converters cannot only reduce voltage/current stresses across the switching components significantly but also achieve a higher voltage gain at moderate duty cycles with a lesser number of

components. Moreover, the proposed converters are designed in such a way that they can maintain a continuous input current, and hence making them useful for power conversion in the battery, fuel cell, and solar PV applications. By using boosting technique five novel high voltage gain DC-DC converters are developed and presented in the dissertation, namely:

1. modified Switched Inductor Boost Converter (mSIBC) with reduced switch voltage stress,

2. Transformer-less Boost Converter (TBC) with reduced voltage stress,

3. Switched-Inductor based DC-DC Converter with reduced switch current stress,

4. Novel High Gain Active Switched Network-Based Converter, and

5. Double Stage Converter with low current stress for Nanogrid

The detailed theoretical analysis of the voltage conversion ratio, parameter design, continuous and discontinuous conduction mode, and advantages are presented. In addition, a detailed comparative study of each converter topology is also given.

The functionality of the proposed power converters is tested in real-time by developing Laboratory prototypes of the proposed converters and the theoretical analysis is validated by obtaining the experimental results. The proposed converter configurations are simulated in MATLAB as well, to verify the theoretical analysis. Simulation results of all the proposed converters are presented indicating clear evidence of the expected predictions in close proximity with experimental results.

# DEDICATION

*To my maternal grandfather (Late Dr. Syed Ainul Hoda) and my mother.*

# ACKNOWLEDGMENTS

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CHAPTER 1: INTRODUCTION

1.1 Overview and Motivation

In the past decade, the rapid development of industries, transport systems, domestic applications, etc. has been observed all over the world. Furthermore, a rapid increase in population during the past decade had led to an increase in the demand for energy and the power generated by the existing fossil fuels (i.e. overuse of coal, oil, gas, etc.). This growing energy demand has led to the exhaustion of fossil fuel energy resources, challenges of global warming associated with the increased emission of carbon dioxide ($CO_2$), and Green House Gases (GHG) [1]. Green House Gases cause a continuous increase in the average temperature of the earth. However, Renewable Energy Sources such as Solar Photo-Voltaic, wind energy, Fuel Cell, geothermal energy, hydropower, ocean energy, etc. are excellent alternatives and useful solutions to these growing challenges [2]-[5]. The Special Report prepared by International Energy Agency (IEA) in 2020 says that the contribution of renewable energy sources in electricity generation has increased from 20% to approximately 28% during the years 2010-2020 globally [6]. However, the contribution of petroleum, natural gas, coal, and nuclear energy is around 70% of the total energy generation and petroleum being the major contributor among all fossil fuels. Significant and unpredictable climate change due to global warming caused by the excessive use of fossil fuels has become the major challenge of the 21st century. Nevertheless, the severe effects of global warming and climate change may still be avoided by transforming the energy generation systems.

Nanogrids are nothing but power distribution systems that are based on renewable energy sources and are apt for low-power home applications. Nanogrid is intended for feeding domestic loads (of the order of 100 W to 5 kW) from renewable energy sources such as wind farms, roof-top solar photovoltaic, biomass, and fuel cell,

etc. Renewable energy resources have the significant capability to oust GHG emissions caused by the power generation from fossil fuels and thus abating climate change as it is naturally taken from the never-ending flow of energy around us. Despite the exceptional advantages of RES, some shortcomings are also associated with them such as lack of generation at night, low voltage generation, and climate dependency, etc. and hence it cannot be fed directly to the applications. The Power Electronics Converters (PEC) play the key role of being an intermediate stage in the power generation process to meet the required demand of end-user applications [7]-[13].

As PEC has been playing a key role in the energy conversion process, it should be capable to transfer energy efficiently to the grid or other auxiliary functions as shown in Fig. 1.1. Wide-Scale adoption of PEC makes these climate-based energy generation sources more controllable. Moreover, if they are strengthened by intelligent control strategies, the PECs can fulfill the requirements imposed by the distribution or transmission system and specific demands from the end-user as well [14]-[17]. Among the various RES, Solar PV-based Electricity Generation is the fastest-growing energy generation system due to its properties such as free availability in nature, pollution-free, virtually no maintenance, etc. The DC-DC converter is an essential component in the controllable energy conversion process starting from PV to the end-user such as DC home appliances, hybrid electric vehicles, in high voltage DC transmission line or AC grid/applications along with inverter [18]-[21].
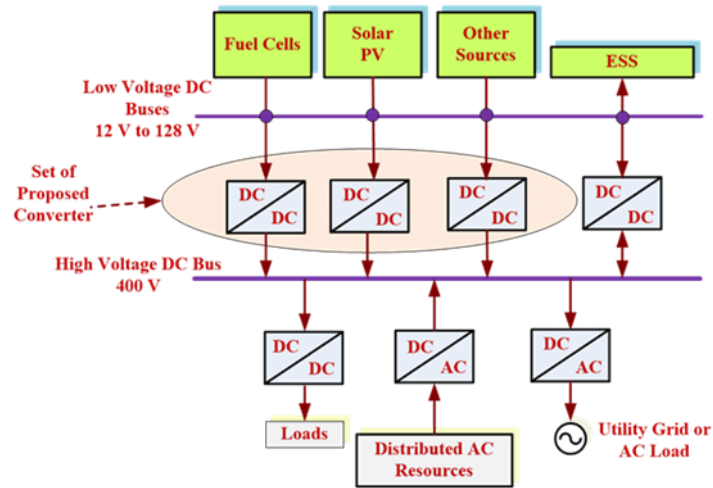
Figure 1.1. The general structure of RES with PECs.

Due to their significant contribution to the energy conversion process, numerous DC-DC converters have been proposed with various boosting techniques such as a switched circuit, cascading of two converters, voltage multipliers, and transformer or coupled inductor based DC-DC Converters in the last decade. The DC-DC converters should have low cost, compact size, high efficiency, high voltage conversion capability, low switch voltage/current stress, and simplified control.

## 1.2 Background

To accomplish the ever-increasing electricity demand and take care of environmental concerns, renewable energy resources are being utilized in the small-scale local power generation systems called Distributed Energy generation systems. Normally, renewable energy sources such as small hydro, solar power, wind power, biomass, biogas, and geothermal power are being used in Distributed Energy Systems. Solar PVs are one of the most commonly used distributed generation resources. The different renewable energy resources are integrated into the DC bus or to the load in DC Nanogrids by utilizing the DC-DC converters as depicted in Fig. 1.1. Most of the renewable energy resources such as Fuel Cells, Solar Photo Voltaic, etc. operate at low voltage (12 to 128V). Therefore, the conversion of low voltage received from these

renewable energy sources into high voltages ($\leq 400$ V) appropriate for the DC bus or load is necessary [22]-[23]. The main motives of DC-DC converters with high voltage gain are high efficiency, lesser component voltage/current stress, affordable overall cost, reduced circuit complexity, moderate power level and power density, and reliability[24]-[25].

## 1.3 Research Problem

Various topologies of DC/DC converters are incorporated to step up the low voltage range of 12-48V to a suitable voltage range of 200-400V [21], [25]. In practice, the voltage gain of a conventional boost converter is limited due to several reasons. The reasons mainly are capacitor and inductor series resistance effect, Electromagnetic Interference (EMI) effect, and the use of components and semiconductor devices with a high rating [26]. Furthermore, a high voltage gain is achieved by operating the converter at an extremely high duty ratio ($\simeq 0.9$), resulting in diode reverse recovery problems, high spikes in voltage, and high conduction losses [27]–[29]. To acquire a high voltage gain, many different topologies of isolated type DC/DC converters have been proposed so far in the literature such as flyback, half or full bridge, forward, and push-pull converters [30]-[34]. However, transformer core saturation is the major drawback of these converters, along with high power loss, and the occurrence of high spikes in the switch voltages caused by the leakage inductance of the transformer. Moreover, extra active clamping techniques and snubber circuits are required to overcome the above drawbacks in isolated DC/DC converters [35]-[36].

Hence, a high gain in voltage can be attained with the use of non-isolated DC-DC converter topologies leading to decreased cost and size, when galvanic isolation is not required. Cascade type boost, quadratic type boost, voltage lift type, capacitor/diode voltage multiplier type, and switched inductor/capacitor integrated conventional boost

converter, are a few high gain and non-isolated type converters [37]-[46]. However, these converters involve several converter stages leading to increased cost and complexity due to various converters connected in parallel. Furthermore, some other drawbacks associated with these converters are high energy dissipation and complex control [47]. Capacitor/diode voltage multiplier or interleaved configurations are some available options in the literature to achieve high voltage gain [48]-[50]. Nevertheless, the involvement of multiple converter stages in these configurations leads to high cost and complexity as several converters are connected all together in parallel. Moreover, high energy dissipation and complex control are the other disadvantages be involved with such converters [51].

## 1.4 Research Objective

To smoothen the fluctuations in power supply and increase the reliability of supply, storage and generation backup is also included within a Nanogrid along with the renewable sources and hence it provides a generation mix. A variable DC voltage or a variable frequency ac output is produced by utilizing all these sources present in the Nanogrid.

To provide power to the Nanogrid, various types of sources (such as Small Scale Wind turbines, solar PV array, and Battery Storage, etc.) can be connected simultaneously in a Nanogrid. Each one of the sources has its own individual working characteristics. Hence, a DC-DC Converter is required for each source to be assimilated into the Nanogrid. A DC-DC converter can convert the source output voltage up to 380 V (standard intermediate DC bus voltage level of Nanogrid for the industry applications) [52]-[55].

The objectives of the research are to design and develop a new class of two switches, non-isolated, non-coupled step-up, high voltage conversion ratio DC-DC

power converter configurations for Nanogrid Applications based on switched inductor circuitry to improve efficiency and reliability while maintaining the continuity of supply. At the same time significantly reducing the voltage/current stresses across the switching components, utilizing a lesser number of components, and reducing the size and cost of the circuit.

In this dissertation, five different DC-DC converter topologies are proposed. The main philosophy behind the design and development of the five DC-DC converter topologies is the choice of the Switched Inductor circuitry to achieve high voltage gain suitable for Nanogrid applications. The prime objective of the Proposed Converter 1 (named as modified Switched Inductor Boost Converter - mSIBC) and Proposed Converter 2 (named as Transformer-less Boost Converter - TBC) is to reduce the switches voltage stress. Whereas, the goal of Proposed Converter 3 (named as Switched-Inductor-based DC-DC converter with reduced switch current stress) and Proposed Converter 5 (named as Double Stage Converter with low current stress) is to reduce the switch current stress. On the other hand, the aim of the Proposed Converter 4 (named as Novel High Gain Active Switched Network-Based Converter) is to reduce the switch voltage stress and the switch current stress at the same time. Hence, all the five converters illustrated in the dissertation belong to the same family for achieving different set objectives. The functionality, feasibility, and operating principle of the converters are verified by simulation and hardware prototype implementation.

## 1.5 Contribution of Research Work

The contributions of the Research Work are as follows:

1) Development of a "modified Switched Inductor Boost Converter (mSIBC) with reduced switch voltage stress" to achieve a high voltage conversion ratio. Which

is much suitable for Nanogrid applications with a minimum number of reactive elements and semiconductor-controlled switches.

2) Design and development of a new type of DC-DC power converter named "Transformer-less Boost Converter (TBC) with reduced voltage stress", based on the voltage boosting techniques. To verify its functionality by MATLAB Simulation and Hardware Implementation.

3) Modelling, Analysis, and Implementation of a Switched-Inductor based DC-DC Converter with reduced switch current stress, based on the voltage boosting techniques. To verify its functionality by MATLAB Simulation and Hardware Implementation.

4) Design and development of a Novel High Gain Active Switched Network-Based Boost Converter, based on voltage lift techniques. To verify its functionality by MATLAB Simulation and Hardware Implementation.

5) Design and development of a Double Stage Converter with low current stress for Nanogrid, based on voltage lift techniques. To verify its functionality by MATLAB Simulation and Hardware Implementation.

## 1.6 Outline of Dissertation

The dissertation work is organized into the following major chapters and chapters 3 to 6 present the original contribution of the Research Work.

**Chapter-1:** "Introduction"

This chapter illustrates the overview and motivation of the research work, the background of the research, research problem, outlines the research objectives, and presents the contribution of the research work.

**Chapter-2:** "Literature Review"

This chapter presents a literature review of Nanogrids, including the importance of Nanogrids, the importance of DC-DC Converters within the Nanogrids, and the role of DC-DC Converters within the Nanogrids.

Furthermore, this chapter presents the literature review of High Gain DC-DC power electronics converters, including the general classification, uni-directional and bi-directional converters, and isolated and non-isolated converters with their applications. This chapter also provides a survey on boosting techniques such as cascading of converters, switched inductor, switched capacitor, voltage lift switched inductor, and voltage multiplier utilized to develop a new power converter for high voltage applications. A detailed study of their structure, advantages, and comparison between each boosting technique is presented. Finally, the conclusion for this chapter is provided.

**Chapter-3:** "Modified Switched Inductor Boost Converter (mSIBC) with Reduced Switch Voltage Stress"

The chapter deals with the detailed study of Modified Switched Inductor Boost Converter (mSIBC). In the beginning, the concept and structure of Modified Switched Inductor Boost Converter (mSIBC) and its derivation from classical Switched Inductor Boost Converter (SIBC) are discussed. The detail working and characteristics waveform in continuous and discontinuous conduction mode are presented with a detailed mathematical analysis of voltage conversion ratio with non-idealities characteristics of circuit elements and design of active and reactive components of mSIBC. The controller design has also been discussed and presented. The functionality of mSIBC configuration is validated by MATLAB simulation and hardware implementation in real-time. A comparative analysis of mSIBC configuration is provided with recently suggested converters for the performances based on components

count, load type, voltage gain, switch voltage, diode voltage, inductor current, switch current, diode current, and efficiency. Finally, the conclusion for this chapter is presented.

**Chapter-4:** "Transformer-less Boost Converter (TBC) with Reduced Voltage Stress"

This chapter deals with the working and characteristics waveform of TBC in continuous and discontinuous conduction mode. The voltage conversion ratio of TBC is derived in both modes. The TBC is analyzed by considering the non-idealities of semiconductor and active-passive devices. The design of the different circuit components and their selection criteria has been discussed. The MATLAB simulation and hardware implementation are carried out to validate the functionality of the converter in real-time. A comparison of the proposed TBC configuration with other related converters is presented in terms of components count, suitable load type, voltage gain, normalized switch/diode voltage stress, switch currents stress, and Efficiency (at rated power). Finally, the conclusion for this chapter is provided.

**Chapter-5:** "Modelling, Analysis, and Implementation of a Switched-Inductor based DC-DC Converter with Reduced Switch Current Stress"

In this chapter, the Modelling, Analysis, and Hardware Implementation of a Switched-Inductor based DC-DC Converter with Reduced Switch Current Stress is presented by utilizing the concept of voltage boosting techniques, and derived from switched inductor module. First of all, the power circuitry of the proposed converter is discussed in detail along with the principle of operation in both CCM and DCM and the Voltage Gain formula is derived. The effect of Non-idealities associated with the different circuit components on the voltage gain has been studied and presented in detail. The design and selection criteria of the different circuit components have been discussed. The functionality of the proposed converter configuration is verified through MATLAB

simulations and Hardware implementation. A detailed comparison of the proposed converter topology with other DC-DC Converters has been presented and finally, the conclusion is given.

**Chapter-6:** "A Novel High Gain Active Switched Network-Based Boost Converter"

In this chapter, a Novel High Gain Active Switched Network-Based Boost Converter is presented by utilizing the concept of voltage boosting techniques and derived with the combination of voltage multiplier and voltage lift switched inductor module. The power circuit of the proposed topology is discussed along with the working principle and a detailed mathematical analysis is presented by displaying the characteristic waveform and deriving the voltage gain formula in both CCM and DCM. The boundary conditions of the CCM and DCM for the proposed converter have also been studied. The effect of inductor mismatch on the converter operation has been analyzed and discussed in detail. The efficiency of the proposed converter is analyzed and the efficiency formula is obtained by studying the losses associated with the different circuit components. Design and selection criteria of the different circuit components have been discussed and presented in detail. The functionality of the proposed converter configuration is verified through MATLAB simulations and Hardware implementation and the results are discussed. A comparison of the proposed converter with other existing DC-DC converters is also presented. Finally, the conclusion of the chapter is given.

**Chapter-7:** "Double Stage Converter with Low Current Stress for Nanogrid"

This chapter deals with the working and characteristics waveform of a Double Stage Converter with Low Current Stress for Nanogrid in continuous and discontinuous conduction mode. The voltage conversion ratio of the proposed converter topology is derived in both modes. The proposed converter is analyzed by considering the non-

idealities of the different circuit components. The design and selection criteria of the different circuit components are discussed. The MATLAB simulation and hardware implementation are carried out to validate the functionality of the converter in real-time and the results have been discussed. A comparative study of the proposed converter configuration with other related converters in terms of components count, suitable load type, voltage gain, normalized switch voltage stress, normalized diode voltage stress, switch currents stress, and Efficiency (at rated power). Finally, the conclusion for this chapter is provided.

**Chapter-8:** "Conclusion and Future Direction"

This chapter deals with the conclusion of this dissertation based on the review, simulation, and experimental investigation of the proposed converter configurations. Finally, few suggestions are provided to extend the research work in the future.

**References**

The referred research papers and books are provided in this section.

**Appendix:** Research Contribution and Publication Details

In this section, the details of the student's research contribution and publication during the Ph.D. are provided.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

To accomplish the ever-increasing electricity demand and take care of environmental concerns, renewable energy resources are being utilized in the small-scale local power generation systems called Distributed Energy generation systems. Normally, renewable energy sources such as small hydro, solar power, wind power, biomass, biogas, and geothermal power are being used in Distributed Energy Systems. Solar PVs are one of the most commonly used distributed generation resources. The different renewable energy resources are integrated into the DC bus or to the load in DC Nanogrids by utilizing the DC-DC converters. The rapidly growing use of renewable energy sources all over the world leads to ever-increasing research in the field of DC-DC power electronic converter topologies to be utilized for application in DC Nanogrids [24]. To enhance the low voltage level of renewable energy sources such as fuel cells and solar photovoltaic (PV), a high-gain and high-efficiency DC-DC converter is an essential requirement of a DC Nanogrid. Most of the renewable energy resources such as Fuel Cells, Solar Photo Voltaic, etc. operate at low voltage (12 to 128V). Therefore, the conversion of low voltage received from these renewable energy sources to a high voltage (up to 400 V) suitable for the DC bus or load is necessary [22]-[23], [56]-[57]. Various DC-DC converter topologies are incorporated to step up the low voltage range of 12-48V to a suitable voltage range of 200-400V [29]. The main motives of DC-DC converters with high voltage gain are high efficiency, lesser component voltage/current stress, affordable overall cost, reduced circuit complexity, moderate power level and power density, and reliability [24]-[25]. Various topologies of DC/DC converters have been proposed in the literature so far to step up the low

voltage range (12-48V) to a suitable high voltage range (200-400V) at an appropriate duty cycle value, low component stress values, and to improve the efficiency [21], [25].

## 2.2 Nanogrids-An Overview

The concept of Nanogrid is comparatively new and pertains to a grid allocated to a distinct building or customer. Typically, there is a single generation unit within a Nanogrid, and it does not utilize either transmission or distribution lines and possibly will utilize a DC network. A Nanogrid is a small electrical system interfacing the grid of up to 100 kW capacity and confined to a solo building or major load or a system of loads up to 5 kW which are connected off-grid, both classifications representing devices (like Diesel Generator, smart loads, Electric Vehicles, and batteries) suitable for islanding and/or producing self-sufficient energy by incorporating an intelligent Distributed Energy Resources (DER) management/controls. Therefore, this combination of Renewable Energy Sources, Energy Storage Devices, and Intelligent control systems leads to improved home energy management, cost-effective solution, and income generation by providing grid support [23], [58].

### 2.2.1 Importance of Nanogrids

In recent past years, a significant amount of research has been carried out to highlight the benefits of distributed generation. In a distributed generation, both the supply and storage are typically DC, and hence the benefits of a DC grid are often discussed in the literature. The need for increased efficiency in the DC power distribution system has led to this extensive research in the field of Nanogrid [58].

### 2.2.2 Importance of DC-DC Converters within the Nanogrids

Several technologies are associated with Nanogrids, but the Nanogrid literature is dominated by the research on converter topologies. Within the Nanogrid, it is the responsibility of the DC-DC converters to manipulate the voltages to fulfill the

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requirements of a particular task. DC-DC converters usually (but not necessarily) connect the sources of Nanogrid to the systems bus/the national grid and connect the bus to loads of Nanogrid. The output voltage of the converter can be lesser or greater in amplitude than the input voltage. Reactive components such as capacitors and inductors, switching components such as diodes, MOSFETs, and IGBTs are utilized by the converters to achieve this variation in voltage amplitude [54], [59].

### *2.2.3 Role of DC-DC Converters within the Nanogrids*

The function of a DC-DC converter is basically to either step up or step down the input voltage subject to the output voltage requirements. The converter Topologies proposed here have to be used as the Source DC-DC Converter within a DC Nanogrid. It can be easily visualized that how a DC Nanogrid possibly will utilize the DC-DC converters. The DC voltage is supplied at the input of the DC to DC converters, and an improved DC voltage is obtained at the output. The variable/low DC input voltage is taken by the source converters and boosted to the required 400V at the output for the DC bus [22], [59]-[60]. Several functions can be performed by using the source DC-DC converter, such as:

- Interfacing of different sources: Different kinds of sources can be connected to a Nanogrid at a time, such as a Solar PV array, Small Scale Wind Turbine, and Battery Storage providing power to the Nanogrid. Each of these sources has its operating characteristics. Therefore, each source needs a DC-DC Converter to assimilate the different sources into the Nanogrid. The regulation of the supply is guaranteed by the converter along with providing protection.

- The voltage at Bus: The source voltage can be converted up to a DC bus voltage level of 380V using a DC-DC converter, which is nowadays the standard, intermediate dc voltage level for industry applications.

In general, the source voltage must be stepped up, so the boost or buck-boost type converters are typically used as the source DC-DC converter. These converters are required to have an efficiency greater than 85% and it is better to be more than 90% [54]. The prime focus of the research being carried out in the field of Nanogrid is to find out the techniques to increase the efficiency of the DC-DC converters used inside the Nanogrid [23], [54], [59]-[60].

## 2.3 High Gain Power Electronic DC-DC Converters

In the past decade, various DC-DC converters are developed to attain high-level voltage and small current applications involving renewable energy sources. The DC-DC converters can be categorized in different ways such as uni-directional/bi-directional converters based on the energy flow, isolated/non-isolated DC-DC converters based on the connection between input and output port, or depending on the output as step-up and step-down DC-DC converters. The same converter topologies are classified based on energy transfer stages such as single-stage converter e.g. Boost converter, two-stage converter e.g. SEPIC as boost stage followed by buck stage.

### *2.3.1 General Classification of DC-DC Converters*

In this section, firstly the classification of DC-DC converters is carried out based on energy flow direction, further, it is classified based on the connection between input/output port as isolated/non-isolated converters as presented in Fig. 2.1. The isolated/non-isolated DC-DC converters are further categorized as single stage, double stage, and multistage converters based on the number of intermediate stages required to transfer the energy from input to output port.
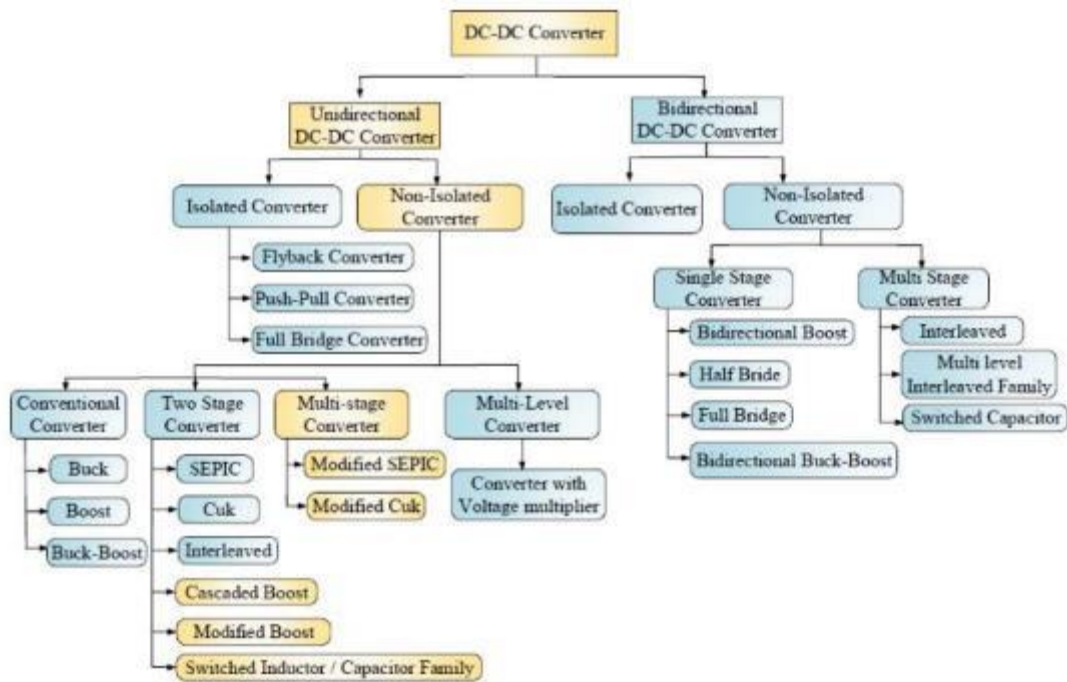
Figure 2.1. General classification of DC-DC Converters.

### *2.3.2 Uni-directional and Bi-directional DC-DC Converters*

The DC-DC converter is classified as uni-directional and bi-directional DC-DC converters based on the energy conversion direction or power flow as shown in Fig. 2.2. In unidirectional DC-DC converters, the energy is transferred from the input source to the load end in either step-up or step-down form. Generally, in uni-directional converters, diodes are incorporated in the power circuit to block the energy flow from load to source end. In solar and fuel cell applications, the generated energy is only transferred to load. In Nanogrid application, the energy flow from the sources to either the systems bus or to the national grid and from the bus to loads is carried out depending on the requirement as in step-up or step-down form [61]-[67].

With the advancement in the railway transport system, renewable energy system, grid application, electric vehicle [68]-[75], the researchers are getting more attracted towards the bi-directional converters. In the bi-directional converters, either energy can be transferred from source to load or load to source depending on the

requirement whether step-up or step-down form. The principle working of bi-directional topologies can be achieved by implementing two uni-directional converters for energy flow from source to load and load to source [12], [76]- [77].

The bi-directional converter topologies are derived from the conventional unidirectional converters (boost [78], buck-boost [79], SEPIC [80], ZETA [81] and CUK [82]) by replacing uncontrolled diode with the controlled switch. The bi-directional converters also have isolated and non-isolated configurations depending upon the transformer [83]-[84] and coupled inductor [85] position. The closed-loop system of the bi-directional converter is more complex as compared to uni-directional due to more number of controlled switches and application demand as energy flows from source to load or vice versa [86]. The objective of the dissertation is to develop a high voltage conversion ratio uni-directional converter. Hence, further discussion on the bi-directional converter has not been covered in this dissertation and it is focused mainly on uni-directional power converter with high gain output configuration.



(a)                                        (b)
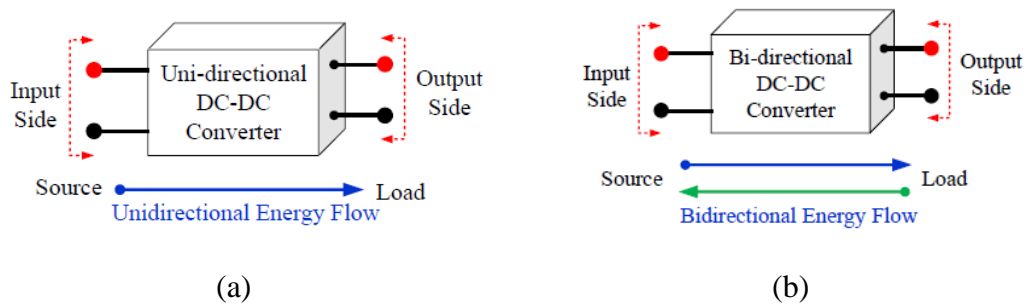
Figure 2.2. Classification of DC-DC converters based on the direction of energy flow (a) uni-directional and (b) bi-directional converter.

### 2.3.3 Isolated and Non-isolated DC-DC Converters

The uni-directional converters are further categorized into two main categories namely isolated and non-isolated converters as presented in Fig. 2.3. The uni-

directional non-isolated converters consist of only inductor/s, coupled inductor/s, capacitor/s, uncontrolled diode/s, and controlled switch/es.

According to the number of controlled switches, non-isolated converters are further classified into a single switch boost converter, double switch interleaved converter, and multiple switch converter. On the other hand, isolated converter topologies consist of transformers including basic elements for isolation and the extra boosting purpose. For the high voltage application, the isolated converters are being selected due to their high voltage conversion capability and electrical isolation for safety purposes [87]-[91].

(a)

(b)
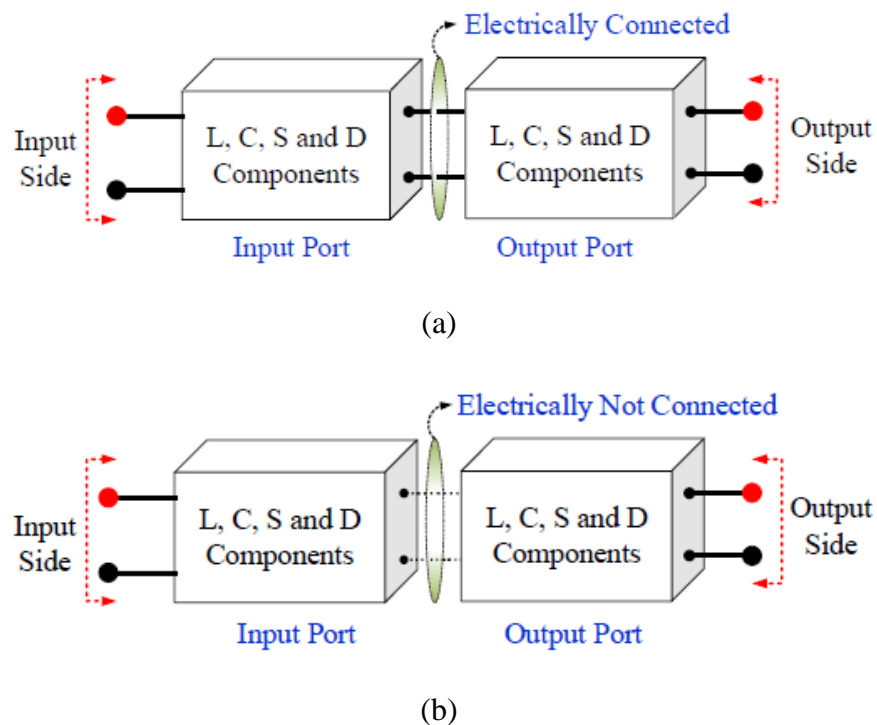
Figure 2.3. Classification of uni-directional DC/DC converters (a) non-isolated type and (b) isolated type converter.

The push-pull, flyback and half-bridge/full-bridge converters [10]-[11], [92] are examples of the transformer-based isolated converters. For electrical isolation between source and load, to reduce the EMI effect [93] and high-frequency noise, the transformer is incorporated in the isolated DC-DC converters as an intermediate stage.

However, the transformer increases the bulkiness of the circuit and decreases the efficiency of the converter [94]-[97]. In high-frequency transformer-based DC-DC converters, DC source voltage is converted into AC with the help of a controlled switch, which increases the number of conversion stages resulting in a decrease in efficiency of the converter. These drawbacks of isolated converter topologies divert the objective of this dissertation towards the non-isolated converter topologies.

In contrast to the isolated converters, the non-isolated converter structures are simple in design, compact in size, and don't need an intermediate stage for converting DC-AC-DC, and have a simple control strategy [98]-[99]. Hence, the researchers are attracted to the development of non-isolated converters for high voltage applications [100]-[102]. The non-isolated converters are further classified as the coupled inductor and non-coupled inductor-based isolated converters. The Coupled inductor is another viable solution to avoid transformer in DC-DC converter configurations for low cost, low weight, and reduced size. Leakage inductance is utilized to limit the diode current falling rate and to reduce the problem of reverse recovery. Moreover, untapped and tapped inductive coupling is also used in the DC/DC converters to attain high voltage gain [103]-[104]. Although, these converters provide a high voltage conversion ratio voltage stress across the switches is higher and efficiency is reduced due to leakage inductance. The voltage conversion ratio of these converter configurations depends upon the coupling ratio, coupling factor, and turn-on time of the switch [105]-[109]. For the reliability of electrical equipment, the input supply should have low ripple contents. To reduce the ripple contents of the system output, the possible way is adopting the high switching frequency which also makes the system compact in size [110]-[112]. The high switching frequency results in high dv/dt and di/dt during switch ON and OFF operations [113], which may result in high EMI and switching losses and

it is lesser in single switch topology while increases with an increase in the number of switches in the converter.

Based on the above discussion, the objective of the dissertation moves towards the development of two switch uni-directional, non-isolated high voltage conversion ratio topologies due to their compact structure, simple control strategy, and high efficiency.

*2.3.4 Voltage Boosting Techniques for DC-DC Converters*

A conventional boost converter is an impeccable solution for low and medium voltage applications due to its small number of active and passive components, simple design, and modeling. A single control switch implies a simple control strategy. Despite these key features, the conventional boost converter also has a few shortcomings. Theoretically, the conventional boost converter achieves high voltage gain at a duty ratio value near unity. Hence, it results in high conduction loss and reverse recovery loss in the output diode. Similar to the boost converter, buck-boost, SEPIC, ZETA, and CUK is derived to be used in high-voltage applications. To overcome the issues of low-voltage and power handling capability, various voltage boost methodologies have been proposed for the DC-DC converters.

*2.3.4.1 Cascading of Converters*

The cascading of converters is one of the possible solutions to increase the voltage conversion ratio of the DC-DC converters [108]. In these types of configurations, the cascaded connection of two or more step-up converters is carried out to boost the input voltage [114]. The cascaded connection is a multistage converter in which each converter is controlled by an individual or integrated single switch [115]. Cascaded converters are designed in such a way that a single switch is used to control the converter, which in turn reduces the complexity of the converter or control scheme.

The possible drawback of the integrated converter is that the duty ratio of two or more converters can no more be independently controlled [114]. The voltage gain of the cascaded converter is relatively high as compared to a single-stage or PWM DC-DC converter [106], [108], [115]-[119]. The cascaded converter operates with wider voltage gain and with narrower duty variation than those of PWM converters, which simplifies the design procedure and control scheme of the closed-loop system.

*2.3.4.2 Voltage Boosting Module*

The voltage gain of conventional converters is lifted/increased by adopting the boosting module at the proper position in the circuit. The broad categorization of voltage boosting techniques is shown in Fig. 2.4. The three major subsections include voltage multiplier, switched structure, and magnetic coupling. The working, advantages, and disadvantages of voltage multiplier and switched structure boosting techniques are discussed below.
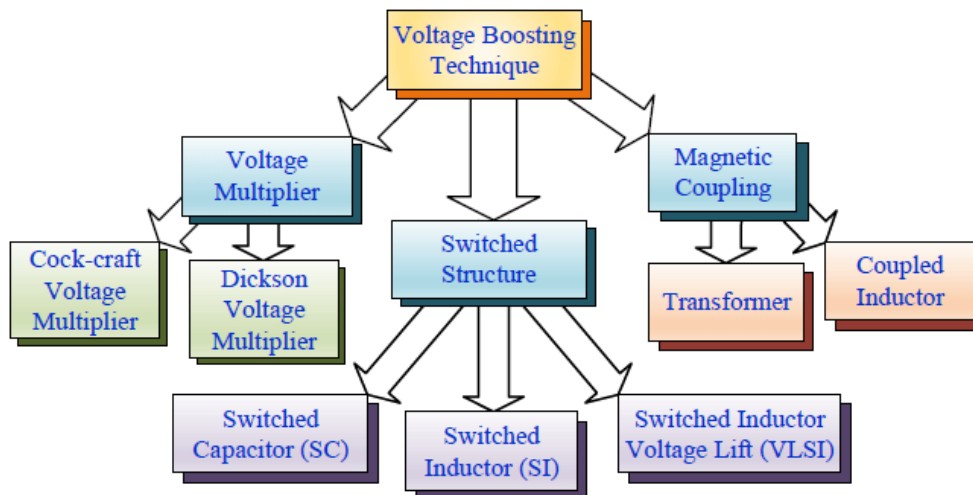


Figure 2.4. General classification of voltage boosting techniques.

*2.3.4.3 Voltage Multiplier (VM)*

The voltage multiplier has fewer components and a modular structure that makes it the simplest boosting technique to step up the input voltage [120]. The VM

placed in the middle of the circuit to reduce the voltage stress across the switch is called Intermediate Stage Voltage Multiplier (IS-VM) and placed at the end of the converter after transformer/coupled inductor to rectify AC or pulsating DC voltage is called Load End Voltage Multiplier (LE-VM).

A few IS-VM structures incorporated in the DC-DC converters are shown in Fig. 2.5. It is noted that some of them only consist of capacitors and diodes to boost the input. These structures utilize parallel charging and series discharging phenomenon of capacitors [121]-[122]. Moreover, IS-VM with capacitors and diodes is also known as switched capacitor voltage multiplier. Furthermore, the performance of these IS-VM structures is the same and increases the gain factor as tabulated in Table 2.1. The VM circuit is shown in Fig. 2.5 (d) which utilizes a switch to connect a capacitor in series to enhance the level of voltage at the output [123]. Fig. 2.5 (e) [124] uses a capacitor and inductor to boost the output voltage and can be implemented in any converter horizontally in place of the inductor. Typically, the voltage multiplier module shown in Fig. 2.5 (f) is implemented in the circuit before the controlled switch [125]. This voltage multiplier module is used in ultra-high gain converters to meet the high voltage demand. Moreover, the series implementation of this module enhances the level of voltage at the output [126].

The LE-VM can be further classified into Cockcroft-Watson Voltage Multiplier (CW-VM) [127]-[133] and Dickson [134]-[136] Voltage Multiplier (D-VM). In D-VM, diodes are used instead of the control switch. The general structure of these Voltage Multipliers (VM) is shown in Fig. 2.6 up to n level, which is responsible to increase the voltage conversion ratio by n times of input voltage between terminal A and B. The key advantage of LE-VM is its modular structure, and hence voltage conversion ratio of the converter can be boosted without disturbing the main circuit.

However, due to the use of diodes and capacitors, the converter has the issue of voltage balancing. The voltage stress across the switch and diode is equal to the output voltage [126].

*2.3.4.4 Switched Structure*

Another way to increase the overall voltage in a DC-DC Converter is the switched structure of capacitors and inductors. It is observed from the literature review that the switched capacitor technique is also known as charge pump (CP) circuits. In the Switched Capacitor (SC) techniques, only the capacitors are responsible to enhance the level of voltage at the output without utilizing the magnetic components. Some charge pump techniques discussed in this section are shown in Fig. 2.7 [137]-[139]. Fig. 2.7 (a) shows the CP circuits with two controlled switches, where the first capacitor is charged from the input when the first switch is turned ON [137]. The stored energy in the first capacitor is now transferred to the second capacitor and so on so forth up to N level. Fig. 2.7 (b) shows another structure of the CP circuit, where the first capacitor is charged from the input when the first switch is turned ON [140]. Now the second switch is turned ON to connect the first capacitor in series with the input supply to charge the second capacitor to double the output voltage. For high voltage applications, the CP connected in series/parallel is shown in Figs. 2.7 (c) and (d) [134]. In Figs. 2.7 (c) and (d), the pair of switches in the basic unit operate complementary to each other to incorporate the series connection of input voltage and capacitor to double the voltage at the output in each level.

(a)



(b)                          (c)                          (d)



(e)                                      (f)
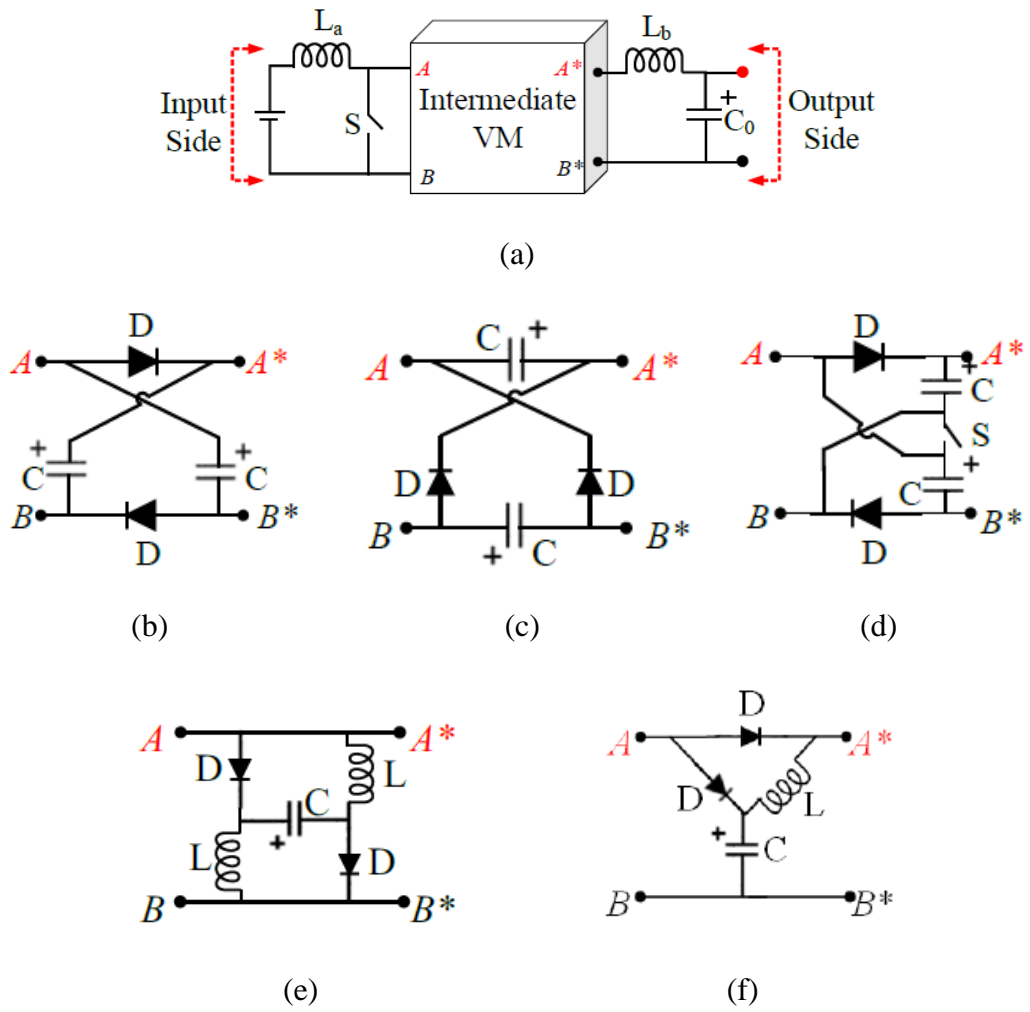
Figure 2.5. (a)-(f) Recently addressed voltage multiplier modules.



(a)                                              (b)
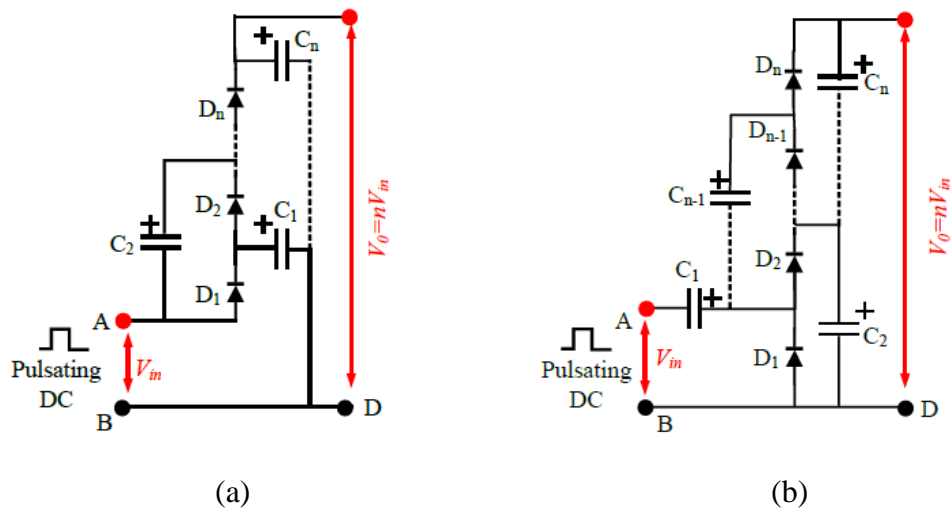
Figure 2.6. (a) Dickson and (b) Cockcroft-Walton voltage multiplier module.

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Table 2.1. Components count and the voltage gain of VM

| Boosting Module | | Number of Components | | | | Voltage Gain |
|---|---|---|---|---|---|---|
| | | L | C | D | S | |
| VM | Fig. 2.5 (b) | - | 2 | 2 | - | (1+D)/(1-D) |
| | Fig. 2.5 (c) | - | 2 | 2 | - | (1+D)/(1-D) |
| | Fig. 2.5 (d) | - | 2 | 2 | 1 | (1+D)/(1-D) |
| | Fig. 2.5 (e) | 2 | 1 | 2 | - | (2+D)/(1-D) |
| | Fig. 2.5 (f) | 1 | 1 | 2 | - | 1/(1-D) |
| | Fig. 2.6 (a), for n level | - | N | n | - | $nV_{in}$ |
| | Fig. 2.6 (b), for n level | - | N | n | - | $nV_{in}$ |

Fig. 2.7 (e) shows the ladder-type SC circuits in which two sets of capacitors are utilized to enhance the voltage at the output [134]. By changing the input port at the respective capacitors, different voltages are obtained. Fig. 2.7 (f) shows the Fibonacci SC circuit, which provides high boosting with lesser components [141]. As compared to the Dickson VM, here the output voltage is increased according to the Fibonacci number sequence (1, 2, 3, 5, 8, 13 …) i.e. the voltage gain increases exponentially with the number of switching devices.

The most critical issue related to the SC circuits is the high current spike, which degrades the power density and efficiency of the converter [142]. However, Fibonacci SC circuits need different rating switches and capacitors at different levels. Most of the

switches are not grounded in Fibonacci SC circuits, which makes the control and driver circuit complex. With the help of an external inductor, the current spike can be eliminated and the efficiency can be improved [138], [141]-[143].



(a)                              (b)                              (c)

(d)                              (e)                              (f)
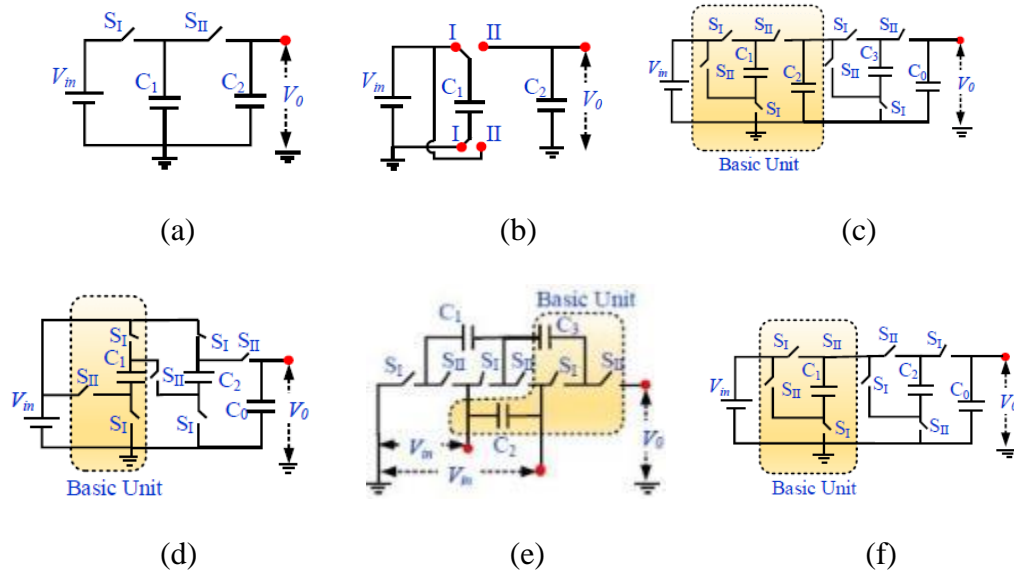
Figure 2.7. (a), (b) basic SC, (c) SC doubler circuit, (d) SC parallel-series circuit, (e) SC ladder circuit and (f) Fibonacci SC circuit.

Switched inductor (SI) technique is another useful method to be used in DC-DC converters to enhance the output voltage. Some of the SI circuits shown in Fig. 2.8 can be adopted in place of the inductor to enhance the level of voltage at the output. These SI structures are incorporated in various converters [144]-[151]. In the SI technique, both inductors are magnetized and demagnetized by the input supply in parallel and series, respectively. The advantageous feature of SI is that both the inductors are identical and integrated into a single core to reduce the size and weight of the circuit [145]-[147]. In Fig. 2.8 (b), a capacitor is placed in the SI circuit such that the capacitor is also charged and discharged with the inductors in parallel and series, respectively to enhance the level of voltage at the output [144]-[145]. Fig. 2.8 (c) shows the SI circuit which is also known as Voltage-Lift-Switched-Inductor (VLSI), and it gives the same voltage gain as the circuit shown in Fig. 2.8 (b) by eliminating both the intermediate

diodes. For high voltage applications, Luo and Ye introduced a double self-lift SI cell with the addition of a few components as shown in Fig. 2.8 (d).
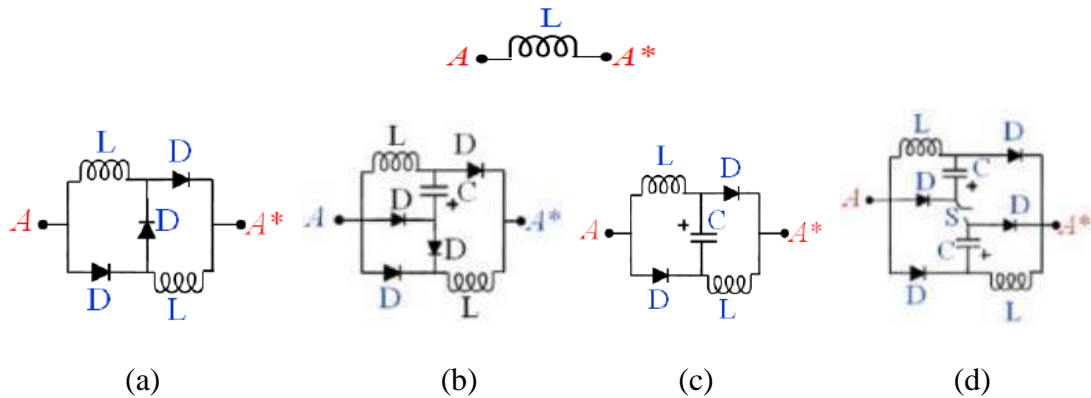


Figure 2.8. Switched inductor structure (a) basic SI, (b) self lift SI, (c) VLSI, and (d) double-lift SI.

In Fig. 2.8 (d), both inductors and capacitors are charged in parallel from the input source with the help of uncontrolled diodes and discharge/demagnetized in series with input supply to enhance the level of voltage at the output by four times. The key features of both SC and SI structures are their modularity, small size, and low weight. Also, the high current transient in SC is overcome by the SI module. Fig. 2.9 shows the SI and VLSI structure for n level. The comparison of SC in terms of the number of inductors, capacitors, and diodes with voltage gain is tabulated in Table 2.2.
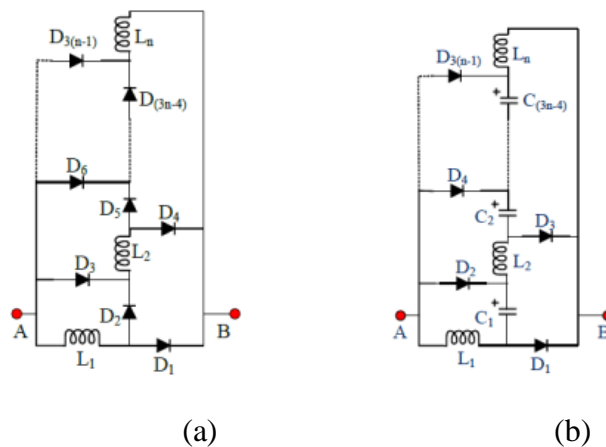


Figure 2.9. (a) SL and (b) VLSI for n level.

Table 2.2. Components count and Voltage Gain of SC circuits

| Boosting Module | | Number of Components | | | | Voltage Gain |
|---|---|---|---|---|---|---|
| | | L | C | D | S | |
| SC | Fig. 2.8 (a) | 2 | - | 3 | - | (1+D)/(1-D) |
| | Fig. 2.8 (b) | 2 | 1 | 4 | - | 2/(1-D) |
| | Fig. 2.8 (c) | 2 | 1 | 2 | - | 2/(1-D) |
| | Fig. 2.8 (d) | 2 | 2 | 4 | 1 | (3-D)/(1-D) |
| | Fig. 2.9 (a), for n level | N | - | 3n-1 | - | $(n-1)V_0$ |
| | Fig. 2.9 (b), for n level | N | n-1 | 3n | - | $nV_0$ |

### 2.3.5 Comparison of different DC/DC Converters

To choose a suitable voltage boosting technique from the above-discussed techniques, it is essential to compare them in terms of the inductor, capacitor, diode, and controlled switch count. The comparisons of discussed voltage boosting techniques in terms of components and voltage conversion ratio are tabulated in Table 2.3.

### 2.4 Summary

In this chapter, the literature review of Nanogrids, including the importance of Nanogrids, the importance of DC-DC Converters within the Nanogrids, and the role of DC-DC Converters within the Nanogrids is presented. Furthermore, the literature review of High-Gain DC/DC power electronics converters is also presented in detail. The DC-DC converters are broadly categorized in two parts as a uni-directional and bi-directional converter, which are further categorized into isolated and non-isolated converters. It mainly focuses on voltage boosting techniques such as cascading of

converters, voltage multiplier, switched capacitor, switched inductor, and voltage lift switched inductor. A brief discussion on the advantage, disadvantages, and key features of each boosting module is presented. In the last, these boosting techniques are compared in terms of voltage conversion ratio and boosting circuit elements.

Table 2.3. Components count and voltage gain of boosting module

| Boosting Module | | Number of Components | | | | Voltage Gain |
|---|---|---|---|---|---|---|
| | | L | C | D | S | |
| VM | Fig. 2.5 (b) | - | 2 | 2 | - | $(1+D)/(1-D)$ |
| | Fig. 2.5 (c) | - | 2 | 2 | - | $(1+D)/(1-D)$ |
| | Fig. 2.5 (d) | - | 2 | 2 | 1 | $(1+D)/(1-D)$ |
| | Fig. 2.5 (e) | 2 | 1 | 2 | - | $(2+D)/(1-D)$ |
| | Fig. 2.5 (f) | 1 | 1 | 2 | - | $1/(1-D)$ |
| | Fig. 2.6 (a) | - | 2 | 2 | - | $2V_0$ |
| | Fig. 2.6 (b) | - | 2 | 2 | - | $2V_0$ |
| SC | Fig. 2.7 (a) | - | 1 | 1 | 1 | $V_{in}$ |
| | Fig. 2.7 (b) | - | 2 | - | 2 | $2V_{in}$ |
| | Fig. 2.7 (c) | - | 2 | - | 4 | $2V_{in}$ |
| | Fig. 2.7 (d) | - | 1 | - | 3 | $2V_{in}$ |
| | Fig. 2.8 (a) | 2 | - | 3 | - | $(1+D)/(1-D)$ |
| | Fig. 2.8 (b) | 2 | 1 | 4 | - | $2/(1-D)$ |
| | Fig. 2.8 (c) | 2 | 1 | 2 | - | $2/(1-D)$ |
| | Fig. 2.8 (d) | 2 | 2 | 4 | 1 | $(3-D)/(1-D)$ |

CHAPTER 3: MODIFIED SWITCHED INDUCTOR BOOST CONVERTER

(MSIBC) WITH REDUCED SWITCH VOLTAGE STRESS

## 3.1 Introduction

Recently, switched inductor (SI) and switched capacitor techniques in dc–dc converters are recommended to achieve high voltage by using the principle of parallel charging and series discharging of reactive elements. It is noteworthy that four diodes, one high-voltage rating switch, and two inductors are required to design classical SI boost converter (SIBC). Moreover, in classical SIBC, the switch voltage stress is equal to the output voltage.

In this chapter, modified SIBC (mSIBC) with reduced voltage stress across active switches is presented. The mSIBC configuration is transformer-less and simply derived by replacing one diode of the classical SI structure with an active switch. As a result, mSIBC requires low-voltage rating active switches, since the total output voltage is shared into two active switches. Moreover, the mSIBC is low in cost, provides higher efficiency, and requires the same number of components compared with the classical SIBC. The continuous conduction mode and discontinuous conduction mode analysis, the effect of non-idealities on voltage gain, design methodology, and comparison are presented in detail. The operation and performance of the designed 500-W mSIBC are experimentally validated under different perturbations.

Fig. 3.1(a) shows the existing configuration of transformer-less high step-up dc–dc converter or classical SIBC [122], [148]. In SIBC, SI circuitry is employed to achieve higher voltage gain compared with the classical boost converter. However, it is noteworthy that the voltage stress across switches increases with voltage gain and total output appears across the switch. Therefore, slight modification without increasing the number of components has been done in the power circuit of classical SIBC to reduce

the voltage stress of switch and achieve the same voltage gain. The proposed dc–dc converter utilizes the inherent switched-inductor technique (parallel charging and series discharging of inductors) to achieve high step-up voltage gain.

## 3.2 Power Circuit Topology

Fig. 3.1(b) shows the power circuit of the proposed mSIBC, which consists of two active switches $S_1$ and $S_2$, three diodes $D_1$, $D_2$, and $D_o$, two inductors $L_1$ and $L_2$, capacitor $C_o$, and load $R_o$. The proposed mSIBC configuration is transformer-less and simply derived by replacing one diode of the SI network of classical SIBC with an active switch. It is noteworthy that the total number of components in the proposed mSIBC and classical SIBC is the same and provides the same voltage gain. However, in the proposed mSIBC, the total output voltage is distributed among the two active switches. Therefore, low-voltage rating switches can be employed to design the power circuit of the proposed mSIBC configuration. Initially, to analyze the steady-state characteristics of the proposed mSIBC configuration in CCM, all components are considered ideal and the voltage drop across semiconductor devices due to ON-state resistance is neglected, and the capacitor is large enough to provide ripple-free voltage. In this section, it is considered that the inductors $L_1$ and $L_2$ are equal in inductance that means $L_1 = L_2 = L$ (ideal case).



(a)                                           (b)
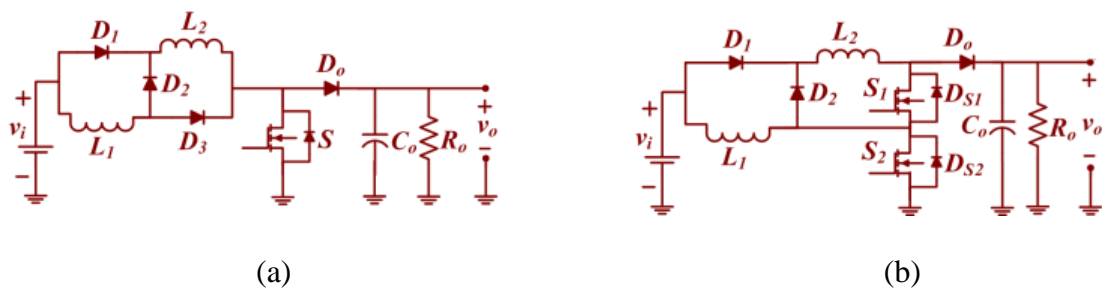
Figure 3.1. Power circuitry (a) existing configuration of transformer-less high step-up DC-DC converter or classical SIBC [122], [148], (b) Proposed converter.

Based on the circuitry, the currents through inductor $L_1$ and $L_2$ are equal and written as

$$i_L = i_{L1} = i_{L2} \qquad (3.1)$$

The typical waveforms of mSIBC for CCM and DCM are shown in Fig. 3.2(a) and (b), respectively; where $T_{ON}$ is the time period for mode I (i.e., time $t_0$–$t_1$), and $T_S$ is the total time period. Table 3.1 briefly summarizes the Operating Principle in both CCM and DCM (*Ch.: Chraged, D/Ch.: Discharged, ZC: Zero current, FB: Forward Biased, RB: Reversed Biased).

Table 3.1. Operating Principle in CCM and DCM

| Operating Modes | | Time | Switches | | Inductors | | Diodes | | | Cap. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $S_1$ | $S_2$ | $L_1$ | $L_2$ | $D_O$ | $D_1$ | $D_2$ | $C_O$ |
| CCM | Mode I | $T_{ON}$ ($t_0$–$t_1$) | ON | ON | Ch. in parallel | Ch. in parallel | RB | FB | RB | D/Ch. |
| | Mode II | $T_{OFF}$ ($t_1$–$t_2$) | OFF | OFF | D/Ch. in series | D/Ch. in series | FB | RB | FB | Ch. |
| DCM | Mode I | $K_1T_S$ or $T_{ON}$ ($t_0$–$t_1$) | ON | ON | Ch. in parallel | Ch. in parallel | RB | FB | RB | D/Ch. |
| | Mode II | $K_2T_S$ or $T_{OFF,1}$ ($t_1$–$t_2$) | OFF | OFF | D/Ch. in series | D/Ch. in series | FB | RB | FB | Ch. |
| | Mode III | $K_3T_S$ or $T_{OFF,2}$ ($t_2$–$t_3$) | OFF | OFF | ZC | ZC | RB | RB | RB | D/Ch. |

3.3 Operating Principle and Small-Signal Modeling in CCM

The working of the proposed mSIBC for CCM is divided into two modes; mode I when both switches $S_1$ and $S_2$ are turned ON (time $t_0$–$t_1$), and mode II when both switches $S_1$ and $S_2$ are turned OFF (time $t_1$–$t_2$).

*1) Mode I (Time $t_0$–$t_1$):* In this mode, inductor $L_1$ is magnetized by input supply ($v_i$) through switch $S_2$, and inductor $L_2$ is magnetized by input supply ($v_i$) through diode

$D_1$ and switches $S_1$ and $S_2$. The capacitor $C_o$ is discharged through the load $R_o$. During this mode, diodes $D_2$ and $D_o$ are reversed biased, and diode $D_1$ is forward biased. The equivalent circuitry of mSIBC for this mode is shown in Fig. 3.3 (a). It is noteworthy that both inductors are magnetized in parallel by input supply $v_i$ with the equal current.



(a)                                                    (b)
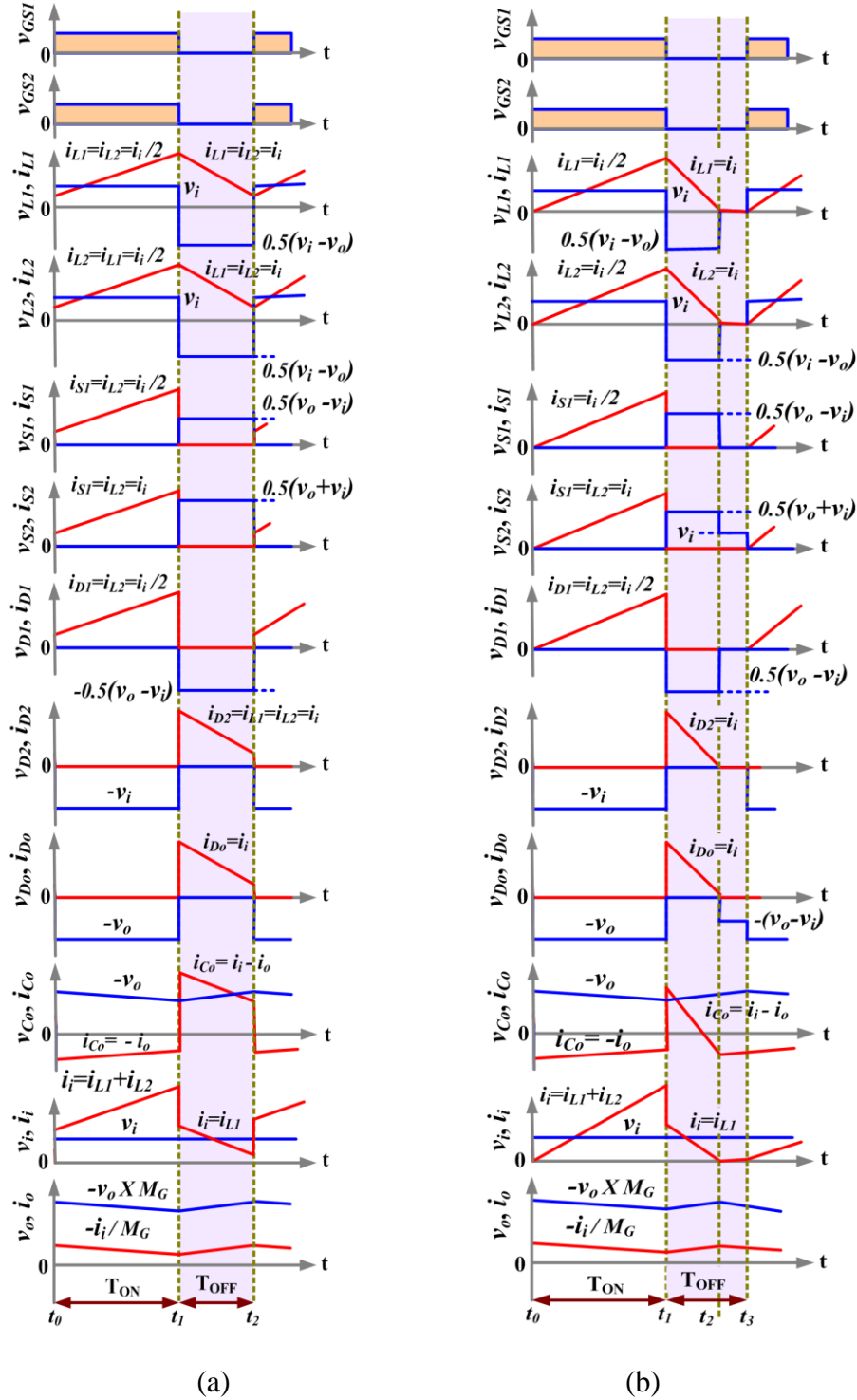
Figure 3.2. Typical waveforms of mSIBC for (a) CCM and (b) DCM.

The voltages across inductors $L_1$ and $L_2$ are obtained as

$$v_L = v_{L1} = v_{L2} = v_i \tag{3.2}$$

The input current $i_i$ is obtained as

$$i_i = 2i_L = 2i_{L1} = 2i_{L2} \tag{3.3}$$

The differential expression for the inductors $L_1$ and $L_2$ and capacitor $C_o$ can be obtained as follows:

$$\frac{d\ i_L}{dt} = \frac{d\ i_{L1}}{dt} = \frac{d\ i_{L2}}{dt} = \frac{v_i}{L}, \frac{d\ v_{Co}}{dt} = \frac{-v_o}{C_o R_o} \tag{3.4}$$

*2) Mode II (Time $t_1$–$t_2$):* In this mode, both the inductors $L_1$ and $L_2$ are demagnetized in series with the input voltage $v_i$ to provide energy to the load $R_o$ and charge the capacitor $C_o$ through diode $D_2$ and $D_o$. During this mode, diodes $D_2$ and $D_o$ are forward biased, and diode $D_1$ is reversed biased. The equivalent circuit of mSIBC for this mode is shown in Fig. 3.3(b).



(a)　　　　　　　　　　　　　(b)
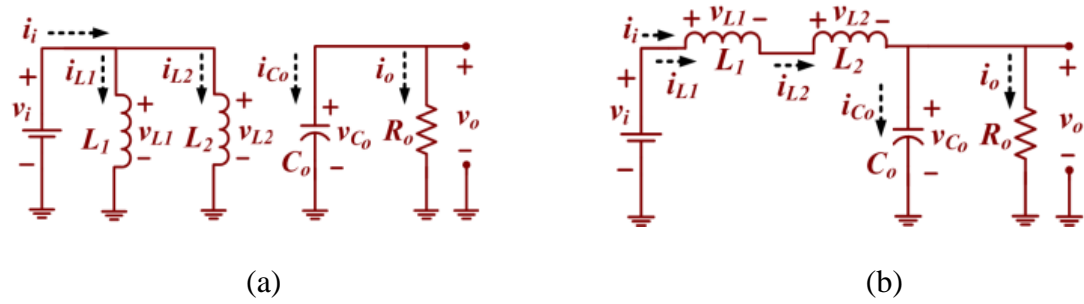
Figure 3.3. Equivalent circuit. (a) ON state. (b) OFF state.

The voltages across inductors $L_1$ and $L_2$ are obtained as

$$v_L = v_{L1} = v_{L2} = \left( v_i - v_o \right) / 2 \tag{3.5}$$

The input current $i_i$ is obtained as

$$i_i = i_L = i_{L1} = i_{L2} \tag{3.6}$$

The differential expression for the inductor $L_1$ and $L_2$ and capacitor $C_o$ can be

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obtained as follows:

$$\frac{d\ i_L}{dt} = \frac{d\ i_{L1}}{dt} = \frac{d\ i_{L2}}{dt} = \frac{v_i - v_o}{2L}, \frac{d\ v_{Co}}{dt} = \frac{1}{C_o}\left(i_L - \frac{v_o}{R_o}\right) \tag{3.7}$$

Assume, in general, $\langle x \rangle$ is the average value of variable $x$. Using (3.2)–(3.7), the average equations are obtained as follows:

$$\begin{cases} L\dfrac{d\langle i_L \rangle}{dt} = \dfrac{\langle v_i \rangle\ 1+d\ -\langle v_o \rangle\ 1-d}{2} \\[2em] C_o\dfrac{d\langle v_{Co} \rangle}{dt} = \langle i_L \rangle\ 1-d\ -\dfrac{\langle v_o \rangle}{R_o}, \langle i_i \rangle = \langle i_L \rangle\ 1+d \end{cases} \tag{3.8}$$

Where $d$ is a variable used for duty. In order to obtain the small signal model from (3.8), perturbation variables are necessary. Therefore, small ac variation with small magnitude is assumed in each variable of (3.8). Therefore,

$$\begin{cases} \langle v_i \rangle = V_i + \hat{v}_i, \langle v_{Co} \rangle = V_{Co} + \hat{v}_{Co}, \langle v_o \rangle = V_o + \hat{v}_o \\[1em] \langle i_L \rangle = I_L + \hat{i}_L, \langle i_i \rangle = I_i + \hat{i}_i, d = D + \hat{d} \end{cases} \tag{3.9}$$

Where

$$\left|\hat{v}_i\right| << V_i, \left|\hat{v}_{Co}\right| << V_{Co}, \left|\hat{v}_o\right| << V_o, \left|\hat{i}_L\right| << I_L, \left|\hat{i}_i\right| << I_i \tag{3.10}$$

Using (3.8)–(3.10)

$$\begin{cases} L\dfrac{d\ I_L + \hat{i}_L}{dt} = \dfrac{V_i + \hat{v}_i\ \ 1+D+\hat{d}\ -\ V_o + \hat{v}_o\ \ 1-D-\hat{d}}{2} \\[2em] C_o\dfrac{d\ V_{Co} + \hat{v}_{Co}}{dt} = I_L + \hat{i}_L\ \ 1-D-\hat{d}\ -\dfrac{V_o + \hat{v}_o}{R_o} \\[2em] I_i + \hat{i}_i = I_L + \hat{i}_L\ \ 1+D+\hat{d} \end{cases} \tag{3.11}$$

Using (3.11), the dc variable equation can be obtained as follows:

$$0 = \frac{V_i\ (1+D)\ -V_o\ (1-D)}{2}\ ,\ 0 = I_L\ (1-D)\ -\frac{V_o}{R_o}\ ,\ I_i = I_L\ (1+D) \qquad (3.12)$$

Using (3.12), the voltage gain of the mSIBC is obtained as follows:

$$M = V_o\ /\ V_i\ =\ (1+D)\ /\ (1-D) \qquad (3.13)$$

Where $M$ is the voltage gain, and $D$ is the duty cycle. It is observed that the voltage gain of mSIBC and classical SIBC is the same. By neglecting second-order term in (3.11), the small-signal ac equations are obtained as follows:

$$
\begin{cases}
L\dfrac{d\ \hat{i}_L}{dt} = \dfrac{(V_i+V_o)\ \hat{d}\ +\ (1+D)\ \hat{v}_i\ -\ (1-D)\ \hat{v}_o}{2} \\[2mm]
C_o\dfrac{d\ \hat{v}_{Co}}{dt} = -I_L\hat{d}\ +\ (1-D)\ \hat{i}_L\ -\ \hat{v}_o\ /\ R_o \\[2mm]
\hat{i}_i = I_L\hat{d}\ +\ (1+D)\ \hat{i}_L
\end{cases}
\qquad (3.14)
$$

Using (3.14), the small-signal model is obtained and shown in Fig. 3.4, in which $T_A$ and $T_B$ are ideal transformers with the turn ratio $1:(1 + D)$ and $(1 - D):1$, respectively.

Using the Laplace transform, the relation between $\hat{d}(S)$, $\hat{v}_i(S)$ and $\hat{v}_o(S)$ is obtained as follows:

$$\hat{v}_o(S) = M_i(S)\hat{v}_i(S) + M_d(S)\hat{d}(S) \qquad (3.15)$$
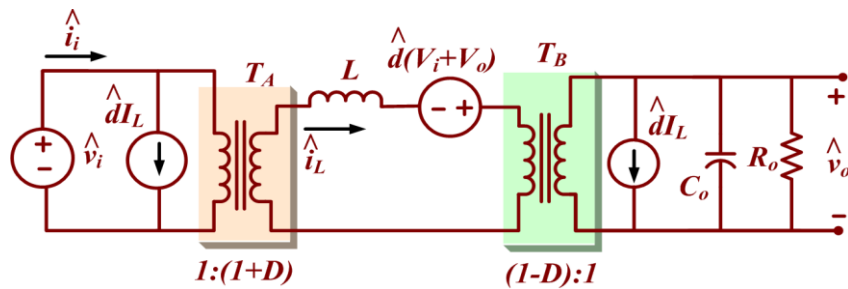


Figure 3.4. Small-signal model of the proposed mSIBC converter ($L_1 = L_2 = L$).

Where $M_i(S)$ and $M_d(S)$ are expressed as follows:

$$M_i(S) = \left.\frac{\hat{v}_o(S)}{\hat{v}_i(S)}\right|_{\hat{d}(S)=0} = \frac{(1+D)/(1-D)}{1+2LS/Ro(1-D)^2+2LC_oS^2/(1-D)^2} \quad (3.16)$$

$$M_d(S) = \left.\frac{\hat{v}_o(S)}{\hat{d}(S)}\right|_{\hat{v}_i(S)=0} = \frac{V_i+V_o /(1-D)-2I_LLS/(1-D)^2}{1+2LS/Ro(1-D)^2+2C_oLS^2/(1-D)^2} \quad (3.17)$$

### 3.4 Operating Principle and Analysis in DCM

The working of the proposed mSIBC for DCM is divided into three modes; one when switches $S_1$ and $S_2$ are turned ON (ON state), second when switches $S_1$ and $S_2$ are turned OFF and inductor currents are non-zero, and third when switches $S_1$ and $S_2$ are turned OFF and inductor currents are zero. Let us assume the inductor current reaches zero at time $t_2$, as shown in Fig. 3.2(b). In typical DCM characteristics [see Fig. 3.2(b)], $K_1T_S$ or $T_{ON}$ is mode I time period (i.e., time $t_0$–$t_1$), $K_2T_S$ or $T_{OFF,1}$ (i.e., time $t_1$–$t_2$) is mode II time period, and $K_3T_S$ or $T_{OFF,2}$ (i.e., time $t_2$–$t_3$) is mode III time period.

*1) Mode I ($t_0$–$t_1$)—Switches $S_1$ and $S_2$ Are Turned on:* For this mode, the operation of mSIBC and equivalent circuitry is the same as CCM mode I. In this mode, both inductors $L_1$ and $L_2$ are magnetized in parallel by input voltage $v_i$. At the starting of this mode (time $t_o$ or $t_o + T_s$), both inductors $L_1$ and $L_2$ currents started from zero level and reached the maximum level at the end of this mode. The maximum current through inductors $L_1$ and $L_2$ can be obtained as follows:

$$I_{L,\max} = I_{L1,\max} = I_{L2,\max} = V_iK_1 / Lf_s \quad (3.18)$$

Where $I_{L1,max}$ and $I_{L2,max}$ are the maximum currents through inductor $L_1$ and $L_2$, respectively, and $f_s = 1/T_S$ is the switching frequency. The current ripples of inductors $L_1$ and $L_2$ can be obtained as

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = V_iK_1 / Lf_s \quad (3.19)$$

Where $\Delta I_{L1}$ and $\Delta I_{L2}$ are the current ripples of inductor $L_1$ and $L_2$, respectively.

*2) Mode II ($t_1$–$t_2$)—Switches $S_1$ and $S_2$ Are Turned off and Inductor Currents Are Non-zero:* For this mode, the operation of mSIBC and equivalent circuitry is the same as CCM mode II. In this mode, inductors $L_1$ and $L_2$ are demagnetized in series with input voltage $v_i$ to charge capacitor $C_o$ and provide energy to load $R_o$. At the starting of this mode (time $t_1$ or $t_1 + T_s$), both inductors $L_1$ and $L_2$ currents started from the maximum current level and reached zero level at the end of this mode (time $t_2$ or $t_2 + T_s$). Another expression for the maximum current level through inductor $L_1$ and $L_2$ can be obtained as follows:

$$I_{L,\max} = I_{L1,\max} = I_{L2,\max} = \ V_o - V_i \ K_2 \ / \ 2Lf_s \tag{3.20}$$

The current ripples of inductors $L_1$ and $L_2$ can be obtained as

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = \ V_o - V_i \ K_2 \ / \ 2Lf_s \tag{3.21}$$

*3) Mode III ($t_2$–$t_3$)—Switches $S_1$ and $S_2$ Are Turned off and Inductor Currents Are Zero:* The equivalent circuitry for this mode is shown in Fig. 3.5. In this mode, switches $S_1$ and $S_2$ are turned OFF and inductors $L_1$ and $L_2$ currents are at zero level. Therefore, stored energies of inductors $L_1$ and $L_2$ are zero. All the diodes $D_o$–$D_2$ are reversed biased, and capacitor $C_o$ is discharged through load $R_o$.
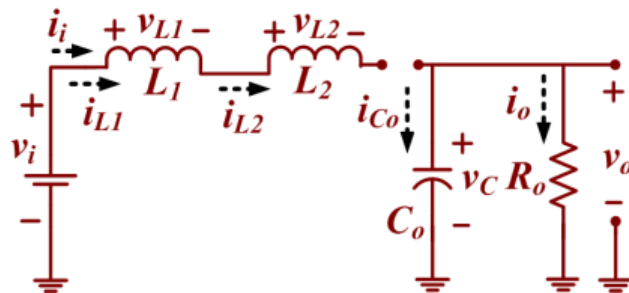


Figure 3.5. Equivalent circuitry for the DCM mode.

Using (3.19) and (3.20), the time period of mode II i.e., $K_2T_s$ or $T_{OFF,1}$ can be obtained as

$$K_2T_s \ or \ T_{OFF,1} = 2V_iK_1 \ / \ \left(V_o - V_i\right) f_s \tag{3.22}$$

It is known that

$$T_{ON} + T_{OFF,1} + T_{OFF,2} = T_s \tag{3.23}$$

The time period for mode I and mode III can be obtained as

$$T_{ON} = \frac{K_1}{f_s}, K_3T_s \ or \ T_{OFF,2} = 1 - \frac{1}{f_s}\left[K_1 + \frac{2V_iK_1}{V_o - V_i}\right] \tag{3.24}$$

From Fig. 3.2(b), the average current through capacitor $C_o$ can be obtained as

$$I_{Co} = 0.5 \ K_2 \times I_{L,\max} - I_o = 0.5 \ K_2 \times I_{L,\max} - V_o \ / \ R_o \tag{3.25}$$

By using (3.22) and (3.25)

$$I_{Co} = 0.5\left(\frac{2V_iK_1}{V_o - V_i} \times \frac{V_iK_1}{Lf_s}\right) - \frac{V_o}{R_o} \tag{3.26}$$

Under steady-state condition, any capacitor average current is always zero. Therefore, (3.26) can be rewritten as

$$\frac{2V_iK_1}{V_o - V_i} \times \frac{V_iK_1}{Lf_s} = \frac{2V_o}{R_o} \tag{3.27}$$

Using (3.27), the quadratic equation is obtained as

$$\left(\frac{V_o}{V_i}\right)^2 - \frac{V_o}{V_i} - \frac{K_1^2}{\xi_L} = 0 \tag{3.28}$$

Where $\xi_L$ is the normalized time constant for inductors $L_1$ and $L_2$, and its value is equal to $Lf_s/R_o$. Therefore, the variation in $\xi_L$ is based on the value of $L$, $f_s$, and $R_o$. By solving (3.28), the voltage gain of mSIBC for DCM ($M_{DCM}$) can be obtained as

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$$M_{DCM} = \frac{V_o}{V_i} = \frac{1}{2} + \left(\frac{0.25\xi_L + K_1^2}{\xi_L}\right)^{1/2} = \frac{1}{2} + \left(\frac{1}{4} + \frac{K_1^2 R_o}{L f_s}\right)^{1/2} \tag{3.29}$$

Suppose that the proposed mSIBC configuration is operated at the boundary of CCM and DCM, then the voltage gain of CCM and DCM is same. Therefore, by using (3.13) and (3.29)

$$\frac{V_o}{V_i} = 0.5 + \left(\frac{0.25\xi_{LB} + K_1^2}{\xi_{LB}}\right)^{1/2} = \frac{1+D}{1-D} \tag{3.30}$$

It is known that the mode I for CCM and DCM is the same. Therefore, $K_1 = D$, and the normalized boundary time constant ($\xi_{LB}$) for inductors $L_1$ and $L_2$ can be obtained as

$$\xi_{LB} = 0.5 \ D^3 - 2D^2 + D \ / \ 1+D \tag{3.31}$$

Fig. 3.6 depicts the plot of $\xi_{LB}$ versus $D$; where DCM and CCM regions are shown. If the value of $\xi_{LB}$ is larger than $\xi_L$, then the proposed mSIBC configuration operates in DCM.
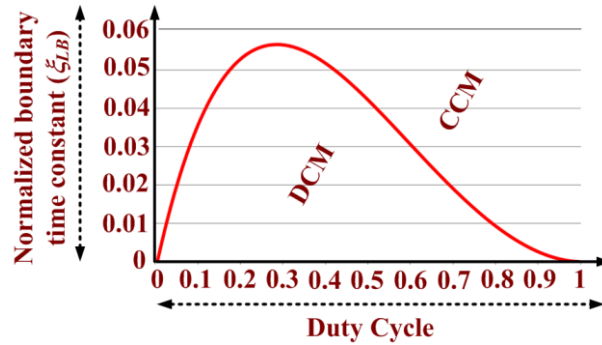


Figure 3.6. Normalized boundary time constant versus duty cycle.

3.5 Effect of Unequal Inductances on Voltage Gain

The operation of the proposed converter depends on the values of the inductors $L_1$ and $L_2$. Mainly, the current waveforms through inductor $L_1$ and $L_2$ are dependent on the values of $L_1$ and $L_2$.

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*A. When the Value of $L_1$ is Larger than the Value of $L_2$ ($L_1$>$L_2$)*

The characteristic waveforms of the inductor $L_1$ and $L_2$ currents are shown in Fig. 3.7(a). In this case, the converter operates in three modes as follows.

*1) Mode I (Time $t_0$–$t_1$):* In this mode, switches $S_1$ and $S_2$ are turned ON, and equivalent circuitry is the same as mode I of CCM. In this mode, inductors $L_1$ and $L_2$ are magnetized by input supply $v_i$, diodes $D_2$ and $D_o$ are reversed biased, diode D1 is forward biased, and the capacitor $C_o$ is discharged through the load $R_o$. The input current $i_i$ is equal to sum of inductor currents, i.e., $i_i = i_{L1} + i_{L2}$. The slope of the inductor $L_1$ and $L_2$ currents can be obtained as follows:

$$\frac{d\ i_{L1}}{dt} \approx \frac{v_i}{L_1}, \frac{d\ i_{L2}}{dt} \approx \frac{v_i}{L_2} \tag{3.32}$$

In this mode, the current through inductor $L_1$ is smaller than the current through inductor $L_2$ due to $L_1$>$L_2$.

*2) Mode II (Time $t_1$–$t_2$):* This mode occurs for short duration [$YT_s$, as shown in Fig. 3.7(a)] when switches $S_1$ and $S_2$ are just turned OFF. The equivalent circuitry is shown in Fig. 3.7(b), where diodes $D_1$ and $D_2$ are forward biased. During this mode, the currents through inductor $L_1$ increase with small positive slope (approximately zero slope) and the currents through inductor $L_2$ decreases with a large negative slope. The inductor $L_1$ is magnetized and inductor $L_2$ is demagnetized through path $v_i - L_1 - D_2 - L_2 - (C_o//R_o)$ and $v_i - D_1 - L_2 - (C_o//R_o)$, respectively. The value of current through inductor $L_2$ is larger than the current through inductor $L_1$. Also, the input current $i_i$ is equal to inductor $L_2$ current, i.e., $i_i = i_{L2}$, and the resultant current through diode $D_1$ is the subtraction of inductors $L_2$ and $L_1$ currents, i.e., $i_{L2} - i_{L1}$. The slope of the inductor $L_1$ and $L_2$ currents is obtained as follows:

$$\frac{d\ i_{L1}}{dt} \approx 0, \frac{d\ i_{L2}}{dt} \approx \frac{v_i - v_o}{L_2} \tag{3.33}$$

This mode ends as soon as the currents through inductor $L_1$ and $L_2$ are equal, and circuitry operates in mode III.



(a)  (b)
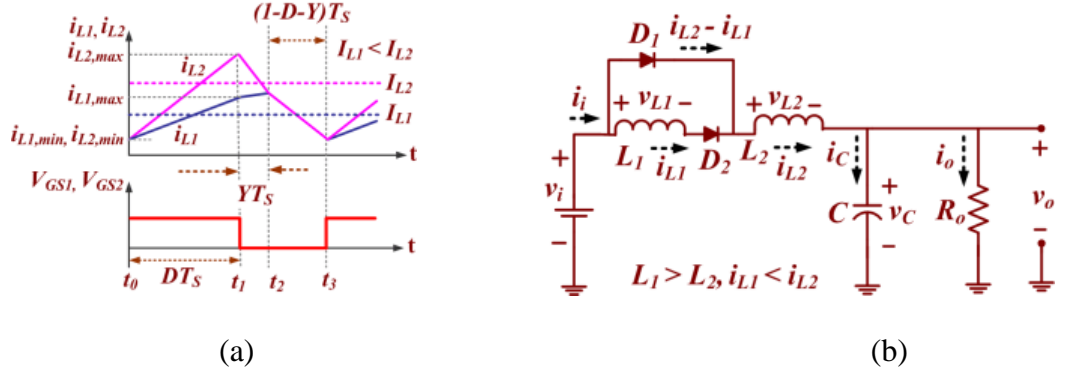
Figure 3.7. When $L_1 > L_2$. (a) Inductor currents (b) Mode II.

*3) Mode III (Time $t_2$–$t_3$):* In this mode, switches $S_1$ and $S_2$ are turned OFF, and equivalent circuitry is the same as CCM mode II. During this mode, diodes $D_2$ and $D_o$ are forward biased, and diode $D_1$ is reversed biased. Throughout this mode, inductors $L_1$ and $L_2$ are discharged in series with input voltage $v_i$ through load $R_o$. In this case, input current and the current through inductor $L_1$ and $L_2$ are equal, i.e., $i_i = i_{L1} = i_{L2}$. The voltage across inductor $L_1$ and $L_2$ is obtained as follows:

$$\frac{d\ i_{L1}}{dt} = \frac{v_i - v_o}{L_1 + L_2}, \frac{d\ i_{L2}}{dt} = \frac{v_i - v_o}{L_1 + L_2} \tag{3.34}$$

Using small approximation and inductor volt second balance

$$For\ L_1 \Rightarrow v_i(D) + \frac{v_i - v_o}{L_1 + L_2} L_1(1 - D - Y) = 0 \tag{3.35}$$

$$For\ L_2 \Rightarrow v_i(D) + \ v_i - v_o \ Y + \frac{v_i - v_o}{L_1 + L_2} L_2(1 - D - Y) = 0 \tag{3.36}$$

Solving (3.35) and (3.36), the voltage gain of mSIBC is obtained as

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$$V_o/V_i\big|_{L_1>L_2} = 1+D \ / \ 1-D \tag{3.37}$$

*B. When the Value of $L_1$ is smaller than the Value of $L_2$ ($L_1<L_2$)*

The typical waveform of the inductor $L_1$ and $L_2$ currents are shown in Fig. 3.8(a). In this case, the converter operates in three modes as discussed in the following sections,

*1) Mode I (Time $t_0$–$t_1$):* In this mode, switches $S_1$ and $S_2$ are turned ON, and equivalent circuitry is the same as mode I of CCM. In this mode, inductors $L_1$ and $L_2$ are magnetized by input supply $v_i$, diodes $D_2$ and $D_o$ are reversed biased, diode $D_1$ is forward biased, and the capacitor $C_o$ is discharged through the load $R_o$. The input current $i_i$ is equal to the addition of inductor currents, i.e., $i_i = i_{L1} + i_{L2}$. The slope of the inductor $L_1$ and $L_2$ currents can be obtained as follows:

$$\frac{d\ i_{L1}}{dt} \approx \frac{v_i}{L_1}, \frac{d\ i_{L2}}{dt} \approx \frac{v_i}{L_2} \tag{3.38}$$

In this case, the current through inductor $L_1$ is larger than the current through inductor $L_2$ due to $L_1 < L_2$.

*2) Mode II (Time $t_1$–$t_2$):* This mode occurs for short duration [$YT_s$, as shown in Fig. 3.8(a)] when switches $S_1$ and $S_2$ are just turned OFF. The equivalent circuitry is shown in Fig. 3.8(b), where diodes $D_1$ and $D_2$ are reversed and forward biased, respectively. During this mode, the currents through inductor $L_1$ decreases with a large negative slope, and the currents through inductor $L_2$ increases with small positive slope (approximate zero slope). The value of current through inductor $L_1$ is larger than the current through inductor $L_2$. The inductor $L_1$ is demagnetized and inductor $L_2$ is magnetized through path $v_i − L_1 − D_{S1} − D_o − (C_o//R_o)$ and $v_i − L_1 − D_2 − L_2 − D_o − (C_o//R_o)$, respectively. However, the input current $i_i$ is equal to inductor $L_1$ current, i.e., $i_i = i_{L1}$, and the resultant current through diode $D_{S1}$ is the subtraction of inductors $L_1$ and

$L_2$ currents, i.e. $i_{L1} - i_{L2}$. The slope of the inductor $L_1$ and $L_2$ currents is obtained as follows:

$$\frac{d\ i_{L1}}{dt} \approx \frac{v_i - v_o}{L_1}, \frac{d\ i_{L2}}{dt} \approx 0 \tag{3.39}$$

This mode end as soon as the currents through inductors $L_1$ and $L_2$ are equal, and circuitry operates in mode III.



(a)                                                                 (b)
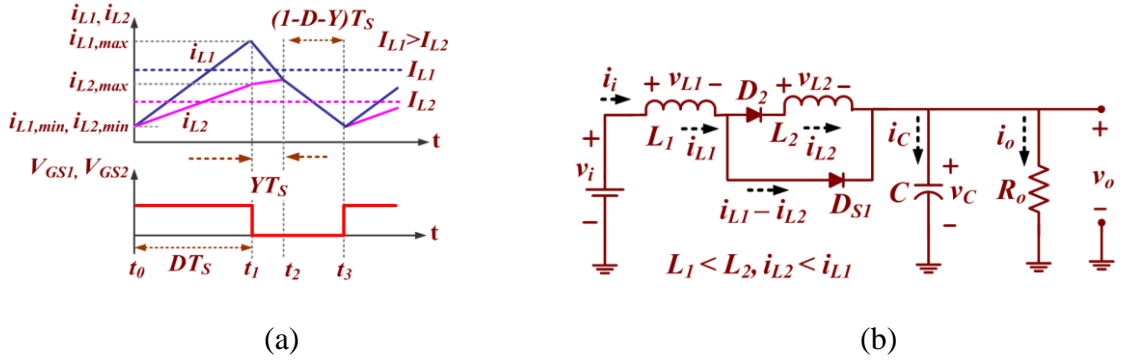
Figure 3.8. When $L_1 < L_2$ (a) inductor currents, and (b) Mode II.

*3) Mode III (Time $t_2$–$t_3$):* In this mode, switches $S_1$ and $S_2$ are turned OFF, and equivalent circuitry is the same as CCM mode II. During this mode, diodes $D_2$ and $D_o$ are forward biased, and diode $D_1$ is reversed biased. Throughout this mode, inductors $L_1$ and $L_2$ are discharged in series with input voltage $v_i$ through load $R_o$. In this case, input current and the current through inductor $L_1$ and $L_2$ are equal, i.e., $i_i = i_{L1} = i_{L2}$. The voltage across inductor $L_1$ and $L_2$ can be obtained as follows:

$$\frac{d\ i_{L1}}{dt} = \frac{v_i - v_o}{L_1 + L_2}, \frac{d\ i_{L2}}{dt} = \frac{v_i - v_o}{L_1 + L_2} \tag{3.40}$$

Using small approximation and inductor volt second balance

$$For\ L_1 \Rightarrow v_i(D) + \ v_i - v_o\ Y + \frac{v_i - v_o}{L_1 + L_2} L_1(1 - D - Y) = 0 \tag{3.41}$$

$$For\ L_2 \Rightarrow v_i(D) + \frac{v_i - v_o}{L_1 + L_2} L_2(1 - D - Y) = 0 \tag{3.42}$$

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Solving (3.41) and (3.42), the voltage gain of mSIBC is obtained as

$$V_o/V_i\big|_{L_1 < L_2} = 1+D \ / \ 1-D \tag{3.43}$$

Therefore in case of unequal inductances, inductor average current is changed. However, voltage gain is $(1 + D)/(1 - D)$, which remains the same as (3.13).

### 3.6 Effect of Non-idealities on Voltage Gain

To analyze the effect of the non-idealities of components and devices on the output voltage, the non-idealities are considered in the power circuit, as shown in Fig. 3.9. The equivalent series resistance (ESR) of inductors $L_1$ and $L_2$ is shown by the resistance $r_L$. The ON-state resistance of switches $S_1$ and $S_2$ is shown by the resistance $r_S$. The forward resistance and the threshold voltage of diodes $D_1$, $D_2$, and $D_o$ are shown by resistance $r_D$ and voltage $V_{FD}$, respectively. The ESR of capacitor $C_o$ is shown by $r_{Co}$.
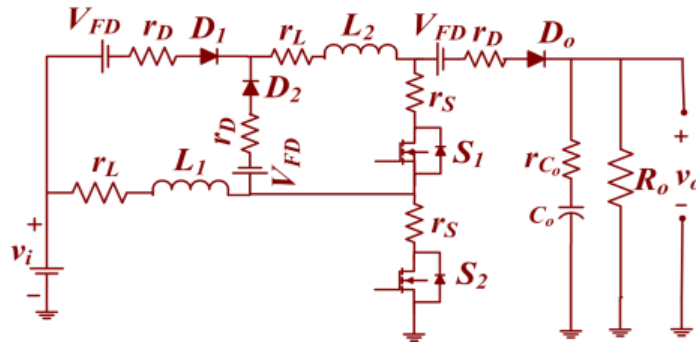


Figure 3.9. Equivalent circuit of mSIBC configuration with non-idealities.

### 3.6.1 Effect of ESR of Inductors on Voltage Gain

In order to analyze the effect of ESR of inductors $L_1$ and $L_2$, the anomaly arising due to other parasitic is ignored, i.e., $r_S = 0$, $r_D = 0$, $r_{Co} = 0$, and $V_{FD} = 0$. Considering this case, the voltages across inductors $L_1$ and $L_2$ are obtained as follows:

$$\text{ON state} \Rightarrow v_{L1} \approx V_i - i_{L1}r_L, v_{L2} \approx V_i - i_{L2}r_L, V_o \approx v_{Co} \tag{3.44}$$

$$\text{OFF state} \Rightarrow v_{L1} + v_{L2} \approx V_i - i_{L1}r_L - i_{L2}r_L - V_o \tag{3.45}$$

Using (3.44) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{L1}r_L - i_{L2}r_L \tag{3.46}$$

Using small approximation and inductor volt-sec balance principle

$$\left(2V_i - i_{L1}r_L - i_{L2}r_L\right) D = -\left(V_i - i_{L1}r_L - i_{L2}r_L - V_o\right)(1-D) \tag{3.47}$$

Using (3.47), the voltage gain of mSIBC is obtained as follows:

$$\left. \frac{V_o}{V_i} \right|_{r_L} = \frac{1+D - \left(i_{L1}r_L + i_{L2}r_L\right)/V_i}{1-D} \tag{3.48}$$

If $L_1 = L_2$, the currents flowing through both the inductors $L_1$ and $L_2$ are equal, i.e., $i_L = i_{L1} = i_{L2}$. Let us assume that the voltage drop due to ESR of the inductor is $V_{d-L}$, i.e., $Vd_{-L} = i_{L1}r_L = i_{L2}r_L$. Thus, (3.48) is rewritten as

$$\left. \frac{V_o}{V_i} \right|_{r_L} = \frac{1+D - 2V_{d-L}/V_i}{1-D} \tag{3.49}$$

Equation (3.49) is graphically plotted in Fig. 3.10(a) by considering the different values for $V_{d-L}/V_i$ and duty cycle $D$; and the effect of ESRs of inductors on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of $V_{d-L}$ and $D$. This fact guides that the ESR of inductance ($r_L$) and duty cycle ($D$) should not be too large.

### 3.6.2 Effect of Diodes on Voltage Gain

In order to analyze the effect of diodes $D_1$, $D_2$, and $D_o$, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0$, $r_{Co} = 0$, and $r_S = 0$. Considering this case, the voltages across inductors $L_1$ and $L_2$ are obtained as follows:

$$\text{ON State} \Rightarrow v_{L1} \approx V_i, v_{L2} \approx V_i - i_{L2}r_D - V_{FD} \tag{3.50}$$

$$\text{OFF State} \Rightarrow v_{L1} + v_{L2} \approx V_i - 2i_{L2}r_D - 2V_{FD} - V_o \tag{3.51}$$

Using (3.50) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{L2}r_D - V_{FD} \tag{3.52}$$

Using small approximation and inductor volt-sec balance principle

$$\left(2V_i - i_{L2}r_D - V_{FD}\right)D = -\left(V_i - 2i_{L2}r_D - 2V_{FD} - V_o\right)\left(1 - D\right) \tag{3.53}$$

Using (3.53), the voltage gain of mSIBC is obtained as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_D, V_{FD}} = \frac{1 + D - \left(\left(i_{L2}r_D + V_{FD}\right)\left(2\text{-}D\right) / V_i\right)}{1\text{-}D} \tag{3.54}$$

Let us assume that the voltage drop due to forward resistance and the threshold voltage of the diode is $V_{d-D}$, i.e., $V_{d-D} = i_{L2}r_D + V_{FD}$. Thus, (3.54) is rewritten as follows:

$$\left.\frac{V_o}{V_i}\right|_{r_D, V_{FD}} = \frac{1 + D - \left(V_{d-D}\left(2-D\right) / V_i\right)}{1-D} \tag{3.55}$$

Equation (3.55) is graphically plotted in Fig. 3.10(b) by considering the different values for $V_{d-D}/V_i$ and $D$, and the effect of diodes on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of $V_{d-D}/V_i$ and $D$. This fact guides that the forward resistance and the threshold voltage of diodes should not be too large.

### 3.6.3 Effect of Switches on Voltage Gain

In order to analyze the effect of switches $S_1$ and $S_2$, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0$, $r_{Co} = 0$, $r_D = 0$, and $V_{FD} = 0$. Considering this case, the voltages across inductor $L_1$ and $L_2$ are obtained as follows:

$$\text{ON State} \Rightarrow v_{L1} \approx V_i - i_{S2}r_S, v_{L2} \approx V_i - i_{S1}r_S - i_{S2}r_S \tag{3.56}$$

$$\textbf{OFF State} \Rightarrow v_{L1} + v_{L2} \approx V_i - V_o \tag{3.57}$$

Using (3.56) and adding voltages across inductors

$$v_{L1} + v_{L2} \approx 2V_i - i_{S1}r_S - 2i_{S2}r_S \tag{3.58}$$

Using small approximation and inductor volt-sec balance principle

$$2V_i - i_{S1}r_S - 2i_{S2}r_S \; D = -\; V_i - V_o \quad 1-D \tag{3.59}$$

Using (3.59), the voltage gain of mSIBC is obtained as follows:

$$\left. \frac{V_o}{V_i} \right|_{r_S} = \frac{1+D \; - \; D \; i_{S1}r_S + 2i_{S2}r_S \; / V_i}{1-D} \tag{3.60}$$

Assume that the voltage drops in switches $S_1$ and $S_2$ are the same, i.e., $V_{d-S} = i_{S1}r_S = i_{S2}r_S$. Thus, (3.60) is rewritten as follows:

$$\left. \frac{V_o}{V_i} \right|_{r_S} = \frac{1+D \; - 3D \; V_{d-S} \; / V_i}{1-D} \tag{3.61}$$

Equation (3.60) is graphically plotted in Fig. 3.10(c) by considering the different values for $V_{d-S}/V_i$ and $D$; and the effect of ON-state resistance of switches on voltage gain is shown. It is observed that there is a decrement in the voltage gain for higher values of $V_{d-S}/V_i$ and $D$. This fact guides that the ON-state resistance of switches should not be too large.

### 3.6.4 Effect of Capacitor and its ESR on Voltage Gain

In order to analyze the effect of ESR of capacitor $C_o$, the anomaly arising due to other parasitic is ignored, i.e., $r_{L1} = 0$, $r_{L2} = 0$, $r_D = 0$, $V_{FD} = 0$, and $r_S = 0$. Let us assume that the voltage drop across resistance $r_{Co}$ is $V_{d-Co}$. When switches are turned

ON, the capacitor $C_o$ is discharged through load $R_o$. The output voltage that is the voltage across capacitor $C_o$ is dropped down, and instantaneous output voltage can be calculated as

$$v_o = V_o - V_{d-C_o} - \frac{I_o}{C_o} t = V_o \left( 1 - \frac{1}{R_o C_o} t \right)$$

(3.62)

At the end of ON-state, change in output voltage ($\Delta V_o$) is

$$\Delta V_o \big|_C = \frac{V_o}{R_o C_o f} \times D$$

(3.63)

This fact provides the guidance that the load resistance $R_o$, switching frequency $f$, and capacitance $C_o$ should not be too small, and ESR and duty ratio should not be too large.

### 3.6.5 Combined Effect of Non-idealities on Voltage Gain

By considering the non-idealities of inductors $L_1$ and $L_2$, diodes $D_1$, $D_2$, and $D_o$, switches $S_1$ and $S_2$, and effect of ESR of capacitor $C_o$, the voltage gain can be obtained as follows:

$$\frac{V_o}{V_i} \approx \frac{1 + D - \dfrac{2V_{d-L}}{V_i} - (2-D)\dfrac{V_{d-D}}{V_i} - 3D\dfrac{V_{d-S}}{V_i} - \dfrac{V_{d-C_o}}{V_i}}{1 - D}$$

(3.64)

### 3.7 Converter Efficiency Analysis

The currents through capacitor Co in ON-state and OFF-state are obtained as follows:

$$i_{Co} = -v_o R_o^{-1} \quad \text{in ON-State,} \quad i_i - v_o R_o^{-1} \quad \text{in OFF-State}$$

(3.65)

In OFF state, the currents through inductors $L_1$ and $L_2$ are the same, i.e., $i_L = i_{L1} = i_{L2}$. Using (3.65), small approximation, and capacitor charge balanced principle

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$$\int_0^{DT_S} \left( \frac{V_o}{R_o} \right) dt = \int_{DT_S}^{T_S} \left( I_L - \frac{V_o}{R_o} \right) dt \Rightarrow \frac{V_o}{R_o} D = \left( I_L - \frac{V_o}{R_o} \right) 1 - D \tag{3.66}$$

Using (3.66), the inductor currents are obtained as

$$I_L = I_{L1} = I_{L2} = \frac{V_o R_o^{-1}}{1 - D} \tag{3.67}$$

It is considered that $P_{SW-S1}$ and $P_{SW-S2}$ are the switching power losses due to switching of switches $S_1$ and $S_2$, respectively. The total loss during switching $P_{SW-T}$ is obtained as follows:

$$P_{SW-T} = \sum_{i=1,2} P_{SW-Si} = \frac{1}{T_S} \left\{ \begin{array}{l} \left( I_{S1} \times V_{S1} \right) \left( t_{r-S1} + t_{f-S1} \right) + \\ \left( I_{S2} \times V_{S2} \right) \left( t_{r-S2} + t_{f-S2} \right) \end{array} \right\} \tag{3.68}$$

Where rising and falling times of switches $S_1$ and $S_2$ are $t_{r-S1}$, $t_{f-S1}$ and $t_{r-S2}$, $t_{f-S2}$, respectively; $I_{S1}$, $V_{S1}$ and $I_{S2}$, $V_{S2}$ are the average current and voltage through/across switches $S_1$ and $S_2$, respectively. The total power at the input and output ports is obtained as follows:

$$P_i \begin{cases} = V_i \left\{ 2I_L D + I_{L1} \left( 1 - D \right) \right\} + P_{SW-T} \\ = \dfrac{V_i V_o R_o^{-1}}{1 - D} \left( 1 + D \right) + P_{SW-T} \end{cases} , P_o = \frac{V_o^2}{R_o} \tag{3.69}$$

Using (3.64)–(3.69), the efficiency is obtained as follows:

$$\eta_{mSIBC} = \frac{1 + D - \dfrac{2V_{d-L}}{V_i} - \dfrac{\left( 2 - D \right) V_{d-D}}{V_i} - \dfrac{3D V_{d-S}}{V_i} - \dfrac{V_{d-C_o}}{V_i}}{\left( 1 + D \right) + P_{SW-T} \dfrac{R_o \left( 1 - D \right)}{V_o V_i}} \tag{3.70}$$

In order to analyze the effect of load and inductors on the efficiency of the converter, the anomaly arising due to other parasitic effects is ignored. Therefore,

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$$\eta_{mSIBC} = \frac{1 + D - 2V_{d-L}}{(1+D) + \dfrac{R_o(1-D)}{V_o V_i}} \qquad (3.71)$$

Fig. 3.10(d) shows the efficiency plot versus the duty cycle for different values of load cases.



(a)

(b)

(c)

(d)
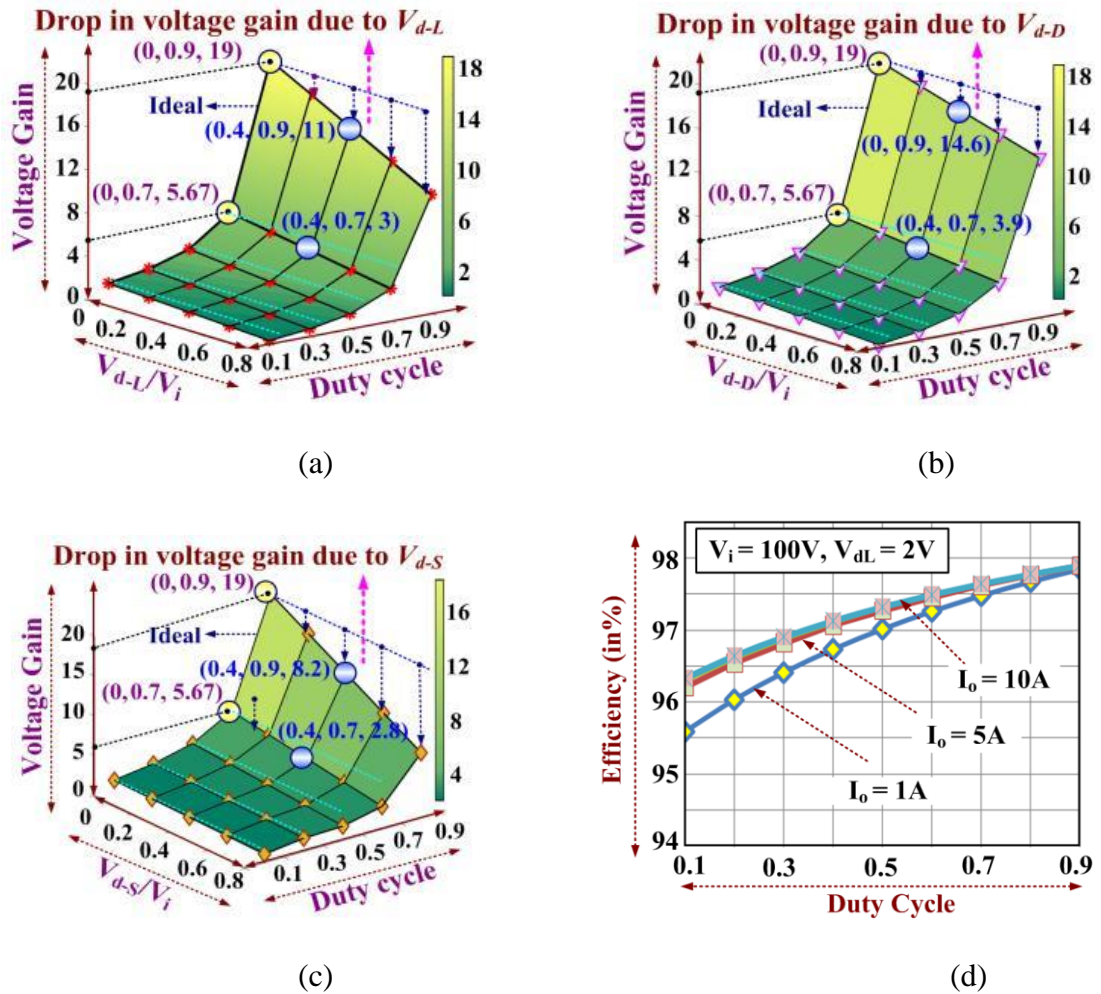
Figure 3.10. Effect of non-idealities on voltage gain and duty cycle. (a) Non-idealities of inductors. (b) Non-idealities of diodes. (c) Non-idealities of switches. (d) Efficiency versus duty cycle.

### 3.8 Design of Circuit Parameters

The mSIBC converter is designed by considering the typical input voltage of 100 V, output power of 500 W, output voltage of 400 V, and switching frequency of 100 kHz to validate functionality and performance.

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### 3.8.1 Design and Selection of Reactive Components

In order to have good performance, the reactive components are designed by considering the worst efficiency ($\eta_w$). Thus, by considering the worst efficiency 90%, the required duty cycle is calculated as

$$D\Big|_{\eta_w=90\%} = \frac{M-1}{\left(M+1\right)\eta_w} = \frac{4-1}{\left(4+1\right)0.90} \approx 66.67\% \tag{3.72}$$

The critical values of inductors $L_1$ and $L_2$ are obtained as

$$L_1\Big|_{critical} = L_2\Big|_{critical} = \frac{100V\times0.67}{2.5A\times100kHz} \approx 268\mu H \tag{3.73}$$

Using (3.73), the critical values of inductors $L_1$ and $L_2$ are calculated by considering the peak to peak ripple of inductor currents (=2.5A) as follows:

$$L_1\Big|_{critical} = L_2\Big|_{critical} = \frac{100V\times0.67}{2.5A\times100kHz} \approx 268\mu H \tag{3.74}$$

The inductance and current rating of the inductors $L_1$ and $L_2$ must be higher than critical inductance and input current, respectively. Thus, ferrite E type core inductors with rating 700 µH/10 A, $r_L$ = 75 mΩ are selected to design the prototype. The critical capacitance of output-side capacitor $C_o$ is obtained as

$$C_o\Big|_{critical} = \frac{P_o}{V_o\Delta V_{Co}}DT_S \tag{3.75}$$

The critical capacitance value of capacitor $C_o$ by considering the peak to peak voltage ripple of the capacitor, i.e., 4 V is calculated as follows:

$$C_o\Big|_{critical} = \frac{500W\times0.67}{400V\times4V\times100kHz} \approx 2.1\mu F \tag{3.76}$$

The voltage rating of the capacitor $C_o$ must be greater than output voltage i.e., 400 V. Therefore, a film-type capacitor with rating 2.2 µF/450 V ($r_{Co}$ = 4 mΩ) is selected to design the prototype.

### 3.8.2 Design and Selection of Semiconductor Devices

The voltage stresses across switches $S_1$ and $S_2$ are obtained as

$$V_{S1}\big|_{stress} = \frac{V_o - V_i}{2} , V_{S2}\big|_{stress} = \frac{V_o + V_i}{2} \tag{3.77}$$

The minimum voltage ratings of the switches $S_1$ and $S_2$ are calculated as follows:

$$V_{S1} = \frac{400V - 100V}{2} = 150V, V_{S2} = \frac{400V + 100V}{2} = 250V \tag{3.78}$$

The current rating of selected switches $S_1$ and $S_2$ must be greater than the input current. Therefore, FDP19N40-ND MOSFET ($r_s$ = 200m $\Omega$) and FDP18N20-ND MOSFET ($r_s$ = 140 m$\Omega$) are selected.

The peak inverse voltage (PIV) ratings of diodes $D_1$, $D_2$, and $D_o$ are calculated as follows:

$$V_{D1}\big|_{PIV} = \frac{V_i - V_o}{2} , V_{D2}\big|_{PIV} = -V_i, V_{Do}\big|_{PIV} = -V_o \tag{3.79}$$

For the given parameters, the minimum PIV ratings of diodes $D_1$, $D_2$, and $D_o$ are calculated as follows:

$$\begin{cases} V_{D1}\big|_{PIV} = \dfrac{-100 - 400}{2} = -250V, V_{D2}\big|_{PIV} = -100V \\ V_{Do}\big|_{PIV} = -400V \end{cases} \tag{3.80}$$

The current rating of selected diodes $D_1$, $D_2$, and $D_o$ must be greater than the input current. Therefore, diodes DPG10I400PM (400 V/10 A, $r_D$ = 19.8m$\Omega$, $V_{FD}$ = 0.77 V) and C3D10060AND (600 V/14 A, $r_D$ = 55.2 m$\Omega$, $V_{FD}$ = 0.91 V) are selected.

### 3.9 Simulation Results and Discussion

The proposed mSIBC converter topology is devised for 500W power, an output voltage of 400V, and an input voltage of 100V. Initially, the design and circuitry of proposed converter is validated through simulation. The obtained voltage and current

waveforms across/through each component is shown in Fig. 3.11(a)-(b), respectively. The obtained waveforms are matched with the typical waveforms discussed in Section 3.2. The average input current drawn by the proposed converter is nearly equal to 5A. However, the output current and both inductor's $L_1$ and $L_2$ currents are nearly equal to the 1.25A and 3A respectively as shown in Fig. 3.11(b). Fig. 3.11(a) displays the input voltage (100V), output voltage (400V), and diodes $D_1$ (150V), $D_2$ (100V) and $D_o$ (400V) voltages waveforms for the proposed converter. It is noteworthy that the voltage across switches $S_1$ and $S_2$ are 150V and 250V, respectively when the output voltage is 400V.



(a)                                             (b)
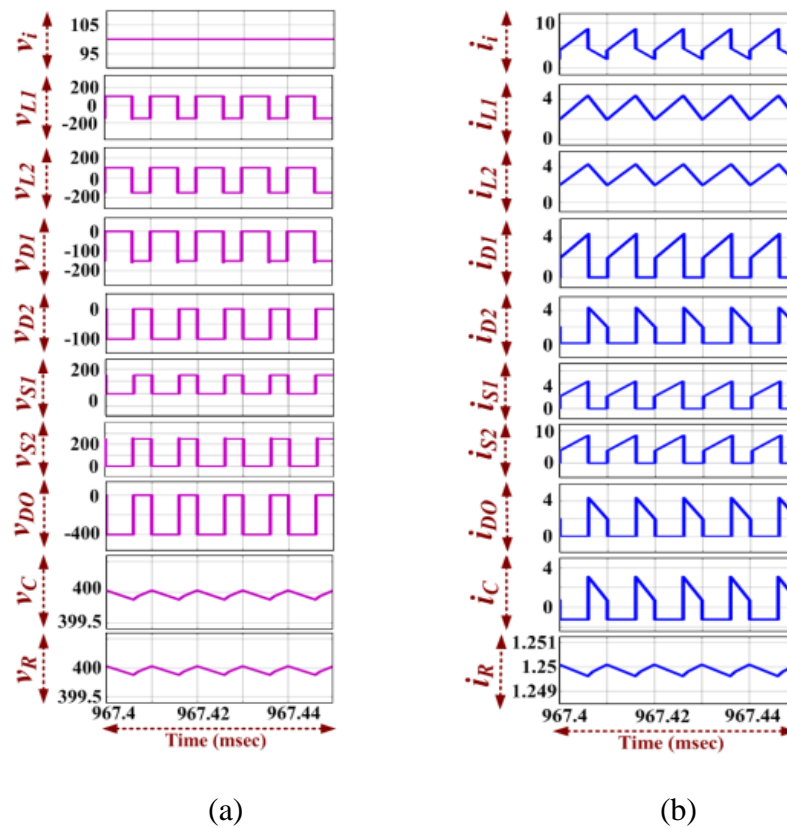
Figure 3.11. Simulation results, (a) voltage waveforms, (b) current waveforms.

### 3.10 Controller Design

The transfer function between the output voltage and duty cycle for the designed values as shown in (3.7) – (3.17), is obtained as

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$$\frac{\hat{v}_o(S)}{\hat{d}(S)} = \frac{-0.02734S + 1250}{1 + 2.73 \times 10^{-5}S + 1.92 \times 10^{-8}S^2} \tag{3.81}$$

The Bode plot for the open-loop transfer function is shown in Fig. 3.12(a). It is observed that the converter is inherently unstable. In order to operate the converter in closed loop, the open-loop transfer function is given with the proportional–integral controller, and the stability is analyzed using the Bode plot. The tuning of the controller is done with the help of the SISO toolbox. The controller is realized using the following controller transfer function:

$$\frac{C(S)}{E(S)} = \frac{(1 + 4S)(1 + 3.3 \times 10^{-6}S)}{1 + 0.0012S} \quad \frac{}{-0.02734S + 1250} \tag{3.82}$$

The stability of the system increases due to the placement of zero and poles at the left side of the S plane. The closed-loop transfer function Bode plot is shown in Fig. 3.12(b), and it can be concluded that the system is stable at 100 kHz with phase margin 64° and infinite gain margin. The tuned system with controller operates at the desired point with enough phase margin (PM) and infinite gain margin (GM) at the desired frequency (100 kHz) of operation. The control scheme is designed with the help of FPGA, as shown in Fig. 3.12(c). The lower and upper saturation limits (0.2–0.9 duty cycle) are set to incorporate the physical restriction of the converter. PMODAD1 (12 Bit, 2 channel) analog-to-digital converter is used for the sensing load voltage signal. Sensing capability of 1 Mega samples for the 12-bit converter and Sallen Key filter with poles set to 500 kHz avoid any aliasing effect. The step size of 100 ns is selected for FPGA to achieve at least 100 steps in each switching period of 10 μs. The control gate pulses of switching frequency 100 kHz are generated and fed via driver GDX 4A2S1 to control switches $S_1$ and $S_2$.
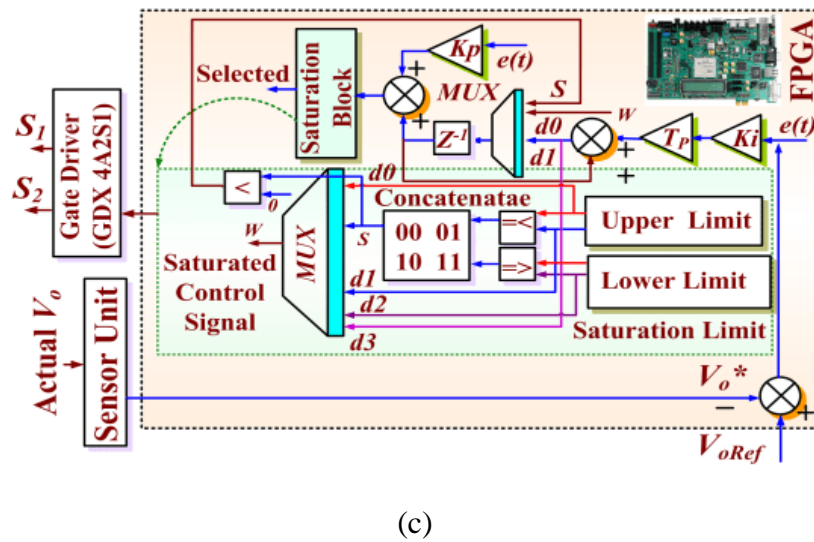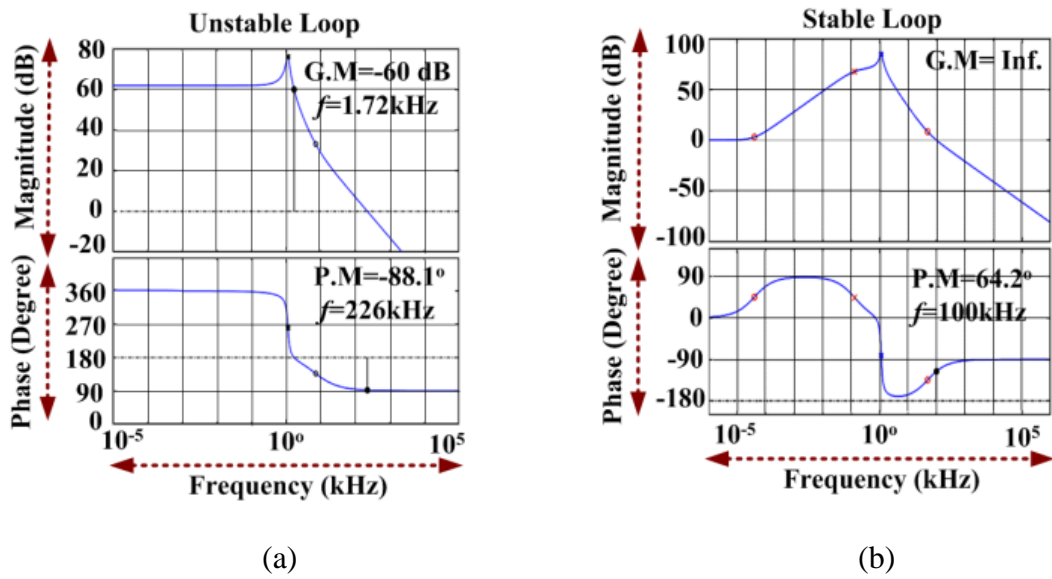
Figure 3.12. Control Scheme. (a) Bode plot in open loop. (b) Bode plot in closed loop. (c) Controller blocks.

3.11 Hardware Implementation, Experimental Results, and Discussion

The performance and functionality of the proposed converter are tested experimentally. The prototype of the mSIBC is implemented in the laboratory to validate the theoretical analysis and performance of the converter. The designed prototype is shown in Fig. 3.13.

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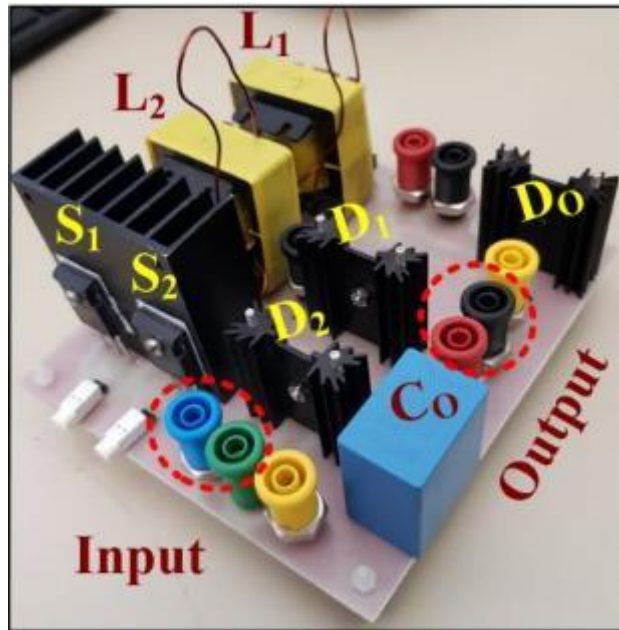
Figure 3.13. Designed 500 W mSIBC prototype.

     The obtained waveforms of output and input voltages and output and input currents are shown in Fig. 3.14(a). The observed average values of output voltage, input voltage, output current, and input current are 401.9 V, 100.1 V, 1.24 A, and 5.13 A, respectively. It is observed that input current is continuous, and the slope of the input current in ON-state and OFF-state is increasing and decreasing due to magnetizing and demagnetizing of both inductors $L_1$ and $L_2$, respectively. The obtained waveforms of voltage and current across/through inductors $L_1$ and $L_2$ are shown in Fig. 3.14(b). It is observed that both the inductors are magnetizing in ON-state with an input voltage of 99.8 V (approx.), and both the inductors $L_1$ and $L_2$ are demagnetizing in OFF-state with a voltage −151.3 V approximately. The observed average value of current through inductors $L_1$ and $L_2$ are 3.17 A and 3.19 A, respectively. In practice, the average value of voltage across inductors $L_1$ and $L_2$ is 0.57 V and 0.43 V, respectively. The obtained waveforms of voltage across switches $S_1$ and $S_2$ and diode $D_o$ are shown in Fig. 3.14(c), and inductor $L_2$ current waveform is also shown for reference and validation purpose. It is observed that both switches are turned-ON and -OFF simultaneously. The average

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and peak values of voltage across switches $S_1$ and $S_2$ are 56.9 V and 94.46 V, 151.3 V and 251.2V, respectively. Therefore, it is notable that the voltage stress for both switches $S_1$ and $S_2$ is lower than the output voltage. It is observed that the diode $D_o$ is forward biased when switches conducted. The average value of voltage across diodes $D_o$ is −249.1 V and PIV is −402.1 V. The waveform of current through switches $S_1$ and $S_2$ is observed and shown in Fig. 3.14(d); where the voltage across switch $S_1$, current through inductor $L_2$, and input current are also shown for reference and validation purposes. The average currents through switches $S_1$ and $S_2$ are 1.62 A and 3.10 A, respectively. In ON-state, it is observed that the slope of current through switch $S_1$ is equal to the slope of inductor $L_2$ current; and the slope of current through switch $S_2$ is equal to the slope of input current. The obtained waveform of voltage and current across/through diodes $D_1$ and $D_2$ is shown in Fig. 3.14(e), and inductor $L_2$ and input currents waveforms are also shown for reference and validation purposes. It is observed that diodes $D_1$ and $D_2$ are forward and reversed biased in ON and OFF states, respectively. The average value of voltage across diodes $D_1$ is −57.91 V and PIV is −150.3 V. The average value of voltage across diodes $D_2$ is −61.03 V and PIV is −99.8 V. The average value of currents through diodes $D_1$ and $D_2$ are 1.62 A and 2.57 A, respectively. In ON-state, it is observed that the slope of current through diode $D_1$ is equal to the slope of inductor $L_2$ current, and in OFF state, the slope of current through diode $D_2$ is equal to the slope of inductor $L_2$ current, which are expected.
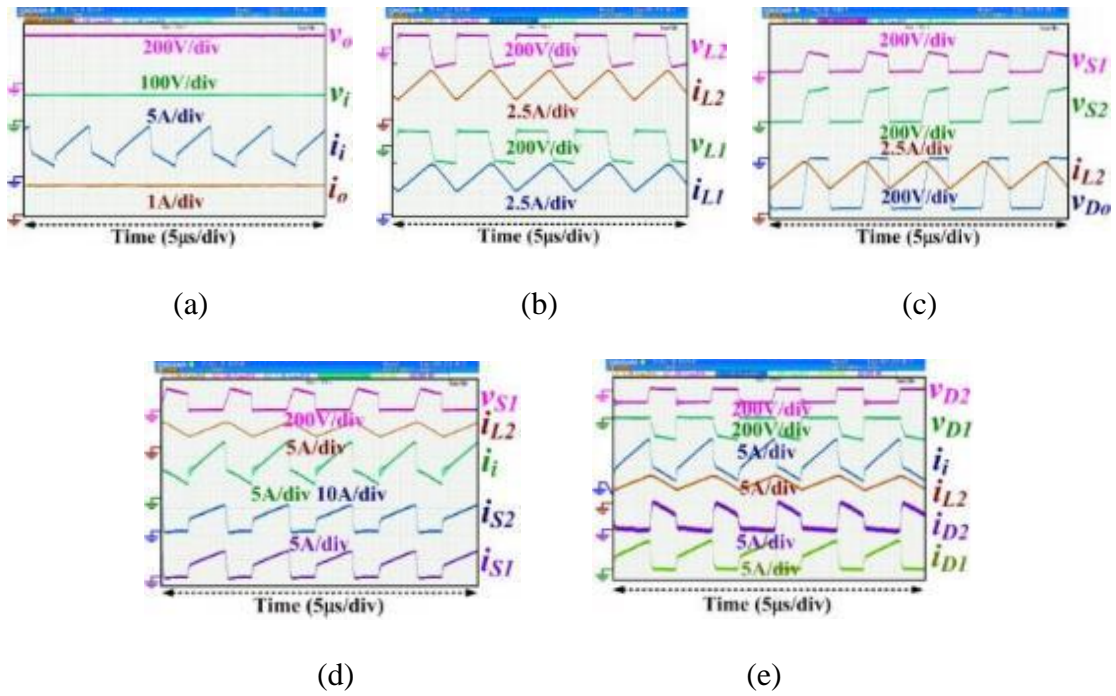
Figure 3.14. Experimental results. (a) Bottom to top: output current, input current, input voltage, and output voltage. (b) Bottom to top: inductor $L_1$ current and voltage, inductor $L_2$ current and voltage. (c) Bottom to top: diode $D_o$ voltage, inductor $L_2$ current, and switches $S_2$ and $S_1$ voltage. (d) Bottom to Top: switches $S_1$ and $S_2$ currents, input current, inductor $L_2$ current, and switches $S_1$ voltage. (e) Bottom to Top: diode $D_1$ and $D_2$ currents and inductor $L_2$ current, input current, diodes $D_1$ and $D_2$ voltage.

In order to test the performance of the designed converter in the DCM mode, the converter operates at low power (40 W) by connecting to 1-kΩ resistive load and output voltage reference is set to 200 V. The obtained input voltage and current and output voltage and current are shown in Fig. 3.15(a). In the presented waveforms, the OFF mode is split into two parts: mode II and mode III, i.e., DCM. It is observed that the input current is nonzero in mode II and zero in mode III, which confirms that the converter operates in DCM mode. It is observed that 200.7 V output voltage is achieved, and the input current is zero in mode III. The performance of the converter is also tested with an unequal inductance ($L_1 = 700$ μH, $L_2 = 450$ μH), and output voltage reference is

set at 400 V. The obtained waveform of current through inductor $L_1$ and $L_2$ currents and

voltage across diodes $D_1$ and $D_2$ are shown in Fig. 3.15(b). One switching period is split

into three modes. It is observed that in mode I, the current through inductor $L_2$ is higher

than the current through $L_1$. In mode II, the current through inductor $L_2$ is decreased

with a higher rate than the current through inductor $L_1$. In mode III, the currents through

inductors $L_1$ and $L_2$ are equal. It is investigated that the average current through inductor

$L_2$ is a little higher (0.6 A) than $L_1$, which is expected since $L_1 > L_2$. It is also investigated

that the diodes $D_1$ and $D_2$ are forward biased in Mode II.



(a)                                                   (b)
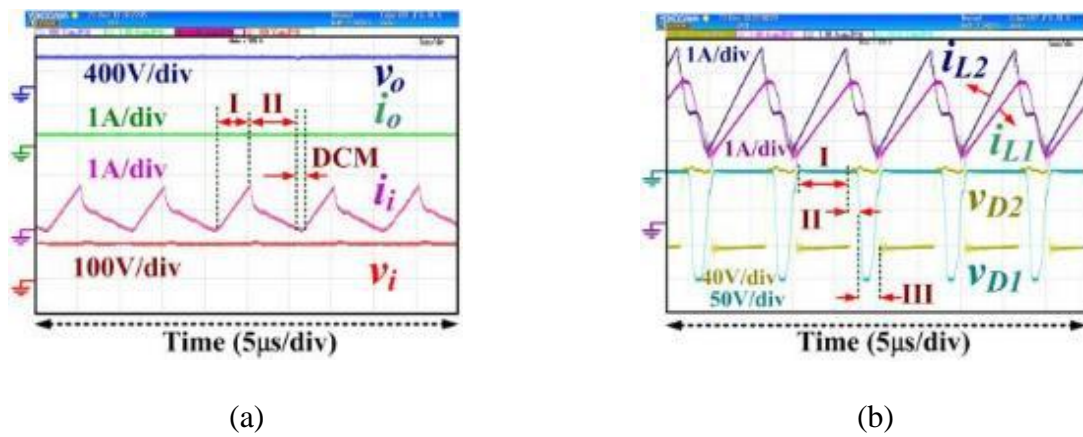
Figure 3.15. Experimental results. (a) Bottom to Top: input voltage, input current,

output current, output voltage in DCM. (b) Bottom to top: diode $D_1$ and $D_2$ voltage and

inductor $L_1$ and $L_2$ currents when $L_1>L_2$.

In order to test the performance of the converter under a perturbed condition,

the perturbation is introduced from load and source sides. Fig. 3.16(a) shows that

constant 401.1 V is achieved at the load when the input voltage is constant i.e., 100 V,

and load power decreased from 500 to 400 W and 400 to 320 W [i.e., A to B and B to

C in Fig. 3.16(a)]. Fig. 3.16(b) shows that constant 401.2 V is achieved at the load when

the input voltage is constant, i.e., 100 V and even when load power is increased from

320 to 400 W and 400 to 500 W [i.e., A to B and B to C in Fig. 3.16(b)]. The zoomed

waveform at P, Q, and R is shown in Fig. 3.16(a) and (b), and it is observed that duty

cycles in A, B, and C are the same; however, the magnitude of input and output current is changed accordingly to maintain power balance at the input and output side. Fig. 3.16(c) shows that constant 400.9 V is achieved at the load when load power is constant, i.e., 500 W and input voltage decreased from 105 to 90 V and 90 to 85 V [i.e., A to B and B to C in Fig. 3.16(c)]. Fig. 3.16(d) shows that constant 400.7 V is achieved at the load when load power is constant, i.e., 500 W and input voltage is increased from 85 to 90V and 90 to 105 V [i.e., A to B and B to C in Fig. 3.16(d)]. The zoomed waveforms at P and Q are shown in Fig. 3.16(c) and (d), and it is observed that the duty cycle is adjusted according to the input voltage to maintain the constant output voltage. Moreover, it is also observed that there is no change in output current even input current changed according to the input voltage. In order to investigate the dynamics of the converter in the initial starting condition, the load power and input voltage is set at 500 W and 100 V, respectively, and the converter is suddenly turned ON from OFF (rest) mode [A to B in Fig. 3.16(e)]. The observed waveforms are shown in Fig. 3.16(e). It is investigated that the steady state 401.7 V is achieved at the output and the settling time of the converter is approx. 0.12 s.

The performance of the converter is investigated at various power levels to investigate the efficiency of the designed prototype. The plot of efficiency versus power and loss distribution at 500W is shown in Fig. 3.17. It is found that most of the power loss takes place in the diodes. At power 500 W, the efficiency of the designed prototype is 97.17%.



(a)                                                                (b)

<center>(c)           (d)           (e)</center>
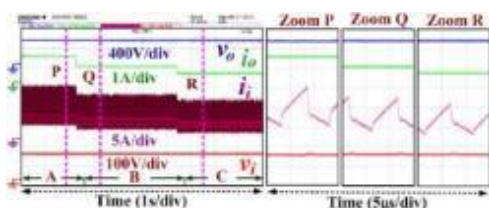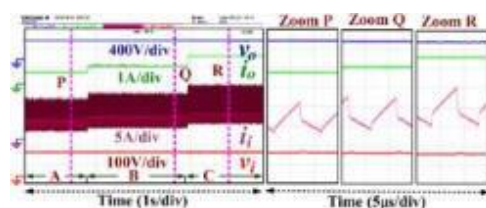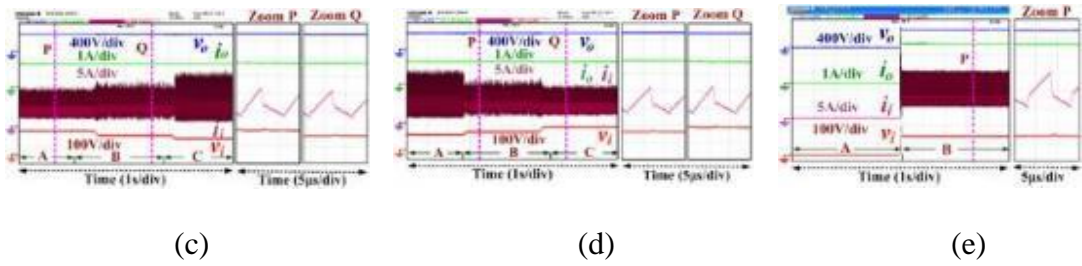
Figure 3.16. Experimental results (input and output voltages, input and output currents) of the proposed converter with perturbation. (a) When load power decreased. (b) When load power increased. (c) When input voltage decreased. (d) When input voltage increased. (e) Initial starting condition.



<center>(a)                       (b)</center>
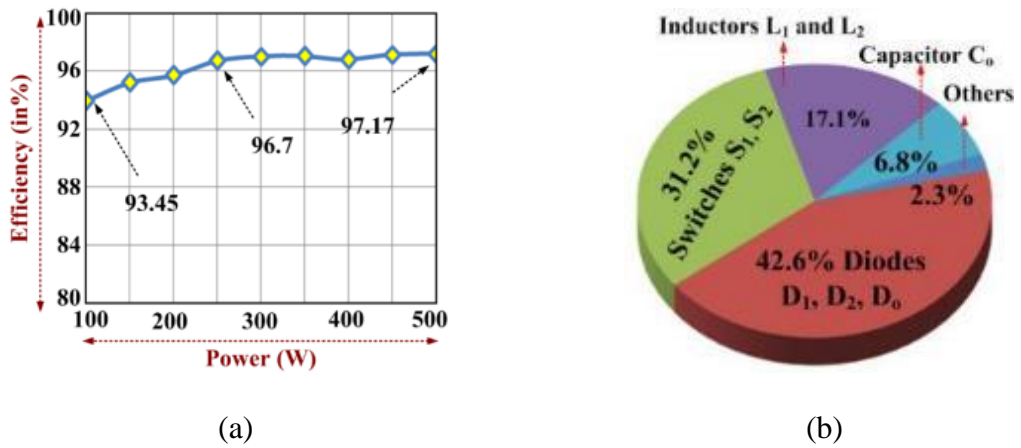
Figure 3.17. Experimental test plots. (a) Efficiency versus power. (b) Loss distribution at 500 W.

<center>3.12 Comparison of different topologies</center>

Recently numerous converters are proposed to achieve high output voltage with additional boosting techniques. In this section, the proposed converter is compared with recently suggested converters whose voltage gain is equal to the proposed converter. The detailed comparison in terms of number of components, voltage and current stresses, efficiency, etc., is shown in Table 3.2.

The total number of components required for the classical SIBC [see Fig. 3.1(a)] [122] and suggested converters in [148] and [47] are 8, 6, and 8, respectively. It is observed that the total requirement of components for the proposed mSIBC is the same

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as SIBC and suggested converter in [47]. In converters presented in [148] and [47], input and outputs are not at common ground, thus these converters are suitable only for floating loads. The efficiency of the converters is dependent on several factors, e.g., total number of components, voltage and current ratings, and their types. The plot of normalized voltage stress across switches and diodes is shown in Fig. 3.18(a) and (b), respectively. In Fig. 3.18(a) and (b), converters are also compared in terms of total voltage stress across switches and diodes, respectively. The total voltage stress across semiconductor devices ($\Sigma T_{SV}$) is the sum of total voltage stresses across diode and switches, the total current stress for semiconductor devices ($\Sigma T_{SC}$) is the sum of total current stresses of diode and switches. The comparison plot of total voltage and current stress for converters is shown in Fig. 3.18(c) and (d), respectively. The relation between total voltage and current stress for converters is as follows:

$$\underbrace{V_i \ 3M + 3}_{Con.[47]} > \underbrace{3V_i M}_{SI} > \underbrace{\frac{V_i}{2} \ 5M + 1}_{Proposed} > \underbrace{2V_i \ M + 1}_{Con.[148]} \tag{3.83}$$

$$\underbrace{4I_o M}_{SI} = \underbrace{4I_o M}_{Con.[47]} = \underbrace{4I_o M}_{Proposed} > \underbrace{2I_o M}_{Con.[148]} \tag{3.84}$$

Notably, the cost of the components is increasing in a parabolic way with components ratings, i.e., high rating, higher cost, and high ON-state resistance The total voltage and current stress per components is calculated as follows:

$$\underbrace{\frac{2V_i}{3} \ M + 1}_{Con.[148]} > \underbrace{\frac{3V_i}{5} \ M + 1}_{Con.[47]} > \underbrace{\frac{3V_i}{5} M}_{SI} > \underbrace{\frac{V_i}{2} \ M + \frac{1}{5}}_{Proposed} \tag{3.85}$$

$$\underbrace{2I_o M / 3}_{Con.[148]} > \underbrace{4I_o M / 5}_{SI} = \underbrace{4I_o M / 5}_{Con.[47]} = \underbrace{4I_o M / 5}_{Proposed} \tag{3.86}$$

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The comparison plots of total voltage and current stress per semiconductor devices of converters are shown in Fig. 3.18(c) and (d), respectively.
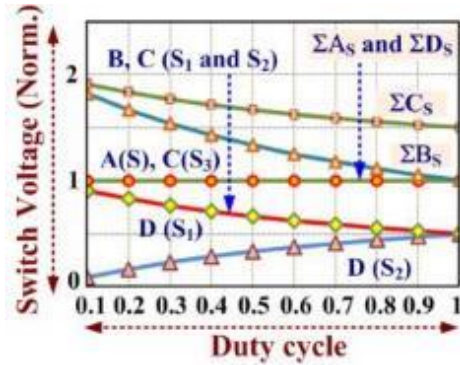


(a)
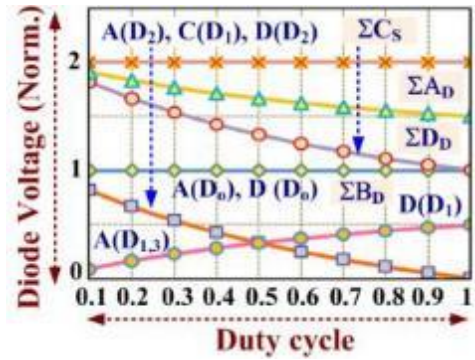
(b)
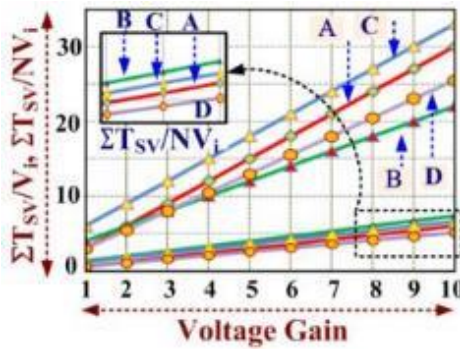
(c)
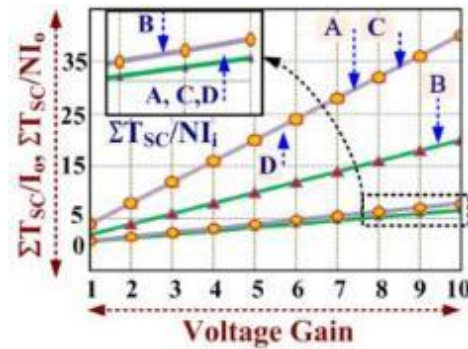
(d)

Figure 3.18. Comparison, (a) Switch voltages versus duty cycle, (b) Diode voltages versus duty cycle, (c) $\Sigma T_{SV}/V_i, \Sigma T_{SV}/NV_i$ versus voltage gain (d) $\Sigma T_{SC}/I_o, \Sigma T_{SC}/NI_o$ versus voltage gain. Note: A represents SIBC [122], B represents converter [148], C represents converter [47], D represents proposed converter. (In general X(Z) mean voltage stress across Z of converter X, and $\Sigma X_S, \Sigma X_D$ are total voltage stress across switches and diodes for converter X).

Table 3.2. Comparison of Converters (Note: $M$ = voltage gain, $a = M\text{-}1$, $b = M\text{+}1$, $P = 1\text{-}D_1\text{-}D_2$.)

| Converter | SIBC [122] | Converter in [148] | Converter in [47] | Proposed Converter ($D$) |
|---|---|---|---|---|
| C/I/D/S/T | 1/2/4/1/8 | 1/2/1/2/6 | 1/2/2/3/8 | 1/2/3/2/8 |
| Load Type | Grounded | Floating | Floating | Grounded |
| Voltage Gain (M) | $\dfrac{1+D}{1-D}$ | $\dfrac{1+D}{1-D}$ | $\dfrac{1+D_1}{1-D_1-D_2}$ | $\dfrac{1+D}{1-D}$ |

Switch Voltage

RMS

$$V_o\sqrt{\dfrac{2}{b}}$$

$$V_{S1,2} = \dfrac{V_o\sqrt{2b}}{2(b-1)}$$

$$V_{S1,2} = \dfrac{V_o\left(\sqrt{D_2}-b\sqrt{1-D_1-D_2}\right)}{2(b-1)}$$
$$V_{S3} = \dfrac{V_o\left(\sqrt{D_1}-M\sqrt{1-D_1-D_2}\right)}{2M}$$

$$V_{S1} = V_o\,\dfrac{a}{2M}\sqrt{2/b}$$
$$V_{S2} = \dfrac{V_o}{2M}\sqrt{2b}$$

Peak

$$V_o$$

$$V_{S1,2} = \dfrac{b}{2M}V_o$$

$$V_{S1,2} = \dfrac{V_o b}{2M},$$
$$V_{S3} = V_o$$

$$V_{S1} = \dfrac{V_o a}{2M},$$
$$V_{S2} = \dfrac{V_o b}{2M}$$

Avg.

$$\dfrac{2V_o}{M+1}$$

$$V_{S1,2} = \dfrac{V_o}{M}$$

$$V_{S1,2} = \dfrac{V_o\left(b(1-D_1)-MD_2\right)}{2M}$$
$$V_{S3} = \dfrac{V_o\left(1-bD_1-MD_2\right)}{2M}$$

$$V_{S1} = \dfrac{V_o a}{Mb},$$
$$S_2 = \dfrac{V_o}{M}$$

| Converter | SIBC [122] | Converter in [148] | Converter in [47] | Proposed Converter ($D$) |
|---|---|---|---|---|
| **Diode Voltage** RMS | $V_{D1,3} = \dfrac{aV_o}{2M}\sqrt{2/b},$ $V_{D2} = \dfrac{V_o}{M}\sqrt{2/a},$ $V_{Do} = V_o\sqrt{a/b}$ | $V_o\dfrac{\sqrt{aM+1}}{M}$ | $V_o\left(\dfrac{\left(b\sqrt{D_2}\right)}{M} + \sqrt{1-D_1-D_2}\right)$ | $V_{D1,2} = \dfrac{a}{2M}\sqrt{\dfrac{2}{b}}V_o,$ $V_{Do} = \sqrt{\dfrac{a}{b}}V_o$ |
| Peak | $V_{D1,3} = \dfrac{aV_o}{2M},$ $V_{D2} = \dfrac{V_o}{M},$ $V_{Do} = V_o$ | $V_o b/M$ | $V_o$ | $V_{D1,2} = aV_o/2M,$ $V_{Do} = V_o$ |
| Avg. | $V_{D1-3} = aV_o/Mb,$ $V_{Do} = aV_o/b$ | $V_o a/M$ | $V_o(M-MD_1+D_2)/M$ | $V_{D1,2} = aV_o/2M,$ $V_{Do} = aV_o/b$ |

| Converter | | SIBC [122] | Converter in [148] | Converter in [47] | Proposed Converter ($D$) |
|---|---|---|---|---|---|
| Inductor Current | RMS | $\sqrt{\dfrac{b^2}{4M^2}I_i^2+\dfrac{1}{12}\left(\dfrac{V_iD}{Lf}\right)^2}$ | $\sqrt{\dfrac{b^2}{4M^2}I_i^2+\dfrac{1}{12}\left(\dfrac{V_iD}{Lf}\right)^2}$ | $\sqrt{\dfrac{b^2}{4M^2}I_i^2+\dfrac{1}{48}\left(\dfrac{V_i(2D_1+D_2)}{Lf}\right)^2}$ | $\sqrt{\dfrac{b^2}{4M^2}I_i^2+\dfrac{1}{12}\left(\dfrac{V_iD}{Lf}\right)^2}$ |
| | Peak | $\dfrac{bI_i}{2M}+\dfrac{aV_i}{2Lfb}$ | $\dfrac{bI_i}{2M}+\dfrac{aV_i}{2Lfb}$ | $\dfrac{aI_i}{2M}+\dfrac{V_i(2D_1+D_2)}{4Lf}$ | $\dfrac{bI_i}{2M}+\dfrac{aV_i}{2Lfb}$ |
| | Avg. | $I_ib\,/\,2M$ | $I_ib\,/\,2M$ | $I_ib\,/\,2M$ | $I_ib\,/\,2M$ |
| Switch Current | RMS | $\sqrt{\left(\dfrac{a}{b}\right)^3 I_i^2+\dfrac{1}{12}\left(\dfrac{a}{b}\right)^3\left(\dfrac{V_i}{Lf}\right)^2}$ | $I_{S1,2}=\sqrt{\left(\dfrac{a}{b}\right)^3\dfrac{I_i^2}{4}+\left(\dfrac{a}{b}\right)^3\left(\dfrac{V_i}{2\sqrt{3}Lf}\right)^2}$ | $I_{S1,2}=\sqrt{\left(\dfrac{a}{b}\right)^3\left[\dfrac{I_i^2}{4}+\dfrac{1}{12}\left(\dfrac{V_i}{Lf}\right)^2\right]}$ <br> $I_{S3}=\sqrt{D_2^3\left(I_i^2+\dfrac{1}{48}\left(\dfrac{V_i}{4Lf}\right)^2\right)}$ | $I_{S1}=\sqrt{\left(\dfrac{a}{b}\right)^3\left(\dfrac{I_i^2}{4}+\dfrac{1}{12}\left(\dfrac{V_i}{Lf}\right)^2\right)}$ <br> $I_{S2}=\sqrt{\left(\dfrac{a}{b}\right)^3\left(I_i^2+\dfrac{1}{12}\left(\dfrac{V_i}{Lf}\right)^2\right)}$ |
| | Peak | $\dfrac{a}{b}\left(I_i+\dfrac{V_i}{2Lf}\right)$ | $I_{S1,2}=\dfrac{a}{b}\left(\dfrac{I_i}{2}+\dfrac{V_i}{2Lf}\right)$ | $I_{S1,2}=\dfrac{I_iD_1}{2}+\dfrac{V_iD_1}{2Lf},$ <br> $I_{S3}=I_iD_2+\dfrac{V_iD_2}{4Lf}$ | $I_{S1}=\dfrac{I_iD}{2}+\dfrac{V_iD}{2Lf},$ <br> $I_{S2}=I_iD+\dfrac{V_iD}{2Lf}$ |
| | Avg. | $I_ia\,/\,b$ | $I_{S1,2}=I_ia\,/\,2b$ | $I_{S1,2}=I_iD_1\,/\,2,$ <br> $I_{S3}=I_iD_2$ | $I_{S2}=I_ia\,/\,b,$ <br> $I_{S1}=I_ia\,/\,2b$ |

| Converter | SIBC [122] | Converter in [148] | Converter in [47] | Proposed Converter ($D$) |
|---|---|---|---|---|
| **Diodes Current** — RMS | $I_{D1,3} = \dfrac{a}{b}\sqrt{\dfrac{a}{b}\left(\dfrac{I_i^2}{4}+\left(\dfrac{V_i}{2\sqrt{3}Lf}\right)^2\right)}$ $I_{D2,o} = \dfrac{1}{b}\sqrt{\dfrac{8}{b}I_i^2+\dfrac{1}{24M}\left(\dfrac{V_o a}{Lf}\right)^2}$ | $\sqrt{\dfrac{b}{2M}I_i+\dfrac{1}{12}\left(\dfrac{V_i D}{Lf}\right)^2}$ | $\sqrt{I_i^2\left(p\right)^3+\left(\dfrac{(V_i-V_o)p}{4\sqrt{3}Lf}\right)^2}$ | $I_{D1} = \dfrac{a}{b}\sqrt{\dfrac{a}{b}\left(\dfrac{I_i^2}{4}+\left(\dfrac{V_i}{2\sqrt{3}Lf}\right)^2\right)}$ $I_{D2,o} = \dfrac{1}{b}\sqrt{\dfrac{8}{b}I_i^2+\dfrac{1}{24M}\left(\dfrac{V_o a}{Lf}\right)^2}$ |
| Peak | $I_{D1,3} = \dfrac{aI_i}{2b}+\dfrac{V_i a}{2bLf},$ $I_{D2,o} = \dfrac{2I_i}{b}+\dfrac{(V_i-V_o)a}{4Lfb}$ | $\dfrac{bI_i}{2M}+\dfrac{aV_i}{2Lfb}$ | $I_i p+\dfrac{(V_i-V_o)p}{4Lf}$ | $I_{D1} = \dfrac{I_i a}{2b}+\dfrac{V_i a}{2Lbf},$ $I_{D2,o} = \dfrac{2I_i}{b}+\dfrac{(V_i-V_o)a}{4Lfb}$ |
| Avg. | $I_{D1,3} = I_i a/2b,$ $I_{D2,o} = I_i/2b$ | $2I_i/b$ | $I_i P$ | $I_{D1} = I_i a/2b,$ $I_{D2,o} = I_i/2b$ |
| Efficiency | 95.2% | 92.7% | 93.1% | 97.1% |

Based on the relations (3.85) and (3.86), on an average, the proposed converter required lower rating components, and hence, the total cost of the converter is less than classical SIBC and converters presented in [148] and [47]. The proposed mSIBC configuration is transformer-less and simply derived by replacing one diode of the SI network of classical SIBC with an active switch. As a result, the total output voltage is distributed among the two active switches. Therefore, low-voltage rating switches can be employed to design the power circuit of the proposed mSIBC configuration. In general, the ON-state resistance of any devices increases with their ratings. It is analyzed that the proposed converter required lower rating components. The efficiencies of the classical SIBC and suggested converter in [148], and [47] are 95.2%, 92.7%, and 93.1%, respectively, and the proposed converter efficiency is 97.17%. Therefore, the proposed converter provides higher efficiency compared with SI converter and converters presented in [148] and [47]. The total switching losses of classical SIBC [see Fig. 3.1(a)] and proposed mSIBC [see Fig. 3.1(b)] are obtained as follows:

$$P_{Sw}{}^{SIBC} = \left( E_S + E_{D1} + E_{D2} + E_{D3} + E_{Do} \right) f_s \tag{3.87}$$

$$P_{Sw}{}^{mSIBC} = \left( E_{S1} + E_{S2} + E_{D1} + E_{D2} + E_{Do} \right) f_s \tag{3.88}$$

Where $E$ is energy loss during switching, and its subscript defines the components. The difference between switching losses of the proposed mSIBC and classical SIBC is obtained as follows:

$$P_{Sw}{}^{mSIBC} - P_{Sw}{}^{SIBC} = \begin{pmatrix} E_{on,S1} + E_{off,S1} + \\ E_{on,S2} + E_{off,S2} \end{pmatrix} f_s - \begin{pmatrix} E_{on,S} + E_{off,S} + \\ E_{on,D3} + E_{off,D3} \end{pmatrix} f_s \tag{3.89}$$

Where $E_{on}$ and $E_{off}$ define the turn ON and OFF energy losses, respectively. By solving (3.89)

$$P_{Sw}{}^{mSIBC} - P_{Sw}{}^{SIBC} = \left( \begin{array}{c} V_{S1}I_{S1} + V_{S2}I_{S2} \\ -V_S I_S \end{array} \right) \left( t_r + t_f \right) f_S - E_{D3} f_S \qquad (3.90)$$

Where $t_r$ and $t_f$ are rise time and fall time, respectively. Using (3.90), the final difference in the switching losses is obtained as

$$P_{Sw}{}^{mSIBC} - P_{Sw}{}^{SIBC} = -\frac{M+1}{4M} V_o I_i D \left( t_r + t_f \right) f_S - E_{D3} f_s < 0 \qquad (3.91)$$

The solution of (3.91) is always negative. Therefore, it can be concluded that the switching losses in mSIBC are lesser than classical SIBC. It is also notable that the proposed converter switches are simultaneously turned ON and OFF and arranged in half-bridge structure, as a result, a single half-bride driver module is suitable to drive switches. Hence, no additional driver is required to control switches of the proposed converter. It is observed that the mSIBC provides a viable solution to achieve given voltage gain with reduced voltage stress, low cost, and higher efficiency.

## 3.13 Summary

In this chapter, the mSIBC with reduced voltage stress across switches was presented. The voltage gain of the mSIBC is higher than the classical boost converter and equal to the classical SI boost converter. Compared with the classical SIBC, the proposed converter requires lesser number of diodes and voltage stress across switches is low compared with the output voltage. Therefore, the requirement of high-voltage rating active switches is eliminated. Furthermore, the cost of the converter can be reduced due to the utilization of lower rating active switches and the elimination of one diode. The detailed CCM and DCM operating principle, voltage gain, boundary conditions, and effect of non-idealities were discussed. The proposed converter was compared with a similar converter and found that the proposed converter provides a viable solution to achieve higher voltage gain with low-voltage rating switches. The

experimental results were presented, which validated the theoretical analysis and functionality, and the efficiency of the designed converter was 97.17%.

# CHAPTER 4: TRANSFORMER-LESS BOOST CONVERTER (TBC) WITH REDUCED VOLTAGE STRESS

## 4.1 Introduction

In this chapter, a new Transformer-less Boost Converter (TBC) is presented which is proposed to achieve high step-up voltage with a reduced voltage across switches. The proposed topology has the advantage of providing a high voltage gain, the low voltage stress on the active switches, simplified control, and high efficiency. The structure is derived by modifying the classical Switched Inductor Boost Converter (SIBC) by replacing two of the diodes with a capacitor and a control switch, which results in a total output voltage equally shared by the two switches. Thus, the proposed converter needs a lesser number of diodes than the conventional SIBC, where the two active switches equally share the total output voltage and thereby reducing the voltage stress across the switches to half. Hence, low voltage rating switches can be used to design the proposed TBC structure. Also, a higher voltage gain is achieved using TBC without increasing the number of components of the existing SIBC. Furthermore, the proposed converter provides the common ground connection of source and load. The detailed analysis, effect of non-idealities, design, and comparison are presented. The experimental results of the proposed TBC are presented to validate its functionality and theoretical analysis.

## 4.2 Power Circuit Topology

A higher voltage conversion ratio than the conventional boost converter can be obtained by using the classical SIBC [152], in which additional switched inductor circuitry is incorporated. However, the voltage stress across the switches is significantly increased with a voltage gain, which in turn leads to developing the total output voltage across the switch. In transformer-less active switched inductor converter [122], two

switches are employed and the voltage stress across switches is reduced. However, the converter is suitable only for floating loads. To overcome these drawbacks Transformer-less Boost Converter (TBC) is proposed and the circuitry is shown in Fig. 4.1. In proposed TBC, voltage stress across the switches is reduced and higher voltage gain is achieved. The circuitry is derived by modifying the power circuitry of the classical SIBC without increasing the number of components. The circuitry of proposed TBC comprises of two control switches $S_a$ and $S_b$, two diodes $D_a$ and $D_b$, two inductors $L_a$ and $L_b$ with equal inductance rating ($L$), two capacitors $C_a$ and $C_b$, and load $R$. The intermediate diodes of the classical SIBC are replaced by capacitor and control switch. The proposed TBC follows the principle of parallel charging of reactive components and series discharging of reactive components. Therefore, in ON state, two inductors and a capacitor are charged in parallel; and in OFF state, discharged in series to charge the load side capacitor and to provide energy to load.
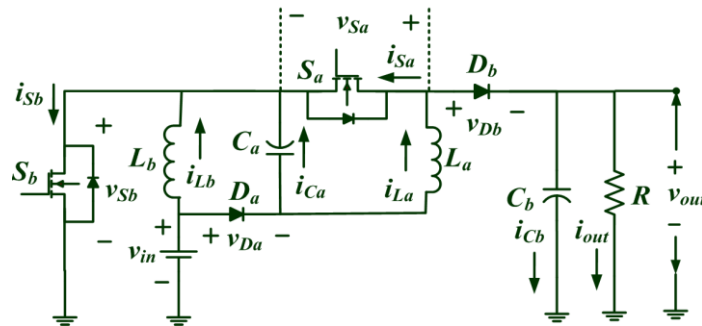


Figure 4.1. The Power circuit of the proposed Transformer-less Boost Converter (TBC).

In proposed TBC, the total output voltage is equally shared by the two active switches and hence reducing the voltage stress across the switches to half. Therefore, the power circuitry of the proposed TBC can be designed by using switches with a low voltage rating. It is important to note that the total number of components in TBC is the same as the classical SIBC converter and a higher voltage gain is achieved. For the proposed circuit,

$$L = L_a = L_b \tag{4.1}$$

To study Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) characteristics, all the circuit components are considered to be ideal by neglecting the voltage drop across semiconductor devices or inductors due to internal resistance and having a capacitor that is too large to produce a constant voltage. Fig. 4.2(a)-(b) shows the typical TBC characteristics waveforms for CCM and DCM modes, respectively; where time $t_o$ to $t_A$ is the time period for mode I (i.e. ON time).
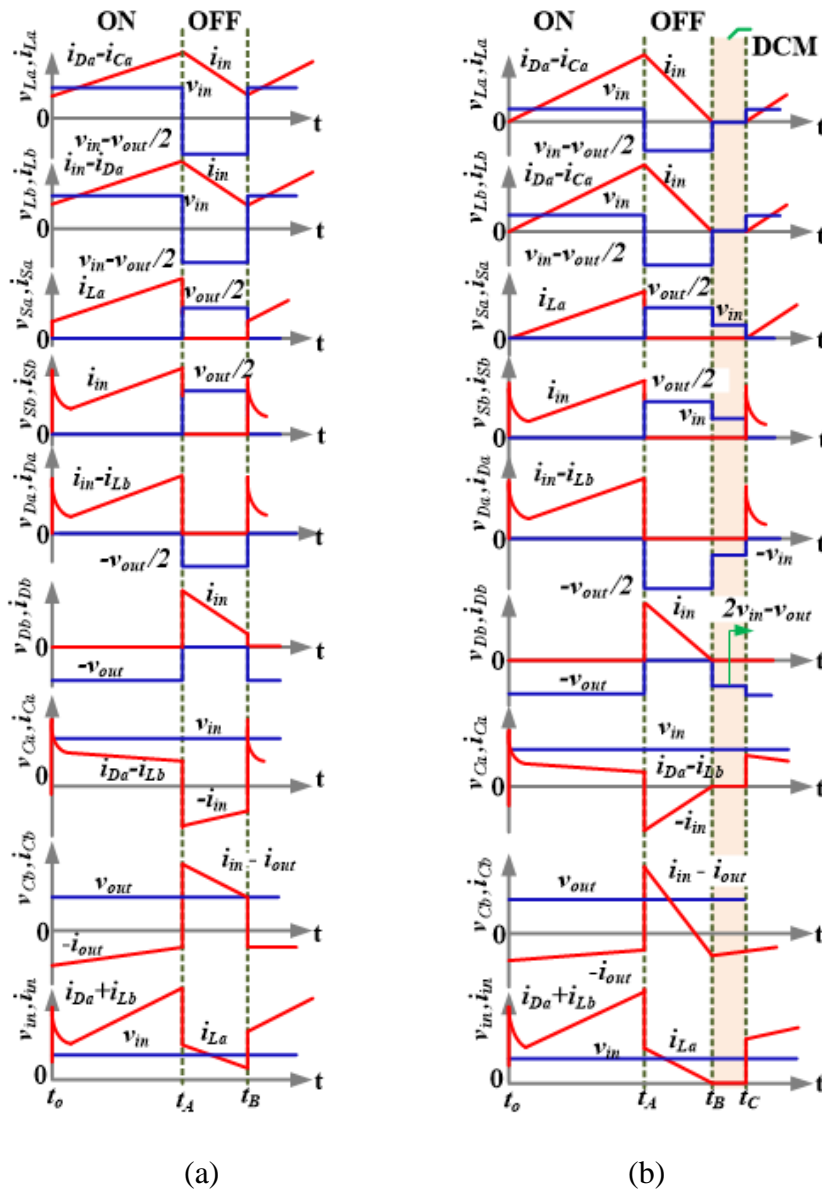


Figure 4.2. Characteristics waveform of proposed TBC (a) CCM, (b) DCM.

4.3 Working Principle and Analysis in CCM

The CCM operation of the proposed TBC is split into two modes; first when both the switches $S_a$ and $S_b$ are in ON state and second when both the switches $S_a$ and $S_b$ are in OFF state.

*1) Mode I (Time $t_o$-$t_A$):* Fig. 4.3(a) shows the equivalent circuit of TBC for mode I. In this mode, inductor $L_b$ is charged by input supply ($V_{in}$) through switch $S_b$, inductor $L_a$ is charged by input supply ($V_{in}$) through diode $D_a$ and switches $S_a$ and $S_b$, capacitor $C_a$ is charged by input supply ($V_{in}$) through diodes $D_a$ and switch $S_b$. It is worth to mention that the inductors $L_a$ and $L_b$, and capacitor $C_a$ are charged in parallel and the capacitor $C_b$ is discharged through the load $R$. During this mode, diodes $D_a$ and $D_b$ are forward and reverse biased, respectively. The voltages across and currents through inductors and capacitors can be expressed as,

Table 4.1 briefly summarizes the Operating Principle in both CCM and DCM (*Ch.: Chraged, D/Ch.: Discharged, ZC: Zero current, FB: Forward Biased, RB: Reversed Biased).

Table 4.1. Operating Principle in CCM and DCM

| Operating Modes | | Time | Switches | | Inductors | | Capacitors | | Diodes | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $S_a$ | $S_b$ | $L_a$ | $L_b$ | $C_a$ | $C_b$ | $D_a$ | $D_b$ |
| CCM | Mode I | $T_{ON}$ ($t_0$–$t_A$) | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | FB | RB |
| | Mode II | $T_{OFF}$ ($t_A$–$t_B$) | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | RB | FB |
| DCM | Mode I | $d_1T$ ($t_0$–$t_A$) | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | FB | RB |
| | Mode II | $d_2T$ ($t_A$–$t_B$) | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | RB | FB |
| | Mode III | $d_3T$ ($t_B$–$t_C$) | OFF | OFF | ZC | ZC | ZC | D/Ch. | RB | RB |

$$v_L{}^I = v_{La}{}^I = v_{Lb}{}^I \approx V_{in}, \; V_{Cb}{}^I \approx V_{out} \tag{4.2}$$

$$i_{in}{}^I = i_{La}{}^I + i_{Lb}{}^I + i_{Ca}{}^I, \; i_{Cb}{}^I = -i_{out} \approx -\frac{V_{out}}{R} \tag{4.3}$$

Where superscript represents the mode I and subscript represent the component.

*2) Mode II (Time $t_A$-$t_B$):* Fig. 4.3(b) shows the equivalent circuit of TBC for mode II. In this mode, both the inductors $L_a$, $L_b$, and the capacitor $C_a$ are discharged in series with the input voltage $V_{in}$; energy is supplied to the load $R$ and capacitor $C_b$ through the diode $D_b$. In this mode, diodes $D_a$ and $D_b$ are reversed and forward biased, respectively. The voltages across and currents through inductors and capacitors can be expressed as,

$$v_L{}^{II} = v_{La}{}^{II} = v_{Lb}{}^{II} \approx V_{in} - \frac{V_{out}}{2}, \; V_{Cb}{}^{II} \approx V_{out} \tag{4.4}$$

$$i_L{}^{II} = i_{La}{}^{II} = i_{Lb}{}^{II} = i_{in}{}^{II}, i_{Cb}{}^{II} \approx i_L{}^{II} - \frac{V_{out}}{R} \tag{4.5}$$

Where superscript represents the mode II and subscript represents the component. Using inductor volt second balance principle, the voltage gain of TBC is expressed as,

$$V_G\big|_{CCM} = \frac{V_{out}}{V_{in}} = \frac{2}{1-d} \tag{4.6}$$

Where the voltage gain and duty cycle is represented by $V_G$, and $d$, respectively. Equation (4.6) validates that the voltage gain of TBC is higher than the classical SIBC and transformer-less active switched inductor converter.

(a)                                          (b)
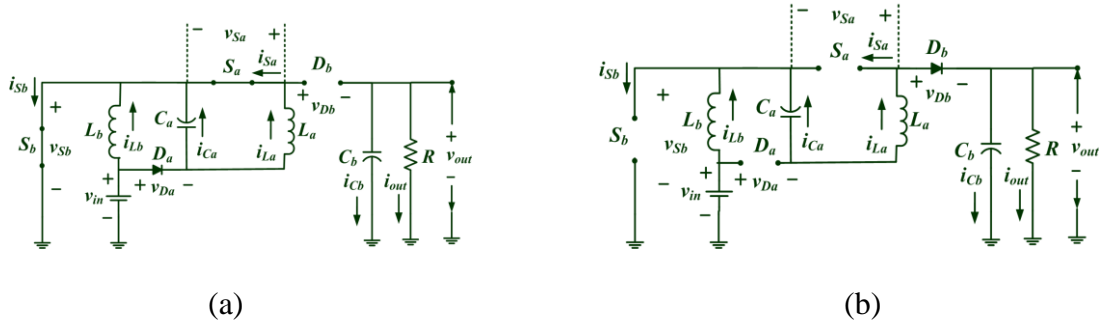
Figure 4.3. Equivalent power circuitry, (a) Mode I ($t_0$-$t_A$), (b) Mode II ($t_A$-$t_B$).

## 4.4 Effect of Unequal Inductances on Voltage Gain in CCM

The operation of the proposed converter depends on the values of the inductors $L_a$ and $L_b$. Hence, the currents through inductors $L_a$ and $L_b$ depend on the values of $L_a$ and $L_b$. The characteristics waveform of the inductors $L_a$ and $L_b$ currents are shown in Fig. 4.4(a) below. In this case, the converter operates in three modes as follows,

*1) Mode I (time $t_0$ to $t_A$):* In this mode, switches $S_a$ and $S_b$ are turned ON and equivalent circuitry is the same as mode I of CCM. The input current $i_{in}$ is the sum of inductor currents and the current through the capacitor $C_a$ i.e. $i_{in}=i_{La}+i_{Lb}+i_{Ca}$. The slope of the inductors $L_a$ and $L_b$ currents can be obtained as follows,

$$\frac{d\ i_{La}}{dt} \approx \frac{v_{in}}{L_a}, \frac{d\ i_{Lb}}{dt} \approx \frac{v_{in}}{L_b} \tag{4.7}$$

In this mode, the current through inductor $L_b$ is larger than the current through inductor $L_a$ since $L_b<L_a$.

*2) Mode II (time $t_A$ to $t_B$):* This mode occurs for a small-time duration ($yT_s$ as shown in Fig. 4.4(a)) when switches $S_a$ and $S_b$ are just turned OFF. The equivalent circuitry is shown in Fig. 4.4(b), where diode $D_a$ is forward biased. During this mode, the current through inductor $L_a$ increases with a positive slope and the current through inductor $L_b$ decreases with a large negative slope. The value of current through inductor $L_b$ is larger than the current through inductor $L_a$. Also, the input current $i_{in}$ is equal to

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inductor $L_b$ current i.e. $i_{in}=i_{Lb}$ and the resultant current through diode $D_a$ is the subtraction of inductors $L_b$ and $L_a$ currents i.e. $i_{Lb}-i_{La}$. The slope of the inductors $L_a$ and $L_b$ currents are obtained as follows,

$$\frac{d\ i_{La}}{dt} \approx \frac{v_{Ca}}{La} \approx \frac{v_{in}}{La}, \frac{d\ i_{Lb}}{dt} \approx \frac{v_{in}-v_{out}}{Lb} \tag{4.8}$$

This mode ends as soon as the currents through inductor $L_a$ and $L_b$ are equal, and circuitry operates in mode III.
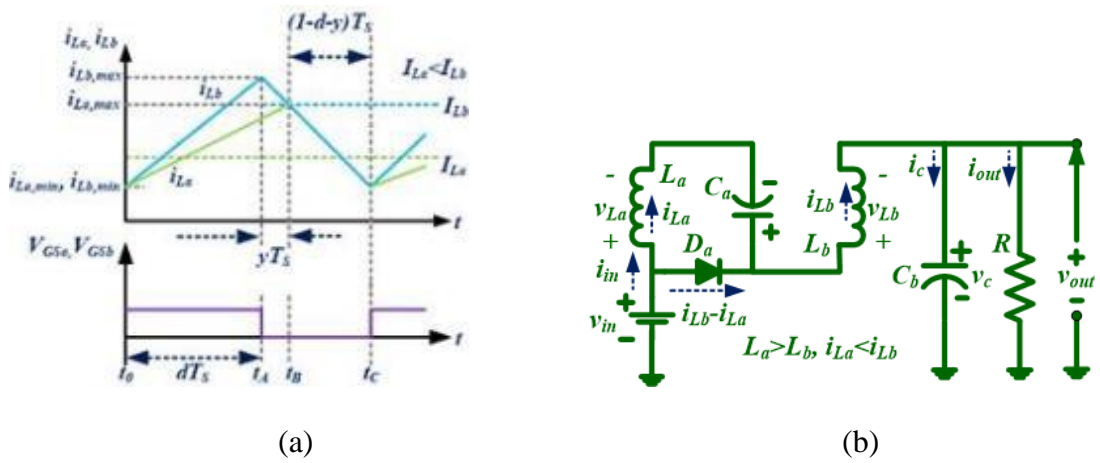


Figure 4.4. When $L_a > L_b$ (a) inductor currents, and (b) Mode II.

*3) Mode III (time $t_B$ to $t_C$):* In this mode, switches $S_a$ and $S_b$ are turned OFF and equivalent circuitry is the same as CCM mode II. In this case, input current and the current through inductor $L_b$ and $L_a$ are equal i.e. $i_{in}=i_{La}=i_{Lb}$. The voltage across inductor $L_a$ and $L_b$ can be obtained as follows,

$$\frac{d\ i_{La}}{dt} = \frac{2v_{in}-v_{out}}{L_a+L_b}, \frac{d\ i_{Lb}}{dt} = \frac{2v_{in}-v_{out}}{L_a+L_b} \tag{4.9}$$

Using small approximation and inductor volt second balance,

$$For\ La \Rightarrow v_{in}(d) + v_{in}(y) + \frac{2v_{in}-v_{out}}{La+Lb} La(1-d-y) = 0 \tag{4.10}$$

$$For\ L_b \Rightarrow v_{in}(d) + \ v_{in} - v_{out}\ \ y + \frac{2v_{in}-v_{out}}{L_a+L_b} Lb(1-d-y) = 0 \tag{4.11}$$

Solving (4.10)-(4.11), the voltage gain of TBC is obtained as,

$$v_{out}/v_{in}\big|_{L_a>Lb} = 2/\ 1-d \qquad (4.12)$$

Similarly, one can easily understand the modes of the converter when inductance $L_a$ is smaller than the value of inductance $L_b$ and the voltage gain can be obtained as,

$$v_{out}/v_{in}\big|_{L_a<Lb} = 2/\ 1-d \qquad (4.13)$$

Therefore, in the case of unequal inductances, the inductor average current is changed. However, voltage gain is still the same i.e. $2/(1-d)$.

### 4.5 Working and Analysis in DCM

The DCM operation of the proposed TBC is split into three modes; first when switches $S_a$ and $S_b$ are in ON state, second when switches $S_a$ and $S_b$ are in OFF state with non-zero inductor currents, and third when switches $S_a$ and $S_b$ are in OFF state with zero inductor currents. Let's consider that, at time $t_B$ the inductor current reaches to zero value as indicated in Fig. 4.2(b). In a particular DCM characteristics (Fig. 4.2(b)), $d_1T$ is mode I time period (i.e. time $t_o$-$t_A$), $d_2T$ (i.e. time $t_A$-$t_B$) is mode II time period, and $d_3T$ (i.e. time $t_B$-$t_C$) is mode III time period.

*1) Mode I (Time $t_o$-$t_A$):* The working of TBC and its equivalent circuit in this mode is the same as mode I of CCM. Consequently, during this mode, inductors $L_a$ and $L_b$ and the capacitor $C_a$ are charged in parallel by the input voltage $V_{in}$. At the beginning of this mode (at the time $t_o$ or $t_o$+$T$), the current through both the inductors $L_a$ and $L_b$ started from level zero and reached to the level of maximum current in the end. The maximum current through inductors $L_a$ and $L_b$, and the capacitor $C_a$ can be expressed as,

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$$I_{L,\max}{}^{I} = I_{La,\max}{}^{I} = I_{Lb,\max}{}^{I} = \frac{1}{L}\, V_{in}d_1T \tag{4.14}$$

The maximum currents through the inductors $L_a$ and $L_b$ in mode I are $I_{La,max}{}^{I}$ and $I_{Lb,max}{}^{I}$, respectively, where superscript denotes the mode I. The current ripples through the inductors $L_a$ and $L_b$ can be expressed as,

$$\Delta I_{L} = \Delta I_{La} = \Delta I_{Lb} = \frac{1}{L}\, V_i d_1T \tag{4.15}$$

Where, the current ripples through the inductors $L_a$ and $L_b$ are $\Delta I_{La}$ and $\Delta I_{Lb}$, respectively.

*2) Mode II (Time $t_A$-$t_B$):* During this mode, the working of TBC and its equivalent circuit is the same as mode II of CCM. Consequently, during this mode, inductors $L_a$ and $L_b$, and the capacitor $C_a$ are discharged in series with input voltage $V_{in}$ to provide energy to capacitor $C_b$ and load $R$. In the beginning of this mode (at time $t_A$ or $t_A+T$), the current through both the inductors $L_a$ and $L_b$ started from the level of maximum current and reached to level zero in the end (at time $t_B$ or $t_B+T$). Another expression for maximum current through inductors $L_a$ and $L_b$ can be obtained as,

$$I_{L,\max}{}^{II} = I_{La,\max}{}^{II} = I_{Lb,\max}{}^{II} = \frac{V_{out}d_2T}{2L} - \frac{V_{in}d_2T}{L} \tag{4.16}$$

The maximum currents through the inductors $L_a$ and $L_b$ in mode II are $I_{La,max}{}^{II}$ and $I_{Lb,max}{}^{II}$, respectively, where superscript denotes the mode II. The current ripples through the inductors $L_a$ and $L_b$ can be expressed as,

$$\Delta I_{L} = \Delta I_{La} = \Delta I_{Lb} = \frac{V_{out}d_2T}{2L} - \frac{V_{in}d_2T}{L} \tag{4.17}$$

*3) Mode III (Time $t_B$-$t_C$):* Fig. 4.5 shows the equivalent circuit for this mode. During this mode, switches $S_a$ and $S_b$ are turned OFF, and currents through inductors

$L_a$ and $L_b$ and capacitor $C_a$ are zero. Consequently, the energies in the inductors $L_a$ and $L_b$ are zero. Throughout this mode, both the diodes $D_a$ and $D_b$ are reversed biased and capacitor $C_b$ is discharged through load $R$. The time period of mode II i.e. $d_2T$ i.e. time $t_A$-$t_B$ can be expressed as follows by using the equations (4.8) and (4.10),

$$d_2T = 2d_1 \times \frac{V_{in}T}{V_{out}-2V_{in}} \Rightarrow d_2 = 2d_1 \times \frac{V_{in}}{V_{out}-2V_{in}} \qquad (4.18)$$
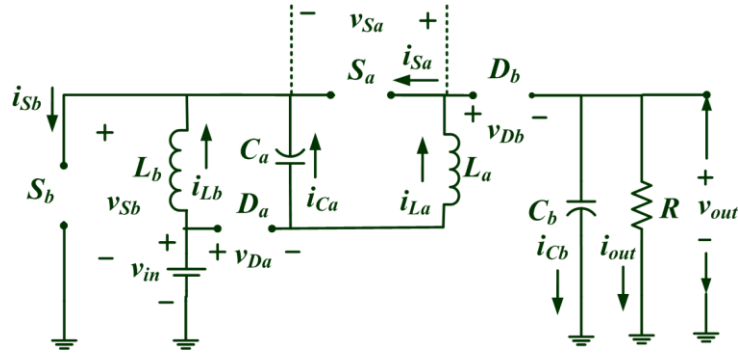


Figure 4.5. DCM Equivalent power circuitry ($t_B$-$t_C$).

It is well known that,

$$d_1 + d_2 + d_3 = 1 \qquad (4.19)$$

The time period for mode III can be expressed as follows by using (4.11) and (4.12),

$$d_3T = T\left(1-\frac{V_{out}d_1}{V_{out}-2V_{in}}\right) = \frac{T\left[V_{out}\ 1-d_1\ -2V_{in}\right]}{V_{out}-2V_{in}} \qquad (4.20)$$

With the use of geometry in Fig. 4.2(b) on the current waveform of the capacitor $C_b$, the average current through capacitor $C_b$ can be expressed as,

$$I_{Cb} = \frac{I_{L,\max}\times d_2}{2} - I_{out} = \frac{I_{L,\max}\times d_2}{2} - \frac{V_{out}}{R} \qquad (4.21)$$

Using equations (4.14), (4.20), and (4.21),

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$$I_{Cb} = \frac{V_{in}^2 d_1^2 T}{L\ V_{out} - 2V_{in}} - \frac{V_{out}}{R} \tag{4.22}$$

Since any capacitor average current is always zero under steady-state condition, equation (4.22) can now be expressed as,

$$\frac{V_{in}^2 d_1^2 T}{L\ V_{out} - 2V_{in}} = \frac{V_{out}}{R} \tag{4.23}$$

Using (4.23),

$$\left(\frac{V_{out}}{V_{in}}\right)^2 - \frac{2V_{out}}{V_{in}} - \frac{d_1^2}{\delta_L} = 0 \tag{4.24}$$

The normalized time constant for inductors $L_a$ and $L_b$ is $\delta_L$, which is equal to $L/TR$. Therefore, $\delta_L$ varies with the variation in the values of $L$, $T$, and $R$. The voltage gain of TBC in DCM ($V_G|_{DCM}$) can be obtained as,

$$V_G|_{DCM} = \frac{V_{out}}{V_{in}} = 1 + \left(\frac{\delta_L + d_1^2}{\delta_L}\right)^{1/2} = 1 + \left(1 + \frac{d_1^2 R}{Lf}\right)^{1/2} \tag{4.25}$$

Where $f$ is the switching frequency. If the proposed TBC is working at the boundary of CCM and DCM, the voltage gain of CCM and DCM operations will be the same. Hence, by using equations (4.6) and (4.25),

$$1 + \left(1 + \frac{d_1^2 R}{Lf_s}\right)^{1/2} = \frac{2}{1-d} \tag{4.26}$$

The mode I for CCM and DCM is the same i.e. $d = d_1$. Hence, the normalized boundary time constant ($\delta_{L-B}$) for inductors $L_a$ and $L_b$ can be obtained as,

$$\delta_{L-B} = \frac{d\left(1+d^2-2d\right)}{4} \tag{4.27}$$

The plot of $\delta_{L\text{-}B}$ versus $d$ is shown in Fig. 4.6 with DCM and CCM boundary regions. The proposed TBC operates in DCM at a value of $\delta_{L\text{-}B}$ larger than $\delta_L$.
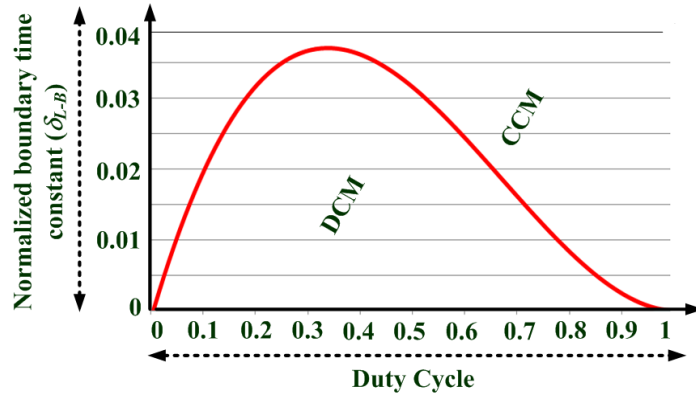


Figure 4.6. Normalized boundary time constant versus duty cycle.

### 4.6 Investigation of Impact of Non-idealities

The effects of non-idealities of different components and devices on the output voltage are studied by taking into account the non-idealities in the power circuit as depicted in Fig. 4.7. The resistance $r_L$ is the Equivalent Series Resistance (ESR) of inductors $L_a$ and $L_b$. The resistance $r_S$ is the ON-state resistance of switches $S_a$ and $S_b$. The resistance $r_d$ and voltage $V_{fd}$ are the forward resistance and threshold voltage of diodes $D_a$ and $D_b$. The ESR of the capacitors $C_a$ and $C_b$ is shown by resistance $r_c$.
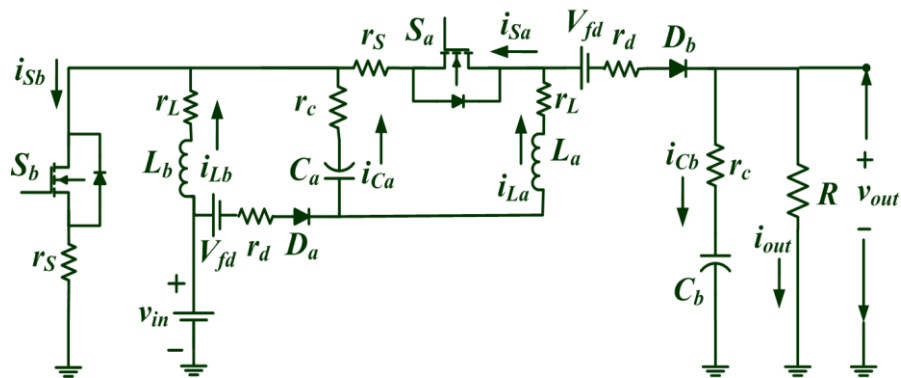


Figure 4.7. The power circuit of TBC with non-idealities.

### 4.6.1 Effect of Inductors on Voltage Gain

The anomaly caused by non-idealities of switches $S_a$ and $S_b$, diodes $D_a$ and $D_b$, capacitor $C_a$ and $C_b$ are ignored (i.e. $r_S$, $r_d$, $r_c$, and $V_{fd}$ are neglected) to study the effect of ESR of inductors $L_a$ and $L_b$. With this consideration, the voltages across inductors $L_a$ and $L_b$ in mode I and II are expressed as follows,

$$v_{La}{}^{I} \approx V_{in} - I_{La}r_L , v_{Lb}{}^{I} \approx V_{in} - I_{Lb}r_L \qquad (4.28)$$

$$v_{La}{}^{II} \approx V_{in} - I_{La}r_L - \frac{V_{out}}{2}, v_{Lb}{}^{II} \approx V_{in} - I_{Lb}r_L - \frac{V_{out}}{2} \qquad (4.29)$$

By using (4.28) and (4.29),

$$v_{La}{}^{I} + v_{Lb}{}^{I} \approx 2V_{in} - I_{La}r_L - I_{Lb}r_L \qquad (4.30)$$

$$v_{La}{}^{II} + v_{Lb}{}^{II} \approx 2V_{in} - I_{La}r_L - I_{Lb}r_L - V_{out} \qquad (4.31)$$

Now applying small approximation and the principle of inductor volt-sec balance,

$$\left(2V_{in} - I_{La}r_L - I_{Lb}r_L\right) d = -\left(2V_{in} - I_{La}r_L - I_{Lb}r_L - V_{out}\right)(1-d) \qquad (4.32)$$

The voltage gain of TBC configuration with consideration of the effect of ESR of inductors $L_a$ and $L_b$ can be obtained as,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_L} = \frac{2 - \frac{r_L}{V_{in}}\left(I_{La} + I_{Lb}\right)}{1-d} \qquad (4.33)$$

It is assumed that $V_{dL}$ is the voltage drop across each inductor due to ESR (i.e. $I_{La}r_L$ and $I_{Lb}r_L$ are equal to $V_{dL}$). Then, (4.33) is written as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_L} = \frac{2\left(1 - \frac{V_{dL}}{V_{in}}\right)}{1-d} = \frac{2}{1-d} - \frac{2}{V_{in}}\frac{V_{dL}}{1-d} \qquad (4.34)$$

From (4.33)-(4.34), it is clear that the voltage gain decreases significantly for greater values of $V_{dL}$ and $d$, which signifies that the inductors ESR ($r_L$) and duty cycle ($d$) should not have a large value.

### 4.6.2 Effect of ON-state Resistances of Switches on Voltage Gain

The anomaly caused by non-idealities of inductors $L_a$ and $L_b$, diodes $D_a$ and $D_b$, capacitors $C_a$ and $C_b$ are ignored (i.e. $r_L$, $r_d$, $r_c$, and $V_{fd}$ are neglected) to study the effect of ON-state resistances of switches. With this consideration, the voltages across inductors $L_a$ and $L_b$ in mode I and II are expressed as follows,

$$v_{La}^{I} \approx V_{in} - \left( I_{Sa} + I_{Sb} \right) r_S, v_{Lb}^{I} \approx V_{in} - I_{Sb} r_S \qquad (4.35)$$

$$v_{La}^{II} \approx V_{in} - \frac{V_{out}}{2}, v_{Lb}^{II} \approx V_{in} - \frac{V_{out}}{2} \qquad (4.36)$$

By using (4.35) and (4.36),

$$v_{La}^{I} + v_{Lb}^{I} \approx 2V_{in} - \left( I_{Sa} + 2I_{Sb} \right) r_S \qquad (4.37)$$

$$v_{La}^{II} + v_{Lb}^{II} \approx 2V_{in} - V_{out} \qquad (4.38)$$

Now applying small approximation and the principle of inductor volt-sec balance,

$$\left( 2V_{in} - \left( I_{Sa} + 2I_{Sb} \right) r_S \right) d = - \left( 2V_{in} - V_{out} \right) \left( 1 - d \right) \qquad (4.39)$$

The voltage gain of TBC configuration with consideration of the effect of ON-state resistance of switches $S_a$ and $S_b$ can be obtained as,

$$\left. \frac{V_{out}}{V_{in}} \right|_{r_S} = \frac{2 - \frac{r_S}{V_{in}} \left( I_{Sa} + 2I_{Sb} \right) d}{1 - d} \qquad (4.40)$$

It is assumed that $V_{ds}$ is the voltage drops due to ON-state resistance of switches $S_a$ and $S_b$ (i.e. $I_{Sa}r_S$ and $I_{Sb}r_S$ are equal to $V_{dS}$). Therefore, (4.40) is now expressed as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_S} = \frac{2 - \dfrac{3V_{dS}}{V_{in}}d}{1 - d} = \frac{2}{1 - d} - \frac{3V_{dS}}{V_{in}}\frac{d}{1 - d} \tag{4.41}$$

From (4.40)-(4.41), it is clear that the voltage gain decreases significantly for greater values of $V_{dS}/V_{in}$ and $d$, which signifies that the ON-state resistance of switches should not have a large value.

### 4.6.3 Effect of Diodes on Voltage Gain

The anomaly caused by parasitic of inductors $L_a$ and $L_b$, capacitors $C_a$ and $C_b$, and switches $S_a$ and $S_b$ are ignored (i.e. $r_L$, $r_C$, and $r_S$ are neglected) to study the effect of diodes $D_a$ and $D_b$. With this consideration, the voltages across inductors $L_a$ and $L_b$ in mode I and II are expressed as follows,

$$v_{La}{}^{I} \approx V_{in} - I_{Da}r_d - V_{fd}, v_{Lb}{}^{I} \approx V_{in} \tag{4.42}$$

$$v_{La}{}^{II} \approx v_{Lb}{}^{II} \approx V_{in} - \frac{I_{Db}r_d + V_{fd} + V_{out}}{2} \tag{4.43}$$

By using (4.42) and (4.43),

$$v_{La}{}^{I} + v_{Lb}{}^{I} \approx 2V_{in} - I_{Da}r_d - V_{fd} \tag{4.44}$$

$$v_{La}{}^{II} + v_{Lb}{}^{II} \approx 2V_{in} - I_{Db}r_d - V_{fd} - V_{out} \tag{4.45}$$

Now applying small approximation and the principle of inductor volt-sec balance,

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$$2V_{in} - I_{Da}r_d - V_{fd} \quad d = - \quad 2V_{in} - I_{Db}r_d - V_{fd} - V_{out} \quad 1-d \qquad (4.46)$$

The voltage gain of TBC configuration with consideration of the effect of diodes $D_a$ and $D_b$ can be obtained as,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_d, V_{fd}} = \frac{2 - \dfrac{V_{fd}}{V_{in}} - d\dfrac{r_d}{V_{in}}I_{Da} - (1-d)\dfrac{r_d}{V_{in}}I_{Db}}{1-d} \qquad (4.47)$$

It is assumed that $V_d$ is the voltage drop due to forward resistance diodes (i.e. $I_{Da}r_d$ and $I_{Db}r_d$ are equal to $V_d$). Therefore, equation (4.47) is now expressed as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_d, V_{fd}} = \frac{2 - \dfrac{1}{V_{in}} \ V_{fd} + V_d}{1-d} = \frac{2}{1-d} - \frac{V_{fd} + V_d}{V_{in} \ 1-d} \qquad (4.48)$$

From (4.47)-(4.48), it is clear that the voltage gain decreases significantly for greater values of $V_d$ and $d$, which signifies that the forward resistance and the threshold voltage of diodes should not have a large value.

### 4.6.4 Effect of Capacitors on Voltage Gain

#### 4.6.4.1 Effects of Intermediate Capacitor

In ON mode, capacitor $C_a$ is charged by input voltage source $V_{in}$. Let's assume the voltage drop across resistance $r_C$ is $Vr_C$. In the OFF state, the capacitor $C_a$ voltage should be dropped down by $\Delta VC_a$ since it is discharged by the current $i_{La}$. Therefore,

$$v_{Ca} = V_{in} - Vr_C - \Delta V_{Ca} \approx V_{in} - \frac{t}{C_a}i_{La} \qquad (4.49)$$

At the end of OFF mode, the voltage across the capacitor $C_a$ is obtained as follows,

$$v_{Ca} = V_{in} - \frac{1}{C_a} \int_{dT}^{T} i_{La} dt = V_{in} - \frac{1-d}{C_a} T i_{La} \qquad (4.50)$$

During OFF mode, the expression for current $i_{La}$ can be expressed as,

$$i_{La} = I_{out} + i_{Cb} = \frac{I_{out}}{1-d} \qquad (4.51)$$

By using (4.50) and (4.51),

$$v_{Ca} = V_{in} - \frac{1-d}{C_a} T \frac{I_{out}}{1-d} = V_{in} - \frac{V_{out}}{fRC_a} \qquad (4.52)$$

It is well known that the inductor currents are increasing and decreasing in ON and OFF mode, respectively. By comparing ON and OFF mode ripples,

$$\frac{dT}{L_a} V_{in} = \frac{1-d}{L_a} T \ V_{out} - V_{in} - v_{Ca} \qquad (4.53)$$

By considering (4.49), the equation (4.53) is re-written as,

$$\frac{dT}{L_a} V_{in} = \frac{1-d}{L_a} T \ V_{out} - 2V_{in} + \Delta V_{Ca} \qquad (4.54)$$

Using (4.52) - (4.54), the voltage gain is obtained as,

$$V_{out}\Big|_{C_1} = \frac{2V_{in}}{1-d\left(1 + \dfrac{t}{1-d \ RC_a}\right)} \qquad (4.55)$$

Using (4.55), it is clear that the standard output voltage in mode II instant is

$$V_{out} = \frac{2V_{in}}{1-d} \qquad (4.56)$$

Further, the output voltage is dropped and at the end of mode II,

$$V_{out}\Big|_{C_a} = \cfrac{2V_{in}}{1-d\left(1+\cfrac{1}{fRC_a}\right)} = \cfrac{2V_{in}}{1-d\left(\cfrac{fRC_a+1}{fRC_a}\right)} \qquad (4.57)$$

Thus, the voltage gain and output voltage drop can be unsurprising if the value of $fRC_a \gg 1$ as,

$$\Delta V_{out}\Big|_{C_1} = \cfrac{2V_{in}}{1-d}\cfrac{1}{fRC_a} = \cfrac{V_{out}}{fRC_a} \qquad (4.58)$$

Using (4.57), the voltage gain can be estimated as,

$$\cfrac{V_{out}}{V_{in}}\Bigg|_{C_a} = \cfrac{2}{1-d\left(1+\cfrac{1}{fRC_a}\right)} \qquad (4.59)$$

This gives the proper selection of the value of the load, switching frequency, and capacitance $C_a$.

### 4.6.4.2 Effects of Load Side Capacitor

Let's assume $Vr_C$ is the voltage drop across resistance $r_C$. In Mode I, the capacitor $C_b$ is discharged through load $R$. Hence, the output voltage which is the voltage across capacitor $C_b$ is decreased and the instantaneous output voltage can be formulated as,

$$v_{Cb} = V_{out} - Vr_C - \cfrac{t}{C_b}I_{out} \approx V_{out}\left(1-\cfrac{t}{RC_b}\right) \qquad (4.60)$$

At the end of the mode I, the final change in output voltage ($\Delta v_{out}$) can be expressed as,

$$\Delta v_{out}\Big|_{C_b} = \cfrac{dV_{out}}{fRC_b} \qquad (4.61)$$

This signifies that the load resistance $R$, switching frequency $f$, and capacitance

$C_b$ should be properly selected.

*4.6.4.3 Combined Effects of Capacitors*

The total output variation due to the combined effect caused by both capacitors $C_a$ and $C_b$ is as follows,

$$\Delta v_{out}\Big|_{C_a+C_b} = \Delta v_{out}\Big|_{C_a} + \Delta v_{out}\Big|_{C_b} = \frac{V_{out}}{fR}\left(\frac{1}{C_a}+\frac{d}{C_b}\right) \quad (4.62)$$

## 4.7 The Efficiency of the converter

By considering the impact of anomaly caused by non-idealities of all the circuit components on voltage gain, the efficiency of the converter can be obtained as,

$$\eta_{TBC} = \frac{2 - \dfrac{2\ V_{dL}}{V_{in}} - \dfrac{3V_{dS}d}{V_{in}} - \dfrac{V_{fd}+V_d}{V_{in}} - \dfrac{V_{rc}}{V_{in}}-V_{rc}}{2+\dfrac{R\ 1-d}{V_{out}\times V_{in}}P_S} \quad (4.63)$$

Where $P_S$ is total switching loss in the switches, and it can be calculated as,

$$P_S = P_{Sa} + P_{Sb} = \frac{I_{Sa}V_{Sa}(T_{ra}+T_{fa})+I_{Sb}V_{Sb}(T_{rb}+T_{fb})}{T} \quad (4.64)$$

Where $P_{Sa}$ and $P_{Sb}$ are switching losses of switches $S_a$ and $S_b$, $I_{Sa}$ and $I_{Sb}$ are average currents through switches $S_a$ and $S_b$, $V_{Sa}$ and $V_{Sb}$ are average voltages across switches $S_a$ and $S_b$, $T_{ra}$ and $T_{rb}$ are rise time for switches $S_a$ and $S_b$, $T_{fa}$ and $T_{fb}$ are fall time for switches $S_a$ and $S_b$.

## 4.8 Design of Circuit Parameters

To verify the working operation and performance of the proposed circuitry, a prototype of TBC configuration is developed in the laboratory. This prototype is developed by considering the parameters with a typical input voltage of 40 V, output power of 500 W, an output voltage of 400 V, and the switching frequency of 100 kHz.

### 4.8.1 Critical Inductances and Capacitances

The inductors and capacitors are designed with consideration of the worst-case scenario to obtain a good performance. Therefore, the required duty cycle is calculated by selecting the 90% worst efficiency ($\eta^{worst}$) as follows,

$$d\big|_{\eta^{worst}=90\%} = 1 - \frac{2}{V_G\big|_{CCM}}\eta^{worst} = 1 - \left(\frac{2}{10} \times 0.90\right) \approx 82\% \tag{4.65}$$

The inductors $L_a$ and $L_b$ critical inductance values can be obtained as,

$$L_{a,c} = L_{b,c} = V_{in}\frac{dT}{\Delta I_L} = V_{in}\frac{dT}{40\% \text{ of } I_L} \tag{4.66}$$

For the given parameters, the critical values are obtained as,

$$L_{a,c} = L_{b,c} = 40 \times \frac{0.82}{4.5A \times 100kHz} \approx 72.5 \ \mu H \tag{4.67}$$

The inductors $L_a$ and $L_b$ must possess a higher inductance and current rating than the obtained critical inductance values and input current, respectively. Hence, the prototype is designed by selecting the ferrite E type core inductors with a rating of 1mH/18A. It is observed that at the instant when switches are turned ON, maximum current is flowing through capacitor $C_a$. Therefore, the critical capacitance of the capacitor $C_a$ is obtained as follows,

$$C_{a,c} = \frac{I_{in}(1-d)}{f\Delta V_{Ca}} = \frac{12.5 \times 0.18}{100kHz \times 2V} = 11.25\mu F \tag{4.68}$$

The capacitor $C_a$ must possess a voltage rating higher than the input voltage i.e. 40V. Hence, the prototype is designed by selecting a film type capacitor rated at 22μF/100V. The critical capacitance capacitor $C_b$ can be obtained as follows,

$$C_{b,c} = d\frac{P_{out}}{V_{out}f\Delta V_{Cb}} = 0.82\frac{500}{400 \times 100kHz \times 4} \approx 2.56\mu F \tag{4.69}$$

The capacitor $C_b$ must possess a voltage rating higher than the output voltage i.e. 400V. Hence, the prototype is designed by selecting a film type capacitor rated at 3.3μF/450V.

*4.8.2 Critical Voltage and Current of Semiconductor Devices*

The critical voltage rating for switches $S_a$ and $S_b$ can be obtained as follows,

$$V_{Sa,c} = \frac{V_{out}}{2} \text{ or } \frac{V_{in}}{1-d}, \quad V_{Sb,c} = \frac{V_{out}}{2} \text{ or } \frac{V_{in}}{1-d} \tag{4.70}$$

For the selected parameters, the switch voltage rating must be greater than 200V. The switches $S_a$ and $S_b$ must possess a current rating higher than the input current i.e. $I_{Sa}$ and $I_{Sb} > I_{in}$. Hence, to design the prototype, switches SQP90142E are selected. The critical voltage rating for diode $D_a$ is obtained as follows,

$$V_{Da,c} = \frac{V_{out}}{2} \text{ or } \frac{V_{in}}{1-d} \tag{4.71}$$

The critical voltage rating for diode $D_b$ is obtained as follows,

$$V_{Db,c} = V_{out} \text{ or } \frac{2V_{in}}{1-d} \tag{4.72}$$

For the selected parameters, the diodes $D_a$ and $D_b$ voltage rating must be greater than 200V and 400V, respectively. The diodes $D_a$ and $D_b$ must possess a current rating higher than the input current i.e. $I_{Da}$ and $I_{Db} > I_{in}$. Hence, to design the prototype, diodes C3D10060A-ND and DPG10I400PM are selected.

## 4.9 Simulation Results and Discussion

The theoretical characteristics waveforms represent the voltage and current behavior of the different circuit components. However, in practical or real conditions non-idealities in the circuit components does exist. Therefore, the experimental waveforms are slightly different than the theoretical waveforms. Some simulation results are shown below for the confirmation. Initially, the design and circuitry of the

proposed TBC is validated through simulation for a 500W power, an output voltage of 400V, and an input voltage of 40V. The obtained voltage and current waveforms across/through each component is shown in Fig. 4.8(a)-(b), respectively. The obtained waveforms are matched with the typical waveforms discussed in Section 4.2. Fig. 4.8(a) displays the input voltage (40V), output voltage (400V), and diodes $D_a$ (200V) and $D_b$ (400V) voltages waveforms for the proposed converter. Both the inductors $L_a$ and $L_b$ are observed to be charging in ON-state with the average voltage value of 40V, and both the inductors $L_a$ and $L_b$ are discharging in OFF-state with the average voltage value of -150V. It is noteworthy that the voltage across each of the switches $S_a$ and $S_b$ is 200V when the output voltage is 400V. Voltage across capacitor $C_a$ is around 39V i.e. approximately equal to the input voltage. The average input current drawn by the proposed converter is nearly equal to 13A. However, the output current is nearly equal to the 1.25A as shown in Fig. 4.8(b). The average current through diode $D_a$ is 5A. The average values of the observed currents through the inductors $L_a$ and $L_b$ is around 11A. It is observed that the average current through switch $S_b$ is 11A.
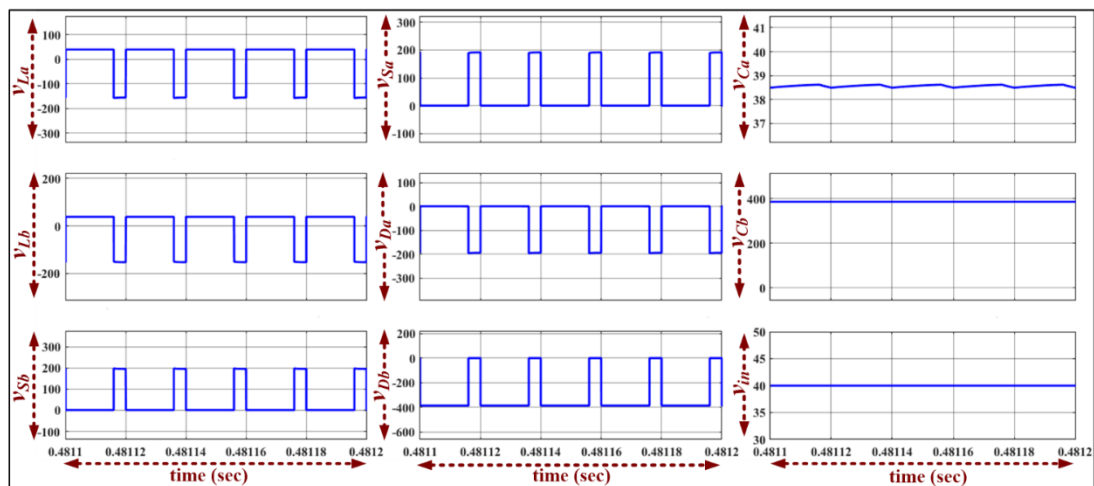


(a) Voltage waveforms
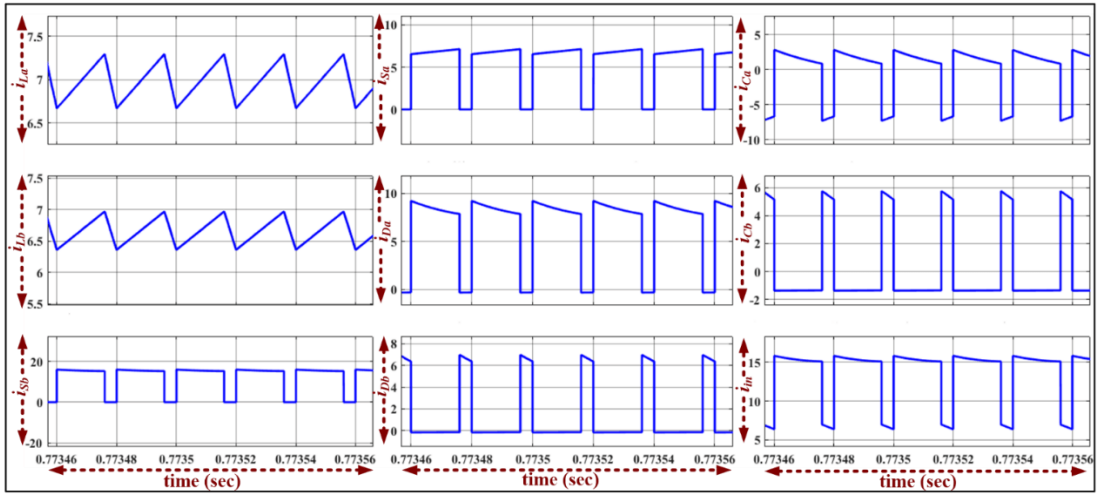
(b) Current waveforms

Figure 4.8. Simulation results

### 4.10 Hardware Implementation, Experimental Results, and Discussion

The prototype of the TBC is implemented in the laboratory to validate the theoretical analysis and performance of the converter. The switches $S_a$ and $S_b$ are controlled with the switching frequency 100kHz using Field Programmable Gate Array (FPGA) and supplied through drivers GDX4A2S1. The designed prototype is shown in Fig. 4.9.
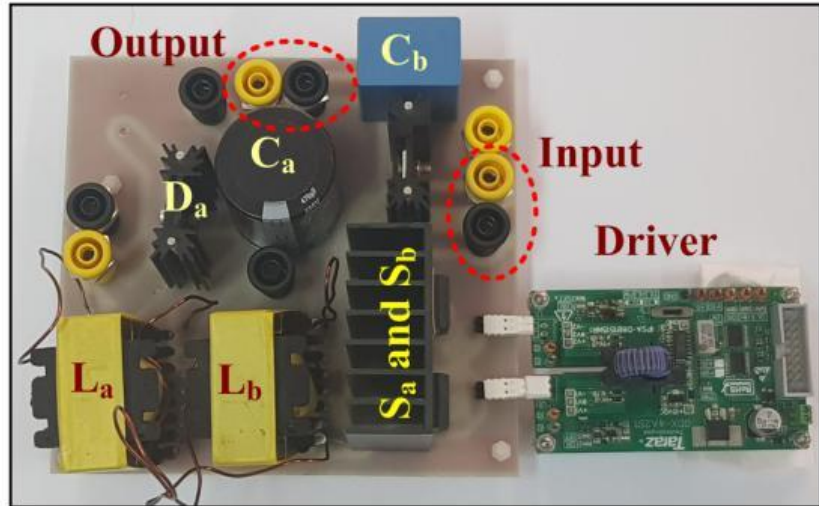


Figure 4.9. Designed 500 W TBC hardware prototype.

The transfer function of the proposed converter is calculated as follows,

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$$G_{vin}(s)\Big|_{\hat{d}(s)=0} = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)} = \frac{2/1-d}{S^2\dfrac{LC_b}{(1-d)^2}+\dfrac{sL}{R(1-d)^2}+1} \tag{4.73}$$

$$G_{d}(s)\Big|_{\hat{v}_{in}(s)=0} = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = \frac{\left(V_{out}/1-d\right)\left(1-sLI_L/V_{out}(1-d)\right)}{S^2\dfrac{LC_b}{(1-d)^2}+\dfrac{sL}{R(1-d)^2}+1} \tag{4.74}$$

The basic PI controller has been implemented to control the output voltage by using the system generator in the Xilinx. The sensed output voltage is converted to the digital signal with the help of the PMOD AD1. The desired voltage reference can be given in the per-unit form (1PU=400V). The suitable minimum and maximum duty ratios have been selected at 0.2 and 0.7 for the safe operation of the proposed converter. Sallen key filters are used to smoothen the signals flowing into and out of the FPGA.

Fig. 4.10(a) shows the obtained experimental waveforms of output- and input voltages, and output- and input- currents. The average values of the observed output voltage, input voltage, output current, and input current are 399.6V, 40.3V, 1.24A, and 13.3A, respectively. Due to the charging and discharging of both inductors $L_a$ and $L_b$, and capacitor $C_a$, the input current is observed to be continuous, and the ON-state and OFF-state slope of the input current is found to be increasing and decreasing, respectively. Fig. 4.10(b) shows the obtained experimental waveforms of voltage and current across/through inductors $L_a$ and $L_b$. The inductors $L_a$ and $L_b$ are observed to be charging in ON-state with the average voltage values of 40.1V and 39.8V, respectively. The inductors $L_a$ and $L_b$ are discharging in OFF-state with the average voltage value of -159.7V and -159.7V, respectively. During the OFF state, the slight slope is observed in inductor voltages due to little practical difference in the values of both the inductances. The average values of the observed currents through inductors $L_a$ and $L_b$ are 11.1A and 10.9A, respectively. Fig. 4.10(c) shows the voltage across diode $D_a$, the

voltage across the capacitor $C_a$, input current, and current through inductor $L_a$. It is observed that the peak voltage across diode $D_a$ is - 200.4V i.e. approximately half of the output voltage. It is observed that the voltage across capacitor $C_a$ is 40.1V i.e. equal to the input voltage. Fig. 4.10(d) shows the experimentally observed voltages across switches $S_a$ and $S_b$, the current through inductor $L_a$, and the voltage across diode $D_b$. It is observed that the voltages across the switches $S_a$ and $S_b$ are 200.7 and 200.4V, respectively i.e. approximately half of the output voltage. Moreover, it is also observed that the voltage stress for both the switches $S_a$ and $S_b$ is approximately the same. It is observed that the peak voltage across diode $D_b$ is -400.3V. The voltage waveform of diode $D_b$ validates that the diode $D_b$ is reversed biased in ON state and forward biased in OFF state. Fig. 4.10(e) shows the voltage and current across/through switch $S_b$. It is observed that the average current through switch $S_b$ is 11.4A.



(a)          (b)          (c)

(d)          (e)
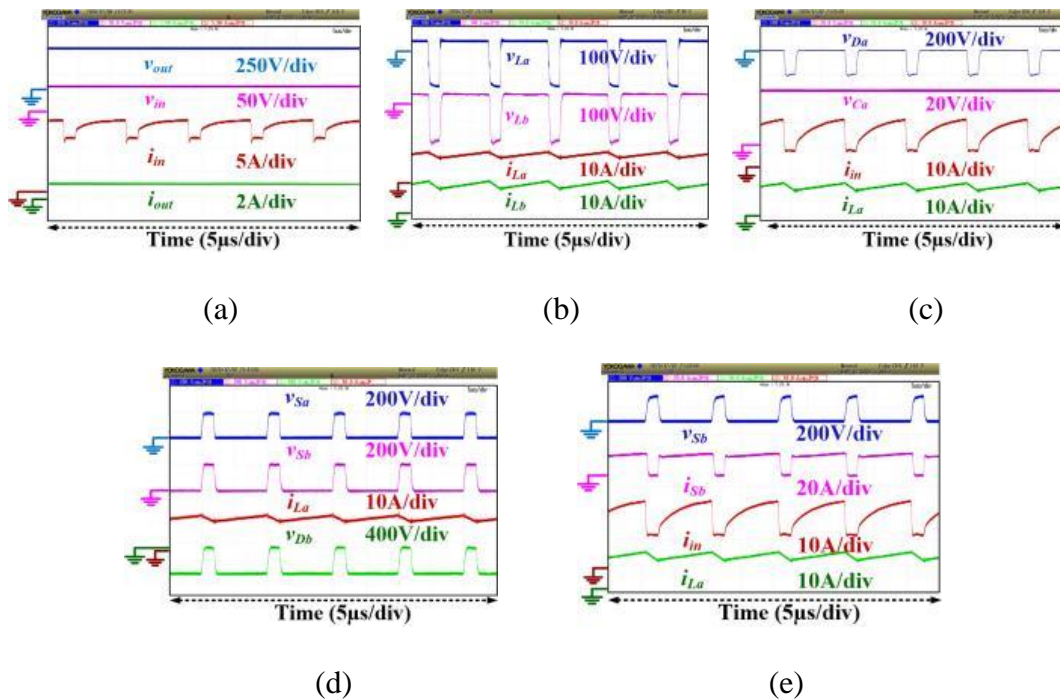
Figure 4.10. Experimental results (a) output- and input- voltages, and output- and input-currents, (b) voltage and current across/through inductors $L_a$ and $L_b$, (c) voltage across diode $D_a$, voltage across capacitor $C_a$, input current, and current through inductor $L_a$,

(d) voltage across switches $S_a$ and $S_b$, current through inductor $L_a$, and the voltage across diode $D_b$, (e) voltage and current across/through switch $S_b$, input current, and current through inductor $L_a$.

A disturbance is initiated from the load and source sides to analyze the proposed converter's performance in a disturbed condition. The reference of the output voltage is set at 400V and the dynamic response of the system by varying the input voltage has been presented in Fig.4.11 (a) and the step-change in the load current in Fig. 4.11(b). As seen from Fig. 4.11(a), constant output voltage of 400V is achieved even when the input voltage varies from the 25V to 45V. The respective variations in the input current to balance the power in the proposed topology and variation in the duty cycle of the converter are observed and the zoomed waveform is shown in Fig. 4.11(a). Similarly, in Fig. 4.11(b) the load is changed and the constant output voltage of 400V is achieved. Here, the load current is varying from 0.7A to 1.24A to 1.34A and the change in the input current can assure the power balance between the input and the output. All the zoomed waveforms have been presented in Fig. 4.11(b) for clarity.



(a)                                                    (b)
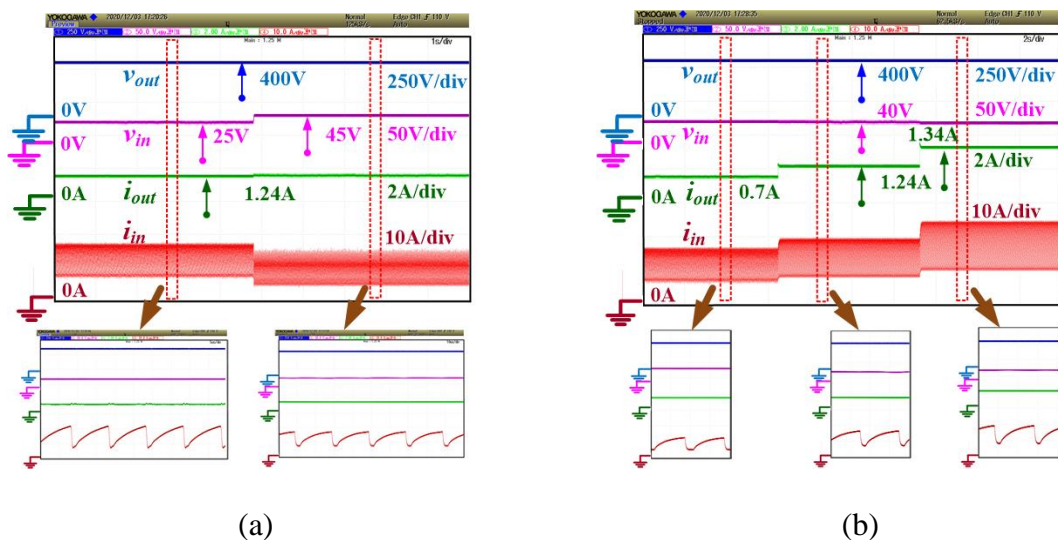
Figure 4.11. Proposed converter TBC Experimental results (input/output voltages and currents) with disturbance, (a) Variation in the input voltage, (b) step change in the load current.

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To analyze the efficiency of the developed prototype, the performance of TBC is examined at different power levels (100W to 500W). Fig. 4.12(a) shows the graphical plot of efficiency versus power. The efficiency of the developed prototype is observed to be 92.43%, at a power of 500W and voltage gain 10. The loss breakdown is shown in Fig. 4.12(b). It is observed that the power loss due to switches, diodes, inductor, and capacitors are 38.9%, 34.4%, 19.2%, and 6.6%, respectively. The power loss due to switches and diodes is higher compared to other elements.



(a)             (b)
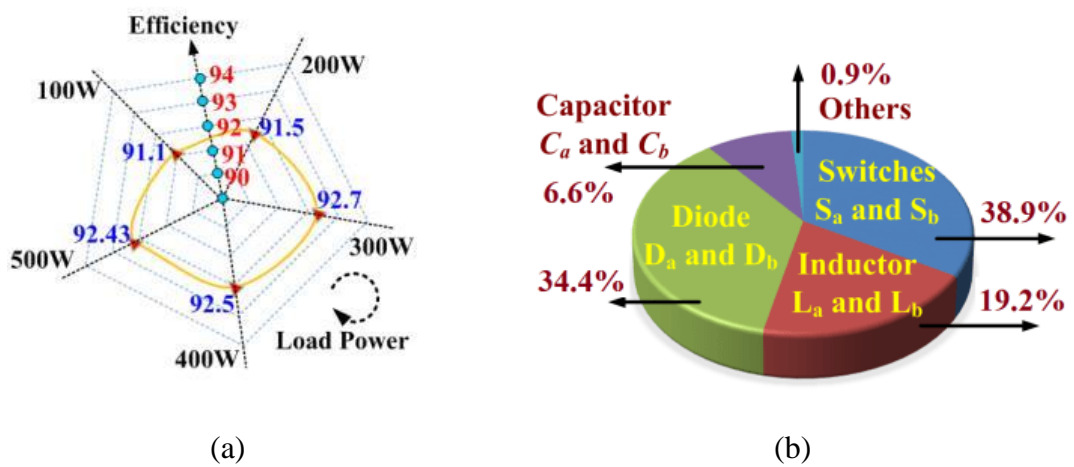
Figure 4.12. Plots (a) Efficiency versus power at voltage gain = 10, (b) Loss breakdown at 500W.

## 4.11 Comparison of different topologies

A comparison of the proposed TBC and other related converters is presented in Table 4.2 to highlight the advantages of the proposed converter. It can be noticed that the voltage stress across switches is reduced to half as well as a higher voltage conversion ratio is obtained with the TBC without increasing the number of components in the circuit. Furthermore, the converter's output terminal is grounded. The proposed converter has a lower input current ripple and a higher voltage gain as compared to the conventional high-boost dc-dc converters. The proposed converter uses two diodes lesser than the Classical switched Inductor Boost converter in [122].

Furthermore, the switch voltage stress is reduced to half of the output voltage by employing one more switch in the circuit.

Thus, low voltage rating active switches are suitable to design the proposed TBC configuration. The total required number of components is the same as the number of components in classical SIBC. Compared with the Transformer-less active switched inductor converter (Converter-I) [148], the proposed converter achieves a higher voltage gain and voltage stress across the switch is also reduced. In comparison with the Converter-II [148], the proposed converter's output terminal is grounded. The converters in [24], [44], and [47], required additional voltage lift networks and complex control. The voltage gain can be increased by using multiple stages but the number of circuit components increase, which results in complex power and control circuit. Moreover, the cost of these circuits is high and efficiency decreases as the number of stages increase to achieve higher voltage as compared to the proposed converter. As compared to the Converter in [29], it can be noticed that a higher voltage conversion ratio is obtained with the proposed TBC without increasing the number of components in the circuit. Also, the proposed TBC uses a lesser number of components as compared to the converter in [46]. Furthermore, the proposed TBC converter provides the common ground connection of source and load, while there is no common ground connection between the source and the load for the converters in [24], [44], [46], [47], and [148].

*$V_s$ is Voltage across the switch, $V_D$ is Voltage across the diode, $V_{out}$ is the output voltage, and $I_{in}$ is the input current. A: Conventional boost converter [26], B: Classical SIBC [122], C: Transformer-less active switched inductor converter [148], D: Converter –II [148], E: converter in [47], F: Converter in [24], G: Converter in [44], H: Converter in [29], I: Converter in [46], J: proposed converter.

Table 4.2. Comparison of Proposed Converter With Related Available Converters

| Converter Performances | | A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Number of devices and components | Total | 4 | 8 | 6 | 8 | 8 | 10 | 10 | 8 | 10 | 8 |
| | Switches | 1 | 1 | 2 | 2 | 3 | 3 | 2 | 2 | 2 | 2 |
| | Diodes | 1 | 4 | 1 | 2 | 2 | 3 | 4 | 3 | 3 | 2 |
| | Inductors | 1 | 2 | 2 | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | Capacitors | 1 | 1 | 1 | 2 | 1 | 2 | 3 | 1 | 3 | 2 |
| Suitable Load Type | | Ground | | | | Floating | | | G | F | G |
| Voltage Gain ($V_G$) | | $1/1\text{-}d$ | $1+d/1\text{-}d$ | | $2/1\text{-}d$ | $(1+d_1)/(1-d_1\text{-}d_2)$ | $2\text{-}d_2/1\text{-}d_1\text{-}d_2$ | $3\text{-}2d/1\text{-}2d$ | $1+d/1\text{-}d$ | $3+d/1\text{-}d$ | $2/1\text{-}d$ |
| Normalized Switch Voltage stress ($V_S/V_{out}$) | | 1 | 1 | $(1+V_G)/2V_G$ | ½, ½ | $(1+V_G)/2V_G$, 1 | ½, $(V_G\text{-}1)/V_G$ | $(1\text{-}V_G)/2$ | ½, ½ | $V_G/3+d$ | ½,½ |
| Normalized Diode Voltage stress ($V_D/V_{out}$) | | 1 | $(V_G\text{-}1)/2V_G$, $1/V_G$, 1 | $(1+V_G)/V_G$ | ½, 1 | 1 | $(1\text{-}V_G)/V_G$, $(1\text{-}V_G)/2V_G$ | $(1\text{-}V_G)/2$, $(1\text{-}V_G)$ | $(1\text{-}V_G)/2V_G$, $1/V_G$, 1 | $2V_G/3+d$ | ½, 1 |
| Switch Current Stress | | $I_{in}$ | $I_{in}$ | $\dfrac{2I_{in}}{1+d}$ | $I_{in}$ | $I_{in}/2$, $I_{in}$ | $I_{in}d_1/2$, $I_{in}d_2$ | $\dfrac{I_{in}}{(3-2d)}$ | $dI_{in}/2$, $dI_{in}$ | $I_{in}/2$, $I_{in}$ | $dI_{in}/2$, $dI_{in}$ |
| Designed Prototypes | Output Power (W) | 200 | 50 | 40 | - | 100 | 500 | 200 | 500 | 200 | 500 |
| | Voltage Gain | 4 | 7 | 5-8 | - | 10 | 10.53 | 4-8 | 4 | 15 | 10 |
| | Efficiency (%) | 98.33 | 95.20 | 92.70 | - | 93.6 | 93.43 | 95.4 | 97.17 | 94.53 | 92.43 |

Therefore, for these converters to be used in PV systems, there will be a requirement of common-mode voltage and leakage current reduction techniques.

## 4.12 Summary

A new TBC configuration is proposed for step-up applications with reduced voltage stress across the switch. The total number of components required is the same as the number of components in classical SIBC. However, the voltage gain of the TBC is higher than the classical boost converter and SIBC. The proposed converter needs a lesser number of diodes than the conventional SIBC, and voltage stress across switches are half of the output voltage. Thus, low voltage rating active switches are suitable to design the proposed TBC configuration. The CCM and DCM modes' working principle, voltage gain, boundary conditions, the effect of non-idealities, comparison with the related converters, and design are presented. It is observed that a higher voltage gain can be achieved by incorporating lower voltage rating switches. The theoretical analysis and operation of the proposed TBC are verified by the experimental investigations and the efficiency is found to be 92.43% at a voltage gain of 10 and output power 500W. The limitation of the proposed converter topology is that the capacitor is directly connected to the input supply in Mode I with the help of diode $D_a$ and switch $S_b$. Therefore, transient high peak current will flow through the capacitor $C_a$ and the current will decrease with time since it is directly connected across the input voltage. However, the average current through any capacitor is zero.

CHAPTER 5: MODELING, ANALYSIS, AND IMPLEMENTATION OF A

SWITCHED-INDUCTOR BASED DC-DC CONVERTER WITH REDUCED

SWITCH CURRENT STRESS

5.1 Introduction

This chapter presents a technique for switch current stress reduction in a

Switched Inductor DC-DC Boost Converter (SIBC). The proposed technique comes up

with a low cost design, high voltage conversion ratio with a less duty cycle value, and

lower current stress without increasing the component count. This topology is basically

a transformer-less design where one diode of the traditional switched inductor

configuration has been replaced with a switch, which is in parallel with the existing

switch, resulting in a design that can incorporate active switches with a low current

rating, since the total input current is equally shared by them. The detailed modes of

operation in both continuous conduction mode (CCM) and discontinuous conduction

mode (DCM) and steady-state analysis, the non-idealities' effect on voltage gain,

design approach, and a comparative study with other DC-DC converters for some

significant performance characteristics are provided. The experimental validations for

the performance and working of the 500 W designed prototype are presented.

To achieve a high voltage gain, derived from the typical switched inductor boost

converter (SIBC) design, this chapter presents an improved converter topology with

reduced current stress for active switches to provide a stable constant boosted DC

voltage. The proposed topology has the advantage of providing a high voltage gain, low

current stress, and low conduction loss on the active switches, simplified control, and

high efficiency. The current is equally shared by both the switches and thereby reducing

the conduction loss. The proposed converter topology is a transformer-less design. Both

the switches are connected in parallel and thereby reducing the switch current stress.

Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. The proposed converter is more appropriate and a better option for PV applications because of its properties of achieving high voltage gain, operation in a wide duty range, and unidirectional power flow. As required for the PV applications, the proposed converter is able to draw a continuous input current with low ripples from the input source. The proposed converter is a viable solution for solar PV applications where a high overall output voltage can be obtained by incorporating the proposed converter with each PV panel.

## 5.2 Power Circuit Topology

The power circuit of the typical SIBC [122] is shown in Figure 5.1(a). SI circuit is incorporated in the SIBC to attain a voltage gain higher than the conventional boost converter. Nonetheless, current stress on the switch increases significantly with voltage gain due to the total input current flowing through the switch. Hence, the power circuitry of the typical SIBC has been improved without increasing the component count to reduce the switch current stress. To attain a high voltage gain, the fundamental concept of switched inductor structures that is charging of inductors in parallel and discharging in series has been exploited. An extra switch is added in place of one diode, which reduces the switch current stress to half of the current stress on the active switch of the SIBC. The current is equally shared by both the active switches.

The power circuitry of the proposed converter is shown in Figure 5.1(b) comprising of diodes $D_A$, $D_B$, and $D_C$, inductors $L_A$ and $L_B$, active switches $S_A$ and $S_B$, $C$ as capacitor, and $R_{out}$ as load. The converter topology put forward is basically a transformer-less design and is originated from the typical Switched Inductor Boost Converter (SIBC) structure by substituting a diode with a switch in the switched inductor circuit.
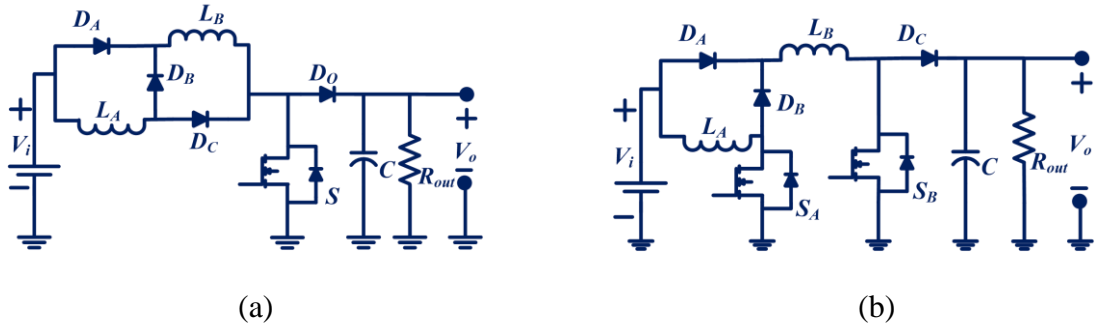
Figure 5.1. Power circuit (a) Typical SIBC [122], (b) Proposed converter.

Both the switches are connected in parallel and thereby reducing the switch current stress to half of the current stress on the active switch of the SIBC. Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. It is important to note that the components count of the proposed converter is the same as that of the typical SIBC and the voltage gain is improved. Firstly, all the circuit elements of the proposed converter topology are considered to be ideal for studying the CCM steady-state characteristics. The capacitance value is sufficiently large to achieve a ripple free voltage, and the ON-state resistance voltage drop across semiconductor devices is ignored. The inductance value of the inductors $L_A$ and $L_B$ are considered to be equal in this section that is, $L_A = L_B = L$ (superior case). Both the inductor $L_A$ and $L_B$ currents are equal as per the above circuit, and are expressed as,

$$I_L = I_{L_A} = I_{L_B} \tag{5.1}$$

Figure 5.2(a)-(b) presents the CCM and DCM characteristic waveforms of the proposed converter; where $T_{on}$ being the Mode I time period (time interval between $t_0$ and $t_a$) and the overall time period is $T$.
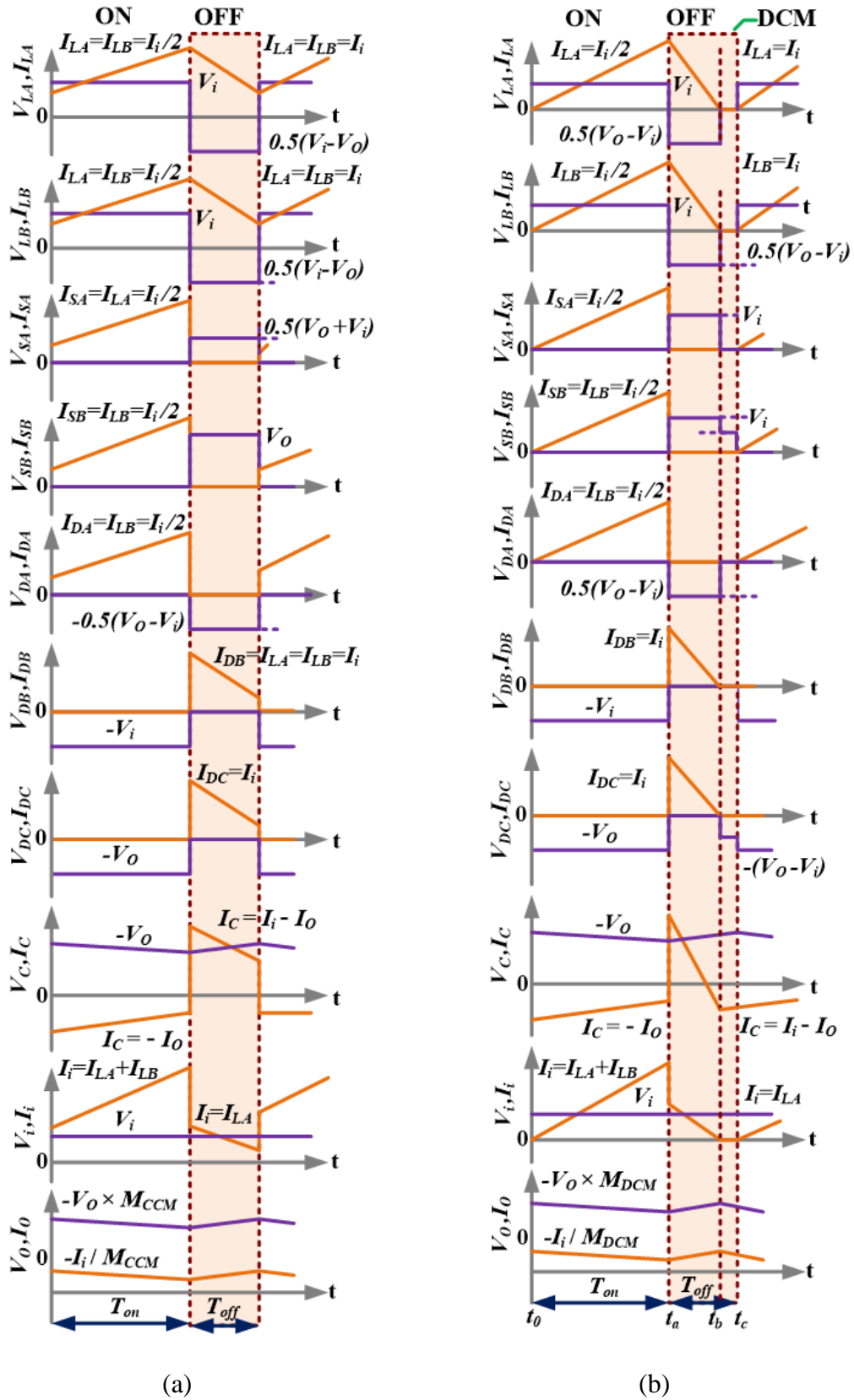
Figure 5.2. Characteristic plots of proposed converter. (a) Continuous conduction mode (CCM). (b) Discontinuous conduction mode (DCM)

## 5.3 Principle of Operation and Analysis in CCM

There are two CCM operation modes of the proposed converter; both the switches $S_A$ and $S_B$ are kept ON in Mode I (between time $t_0$ and $t_a$) while switches $S_A$ and $S_B$ are kept OFF in Mode II (between time $t_a$ and $t_b$).

*Mode I (between time $t_0$ and $t_a$):* Input voltage ($V_i$) charges the Inductor $L_A$ via switch $S_A$, while input voltage ($V_i$) charges inductor $L_B$ via diode $D_A$ and switch $S_B$, and capacitor $C$ is getting discharged via load $R_{out}$. Diode $D_A$ is forward biased and diodes $D_B$ and $D_C$ are reversed biased. Figure 5.3(a) shows the equivalent circuit of the proposed converter for Mode I. Both the inductors are observed to be charged by the input voltage ($V_i$) in parallel and with the same values of current. Inductors $L_A$ and $L_B$ voltages and currents are expressed as,

Table 5.1 briefly summarizes the Operating Principle in both CCM and DCM (*Ch.: Chraged, D/Ch.: Discharged, ZC: Zero current, FB: Forward Biased, RB: Reversed Biased).

Table 5.1. Operating Principle in CCM and DCM

| Operating Modes | Time | Switches | | Inductors | | Diodes | | | Cap. |
|---|---|---|---|---|---|---|---|---|---|
| | | $S_A$ | $S_B$ | $L_A$ | $L_B$ | $D_A$ | $D_B$ | $D_C$ | $C$ |
| **CCM** Mode I | $T_{on}$ ($t_0$–$t_a$) | ON | ON | Ch. in parallel | Ch. in parallel | FB | RB | RB | D/Ch. |
| **CCM** Mode II | $T_{OFF}$ ($t_a$–$t_b$) | OFF | OFF | D/Ch. in series | D/Ch. in series | RB | FB | FB | Ch. |
| **DCM** Mode I | $Y_I T$ or $T_{on}$ ($t_0$–$t_a$) | ON | ON | Ch. in parallel | Ch. in parallel | FB | RB | RB | D/Ch. |
| **DCM** Mode II | $Y_{II}T$ or $T_{off,I}$ ($t_a$–$t_b$) | OFF | OFF | D/Ch. in series | D/Ch. in series | RB | FB | FB | Ch. |
| **DCM** Mode III | $Y_{III}T$ or $T_{off,II}$ ($t_b$–$t_c$) | OFF | OFF | ZC | ZC | RB | RB | RB | D/Ch. |

$$V_L = V_{LA} = V_{LB} = V_i, \quad V_C = V_o \tag{5.2}$$

$$I_L = I_{LA} = I_{LB} = \frac{I_i}{2}, \quad I_C = -I_o = -\frac{V_o}{R_{out}} \tag{5.3}$$

Where $I_i$ is the input current. The switches $S_A$ and $S_B$ voltages and currents are expressed as,

$$V_S = V_{SA} = V_{SB} = 0, \quad I_S = I_{SA} = I_{SB} = \frac{I_i}{2} \tag{5.4}$$

*Mode II (between time $t_a$ and $t_b$):* Both the inductors $L_A$ and $L_B$ are discharging in series having the input supply $V_i$ for charging capacitor $C$ via diodes $D_B$ and $D_C$ and supplying energy to the load $R_{out}$. Diode $D_A$ is reversed biased and diodes $D_B$ and $D_C$ are forward biased. Figure 5.3(b) displays the proposed converter equivalent circuitry for Mode II. The inductors $L_A$ and $L_B$ voltages and currents are expressed as,



(a)                                    (b)
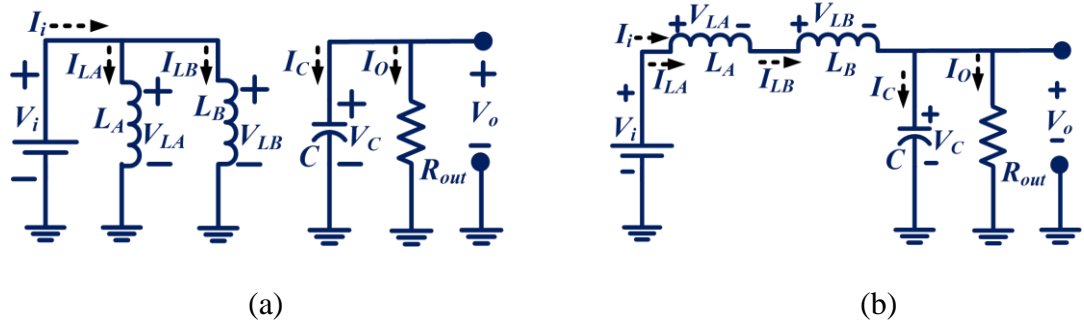
Figure 5.3. Diagram of equivalent circuitry. (a) Mode I, (b) Mode II

$$V_L = V_{LA} = V_{LB} = \frac{V_i - V_o}{2}, \quad V_C = V_o \tag{5.5}$$

$$I_L = I_{LA} = I_{LB} = I_i, \quad I_C = I_L - \frac{V_o}{R_{out}} \tag{5.6}$$

The switches $S_A$ and $S_B$ voltages and currents are expressed as,

$$V_{SA} = \frac{1}{(1-D)} V_i, \quad V_{SB} = \frac{(1+D)}{(1-D)} V_i, \quad I_S = I_{SA} = I_{SB} = 0 \qquad (5.7)$$

The voltage gain of the proposed converter can be expressed as,

$$M_{CCM} = V_o / V_i = 1+D \ / \ 1-D \qquad (5.8)$$

Where the duty cycle is denoted by $D$ and the voltage gain is denoted by $M_{CCM}$. The proposed converter's voltage gain is observed to be equal to that of the typical SIBC.

## 5.4 Principle of Operation and Analysis in DCM

There are three modes of operation of the proposed converter for DCM; switches $S_A$ and $S_B$ are kept ON in the first mode that is ON State, switches $S_A$ and $S_B$ are kept OFF in the second mode with a non-zero value of inductor currents and switches $S_A$ and $S_B$ are kept OFF with zero inductor currents during the third mode. Figure 5.2(b) shows that the inductor current comes to zero, let us say at time $t_b$. Figure 5.2(b) shows the characteristic waveform for DCM, where the time period for the first mode is indicated as $Y_IT$ or $T_{on}$ that is the time between $t_0$ and $t_a$, the time period for the second mode is indicated as $Y_{II}T$ or $T_{off,I}$ that is the time between $t_a$-$t_b$, and the time period for the third mode is indicated as $Y_{III}T$ or $T_{off,II}$ that is the time between $t_b$-$t_c$.

*Mode I (between time $t_0$ and $t_a$)—Both $S_A$ and $S_B$ are kept ON:* The proposed converter's equivalent circuitry and working in this mode are the same as that of mode I of CCM. Both inductors $L_A$ and $L_B$ are charged in parallel by the input supply $V_i$. The currents through inductors $L_A$ and $L_B$ started from zero value at the beginning of this mode that is at the time $t_0$ or $t_0+T$ and attained the highest value at the end of this mode. Inductor $L_A$ and $L_B$ maximum currents can be expressed as,

$$I_{L\max} = I_{LA\max} = I_{LB\max} = V_i Y_I \ / \ Lf \qquad (5.9)$$

The maximum currents through inductor $L_A$ and $L_B$ are denoted by $I_{LAmax}$ and $I_{LBmax}$, respectively, and the switching frequency is denoted by $f = 1/T$. The current ripples of inductors $L_A$ and $L_B$ can be expressed as,

$$\Delta I_L = \Delta I_{LA} = \Delta I_{LB} = V_i Y_I \ / \ Lf \tag{5.10}$$

The inductor $L_A$ and $L_B$ current ripples are denoted by $\Delta I_{LA}$ and $\Delta I_{LB}$, respectively.

*Mode II (between time $t_a$ and $t_b$)—Both $S_A$ and $S_B$ are kept OFF with non-zero value of inductor currents:* The equivalent circuit and working of the proposed converter for this mode are the same as that of mode II of CCM. Inductors $L_A$ and $L_B$ are discharged in series by the input supply $V_i$, and the capacitor $C$ is charged to supply energy to load $R_{out}$. The currents through inductors $L_A$ and $L_B$ started from the maximum value at the beginning of this mode that is at time $t_a$ or $t_a+T$ and zero value is reached by the inductor currents at the end of this mode that is at the instant $t_b$ or $t_b+T$. Inductor $L_A$ and $L_B$ maximum currents can also be expressed alternately as,

$$I_{L\max} = I_{LA\max} = I_{LB\max} = \ V_o - V_i \ \ Y_{II} \ / \ 2Lf \tag{5.11}$$

The current ripples of inductors $L_A$ and $L_B$ are expressed as,

$$\Delta I_L = \Delta I_{LA} = \Delta I_{LB} = \ V_o - V_i \ \ Y_{II} \ / \ 2Lf \tag{5.12}$$

*Mode III (between $t_b$ and $t_c$)—Both $S_A$ and $S_B$ are kept OFF with zero value of inductor currents:* Figure 5.4 shows the DCM mode III equivalent circuit. Both the switches $S_A$ and $S_B$ are kept OFF and currents through inductors $L_A$ and $L_B$ are zero. Hence, the energy accumulated by inductors $L_A$ and $L_B$ is also zero, capacitor $C$ is discharged through load $R_{out}$, and all the three diodes are reversed biased in this mode. Mode II time period which is denoted by $Y_{II}T$ or $T_{off,I}$ can be obtained from Equations (5.10) and (5.11), and is expressed as,

$$Y_{II}T \quad or \quad T_{off,I} = 2V_iY_I \; / \; V_o - V_i \quad f \tag{5.13}$$

We know that,

$$T_{on} + T_{off,I} + T_{off,II} = T \tag{5.14}$$

The time periods for Mode I and III, respectively are expressed as,

$$T_{on} = \frac{Y_I}{f}, Y_{III}T \quad or \quad T_{off,II} = 1 - \frac{1}{f}\left[Y_I + \frac{2V_iY_I}{V_o - V_i}\right] \tag{5.15}$$
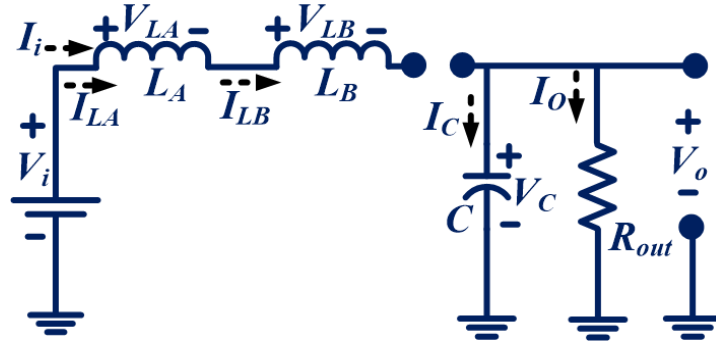


Figure 5.4. DCM mode III equivalent circuit.

The capacitor $C$ average current can be obtained from Figure 5.2(b) and is expressed as,

$$I_C = 0.5 \; Y_{II} \times I_{L\max} \; - I_o = 0.5 \; Y_{II} \times I_{L\max} \; - V_o \, / \, R_{out} \tag{5.16}$$

From Equations (5.15) and (5.16),

$$I_C = 0.5\left(\frac{2V_iY_I}{V_o-V_i} \times \frac{V_iY_I}{Lf}\right) - \frac{V_o}{R_{out}} \tag{5.17}$$

The average current through a capacitor is always zero in a steady-state condition. Hence, Equation (5.17) can also be written as,

$$\frac{2V_iY_I}{V_o - V_i} \times \frac{V_iY_I}{Lf} = \frac{2V_o}{R_{out}} \tag{5.18}$$

The quadratic equation obtained from Equation (5.18), is calculated by using the following expression,

$$\left(\frac{V_o}{V_i}\right)^2 - \frac{V_o}{V_i} - \frac{Y_I^2}{\lambda_L} = 0 \qquad (5.19)$$

Where inductors $L_A$ and $L_B$ normalized time constant is denoted by $\lambda_L$ and has a value equal to $fL/R_{out}$. Hence, $L$, $f$, and $R_{out}$ values control the variation in $\lambda_L$. The voltage gain of the proposed converter for DCM denoted by $M_{DCM}$ can be obtained by simplifying the Equation (5.19) and is expressed as,

$$M_{DCM} = \frac{V_o}{V_i} = \frac{1}{2} + \left(\frac{0.25\lambda_L + Y_I^2}{\lambda_L}\right)^{1/2} = \frac{1}{2} + \left(\frac{1}{4} + \frac{Y_I^2 R_{out}}{Lf}\right)^{1/2} \qquad (5.20)$$

The CCM and DCM voltage gains are observed to be the same when the CCM and DCM boundary is considered as the proposed converter's operating point. Hence, from the Equations (5.8) and (5.20),

$$\frac{V_o}{V_i} = 0.5 + \left(\frac{0.25\lambda_{Lb} + Y_I^2}{\lambda_{Lb}}\right)^{1/2} = \frac{1+D}{1-D} \qquad (5.21)$$

We know that the CCM and DCM mode I are the same. Hence, $Y_I$ is the same as $D$ and inductors $L_A$ and $L_B$ normalized boundary time constant which is denoted by $\lambda_{Lb}$ can be expressed as,

$$\lambda_{Lb} = \left(D^3 - 2D^2 + D\right)/2\left(1+D\right) \qquad (5.22)$$

The plot of $\lambda_{Lb}$ versus $D$ is shown in Figure 5.5 indicating the DCM and CCM regions. It indicates that the proposed converter works in DCM mode when the value of $\lambda_{Lb}$ is more than $\lambda_L$.
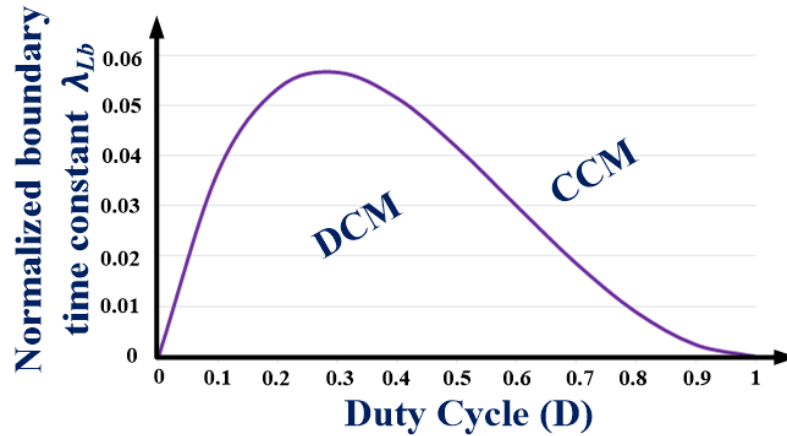
Figure 5.5. Normalized boundary condition w.r.t. duty cycle.

## 5.5 Effects of Non-idealities on Voltage Gain

Figure 5.6 displays the power circuitry of the proposed converter by taking into account the non-idealities of different circuit elements for analyzing their effect on the output voltage. Each of the inductors $L_A$ and $L_B$ Equivalent Series Resistance (ESR) is denoted by the resistances $R_L$. Each of the switches' $S_A$ and $S_B$ ON-state resistance is denoted by the resistances $R_S$. Each of the diodes $D_A$, $D_B$, and $D_C$ threshold voltage and forward resistance are denoted by voltage $V_{FD}$ and resistances $R_D$, respectively; for the capacitor $C$, ESR is denoted by $R_C$.
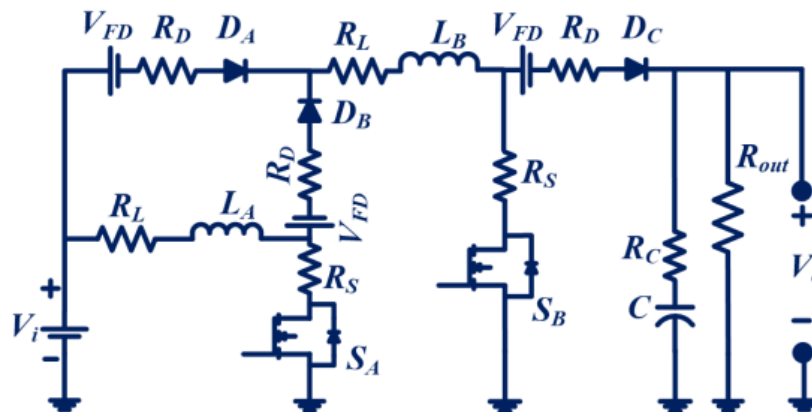


Figure 5.6. Equivalent circuit including non-idealities of the proposed topology

### 5.5.1 Effect of ESR of Inductors on Voltage Gain

Other parasitic irregularities are neglected for analyzing the inductors $L_A$ and $L_B$ ESR effect on voltage gain that is by considering $R_S = 0$, $R_D = 0$, $R_C = 0$, and $V_{FD} = 0$. Hence, in this case, the voltages across the inductors $L_A$ and $L_B$ can be expressed as,

$$\text{on state}: V_{LA} \approx V_i - I_{LA}R_L, V_{LB} \approx V_i - I_{LB}R_L, V_o \approx V_C \qquad (5.23)$$

$$\text{off state}: V_{LA} + V_{LB} \approx V_i - I_{LA}R_L - I_{LB}R_L - V_o \qquad (5.24)$$

From Equation (5.23) and addition of voltages across inductors,

$$V_{LA} + V_{LB} \approx 2V_i - I_{LA}R_L - I_{LB}R_L \qquad (5.25)$$

From the inductor volt second balance method and the method of small approximation,

$$2V_i - I_{LA}R_L - I_{LB}R_L \quad D = - \quad V_i - I_{LA}R_L - I_{LB}R_L - V_o \quad 1 - D \qquad (5.26)$$

From Equation (5.26), the proposed converter voltage gain is calculated by using the following expression,

$$\left.\frac{V_o}{V_i}\right|_{R_L} = \frac{1+D - \quad I_{LA}R_L + I_{LB}R_L \quad / V_i}{1 - D} \qquad (5.27)$$

Both the inductors $L_A$ and $L_B$ currents have the same value that is $I_L = I_{LA} = I_{LB}$ when $L_A = L_B$. If the inductor voltage drop because of ESR is denoted by $V_{DL}$, then $V_{DL} = I_{LA}R_L = I_{LB}R_L$. Therefore, Equation (5.27) can also be expressed alternately as,

$$\left.\frac{V_o}{V_i}\right|_{R_L} = \frac{1+D - 2V_{DL} / V_i}{1 - D} \qquad (5.28)$$

It is observed from (5.27)-(5.28) that for larger values of $V_{DL}$ and $D$, the voltage

gain is decreasing. Hence, moderate values of the duty cycle ($D$) and the ESR of inductance ($R_L$) should be considered.

### 5.5.2 Effect of Diodes on Voltage Gain

Other parasitic irregularities are neglected for analyzing the diodes $D_A$, $D_B$, and $D_C$ effect on voltage gain that is by considering $R_{LA} = 0$, $R_{LB} = 0$, $R_C = 0$, and $R_S = 0$. Hence, in this case, the voltages across the inductors $L_A$ and $L_B$ can be expressed as,

$$\text{Mode I}: V_{LA} \approx V_i, V_{LB} \approx V_i - I_{LB}R_D - V_{FD} \tag{5.29}$$

$$\text{Mode II}: V_{LA} + V_{LB} \approx V_i - 2I_{LB}R_D - 2V_{FD} - V_o \tag{5.30}$$

From Equation (5.29) and addition of inductor voltages,

$$V_{LA} + V_{LB} \approx 2V_i - I_{LB}R_D - V_{FD} \tag{5.31}$$

From the inductor volt second balance method and the method of small approximation,

$$2V_i - I_{LB}R_D - V_{FD} \quad D = - \quad V_i - 2I_{LB}R_D - 2V_{FD} - V_o \quad 1 - D \tag{5.32}$$

From Equation (5.32), the proposed converter voltage gain is calculated by using the following expression,

$$\left.\frac{V_o}{V_i}\right|_{R_D, V_{FD}} = \frac{1+D - I_{LB}R_D + V_{FD} \quad 2-D / V_i}{1-D} \tag{5.33}$$

If the diode voltage drop because of the threshold voltage and forward resistance is denoted by $V_{DD}$, then $V_{DD} = I_{LB}R_D + V_{FD}$. Therefore, Equation (5.33) can also be expressed alternately as,

$$\left.\frac{V_o}{V_i}\right|_{R_D, V_{FD}} = \frac{1+D - V_{DD} \quad 2-D / V_i}{1-D} \tag{5.34}$$

It is observed from (5.33) and (5.34) that for larger values of $V_{DD}/V_i$ and $D$, the voltage gain is decreasing. Hence, moderate values of threshold voltage and forward resistance should be considered.

### 5.5.3 Effect of Switches on Voltage gain

Other parasitic irregularities are neglected for analyzing the switches $S_A$ and $S_B$ effect on voltage gain that is by considering $R_{LA} = 0$, $R_{LB} = 0$, $R_C = 0$, $R_D = 0$, and $V_{FD} = 0$. Hence, in this case, the inductors $L_A$ and $L_B$ voltages can be expressed as,

$$\text{Mode I}: V_{LA} \approx V_i - I_{SA}R_S, V_{LB} \approx V_i - I_{SB}R_S \tag{5.35}$$

$$\text{Mode II}: V_{LA} + V_{LB} \approx V_i - V_o \tag{5.36}$$

From Equation (5.35) and addition of inductor voltages,

$$V_{LA} + V_{LB} \approx 2V_i - I_{SA}R_S - I_{SB}R_S \tag{5.37}$$

From the inductor volt second balance method and the method of small approximation,

$$2V_i - I_{SA}R_S - I_{SB}R_S \quad D = - \quad V_i - V_o \quad 1 - D \tag{5.38}$$

From Equation (5.38), the proposed converter voltage gain is calculated by using the following expression,

$$\left. \frac{V_o}{V_i} \right|_{R_S} = \frac{1 + D \quad - \quad D \quad I_{SA}R_S + I_{SB}R_S \quad / V_i}{1 - D} \tag{5.39}$$

The switches $S_A$ and $S_B$ voltage drops are considered to be the same, and hence $V_{DS} = I_{SA}R_S = I_{SB}R_S$. Therefore, Equation (5.39) can also be expressed alternately as,

$$\left. \frac{V_o}{V_i} \right|_{R_S} = \frac{1 + D \quad - 2D \quad V_{DS} \quad / V_i}{1 - D} \tag{5.40}$$

It is observed from (5.39)-(5.40) that for larger values of $V_{DS}/V_i$ and $D$, the voltage gain is decreasing. Hence, moderate values of the switches ON-state resistance should be considered.

### 5.5.4 Effect of capacitor on Voltage Gain

Other parasitic irregularities are neglected for analyzing capacitor $C$, ESR effect on voltage gain that is by considering $R_{LA} = 0$, $R_{LB} = 0$, $R_D = 0$, $V_{FD} = 0$, and $R_S = 0$. Here, the voltage drop across resistance $R_C$ is denoted by $V_{DC}$. The capacitor $C$ is being discharged via load $R_{out}$ when the switches are kept at ON position. There is a decrement in voltage across the capacitor $C$ which is the same as the output voltage and the instantaneous value of output voltage is obtained as follows,

$$v_{out} = V_o - V_{DC} - \frac{I_o}{C}t = V_o\left(1 - \frac{1}{R_{out}C}t\right) - V_{DC} \tag{5.41}$$

Hence, output voltage variation ($\Delta V_o$) at the end of ON-state is,

$$\Delta V_o\big|_C = \frac{V_o}{R_{out}Cf} \times D \tag{5.42}$$

### 5.5.5 Non-idealities' integrated effect on voltage gain

The non-idealities associated with the inductors $L_A$ and $L_B$, diodes $D_A$, $D_B$, and $D_C$, switches $S_A$ and $S_B$, and their ESR effects on voltage gain have been considered; the voltage gain is expressed as,

$$\frac{V_o}{V_i} \approx \frac{1 + D - \frac{2V_{DL}}{V_i} - (2-D)\frac{V_{DD}}{V_i} - 2D\frac{V_{DS}}{V_i}}{1 - D} \tag{5.43}$$

### 5.6 Evaluation of Converter Efficiency

For capacitor $C$, ON-state and OFF-state currents can be expressed as,

$$\text{ON-State}: I_C = -V_o R_{out}^{-1}, \; \text{OFF-State}: I_C = I_i - V_o R_{out}^{-1} \tag{5.44}$$

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Inductors $L_A$ and $L_B$ currents are equal in the OFF state that is $I_L = I_{LA} = I_{LB}$. Now, considering the capacitor charge balance principle, and the method of small approximation, together with Equation (5.44),

$$\int_0^{DT}\left(\frac{V_o}{R_{out}}\right)dt = \int_{DT}^{T}\left(I_L - \frac{V_o}{R_{out}}\right)dt \Rightarrow \frac{V_o}{R_{out}}D = \left(I_L - \frac{V_o}{R_{out}}\right)1-D \qquad (5.45)$$

Inductor currents are calculated by using Equation (5.45) as,

$$I_L = I_{LA} = I_{LB} = \frac{V_o R_{out}^{-1}}{1-D} \qquad (5.46)$$

The switching power losses of switches $S_A$ and $S_B$ are denoted by $P_{SW\text{-}SA}$ and $P_{SW\text{-}SB}$, respectively. The total switching loss during switching is denoted by $P_{SW\text{-}TOT}$ and can be expressed as,

$$P_{SW-TOT} = \sum_{i=A,B} P_{SW-Si} = \frac{1}{T}\left\{\begin{array}{l}\left(I_{SA}{\times}V_{SA}\right)\left(t_{R-SA}+t_{F-SA}\right)+\\\left(I_{SB}{\times}V_{SB}\right)\left(t_{R-SB}+t_{F-SB}\right)\end{array}\right\} \qquad (5.47)$$

Where, $t_{R\text{-}SA}$, $t_{F\text{-}SA}$, and $t_{R\text{-}SB}$, $t_{F\text{-}SB}$ being the respective rising and falling times for the switches $S_A$ and $S_B$; the switches $S_A$ and $S_B$ average currents are $I_{SA}$ and $I_{SB}$, and the average voltages across the switches $S_A$ and $S_B$ are $V_{SA}$, and $V_{SB}$ respectively. The total input and output power can be expressed as,

$$P_{in}\begin{cases}= V_i\left\{2I_L D + I_{LA}\left(1-D\right)\right\} + P_{SW-TOT}\\[2mm]= \dfrac{V_i V_o R_{out}^{-1}}{1-D}\left(1+D\right) + P_{SW-TOT}\end{cases} \quad , P_{out} = \frac{V_o^2}{R_{out}} \qquad (5.48)$$

The proposed converter's efficiency $\eta_{PRO}$ is obtained from Equations (5.43)–(5.48), and is expressed as,

$$\eta_{PRO} = \frac{1 + D - \dfrac{2V_{DL}}{V_i} - \dfrac{(2-D)V_{DD}}{V_i} - \dfrac{2DV_{DS}}{V_i}}{(1+D) + P_{SW-TOT}\dfrac{R_{out}(1-D)}{V_o V_i}} \qquad (5.49)$$

## 5.7 Design of Circuit Parameters

To validate the operation and performance of the proposed converter it is designed by taking into account the typical values of input voltage as 100 V, output voltage as 400 V, power output as 500 W, and the switching frequency as 100 kHz.

### *5.7.1 Reactive components*

The worst possible efficiency ($\eta_{worst}$) has been taken into account for the design of the reactive components to obtain a good performance. Therefore, the required duty cycle can be calculated by considering the worst efficiency as 90%, and is expressed as,

$$D\Big|_{\eta_{worst}=90\%} = \frac{M_{CCM} - 1}{(M_{CCM} + 1)\eta_{worst}} = \frac{4-1}{(4+1)0.90} \approx 66.67\% \qquad (4.50)$$

The inductors $L_A$ and $L_B$ critical values are calculated as,

$$L_A\Big|_{critical} = L_B\Big|_{critical} = \frac{V_i}{\Delta I_L}DT = \frac{V_i}{40\% \text{ of } I_L}DT \qquad (4.51)$$

The ripple value of peak to peak inductor currents is considered as 1A to calculate the critical values of inductor $L_A$ and $L_B$ and are expressed as,

$$L_A\Big|_{critical} = L_B\Big|_{critical} = \frac{100V \times 0.67}{1A \times 100kHz} \approx 670\mu H \qquad (4.52)$$

The inductors' $L_A$ and $L_B$ current rating and inductance value should be more than the value of input current and critical inductance values, respectively. Therefore, the prototype is designed by selecting 1 mH/10 A rated core inductors of ferrite E type having $R_L = 75$ mΩ.

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The critical capacitance of capacitor $C$ at the output side is calculated by,

$$C\big|_{critical} = \frac{P_{out}}{V_o \Delta V_C} DT \tag{4.53}$$

The peak to peak ripple value of the capacitor voltage is considered as 4 V to calculate the capacitor $C$ critical capacitance and is obtained as,

$$C\big|_{critical} = \frac{500W \times 0.67}{400V \times 4V \times 100kHz} \approx 2.1\mu F \tag{4.54}$$

The capacitor $C$ voltage rating should be more than the value of output voltage that is 400 V. Thus, the prototype is designed by selecting a 2.2 μF/450 V ($R_C = 4$ mΩ) rated film type capacitor.

*5.7.2 Semiconductor devices*

The switches $S_A$ and $S_B$ voltage stresses are calculated as,

$$V_{SA}\big|_{stress} = \frac{V_o + V_i}{2}, V_{SB}\big|_{stress} = V_o \tag{4.55}$$

The switches $S_A$ and $S_B$ minimum voltage rating can be calculated as,

$$V_{SA} = \frac{400V + 100V}{2} = 250V, V_{SB} = 400V \tag{4.56}$$

The selected switches $S_A$ and $S_B$ current ratings should be higher than the value of input current. Thus, FDP19N40-ND ($R_s = 200$ mΩ) MOSFET and FDP18N20-ND ($R_s = 140$ mΩ) MOSFET have been chosen.

The diodes $D_A$, $D_B$, and $D_C$ Peak Inverse Voltage (PIV) rating can be obtained as,

$$V_{DA}\big|_{PIV} = \frac{V_i - V_o}{2}, V_{DB}\big|_{PIV} = -V_i, V_{DC}\big|_{PIV} = -V_o \tag{4.57}$$

The diodes $D_A$, $D_B$, and $D_C$ minimum PIV rating considering the given parameters can be obtained as,

$$\begin{cases} V_{DA}\Big|_{PIV} = \dfrac{100-400}{2} = -150V, V_{DB}\Big|_{PIV} = -100V \\ V_{DC}\Big|_{PIV} = -400V \end{cases} \qquad (4.58)$$

The selected diodes $D_A$, $D_B$, and $D_C$ current ratings should be higher than the value of input current. Thus, DPG10I400PM (400 V/10 A, $R_D$ = 19.8 mΩ, $V_{FD}$ = 0.77 V) and C3D10060AND (600 V/14 A, $R_D$ = 55.2 mΩ, $V_{FD}$ = 0.91 V) diodes have been chosen.

## 5.8 Simulation Results and Discussion

The theoretical characteristics waveforms represent the voltage and current behavior of the different circuit components. However, in practical or real conditions non-idealities in the circuit components does exist. Therefore, the experimental waveforms are slightly different than the theoretical waveforms. Some simulation results are shown below for the confirmation.

Initially, the design and circuitry of the proposed TBC is validated through simulation for 500W power, an output voltage of 400V, and an input voltage of 100V. The obtained voltage and current waveforms across/through each component is shown in Fig. 5.7(a)-(b), respectively. The obtained waveforms are matched with the typical waveforms discussed in Section 5.2. Fig. 5.7(a) displays the input voltage (100V), output voltage (400V), and diodes $D_A$ (150V), $D_B$ (100V) and $D_C$ (400V) voltages waveforms for the proposed converter. Both the inductors $L_A$ and $L_B$ are observed to be charging in ON-state with the average voltage value of 100V, and both the inductors $L_A$ and $L_B$ are discharging in OFF-state with the average voltage value of -100V. It is noteworthy that the voltage across the switch $S_A$ is 250V and $S_B$ is 400V when the output voltage is 400V. The average input current drawn by the proposed converter is nearly equal to 5A. However, the output current is nearly equal to the 1.25A as shown in Fig.

5.7(b). The switches $S_A$ and $S_B$ average current values are observed as 1.5A each. The average values of the observed currents through the inductors $L_A$ and $L_B$ is around 3A.
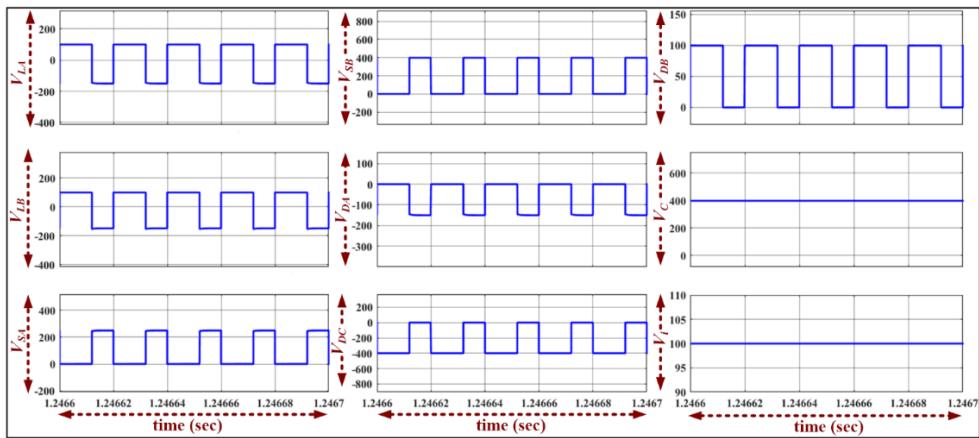


(a) Voltage waveforms
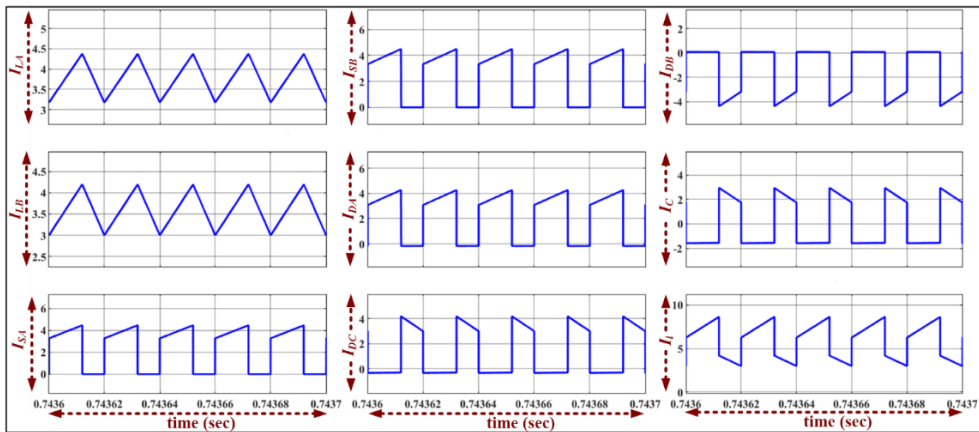


(b) Current waveforms

Figure 5.7. Simulation results.

### 5.9 Hardware Implementation, Experimental Results, and Discussion

The proposed converter's operation and performance have been experimentally verified. The prototype of the proposed converter is implemented in the laboratory to validate the theoretical analysis and performance of the converter. The designed prototype is shown in Fig. 5.8.
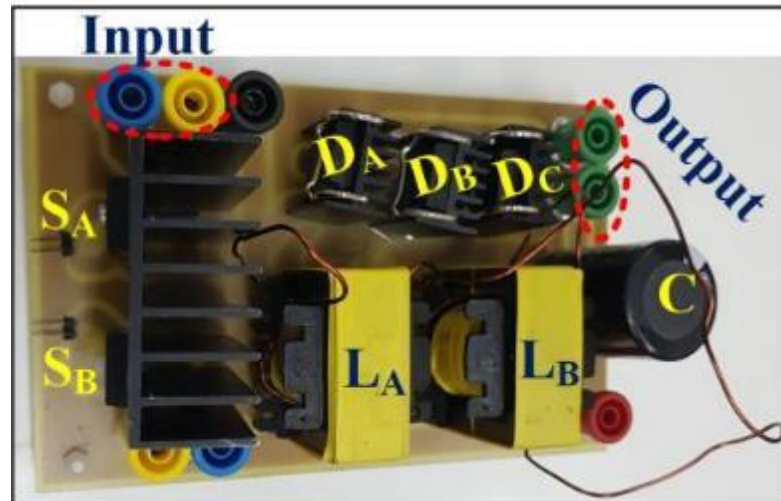
Figure 5.8. Designed 500 W laboratory prototype of the proposed converter.

Figure 5.9(a) displays the input and output voltages and currents waveforms obtained experimentally. The output voltage, output current, input current, and input voltage average values are observed as 398 V, 1.2 A, 5.35 A, and 100 V, respectively. The input current is observed to be continuous in nature; charging and discharging of the inductors $L_A$ and $L_B$ during ON-state and OFF-state causes the input current slope to be increasing and decreasing, respectively. Figure 5.9(b) demonstrates the effect of the step change in load on input/output voltages and currents that is the dynamic behavior of the input/output voltages and currents for the proposed converter with a change in load at a constant duty ratio. It is observed from the experimentally obtained results, that the proposed system is developing stable input/output voltages and currents. The experimentally obtained waveforms of the currents through switches $S_A$ and $S_B$ are shown in Figure 5.9(c); where the output voltage and input current waveforms are included to refer and validate. The switches $S_A$ and $S_B$ average current values are observed as 1.54 A and 1.62 A, respectively. Both the switches $S_A$ and $S_B$ current slopes are observed to be the same as the input current slope during the ON-state. Figure 5.9(d) shows the experimentally observed waveforms of currents through inductors $L_A$ and $L_B$, and the voltage across the diode $D_B$; where the switch $S_A$ current

waveform is shown for reference and validation. The inductors $L_A$ and $L_B$ average current values are observed as 2.99 and 3.1 A, respectively. The PIV across the diode $D_B$ is observed as 100 V. Figure 5.9(e) shows the experimentally observed waveforms for the voltages across Switch $S_B$ and the output diode $D_C$; where the switch $S_B$ current and the output voltage waveforms are shown to refer and validate. Both switches are observed to be turned ON and turned OFF together at the same time. The peak value of switch voltage across the switch $S_B$ is observed as 399.4 V. When the switches are conducted, the output diode $D_C$ is observed to be forward biased. The PIV across the diode $D_C$ is observed as -399.2 V. The diodes $D_A$ and $D_B$ are observed to be forward biased in ON state and reversed biased in OFF state, respectively.



(a)　　　　　　　　　　(b)　　　　　　　　　　(c)

(d)　　　　　　　　　　　　　(e)
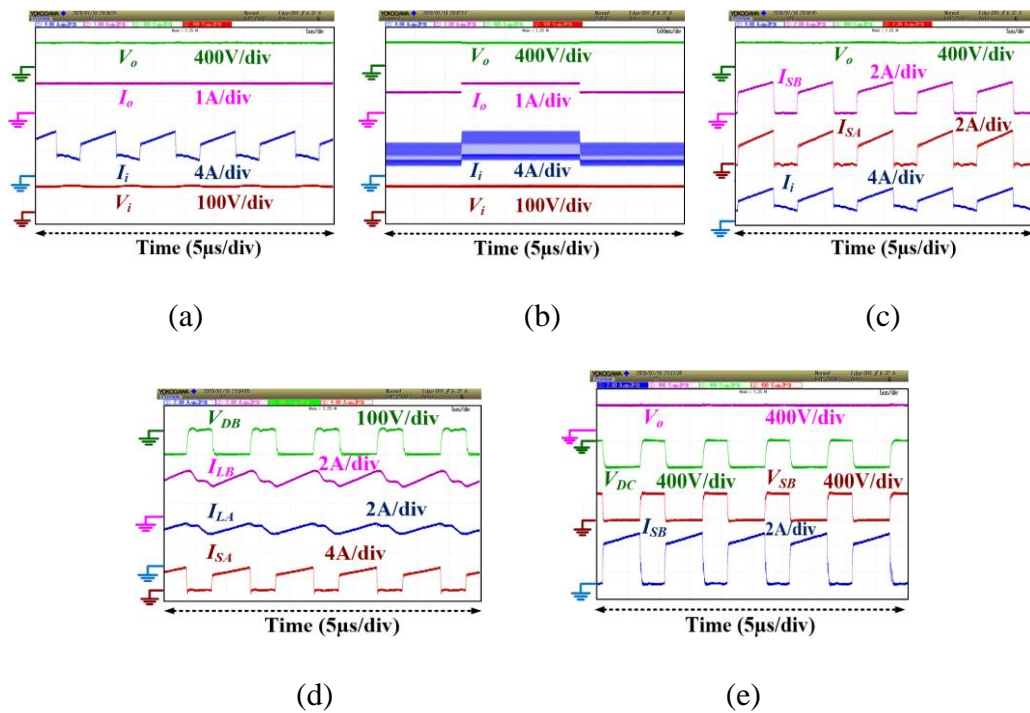
Figure 5.9. Experimentally obtained results. (a) Output voltage, output current, input current, input voltage, (b) effect of step change in load: output voltage, output current, input current, input voltage, (c) output voltage, switches $S_B$ and $S_A$ currents, input current, (d) diode $D_B$ voltage, inductors $L_B$ and $L_A$ currents, switch $S_A$ current, (e) output voltage, diode $D_C$ voltage, switch $S_B$ voltage and current.

To study the efficiency of the developed prototype, the converter's performance is studied at different power levels and input voltage. Figure 5.10(a) shows the efficiency of the designed prototype with variation in power and input voltage. The efficiency of the developed prototype is 93.12% when the input voltage is 100 V and output power is 500 W. The power loss distribution is given in Figure 5.10(b) when load power is 500 W and the input voltage is 100 V. It is investigated that power loss across switches is high compared to other elements of the converter.



(a)                                                      (b)
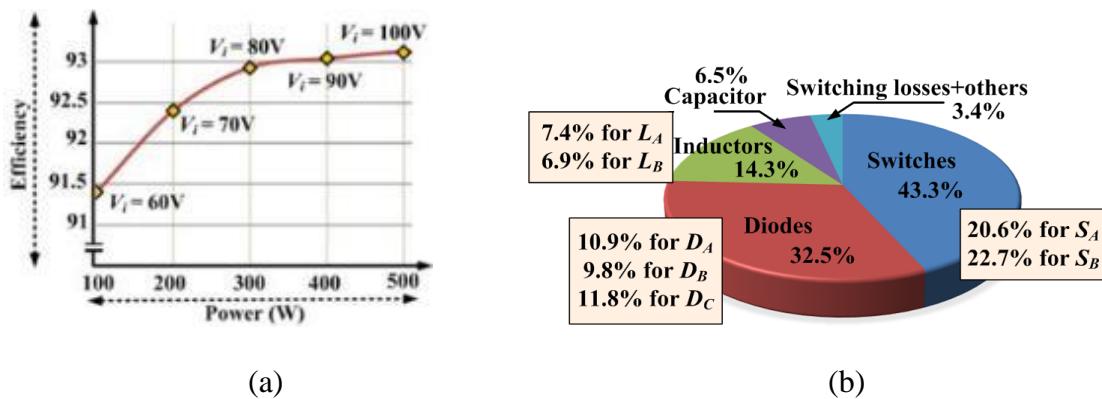
Figure 5.10. Plots. (a) Efficiency versus power for different input voltage. (b) Loss distribution at load power 500 W and input voltage 100 V.

## 5.10 Comparison of Different Topologies

To achieve a high voltage gain and an improved efficiency several DC-DC boost converters have been proposed in the past decade. This section presents a comparison of the proposed converter with some similar high gain DC-DC converters. The converters are compared for the voltage gain, switch current stress, components count, and efficiency and presented in Table 5.2. The components count for the proposed converter is observed to be the same as that of the converters discussed in [122, 153], and [47], while the components count for the converter presented in [148] is lesser than the converter proposed here. However, the proposed converter's

efficiency is more than the converter in [148]. Furthermore, the output and input of the proposed converter and the converters in [122, 154], and [153] are on common ground, while the rest of the converters are only suitable in the conditions of floating load. The converter's efficiency depends on different factors such as the components count, their types, and voltage/current ratings. The comparison with regards to switch current stress among the different converters indicates that the proposed converter has the lowest current stress across the active switches and is equal to half of the input current. The proposed topology is based on a transformer-less design and it is developed by substituting a diode of the traditional switched inductor configuration with a switch in parallel with the existing switch. Hence, low current rating switches can be incorporated, as the total input current is equally shared by the two switches. Generally, the increase in the rating of a device leads to an increment in its ON-state resistance. Components with lower rating are required for the proposed converter topology and hence it comes up with a low-cost design and generates a high efficiency with the same number of components used in the traditional SIBC. The efficiency of the proposed converter is 93.12%, which is higher than the efficiency of the converters presented in [153] and [148] which are 92.2% and 92.7%, respectively. The proposed converter's efficiency is nearly equal to the converters in [24] and [47], while the proposed converter's efficiency is lesser than the converters in [26] and [122].

Therefore, the converter proposed is highly suitable for high voltage gain with reduced switch current stress and less duty cycle, high efficiency, and low-cost applications.

Table 5.2. Comparison of DC-DC Converters

| Converter | Number of reactive components | | Number of Semiconductor devices | | Total components | CCM Voltage gain (M) | Switch current stress | Efficiency | Output port |
|---|---|---|---|---|---|---|---|---|---|
| | Inductor | capacitor | Control Switches | Diodes | | | | | |
| A | 1 | 1 | 1 | 1 | 4 | $1/1-D$ | $I_i$ | - | Grounded |
| B | 2 | 1 | 1 | 4 | 8 | $1+D/1-D$ | $I_i$ | 95.2% at 50W | Grounded |
| C | 2 | 1 | 2 | 1 | 6 | $1+D/1-D$ | $2I_i/1+D$ | 92.7% at 40W | Floating |
| D | 2 | 3 | 2 | 4 | 11 | $1+D/D(1-D)$ | $2I_i/1+D$ | - | Grounded |
| E | 2 | 3 | 1 | 2 | 8 | $2/1-D$ | $I_i$ | 92.2% at 100W | Grounded |
| F | 6 | 1 | 3 | 12 | 22 | $1+5D/1-D$ | $I_i(1+D)/(1+5D)$ | 95.6% at 200W | Floating |
| G | 2 | 1 | 3 | 2 | 8 | $1+D_1/1-D_1-D_2$ | $I_i/2, I_i$ | 93.6% at 100W | Floating |
| H | 2 | 2 | 3 | 3 | 10 | $2-D_2/1-D_1-D_2$ | $I_iD_1/2, I_iD_2$ | 93.43% at 500W | Floating |
| I | 2 | 1 | 2 | 3 | 8 | $1+D/1-D$ | $I_i/2, I_i/2$ | 93.12% at 500W | Grounded |

A: Traditional Boost Converter, B: Conventional switched inductor based boost converter [122], C: converter-I [148], D: Non-isolated voltage lift converter [154], E: modified SEPIC converter [153], F: Active-passive switched inductor converter [26], G: High gain converter [47], H: DDTM converter [24], I: proposed converter.

## 5.11 Summary

A high gain DC-DC converter with reduced switch current stress has been successfully developed through this study. The proposed converter has a higher gain in voltage in comparison to the traditional boost converter and is equal to the gain in voltage of the conventional SIBC at a small duty cycle value. The proposed converter offers the advantage of common ground, continuous input current, and reduced current stress on the active switches using the same number of components as that of a conventional SIBC. Therefore, low current stress active switches can be employed, leading to reduction in losses. Resulting in a low cost and highly efficient converter because of the use of active switches with lower current rating and elimination of a diode. The operating principle in both CCM and DCM including the boundary conditions, the voltage gain, and the effect of non-idealities have been discussed in detail. The comparison of the proposed converter with other similar converters has been presented, which indicates that the proposed converter is feasible to attain a high voltage gain by incorporating low current rating switches. The principle of operation and theoretical analysis have been validated by the experimental results of the developed laboratory prototype, the efficiency at 500 W load power was observed to be 93.12%. Hence, the proposed converter topology provides a viable solution for an efficient renewable energy conversion which can easily be extended further to other power conversion systems for applications where high voltage is required.

CHAPTER 6: A NOVEL HIGH GAIN ACTIVE SWITCHED NETWORK-BASED

CONVERTER

## 6.1 Introduction

This chapter deals with an active switched inductor network-based high gain boost converter. By using less number of components in circuit topology, a higher gain in voltage can be attained at a small duty cycle value by using the proposed converter, which helps in reducing the switch voltage stress and conduction loss. In addition, it draws continuous input current, has lower diode voltage stress, and lower passive component voltage ratings. The operating principles and key waveforms in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) are presented. Parameter design, power loss calculation, characteristics, and comparative study with other non-isolated converters have been presented. Finally, a 200W hardware prototype is constructed and the viability of the proposed converter is verified through the experimentally obtained results.

To achieve a high gain in voltage, a novel converter topology with reduced current stress across active switches to provide a stable constant dc voltage is presented in this chapter. The proposed topology has the advantage of providing a high voltage gain, low current stress, and low conduction loss on the active switches, simplified control, and high efficiency. The current is equally shared by both the switches and thereby reducing the conduction loss. The proposed converter topology is a transformer-less design. Both the switches are connected in parallel and thereby reducing the switch current stress. Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. The proposed converter is more appropriate and a better option for PV applications because of its properties of achieving high voltage gain, operation in a wide duty range, and unidirectional power

flow. As required for the PV applications, the proposed converter is able to draw a continuous input current with low ripples from the input source. To step-up the voltage, the stages of diode/capacitor are cascaded together which in turn limits the switches, diodes, and capacitors voltage stresses. The proposed converter is a viable solution for solar PV applications where a high overall output voltage can be obtained by incorporating the proposed converter with each PV panel.

## 6.2 Power Circuit Topology

The power circuit of the proposed converter is displayed in Fig. 6.1. It is consisting of two inductors $L_1$ and $L_2$ which have the same inductance value and switch $S_1$ and switch $S_2$ are both being turned ON and OFF at once. There are four diodes ($D_0$ to $D_3$) and four capacitors ($C_0$ to $C_3$) in the circuit. The working principles and the steady-state analysis of the proposed converter in both CCM and DCM are discussed below.
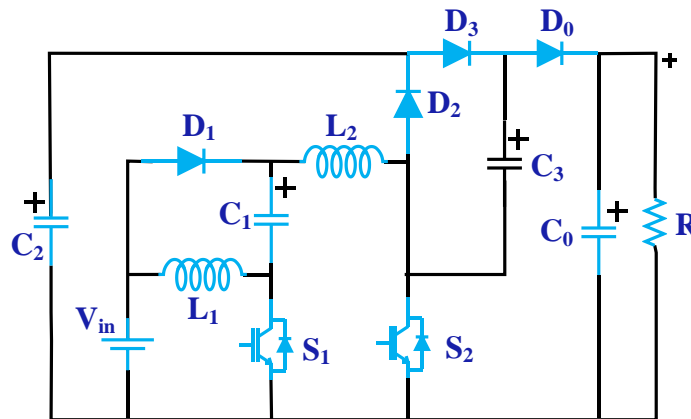


Figure 6.1. Power circuit of the proposed converter.

The analysis of the steady-state characteristics for the proposed converter has been carried out on the basis of certain assumptions. First of all, considering all the circuit components to be ideal. Neglecting the ON-state resistance of the active switches, the forward voltages drop of the diodes and the effective series resistance (ESR) of the inductors and capacitors. However, it is assumed that both the inductors

have equal inductance value and all the capacitors are large enough, and the capacitor voltages are considered to be constant.

## 6.3 Working Principle in CCM

The proposed converter is consisting of two switches that are operating at the same time with the same duty pulse and duty ratio. Therefore, the proposed converter has two operating modes in CCM as $CCM_1$ and $CCM_2$. Table 6.1 briefly summarizes the Operating Principle in both CCM and DCM (*Ch.: Chraged, D/Ch.: Discharged, ZC: Zero current, FB: Forward Biased, RB: Reversed Biased)

Table 6.1. Operating Principle in CCM and DCM

| Operating Modes | | Switches | | Inductors | | Capacitors | | | | Diodes | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $S_1$ | $S_2$ | $L_1$ | $L_2$ | $C_1$ | $C_2$ | $C_3$ | $C_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ |
| CCM | $CCM_1$ | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | Ch. | D/Ch. | FB | RB | FB | RB |
| | $CCM_2$ | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | D/Ch. | Ch. | RB | FB | RB | FB |
| DCM | $DCM_1$ | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | Ch. | D/Ch. | FB | RB | FB | RB |
| | $DCM_2$ | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | D/Ch. | Ch. | RB | FB | RB | FB |
| | $DCM_3$ | OFF | OFF | ZC | ZC | ZC | D/Ch. | ZC | D/Ch. | RB | RB | RB | RB |

$CCM_1$: The switch $S_1$ and switch $S_2$ both are kept ON during mode 1. The equivalent circuit of the proposed converter for this mode is displayed in Fig. 6.3(a). The input supply $V_{in}$ charges inductor $L_1$ via switch $S_1$, the capacitor $C_1$ via diode $D_1$ and switch $S_1$, and inductor $L_2$ via diode $D_1$ and switch $S_2$, respectively. Simultaneously, capacitor $C_3$ is charged by capacitor $C_2$ via diode $D_3$ and switch $S_2$, and the energy stored in capacitor $C_0$ is transferred to the load $R$. Therefore, the voltages across the inductors $L_1$ and $L_2$, and capacitors $C_1$ and $C_3$ can be expressed as,

$$\begin{cases} V_{L1} = V_{L2} = V_{in} \\ V_{C1} = V_{in} \\ V_{C3} = V_{C2} \end{cases} \qquad (6.1)$$

Where, $V_{L1}$ and $V_{L2}$ are the voltages across inductors $L_1$ and $L_2$, respectively; the voltages across capacitors $C_1$ and $C_3$ are $V_{C1}$ and $V_{C3}$, respectively. The characteristics waveform of the proposed converter for each component in ideal condition is displayed in Fig. 6.2.
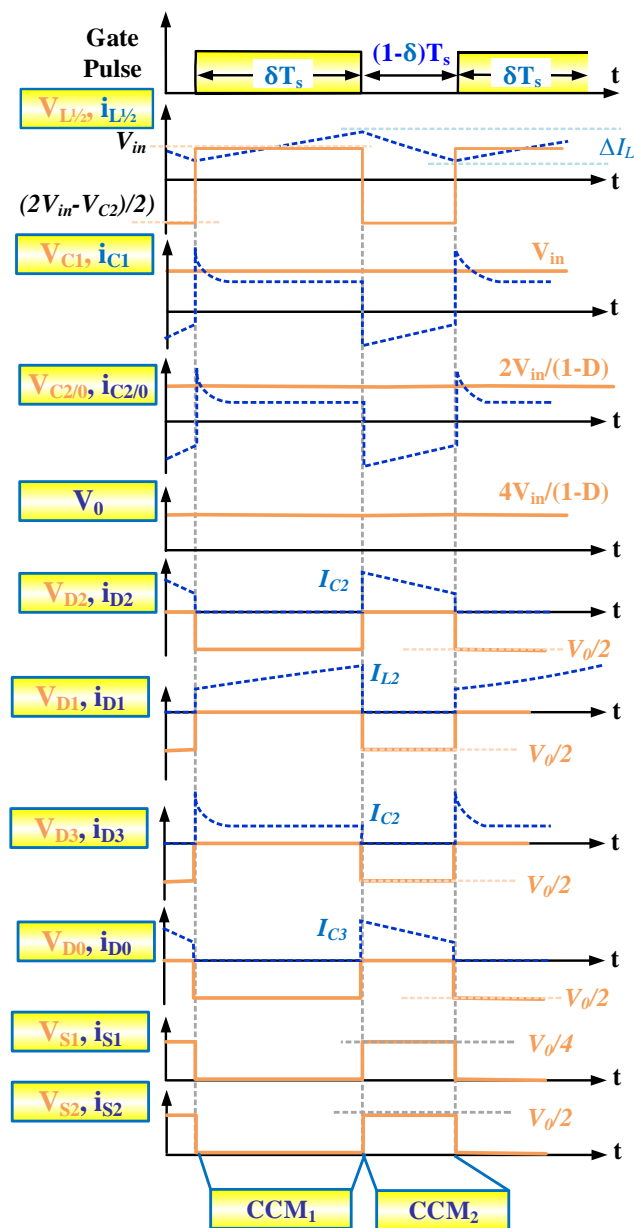


Figure 6.2. Characteristics waveform of the proposed converter in CCM.

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*CCM₂:* During mode 2, switch $S_1$ and switch $S_2$ are both being turned OFF simultaneously. Mode 2 equivalent circuit of the proposed converter is displayed in Fig. 6.3(b). In mode 2, the input supply $V_{in}$ charges the output capacitor $C_0$ by inductor $L_1$, capacitor $C_1$, inductor $L_2$, and capacitor $C_3$ via diode $D_0$. At the same time, capacitor $C_2$ is charged by the input supply voltage $V_{in}$, inductor $L_1$, capacitor $C_1$, and inductor $L_2$ through diode $D_2$.



(a)  (b)
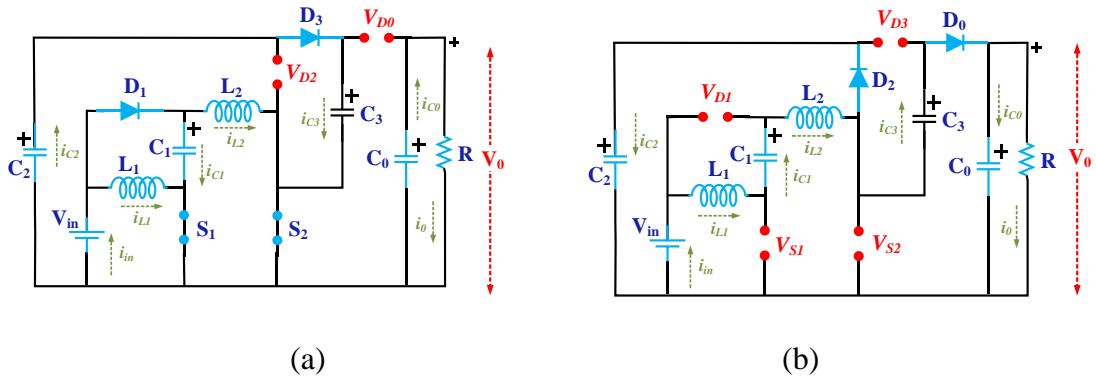
Figure 6.3. Modes of operation of the proposed converter (a) *CCM₁* and (b) *CCM₂*.

Therefore, the voltages across the inductors $L_1$ and $L_2$ can be calculated by using equations (6.2) and (6.3),

$$\begin{cases} V_{L1} + V_{L2} = V_{in} + V_{C1} + V_{C3} - V_0 \\ V_L = \dfrac{2V_{in} + V_{C3} - V_0}{2} \end{cases} \quad (6.2)$$

$$\begin{cases} V_{L1} + V_{L2} = V_{in} + V_{C1} - V_{C2} \\ V_L = \dfrac{2V_{in} - V_{C2}}{2} \end{cases} \quad (6.3)$$

Where $V_{L1} = V_{L2} = V_L$; the value of capacitor voltage for the output capacitor $C_0$ is same as the output voltage $V_0$. From (6.1) and (6.3),

$$\begin{cases} V_{in}\delta + \left( V_{in} - \dfrac{V_{C2}}{2} \right)(1-\delta) = 0, \\ V_{C2} = \dfrac{2V_{in}}{1-\delta} \end{cases} \quad (6.4)$$

Where $\delta$ is the duty ratio. From (6.1) and (6.2),

$$\begin{cases} V_{in}\delta + \dfrac{2V_{in}+V_{C3}-V_0}{2}\ \ 1-\delta\ = 0, \\[3mm] V_0 = \dfrac{2V_{in}}{1-\delta} + V_{C2} \end{cases} \tag{6.5}$$

From (6.4) and (6.5), in the ideal condition, the output voltage and output current are expressed as,

$$\begin{cases} V_0 = \dfrac{4V_{in}}{1-\delta} \\[3mm] I_0 = \dfrac{1-\delta}{4}\ I_{in} \end{cases} \tag{6.6}$$

Therefore, by simplifying (6.6) the voltage gain is expressed as,

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{4}{1-\delta} \tag{6.7}$$

### 6.4 Working Principle in DCM

The proposed converter works in DCM as soon as the inductor current reaches zero level in $CCM_2$ of CCM. Therefore, there are three different working modes in DCM for the proposed converter: $DCM_1$, $DCM_2$; and $DCM_3$.

$DCM_1$: The working principle of $DCM_1$ is the same as that of $CCM_1$. The peak values of currents through the inductors $L_1$ and $L_2$ can be calculated by using equation (6.8),

$$I_{L1}{}^I{}_P = I_{L2}{}^I{}_P = \frac{V_{in}\delta T_S}{L} \tag{6.8}$$

$DCM_2$: During mode 2, both the switches $S_1$ and $S_2$ are kept OFF. The peak values of currents through the inductors $L_1$ and $L_2$ in this mode can be calculated by using equation (6.9),

$$I_{L1}{}^{II}{}_P = I_{L2}{}^{II}{}_P = \frac{2V_{in}-V_{C2}-V_0\ \delta_2 T_S}{2L} \tag{6.9}$$

$DCM_3$: During mode 3, switch $S_1$ and switch $S_2$ are both being turned OFF simultaneously. The characteristics waveform in $DCM_3$ in ideal condition is displayed

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in Fig. 6.4 and the power circuit in $DCM_3$ for the proposed converter is displayed in Fig. 6.5. Zero energy is stored in both the inductors $L_1$ and $L_2$. Hence, only the energy stored in the capacitor $C_0$ connected at the output is transferred to the load $R$. The value of $\delta_2$ can be obtained by (6.8) and (6.9),

$$\delta_2 = \frac{2V_{in}\delta}{2V_{in}-V_{C2}-V_0} \tag{6.10}$$

From the characteristics waveform, the average value of the current through the output capacitor for one switching period is expressed as,

$$I_{C0} = \frac{\frac{1}{2}\delta_2 T_S \ I_{L1 \ P} - I_0 T_S}{T_S} = \frac{1}{2}\delta_2 \ I_{L1 \ P} - I_0 \tag{6.11}$$
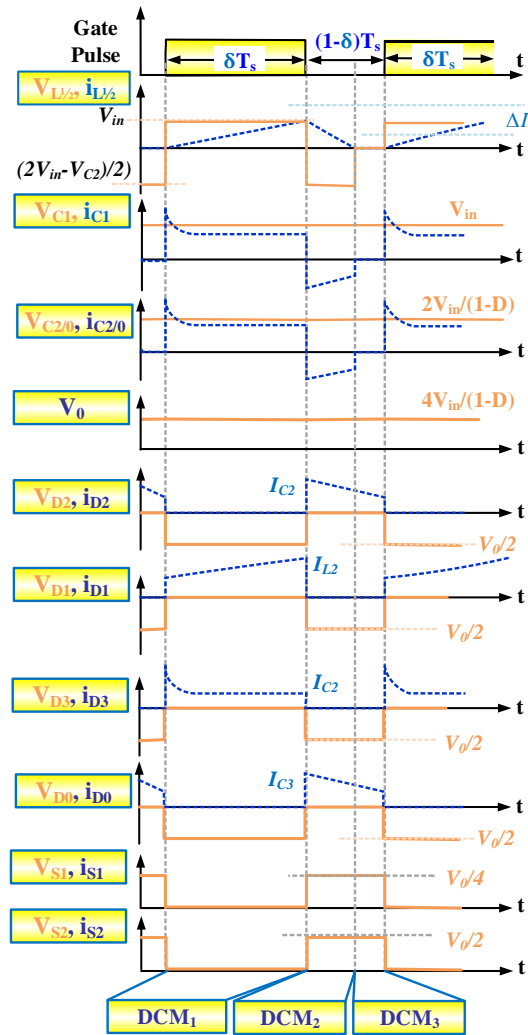


Figure 6.4. Characteristics waveform of the proposed converter in DCM.
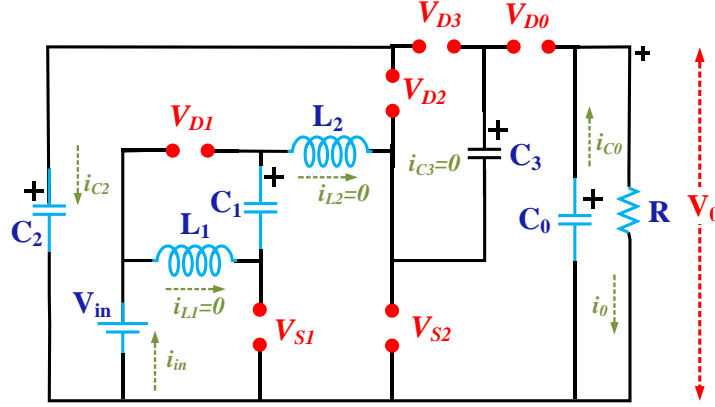
Figure 6.5. Power circuitry in $DCM_3$.

From (6.8) & (6.10), under steady-state conditions

$$\frac{V_{in}\delta^2 T_S}{2V_{in}-V_{C2}-V_0\ L} = \frac{V_0}{R} \tag{6.12}$$

After rearranging (6.12),

$$G_{DCM} = \frac{\delta}{1-\delta} + \delta\sqrt{\frac{\delta}{1-\delta^2}+\frac{1}{\tau_L}} \tag{6.13}$$

Where the normalized time constant for the inductor ($\tau_L$) is defined as $\tau_L = \frac{L}{RT_S}$

. Fig. 6.6(a) shows the variation of the voltage gain of the proposed converter in DCM with the change in duty ratio. Boundary conditions can be obtained by equating $G_{CCM}$ = $G_{DCM}$. Thus, the normalized boundary time constant for the inductor ($\tau_{LB}$) can be obtained as,

$$\tau_{LB} = \frac{1-\delta^2\delta^2}{4-2\delta} \tag{6.14}$$

Fig. 6.6(b) shows the boundary condition of CCM and DCM of the proposed converter w.r.t. duty ratio. It is also observed that, if $\tau_L$ is greater than $\tau_{LB}$, the proposed converter works in CCM.

(a)                                                              (b)
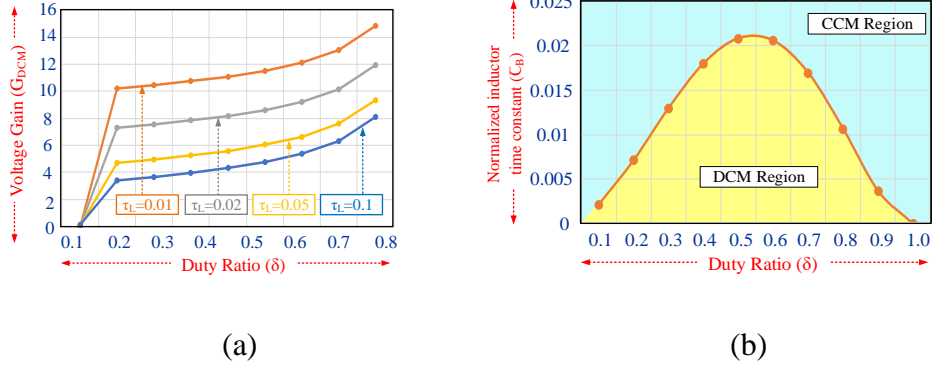
Figure 6.6. (a) Gain in Voltage and (b) DCM boundary condition w.r.t. duty ratio for the proposed converter.

## 6.5 Effect of Mismatching of Inductors

The operation of proposed converter depends on the values of the inductors $L_1$ and $L_2$. Hence, the currents through inductors $L_1$ and $L_2$ depend on the values of inductors $L_1$ and $L_2$.

### A. When Value of $L_1$ Larger than value of $L_2$

The characteristics waveform of the inductors $L_1$ and $L_2$ currents are shown in Fig. 6.7(a) below. In this case the converter operates in three modes as follows,

*1) MODE I ($\delta T_S$):* In this mode, switches $S_1$ and $S_2$ are turned ON and equivalent circuitry is same as mode I of CCM. The input supply $V_{in}$ charges inductor $L_1$ via switch $S_1$, the capacitor $C_1$ via diode $D_1$ and switch $S_1$, and inductor $L_2$ via diode $D_1$ and switch $S_2$, respectively. Simultaneously, capacitor $C_3$ is charged by capacitor $C_2$ via diode $D_3$ and switch $S_2$, and the energy stored in capacitor $C_0$ is transferred to the load $R$. The input current $I_{in}$ is the sum of inductors currents i.e. $I_{in}=I_{L1}+I_{L2}+I_{C1}$. The slope of the inductor $L_1$ and $L_2$ currents can be obtained as follows,

$$\frac{d\,I_{L1}}{dt} \approx \frac{V_{in}}{L1}, \frac{d\,I_{L2}}{dt} \approx \frac{V_{in}}{L2} \tag{6.15}$$

In this mode, the current through inductor $L_2$ is larger than current through inductor $L_1$ since $L_2 < L_1$.

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*2) MODE II (kT$_S$):* This mode occurs for small time duration of $kT_s$ as shown in Fig. 6.7(a). When switches $S_1$ and $S_2$ are just turned OFF. The equivalent circuitry is shown Fig. 6.7(b), where diode $D_1$ is forward biased. During this mode, the current through inductor $L_1$ increases with a positive slope and the current through inductor $L_2$ decreases with large negative slope. The value of current through inductor $L_2$ is larger than current through inductor $L_1$. Also, the input current $I_{in}$ is equal to inductor $L_2$ current i.e. $I_{in}=I_{L2}$ and the resultant current through diode $D_1$ is subtraction of inductors $L_2$ and $L_1$ currents i.e. $I_{L2}$-$I_{L1}$. The slope of the inductors $L_1$ and $L_2$ currents are obtained as follows,

$$\frac{d\ I_{L1}}{dt} \approx \frac{V_{C1}}{L1} \approx \frac{V_{in}}{L1}, \frac{d\ I_{L2}}{dt} \approx \frac{V_{in}-V_{C2}}{L2} \approx \frac{V_{in}+V_{C3}-V_o}{L2} \qquad (6.16)$$

This mode ends as soon as the currents through inductor $L_1$ and $L_2$ are equal, and circuitry operates in mode III.



(a)            (b)
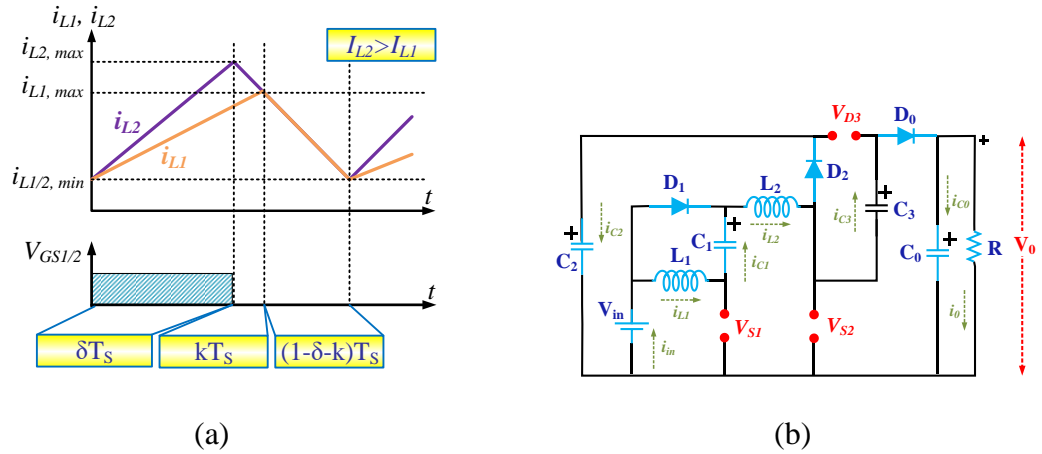
Figure 6.7. When $L_1 > L_2$ (a) inductor currents, and (b) Mode II.

*3) MODE III (1-k-T$_S$):* In this mode, switches $S_1$ and $S_2$ are turned OFF and equivalent circuitry is same as CCM mode II. In mode III, the input supply $V_{in}$ charges the output capacitor $C_0$, inductor $L_1$, capacitor $C_1$, inductor $L_2$, and capacitor $C_3$ via diode $D_0$. At the same time, capacitor $C_2$ is charged by the input supply voltage $V_{in}$, inductor $L_1$, capacitor $C_1$, and inductor $L_2$ through diode $D_2$. In this case, input current

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and the current through inductor $L_2$ and $L_1$ are equal i.e. $I_{in}=I_{L1}=I_{L2}$. The voltage across inductor $L_1$ and $L_2$ can be obtained as follows,

$$\frac{d\ I_{L1}}{dt}=\frac{2V_{in}-V_o}{L_1+L_2}, \frac{d\ I_{L2}}{dt}=\frac{2V_{in}-V_o}{L_1+L_2} \tag{6.17}$$

Using small approximation and inductor volt second balance,

$$For\ L_1 \Rightarrow V_{in}(\delta)+V_{in}(k)+\frac{2V_{in}+V_{C3}-V_o}{L_1+L_2}L_1(1-k-\delta)=0 \tag{6.18}$$

$$For\ L_2 \Rightarrow V_{in}(\delta)+(V_{in}+V_{C3}-V_o)k+\frac{2V_{in}-V_o}{L_1+L_2}L_2(1-k-\delta)=0 \tag{6.19}$$

Solving (6.18)-(6.19), voltage gain of TBC is obtained as,

$$\left.\frac{V_o}{V_{in}}\right|_{L_1>L_2}=\frac{4}{(1-\delta)} \tag{6.20}$$

## 6.6 Efficiency Analysis

The total power loss for the proposed converter comprises of the loss in the inductors, loss in the switches, and loss in the diodes. The power circuit of the proposed converter considering the non-ideality of different circuit components is displayed in Fig. 6.8. Where Equivalent Series Resistance (ESR) for the inductor $L_1$ and inductor $L_2$ are indicated by $r_{L1}$ and $r_{L2}$, respectively. Similarly, $r_{D1}$, $r_{D2}$, $r_{D3}$, and $r_{D0}$ are internal resistance; the drops in forward voltages for the diodes $D_1$, $D_2$, $D_3$, and $D_0$ are $V_{F1}$, $V_{F2}$, $V_{F3}$, and $V_{F0}$, respectively. Whereas, the forward ON state resistances of the control switches $S_1$ and $S_2$, are indicated by $R_{S1}$ and $R_{S2}$, respectively.

### 6.6.1 Inductor Loss

The power loss in the inductor includes the core loss and the copper loss.

$$P_L = Core\ Loss + Copper\ Loss \tag{6.21}$$

For an MPP of 125 μ, the inductor core loss is obtained as follows:

$$P_{Lcore} = 0.33B^{1.98}f^{1.64}A_Cl_m \tag{6.22}$$

Where, $B$ is the half of the ac flux swing, $f$ is the frequency, $A_C$ is the core cross-sectional area, and $l_m$ is the core mean magnetic path length.
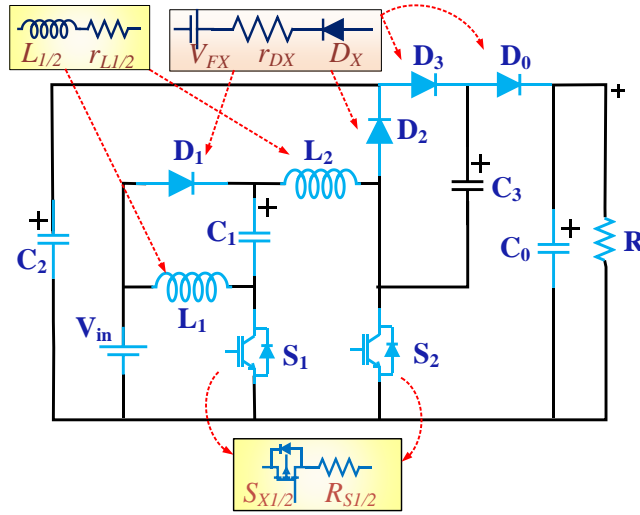


Figure 6.8. The power circuit of the proposed converter considering the non-ideality of different circuit components.

The RMS value of inductor $L_1$ and $L_2$ is calculated as

$$\left.\begin{aligned} I_{L1(RMS)} &= \frac{I_{in}}{2} = \frac{V_0^2}{RV_{in}} \\ I_{L2(RMS)} &= \frac{I_{in}}{2} = \frac{V_0^2}{RV_{in}} \end{aligned}\right\} \tag{6.23}$$

Thus, total inductor copper loss is calculated as

$$\left.\begin{aligned} P_{LCu} &= I_{L1(RMS)}^2 r_{L1} + I_{L2(RMS)}^2 r_{L2} \\ &= \left(\frac{32V_{in}}{(1-\delta)^2 R}\right)^2 r_L \end{aligned}\right\} \tag{6.24}$$

Thus, total inductor power loss is calculated as

$$P_L = 0.33B^{1.98}f^{1.64}A_C l_m + \left(\frac{32V_{in}}{(1-\delta)^2 R}\right)^2 r_L \tag{6.25}$$

### 6.6.2 Switch Loss

The switching power losses of $S_1$ and $S_2$ are denoted by $P_{SW\text{-}S1}$ and $P_{SW\text{-}S2}$, respectively. Where $P_{SW\text{-}S}$ denotes the total switching loss during switching and can be expressed as,

$$P_{SW-S} = \sum_{i=1,2} P_{SW-Si} = \frac{1}{2T}\left\{\begin{array}{l}\left(I_{S1}{\times}V_{S1}\right)\left(t_{R-S1}+t_{F-S1}\right)+ \\ \left(I_{S2}{\times}V_{S2}\right)\left(t_{R-S2}+t_{F-S2}\right)\end{array}\right\} \tag{6.26}$$

Where, the rising and falling times of $S_1$ and $S_2$ are indicated by $t_{R\text{-}S1}$, $t_{F\text{-}S1}$, and $t_{R\text{-}S2}$, $t_{F\text{-}S2}$, respectively; the value of average switch current through $S_1$ and $S_2$ are indicated by $I_{S1}$ and $I_{S2}$, and the switch voltages of $S_1$ and $S_2$ are indicated by $V_{S1}$, and $V_{S2}$ respectively. The switch conduction losses of $S_1$ and $S_2$ are calculated by using equation (6.27)

$$\left.\begin{array}{l} P_{con} = I^2_{S1(RMS)}r_{DS1} + I^2_{S2(RMS)}r_{DS2} \\ \\ = \left(\frac{32V_{in}\delta}{(1-\delta)^2 R}\right)^2 r_{DS} \end{array}\right\} \tag{6.27}$$

Thus, the total loss by the switches is calculated as

$$P_S = P_{SW-S} + P_{con} \tag{6.28}$$

### 6.6.3 Diode Loss

The power loss contributed by the diode is the addition of loss by internal forward voltage drop ($V_F$) and loss by internal forward resistance ($r_D$) which is calculated as

$$P_{D,loss} = P_{D(VF)} + P_{D(rD)} \tag{6.29}$$

The power loss by the diode due to the forward voltage drop of $V_F$ is calculated

as,

$$P_{D(VF)} = \left. \begin{array}{l} I_{D1(avg)}+I_{D2(avg)}+I_{D3(avg)}+I_{D0(avg)} \ V_F \\[2mm] = \left(\dfrac{8(1-\delta)V_{in}}{(1-\delta)^2 R}\right)^2 V_F \end{array} \right\} \tag{6.30}$$

The diode power loss caused by the internal forward resistance $r_L$ is calculated as,

$$P_{D(r_D)} = \left. \begin{array}{l} I_{D1(RMS)}+I_{D2(RMS)}+I_{D3(RMS)}+I_{D0(RMS)} \ ^2 \ r_D \\[2mm] = \left(\dfrac{4(4-3\delta)V_{in}}{(1-\delta)^2 R}\right)^2 r_D \end{array} \right\} \tag{6.31}$$

*6.6.4 Overall Efficiency*

Therefore, the efficiency of the proposed converter can be calculated by using equations (6.25)-(6.31) as (6.32),

$$\left. \begin{array}{l} \eta = \dfrac{P_o}{P_{in}+P_{loss}} = \dfrac{P_o}{P_{in}+P_L+P_S+P_{D,loss}} \\[3mm] = \dfrac{P_o}{P_{in}+P_{LCore}+P_{LCu}+P_{SW-S}+P_{con}+P_{D(VF)}+P_{D(r_D)}} \\[3mm] = \dfrac{2(1-\delta)^4 I_{in}RV_o{}^2 T}{\left[2T\left[\begin{array}{l}(1-\delta)^4 R \ V_{in}R+0.33B^{1.98}f^{1.64}A_Cl_mI_{in} \\[2mm] +16V_{in}{}^2 I_{in} \ 64 \ r_L+\delta^2 r_{DS} \ +4(1-\delta)^2 V_F +(4-3\delta)^2 r_D \end{array}\right]\right]+} \\[3mm] \quad +V_{in}I_{in}(1-\delta)^3 R^2 \ _{S1} \ \!_{R-S1}+t_{F-S1} \ 2I_{S2} \ _{R-S2}+t_{F-S2} \end{array} \right\} \tag{6.32}$$

6.7 Design of Circuit Components

The inductor and capacitor design is an essential element of the converter design. The selection of inductors is done on the basis of the inductor current, while the capacitor is selected on the basis of the capacitor voltage.

### 6.7.1 Inductor Design

The equivalent voltage developed across both the inductors $L_1$ and $L_2$ are obtained as,

$$V_{L1} = V_{L2} = L\frac{di}{dt} \tag{6.33}$$

The inductor value is selected on the basis of the average value of charging current, its ripples, duty ratio, and switching frequency. The ripple current through each inductor in the charging condition is obtained as follows,

$$\frac{V_{in}\delta T_S}{L} = \Delta i_{L1} = \Delta i_{L2} \tag{6.34}$$

Where, the values of ripple currents for the inductor $L_1$ and inductor $L_2$ are indicated by $\Delta i_{L1}$ and $\Delta i_{L2}$, respectively. Therefore, for the CCM operation of the proposed converter, the critical values of each inductor can be calculated as,

$$L_1{}_{Cri} = L_2{}_{Cri} = \frac{V_{in}\delta T_S}{\Delta i_{L1/2}} = \frac{V_{in}\delta}{\Delta i_{L1/2} f_S} \tag{6.35}$$

Thus, the value of both the inductors can be chosen based on (6.29), where $\Delta i_{L2}$ is 20-40% of the average inductor current value and $f_s$ is the switching frequency to control the switch.

### 6.7.2 Capacitor Design

The capacitor value is controlled by its charging current, the voltage ripple across it, duty ratio, and switching frequency. During $CCM_1$ the Capacitors $C_1$ and $C_3$ are being charged and being discharged during $CCM_2$ with a value of current equal to $I_{L1}$. Thus, the capacitor voltage ripple for $C_1$ and $C_3$ can be obtained as follows,

$$\Delta V_{C1} = \frac{i_{L1}\ 1-\delta\ T_S}{C_1} = \frac{i_{L1}\ 1-\delta}{C_1 f_S} = \Delta V_{C3} \tag{6.36}$$

Capacitors $C_0$ is charged in Mode I and discharged in Mode II with a value of

current equal to $I_0$. Thus, the capacitor voltage ripple for $C_0$ can be obtained as,

$$\Delta V_{C0} = \frac{i_0\ 1-\delta\ T_S}{C_0} = \frac{i_0\ 1-\delta}{C_0 f_S} \tag{6.37}$$

Capacitors $C_2$ is charged in Mode II with a value of current equal to $I_{L1}$. Thus, the capacitor voltage ripple for $C_2$ can be obtained as,

$$\Delta V_{C2} = \frac{i_{in}\ 1-\delta\ T_S}{2C_2} = \frac{i_{in}\ 1-\delta}{2C_2 f_S} \tag{6.38}$$

With the help of (6.36)-(6.38), the critical values of capacitors $C_1$, $C_2$, $C_3$, and $C_0$ can be calculated by using equations (6.36)-(6.41),

$$C_1 = C_3 \geq \frac{i_{in}\ 1-\delta}{2\Delta V_{C1} f_S} \tag{6.39}$$

$$C_0 \geq \frac{i_0\ 1-\delta}{\Delta V_{C0} f_S} \tag{6.40}$$

$$C_2 \geq \frac{i_{in}\ 1-\delta}{2\Delta V_{C2} f_S} \tag{6.41}$$

Where, $\Delta V_{C1}$, $\Delta V_{C2}$, and $\Delta V_{C0}$ are the voltage ripple contents of the capacitors $C_1$, $C_2$, and $C_0$ respectively; $i_0$ is the output current.

### 6.7.3 Selection of Diodes

It is observed that diodes $D_1$ and $D_3$ are only conducting in Mode I to charge the Capacitors $C_1$ and $C_3$, respectively. The diodes $D_2$ and $D_0$ are conducting in Mode 2 to charge the Capacitors $C_2$ and $C_0$, respectively. The maximum value of voltage stress across all the diodes are expressed as follows,

$$Diode\quad D_1: \begin{cases} 0, & 0<t<\delta \\ -\dfrac{V_0}{4}, & \delta<t<\delta T_S \end{cases} \tag{6.42}$$

$$Diode \quad D_2 : \begin{cases} -\dfrac{V_0}{2}, & 0 < t < \delta \\ 0, & \delta < t < \delta T_S \end{cases} \tag{6.43}$$

$$Diode \quad D_3 : \begin{cases} 0, & 0 < t < \delta \\ -\dfrac{V_0}{2}, & \delta < t < \delta T_S \end{cases} \tag{6.44}$$

$$Diode \quad D_0 : \begin{cases} -\dfrac{V_0}{2}, & 0 < t < \delta \\ 0, & \delta < t < \delta T_S \end{cases} \tag{6.45}$$

Therefore, the diodes are selected to sustain the voltage stress shown in (6.46).

$$V_{D_1} \geq \dfrac{V_0}{4}, V_{D_2} = V_{D_3} = V_{D_0} \geq \dfrac{V_0}{2} \tag{6.46}$$

### 6.7.4 Selection of Switches

The switches $S_1$ and $S_2$ have been selected on the basis of their respective voltage stress values in the circuit. The switch voltages across $S_1$ and $S_2$ are observed to be zero in Mode I. The maximum voltage stress values of the switches $S_1$ and $S_2$ is expressed as follows,

$$Switch \quad S_1 : \begin{cases} 0, & 0 < t < \delta \\ \dfrac{V_0}{4}, & \delta < t < \delta T_S \end{cases} \tag{6.47}$$

$$Switch \quad S_2 : \begin{cases} 0, & 0 < t < \delta \\ \dfrac{V_0}{2}, & \delta < t < \delta T_S \end{cases} \tag{6.48}$$

Therefore, the switches $S_1$ and $S_2$ have been selected to sustain the voltage stress shown in (6.49).

$$V_{S_1} \geq \dfrac{V_0}{4}, V_{S_2} \geq \dfrac{V_0}{2} \tag{6.49}$$

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## 6.8 Simulation Results and Discussion

The proposed converter topology is devised for 200W power, an output voltage of 400V, and an input voltage of 30V with a duty cycle value of 0.7. The proposed converter has been simulated in MATLAB and the simulation results are shown in Fig.6.9. The average values of output voltage and output current are observed as 400V and 0.5A, while the input voltage and input current average values are observed as 30V and 6A. The average values of the inductor currents for inductor $L_1$ and inductor $L_2$ are observed as 3A and 3.2A, respectively. The PIV across diode $D_1$ is 25% of the output voltage and its value is equal to (-100V). The voltage across capacitor $C_1$ is observed as 30V which is almost the same as input voltage. The PIV across all the diodes $D_2$, $D_3$, and $D_0$ is the same as output voltage i.e. -200V. The value of average output current is observed as 0.5A. The voltages across capacitors $C_2$, $C_3$, and $C_0$ are observed as 200V, 200V, and 400V respectively. The maximum value of switch voltage stress across $S_2$ is observed as 200V in $CCM_2$ which is 50% of the output voltage value.
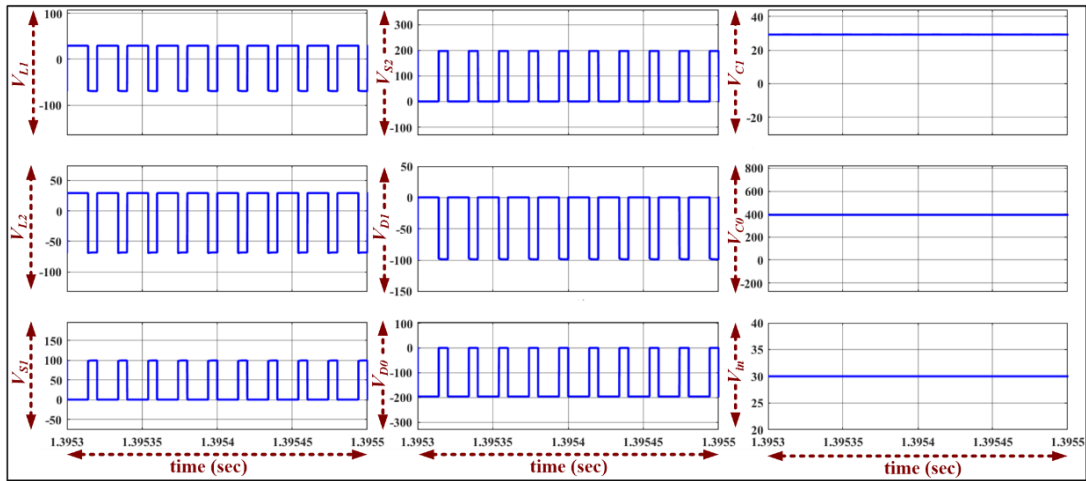


(a) Voltage waveforms
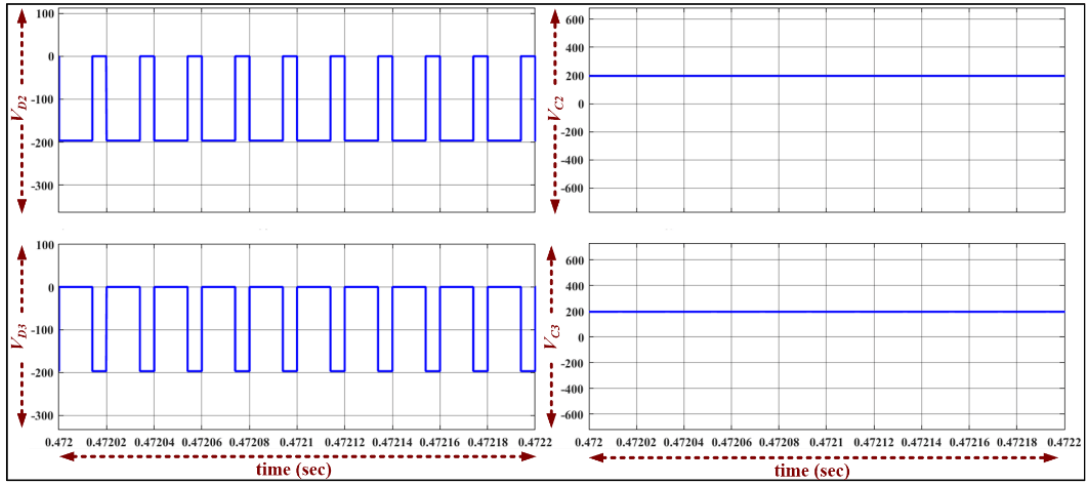
(b) Diodes $D_2$, $D_3$ and Capacitors $C_2$, $C_3$ Voltage waveforms
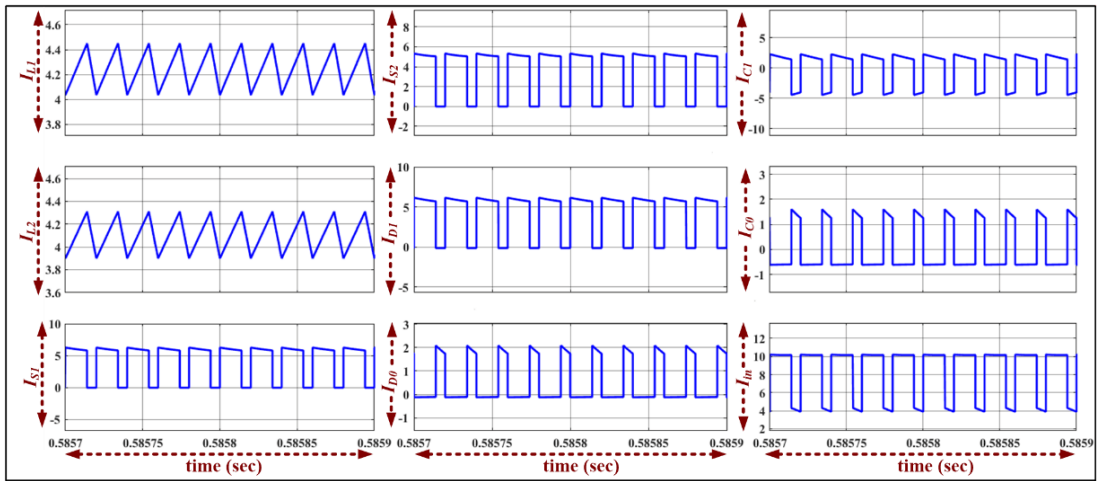


(c) Current waveforms

Figure 6.9. Simulation results

6.9 Hardware Implementation, Experimental Results, and Discussion

A 200W prototype of the proposed converter is developed and implemented in the laboratory to validate the theoretical analysis and performance of the converter. The designed prototype is shown in Fig. 6.10. A list of specifications for the different circuit components of the prototype is presented in Table 6.1.
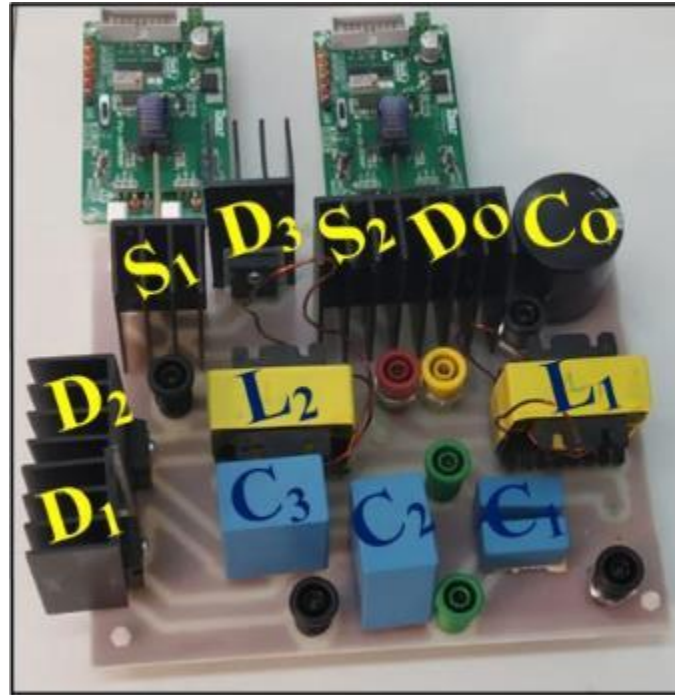
Figure 6.10. Designed 200 W prototype of the proposed converter.

Table 6.2. Design Considerations for the Proposed Converter

| Parameters | Prototype |
|---|---|
| Power | 200 W |
| Input Voltage ($V_{in}$) | 30 V (Ideal)/32V (expt.) |
| Duty ratio | 0.7 |
| Output Voltage ($V_0$) | 400 V |
| Load | 800 Ω |
| Switching Freq. | 100 kHz |
| Inductor $L_1$ and $L_2$ | ≈ 300 μH, 20A (shell type) |
| Capacitor $C_1$ | ≈ 50 μF, 400 V |
| Switches $S_1$, $S_2$ | $V_{DS}$ = 900 V, $i_D$ = 36 A, $R_{ON}$ = 65 mΩ (C3M0065090) |
| Diodes ($D_0$-$D_3$) | $V_{RRM}$ = 400 V, $i_F$ = 30 A, $R_{ON}$ = 0.01Ω, $V_F$ = 0.8 V (STTH30R04) |

Furthermore, the ultra-fast recovery diode STTH30R04 is used for all the diodes $D_1$, $D_2$, $D_3$, and $D_0$, and silicon carbide MOSFET C3M0065090 is used as the switches $S_1$ and $S_2$ for high switching operation and better efficiency. The experimental results are presented in Fig. 6.11 with the values of $V_{in}$ = 32V, $V_0$ = 400V, $f_s$ = 100 kHz, and $P_0$ = 200W. The experimentally obtained waveforms of input/output voltages and

currents are displayed in Fig. 6.11(a). The average values of output voltage and output current are observed as 399V and 480mA, while the input voltage with non-ideality and input current average values are observed as 31.5V and 6.3A. The input current is observed to be continuous and increasing with a constant slope in the ON-state and decreasing in the OFF-state because of charging and discharging of inductor $L_1$ and inductor $L_2$, respectively. The experimentally obtained waveforms of the currents through inductor $L_1$ and inductor $L_2$ along with the voltages across diode $D_1$ and capacitor $C_1$ are displayed in Fig. 6.11(b).



(a)                                      (b)
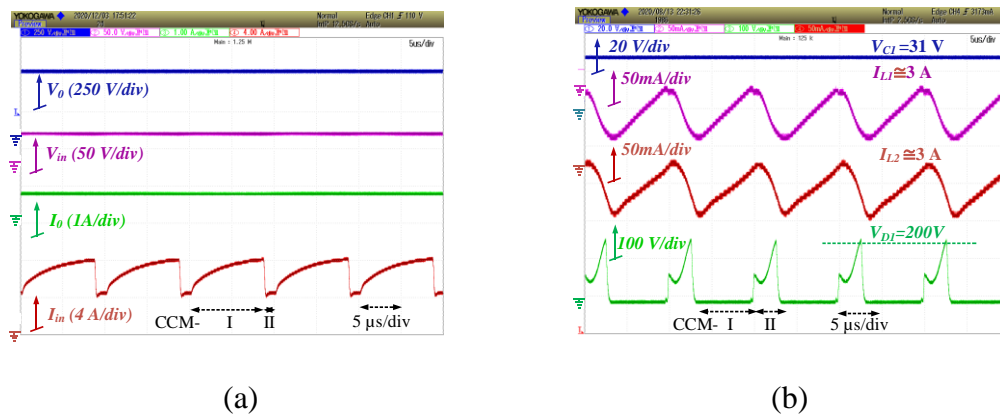
Figure 6.11. Experimentally resulted waveforms for the proposed converter (a) input/output currents and voltages, and (b) inductor currents, voltage across capacitor $C_1$ and diode $D_1$.

The average values of the inductor currents for inductor $L_1$ and inductor $L_2$ are observed as 3A and 3.2A, respectively. The experimentally obtained results for the inductor currents have an offset of 3.5A to show the inductor current ripples. The diode $D_1$ is observed to be forward-biased in the ON state and reversed biased in the OFF state. The PIV across diode $D_1$ is 25% of the output voltage and its value is equal to (-100V). Fluctuations in voltage waveform are observed for the diode $D_1$ due to the practical mismatch of inductance value ($L_1$ and $L_2$). The voltage across capacitor $C_1$ is observed as 31V which is almost the same as input voltage. In order to refer and validate

the experimentally obtained waveforms of the voltages across diodes $D_2$, $D_3$, and $D_0$, the waveform of the output current $I_0$ is also displayed in Fig. 6.12(a). The PIV across all the diodes $D_2$, $D_3$, and $D_0$ is 50% of the output voltage i.e. -200V. The value of average output current is observed as 480mA. Fig. 6.12(b) displays the experimentally obtained waveforms of the voltages across capacitors $C_2$, $C_3$, and $C_0$ and waveform of the input current $I_{in}$ in order to refer and validate. The voltages across capacitors $C_2$, $C_3$, and $C_0$ are observed as 199V, 198V, and 398V respectively. Fig. 6.12(c) presents the experimentally obtained waveforms of the currents through switches $S_1$ and $S_2$ and the voltage across switch $S_2$, the output voltage is also shown for reference and validation purposes. The maximum value of switch voltage stress across $S_2$ is observed as 200V in $CCM_2$ which is 50% of the output voltage value. The currents through the switches $S_1$ and $S_2$ are observed to be almost same. Fig. 6.12(d) shows the dynamic behavior of the proposed converter with a change in input voltage at the constant duty ratio and load. It is observed from the experimentally obtained results, that the proposed system gives stable output voltage and current.
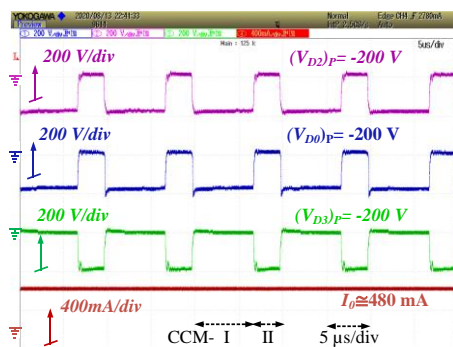


(a)
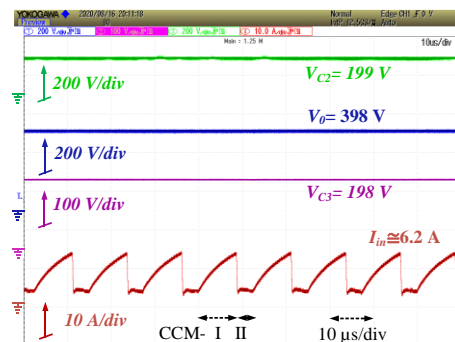


(b)
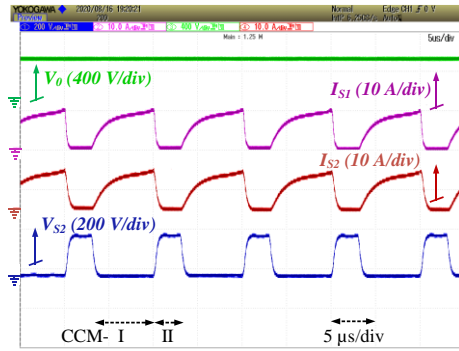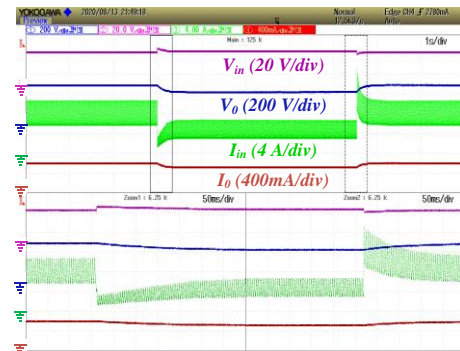
(c)                                                    (d)

Figure 6.12. Experimental waveform of (a) voltage across diode $D_2$, $D_0$, $D_3$ and output current (b) voltage across capacitor $C_2$, $C_3$, $C_0$ and input current, (c) switch voltage and switch current stress for $S_1$ and $S_2$ and (d) dynamic variation of input-output voltage and current with change in duty ratio from 0.6 to 0.5 to 0.6.

A disturbance is initiated from the load and source sides to analyze the proposed converter's performance in disturbed condition. The reference of output voltage is set at 400V and the dynamic response of the system is verified by varying the input voltage and the step change in the load resistance as shown in Fig. 6.13(a) and Fig. 6.13(b), respectively. As seen from Fig. 6.13(a), constant output voltage 400V is achieved even when the input voltage varies from the 32V to 40V at the constant power (fixed load resistance). It is observed that, there is no spike in input current during the transition. Similarly, the load resistance is changed to examine the stability of the proposed converter in closed loop to achieve the constant output voltage 400.19V as shown in Fig. 6.13(b). Here, the load current is varying from 0.03mA to 0.48mA to 0.6mA and the change in the input current can assure the power balance between the input and the output.
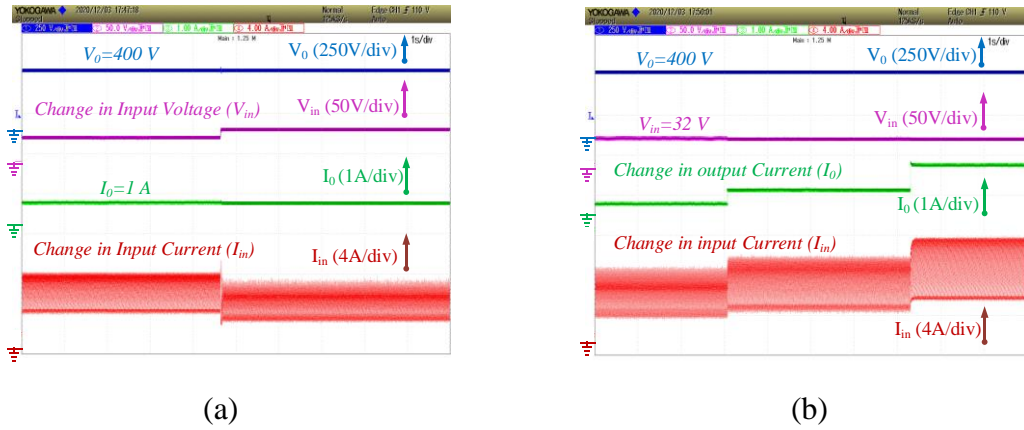
Figure 6.13. Dynamic variation of input-output voltage and current with change in (a) input voltage at constant load and (b) change in load at constant input voltage.

The theoretically and experimentally achieved voltage gain of the proposed converter is shown in Fig. 6.14(a). The parasitic internal resistance of different circuit components is the main cause of the difference between theoretical and experimentally achieved voltage gain values. It can be observed from the mathematical analysis, that the drop in voltage gain is inversely proportional to the input voltage. Hence with increase in the input voltage, the drop in the output voltage is decreasing. The conduction loss in the proposed converter depends on the current through each of the components and most of the current through each component directly depends on the input current. Hence at a constant power, the input current is decreasing with increase in the input voltage. Therefore, from mathematical analysis at different input voltages with constant power, the proposed converter is experimentally verified and the observed efficiency at different input voltages is plotted in the Fig. 6.14(b). It can be observed that, the maximum efficiency achieved by the proposed converter is 96.5% at the 200W power with 32V as input voltage.
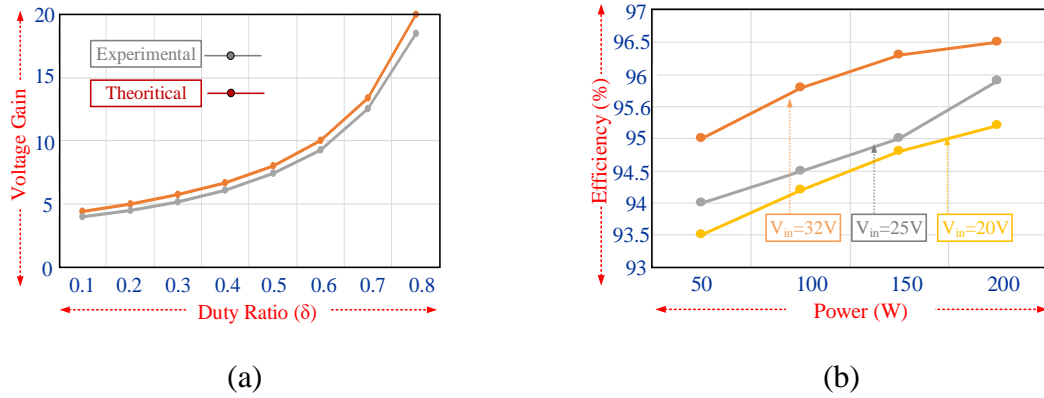
Figure 6.14. (a) Voltage gain comparison between theoretical and experimental value and (b) efficiency with respect to output power for the proposed converter.

## 6.10 Comparison of Different Topologies

In this section, a comparative study of the proposed converter with other similar high gain converter structures is presented, such as the multilevel boost converter [155], non-isolated DC-DC boost converter with voltage-lift technique [154], Traditional switched inductor based DC-DC boost converter [122], converter-I in [148], modified SEPIC converter in [153], ASL-SU2C-VO-conguration [156], and modified SEPIC converter (MSC) [157]. The number of components, normalized voltage stress across the switches, switch current stress, efficiency at rated power, and the gain in voltage for these converters are presented in Table 6.3.

The proposed converter achieves a higher voltage gain as compared to the topologies presented in [154], [122], [148], [153], [156], [157] and [155] for the same duty cycle range. Therefore, small voltage rating active switches having small ON-state resistance can be used in the circuit, which leads to the reduction of cost. The converters presented in [122], [153], and [157] utilizes only one power switch. However, high voltage stress has been generated across the switch and the voltage gain is lower than the topology proposed. The number of diodes used in the converters [154] and [122] is the same as the proposed converter. However, their voltage gain is lower

and the switch voltage stress is higher than the proposed converter. Table 6.3 indicates that the proposed converter provides a lesser switch voltage stress as compared to the converters in [154], [122], [148], [153], [156], and [157]. The efficiency of the proposed converter is observed to be higher than all the other converters. The efficiency of a converter depends on different factors such as the components count, their types, and voltage/current ratings. The comparison with regards to switch current stress among the different converters indicates that the proposed converter has the lowest switch current stress through the active switches and the value is half the value of input current. Hence, active switches with low current rating are required as the total input current is shared by these two active switches. Generally, the increase in the rating of a device leads to an increment in its ON-state resistance. The proposed converter topology requires lower rating components and hence it comes up with a low-cost design and generates higher efficiency.

A: Traditional Boost Converter, B: multilevel boost converter [155], C: non-isolated DC-DC boost converter with voltage-lift technique [154], D: Traditional switched inductor based DC-DC boost converter [122], E: converter-I in [148], F: modified SEPIC converter in [153], G: qZS-BCVLSI-configuration [156], H: modified SEPIC converter (MSC) [157], I: proposed converter.

Table 6.3. Comparative Study of the Proposed Converter with other Existing DC-DC Converters

| Conv. | Reactive components count | | Semiconductor Components count | | Total compo nents | CCM Voltage gain (M) | Normalized Switch voltage stress | Switch current stress | Efficiency | Output port |
|---|---|---|---|---|---|---|---|---|---|---|
| | Inductor | Capacitor | Switches | Diodes | | | | | | |
| A | 1 | 1 | 1 | 1 | 4 | $1/(1-\delta)$ | 1 | $I_{in}$ | - | Grounded |
| B | 1 | 3 | 1 | 3 | 8 | $2/(1-\delta)$ | 1/2 | $I_{in}+I_{C1}$ | 94.6% at 100W | Grounded |
| C | 2 | 2 | 2 | 4 | 10 | $(1+\delta)/\delta(1-\delta)$ | $1/(1-\delta)M$ | $2I_{in}/1+\delta$ | - | Grounded |
| D | 2 | 1 | 1 | 4 | 8 | $(1+\delta)/(1-\delta)$ | 1 | $I_{in}$ | 95.2% at 50W | Grounded |
| E | 2 | 1 | 2 | 1 | 6 | $(1+\delta)/(1-\delta)$ | $(1+M)/M$ | $2I_{in}/1+\delta$ | 92.7% at 40W | Floating |
| F | 2 | 3 | 1 | 2 | 8 | $(1+\delta)/(1-\delta)$ | $(1+M)/2M$ | $I_{in}$ | 92.2% at 100W | Grounded |
| G | 3 | 4 | 1 | 4 | 12 | $(3+\delta)/(1-\delta)$ | $M/(3+\delta)$ | $I_{in}+I_{C1}$ | 94.4% at 250W | Floating |
| H | 3 | 3 | 1 | 3 | 10 | $\delta/(1-\delta)^2$ | 1 | $I_{in}+I_{C1}+I_{C2}$ | 91.4% at 100W | Grounded |
| I | 2 | 4 | 2 | 4 | 12 | $4/(1-\delta)$ | 1/2, 1/2 | $I_{in}/2,$ $I_{in}/2$ | 96.5% at 200W | Grounded |

From Fig. 6.15, the proposed converter is observed to be providing a higher gain in voltage in comparison with the converters presented in [122], [148], [153], [156], [157] and [155]. Furthermore, the output and input of the proposed converter and the converters in [154], [122], [153], and [155] are at common ground, while the rest of the other converters are suitable for floating load conditions only.
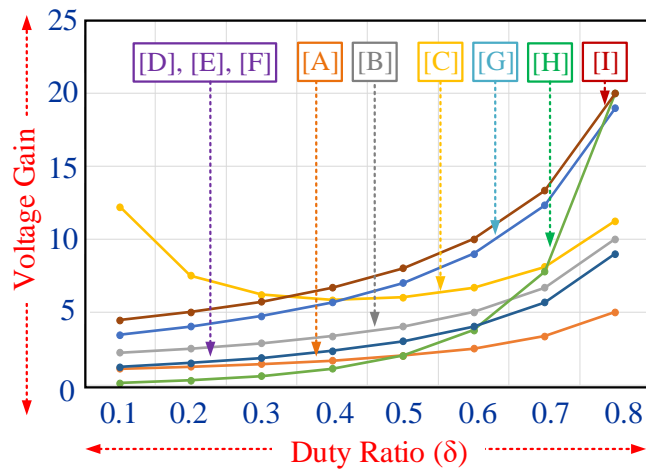


Figure 6.15. A Comparative graphical representation of the proposed converter with different converters for the voltage gain with respect to duty ratio.

From the comparative analysis, the proposed converter is observed to be providing a reduced value of switch voltage and switch current stresses in comparison with the other converters. Hence, small voltage rating active switches having small ON-state resistance can be used in the circuit. The proposed converter can attain a high voltage gain and an improved efficiency as compared to the other converters. Furthermore, the common ground connection of source and load in the proposed converter circuit makes it highly suitable for solar PV applications.

## 6.11 Summary

The DC-DC high gain boost converter with active switched inductor network has been presented in this chapter. The proposed converter has utilized two switches to reduce the current stress. The active switched inductor network and voltage multiplier

structure have been effectively arranged to boost the output voltage and for the equal distribution of capacitor voltage stress. Furthermore, the presented topology drains a continuous current from the input supply. Hence, high-voltage boost ability and continuous input current make it suitable for PV and fuel cell applications. A detailed CCM and DCM analysis of the proposed converter has been presented along with the discussion about their boundary conditions. The theoretical and mathematical analysis has been validated by the experimental results. The converter has been regulated at different duty cycle values to test and verify its performance and the peak efficiency is achieved by the proposed converter at 200 W and its value is 96.5%.

CHAPTER 7: DOUBLE STAGE CONVERTER WITH LOW CURRENT STRESS

FOR NANOGRID

## 7.1 Introduction

A low to high voltage conversion technique using double stages of switched inductors for Nanogrid applications has been presented in this chapter. The proposed converter topology utilizes fewer components, achieves high voltage gain at a small value of duty ratio, and has high efficiency. Moreover, the proposed converter provides a reduced switch current stress to obtain a stable constant boosted DC voltage. Therefore, it requires low-current rating switches and hence leads to cost reduction. Additionally, the load and the source end are connected to the same ground. The principle of operation, theoretical waveforms in Continuous Conduction Mode (CCM), and Discontinuous Conduction Mode (DCM) with steady-state analysis are discussed. A detailed discussion about the effect of non-idealities on the high voltage conversion, the design of components, and a comparison of the performance characteristics such as the number of components, Voltage Gain in CCM, switch current stress, normalized switch voltage stress, and efficiency of the proposed converter topology with other converters are presented. The experimental results of the 500W laboratory prototype are also shown to validate the operation of the proposed converter.

The proposed converter utilizes a very simple structure incorporating very few components and provides very high efficiency. The proposed converter draws a continuous input current from the input source with low ripple and achieves a higher voltage gain at a small value of duty ratio. The proposed converter provides a reduced switch current stress to obtain a constant DC step-up voltage. Therefore, it requires switches with low-current rating, since the two switches equally share the total input current. Normally, as the rating of a device increases its ON-state resistance increases.

It is observed that lower rating components are required for the proposed converter and hence it is a low-cost design. The active switches of the proposed converter have low conduction loss, its design is transformer-less, and has a simplified control. Moreover, the load and source end of the proposed converter has a common ground connection. Therefore, for this converter to be used in PV systems, common-mode voltage and leakage reduction techniques are not required, and hence making the proposed converter is highly suitable for integration of solar PV panels with the DC Nanogrid system at the 400 V bus.

## 7.2 Power Circuit Topology

Fig. 7.1 shows the proposed double stage converter power circuitry for Nanogrid low to high voltage conversion. It comprises two active switches $S_1$ and $S_2$, two inductors $L_1$ and $L_2$, diodes $D_1$ and $D_2$, two capacitors $C_1$ and $C_2$, and a load $R$. The switching frequency at which the switch $S_1$ and switch $S_2$ are being turned ON and OFF is indicated by $f_S$.
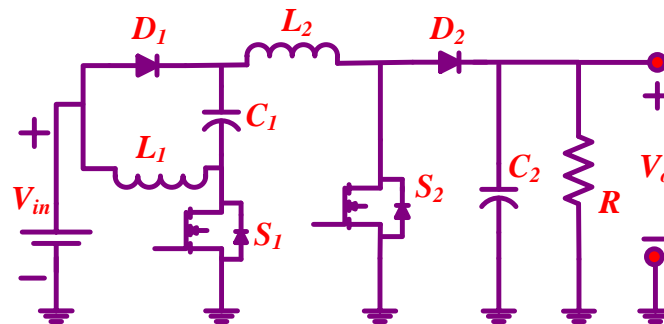


Figure 7.1. Power circuitry of the proposed converter.

To discuss the steady-state operational theory of the proposed converter, the circuit elements are considered ideal. The equivalent series resistance (ESR) effects of the inductors and capacitors, ON-state switch resistance, and forward voltage drop across the diodes have not been taken into account. Also, for the output voltage to remain constant, the capacitance value of the output capacitor $C_2$ is considered to be

large enough. The value of inductance for both the inductors $L_1$ and $L_2$ is assumed to be equal. Therefore,

$$L = L_1 = L_2 \tag{7.1}$$

The steady-state mathematical analysis in CCM and DCM and the principle of operation are discussed below. The CCM and DCM characteristics waveforms for the proposed converter are displayed in Fig. 7.2.

### 7.3 Working principle and analysis in CCM

The two working modes involved in the Continuous Conduction Mode (CCM) of the proposed converter are explained in this section, and the equivalent circuit is depicted in Fig. 7.3. During one switching period $T_S$, both the switches of the proposed converter are simultaneously operated using the same values of duty pulse as well as the duty ratio. Hence, there are two working modes in CCM: $CCM_I$ and $CCM_{II}$ for the proposed converter. Both the switches ($S_1$ and $S_2$) are ON in $CCM_I$, while switches ($S_1$ and $S_2$) are at OFF position in $CCM_{II}$.

$CCM_I$: Fig. 7.3(a) shows the power circuit for this mode. Both the switches $S_1$ and $S_2$ are at ON position during this mode. The input voltage supply ($V_{in}$) charges inductor $L_1$ (via switch $S_1$), the capacitor $C_1$ (via diode $D_1$ and switch $S_1$), and inductor $L_2$ (via $D_1$ and $S_2$), and the energy of the capacitor $C_2$ is supplied to the load ($R$). Diode $D_1$ is forward biased, and diode $D_2$ is reversed biased. It is observed that the input voltage ($V_{in}$) charges both the inductors ($L_1$ and $L_2$) and the capacitor $C_1$ in parallel. Therefore, in this mode, the inductors $L_1$ and $L_2$ voltages/currents are indicated by the following expressions:

$$V_L = V_{L1} = V_{L2} = V_{C1} = V_{in}, \ \ V_{C2} = V_o \tag{7.2}$$

$$I_{in} = I_{L1} + I_{L2} + I_{C1}, \ I_{C2} = -I_o \approx -\frac{V_o}{R} \tag{7.3}$$

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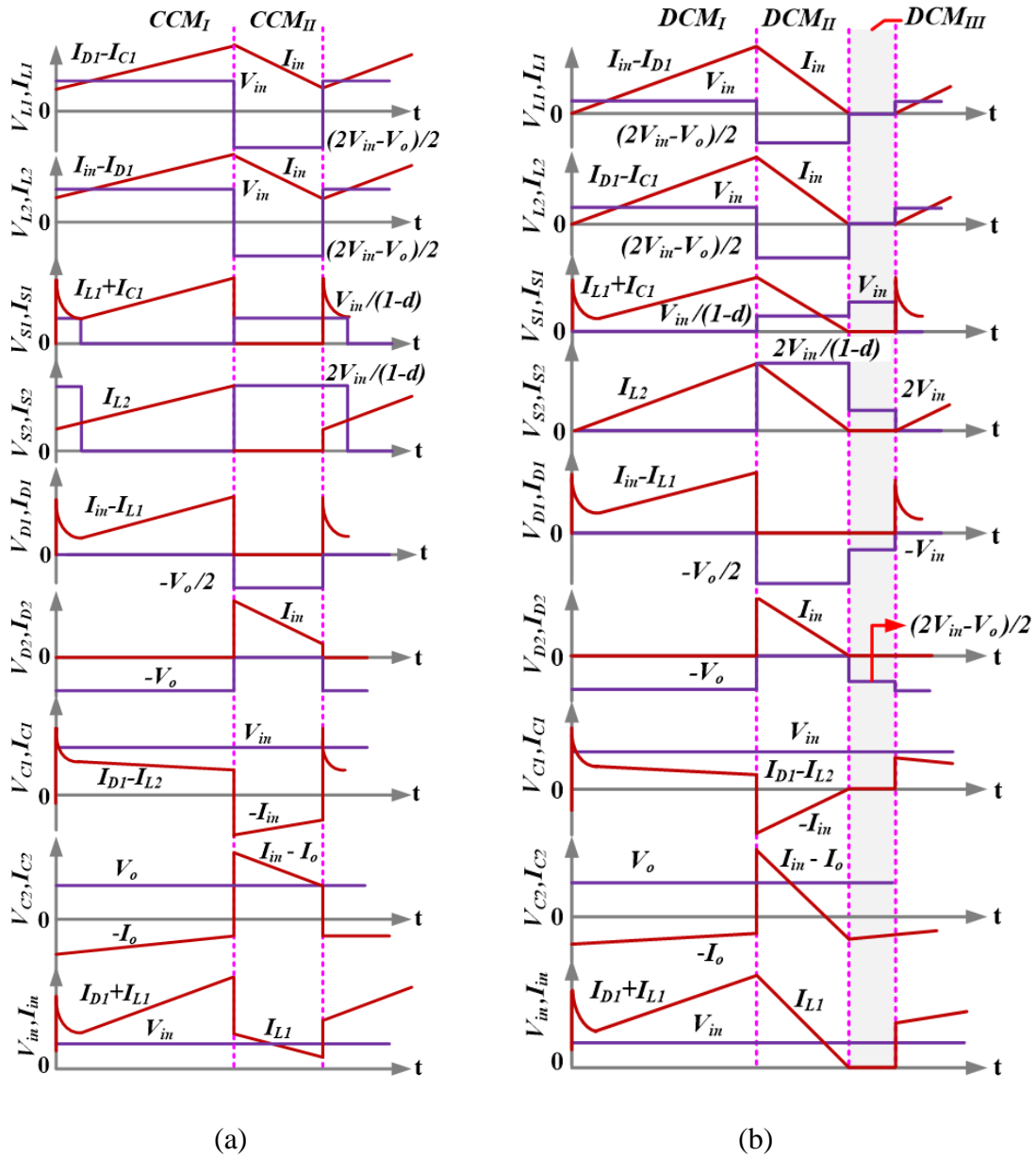
Figure 7.2. Typical characteristics waveforms indicating the variations in voltages and currents for different circuit components with respect to time in (a) CCM, (b) DCM. *The units for all the given voltages are Volts, for all the given currents are Ampere, and for all the given times are Second.

Table 7.1 briefly summarizes the Operating Principle in both CCM and DCM (*Ch.: Chraged, D/Ch.: Discharged, ZC: Zero current, FB: Forward Biased, RB: Reversed Biased).

Table 7.1. Operating Principle in CCM and DCM

| Operating Modes | | Time | Switches | | Inductors | | Capacitors | | Diodes | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $S_1$ | $S_2$ | $L_1$ | $L_2$ | $C_1$ | $C_2$ | $D_1$ | $D_2$ |
| CCM | $CCM_I$ | $T_{ON}$ | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | FB | RB |
| | $CCM_{II}$ | $T_{OFF}$ | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | RB | FB |
| DCM | $DCM_I$ | $K_I T_S$ | ON | ON | Ch. in parallel | Ch. in parallel | Ch. in parallel | D/Ch. | FB | RB |
| | $DCM_{II}$ | $K_{II} T_S$ | OFF | OFF | D/Ch. in series | D/Ch. in series | D/Ch. in series | Ch. | RB | FB |
| | $DCM_{III}$ | $K_{III} T_S$ | OFF | OFF | ZC | ZC | ZC | D/Ch. | RB | RB |

Where output voltage (average) is indicated by $V_o$, the input current is indicated by $I_{in}$, the output current is indicated by $I_o$, voltages across capacitors $C_1$ and $C_2$ are indicated by $V_{C1}$ and $V_{C2}$, and currents through capacitors $C_1$ and $C_2$ are indicated by $I_{C1}$ and $I_{C2}$, the currents through the inductors $L_1$ and $L_2$ are indicated by $I_{L1}$ and $I_{L2}$, the voltages across inductors $L_1$ and $L_2$ are indicated by $V_{L1}$ and $V_{L2}$, respectively.

The switches $S_1$ and $S_2$ voltages/currents are indicated by the following expression:

$$V_S = V_{S1} = V_{S2} = 0, \ I_{S1} = I_{L1} + I_{C1}, I_{S2} = I_{L2} \tag{7.4}$$

$CCM_{II}$: The power circuitry of this mode is shown in Fig. 7.3(b). Both switch $S_1$ and switch $S_2$ are being turned OFF simultaneously during this mode. During this mode, the output capacitor $C_2$ is charged by the series combination of input voltage supply ($V_{in}$), inductor $L_1$, capacitor $C_1$, inductor $L_2$. Also, via diode $D_2$, the input side energy is supplied to the load $R$. In this mode, Diode $D_2$ and diode $D_1$ are forward and

reversed biased, respectively. Therefore, in this mode, inductors $L_1$ and $L_2$ voltages/currents are indicated by the following expressions:

$$V_L = V_{L1} = V_{L2} = \frac{2V_{in} - V_o}{2}, \quad V_{C2} = V_o \tag{7.5}$$

$$I_L = I_{L1} = I_{L2} = I_{in} = I_{C1}, \quad I_{C2} \approx I_L - \frac{V_o}{R} \tag{7.6}$$



(a)                                      (b)
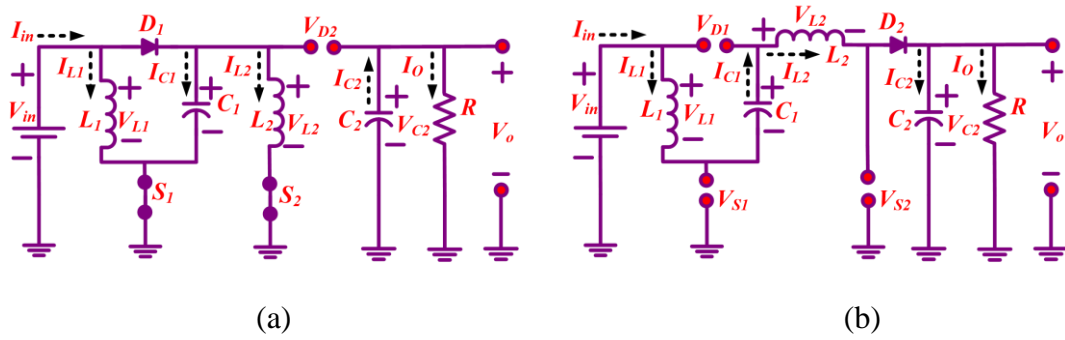
Figure 7.3. Operating modes in CCM (a) $CCM_I$ and (b) $CCM_{II}$.

The switches S1 and S2 voltages/currents are indicated by the following expressions:

$$\begin{cases} V_{S1} = \dfrac{V_{in}}{(1-d)}, \quad V_{S2} = \dfrac{2V_{in}}{(1-d)}, \\[2mm] I_{S1} = I_{S2} = 0 \end{cases} \tag{7.7}$$

Therefore, the gain in voltage for the proposed converter in CCM is shown as,

$$M_{CCM} = V_o / V_{in} = 2 / \ 1-d \tag{7.8}$$

Where ($d$) is the duty cycle of the proposed converter and ($M$) is the gain in voltage and the voltage gain for CCM (Continuous Conduction Mode) is indicated as $M_{CCM}$.

7.4 Working principle and Analysis in DCM

Discontinuous Conduction Mode (DCM) has three modes of operation: $DCM_I$, $DCM_{II}$, and $DCM_{III}$ for the proposed converter. In $DCM_I$, both the switches $S_1$ and $S_2$

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are at ON position, in $DCM_{II}$ switches $S_1$ and $S_2$ are at OFF position with the inductor currents having a non-zero value, and in $DCM_{III}$, switch $S_1$ and switch $S_2$ are at OFF position with inductor current values equal to zero. The three working modes involved in the DCM of the proposed converter are explained in this section, and power circuitry for $DCM_{III}$ is depicted in Fig. 7.4. The characteristic waveform of DCM is displayed in Fig. 7.2(b), where $K_I T_S$ is the time period for $DCM_I$, $K_{II} T_S$ is the time period for $DCM_{II}$, and $K_{III} T_S$ is the time period for $DCM_{III}$; $K_I$, $K_{II}$, and $K_{III}$ are the constant multiples of the time period for $DCM_I$, $DCM_{II}$, and $DCM_{III}$, respectively.

$DCM_I$: The proposed converter's operating principle and power circuit in $DCM_I$ are the same as that in $CCM_I$; both the switches ($S_1$ and $S_2$) are at ON position. The input voltage ($V_{in}$) is charging both the inductors ($L_1$ and $L_2$) and the capacitor $C_1$ in parallel. In this mode, the inductors ($L_1$ and $L_2$) currents initiated at zero value and reached a maximum value at the end. The maximum current values through $L_1$ and $L_2$ can be obtained from the following expression:

$$I_{L\max} = I_{L1\max} = I_{L2\max} = V_{in}K_I \ / \ Lf_s \tag{7.9}$$

Where the maximum value of inductor ($L_1$ and $L_2$) currents are indicated by $I_{L1max}$ and $I_{L2max}$, respectively, and $f_S = 1/T_S$ indicates the switching frequency. The inductors $L_1$ and $L_2$ ripple currents can be shown as,

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = V_{in}K_I \ / \ Lf_s \tag{7.10}$$

where the inductors ($L_1$ and $L_2$) ripple currents are indicated by $\Delta I_{L1}$ and $\Delta I_{L2}$, respectively.

$DCM_{II}$: The proposed converter's operating principle and power circuit in $DCM_{II}$ are the same as that in $CCM_{II}$; switch $S_1$ and switch $S_2$ are at OFF position with non-zero inductor currents. The output capacitor $C_2$ is charged by the series combination of input voltage supply ($V_{in}$), inductor $L_1$, capacitor $C_1$, inductor $L_2$. Via

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diode $D_2$, energy is supplied to the load $R$. In this mode, the inductors $L_1$ and $L_2$ currents started initially from a maximum value and reached a zero value at the end. The maximum currents flowing through inductors $L_1$ and $L_2$ can be obtained from the following expression:

$$I_{L\max} = I_{L1\max} = I_{L2\max} = \left(2V_{in} - V_o\right)K_{II} / 2Lf_s \qquad (7.11)$$

The inductors $L_1$ and $L_2$ ripple currents can be shown as,

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = \left(2V_{in} - V_o\right)K_{II} / 2Lf_s \qquad (7.12)$$

*DCM$_{III}$:* The equivalent circuit of the proposed converter in *DCM$_{III}$* is displayed in Fig. 7.4. In this mode, switches $S_1$ and $S_2$ are at the OFF position with zero inductor current values.
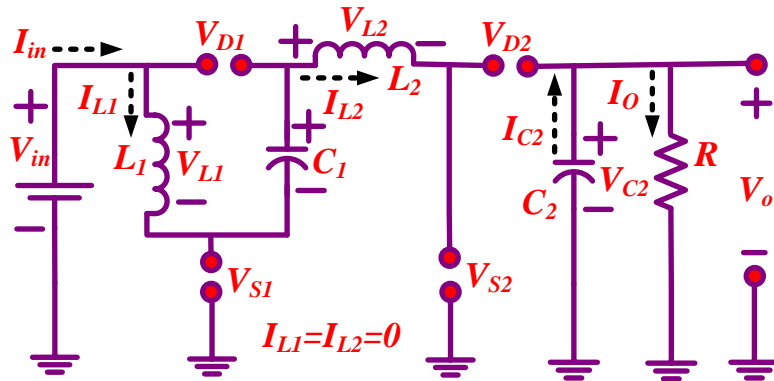


Figure 7.4. Power circuitry of the proposed converter in *DCM$_{III}$*.

Therefore, both the inductors $L_1$ and $L_2$ are completely de-energized. Both the diodes ($D_1$ and $D_2$) are reversed biased in this mode and the energy stored in the output capacitor $C_2$ only is supplied to the load $R$. From Eqs. (7.9) and (7.11) $K_{II}$ is shown by the following expression:

$$K_{II} = \frac{2V_{in}K_I}{2V_{in} - V_o} \qquad (7.13)$$

The average current through the output capacitor $C_2$ for one switching period can be obtained as follows,

$$I_{C2} = \frac{1}{2} K_{II} I_{Lmax} - I_o = \frac{1}{2} K_{II} I_{Lmax} - \frac{V_o}{R_o} \tag{7.14}$$

From Eqs. (7.9), (7.13), & (7.14)

$$I_{C2} = \frac{V_{in} K_I^2 T_S}{2V_{in} - V_o} \frac{1}{L} - \frac{V_o}{R} \tag{7.15}$$

In steady-state conditions, the average current flowing through a capacitor is always zero, hence Eq. (7.15) can also be written as,

$$\frac{V_{in} K_I^2 T_S}{2V_{in} - V_o} \frac{1}{L} = \frac{V_o}{R} \tag{7.16}$$

From (7.16), the quadratic equation obtained is as follows,

$$\left(\frac{V_o}{V_{in}}\right)^2 - \frac{V_o}{V_{in}} - \frac{K_I^2}{\xi_L} = 0 \tag{7.17}$$

Where normalized time constant ($\xi_L$) for the inductor $L_1$ and inductor $L_2$ and is expressed as $\xi_L = L/RT_S$. Hence, the value of ($\xi_L$) changes with the change in $L$, $R$, and $T_S$. The gain in voltage for the proposed converter in DCM is indicated by $M_{DCM}$ and can be expressed as,

$$M_{DCM} = \frac{V_o}{V_{in}} = 1 + \left(\frac{\xi_L + K_I^2}{\xi_L}\right)^{1/2} = 1 + \left(1 + \frac{K_I^2 R}{Lf_s}\right)^{1/2} \tag{7.18}$$

The switching frequency is indicated by $f_S$. When the gain in CCM is equal to the gain in DCM, a boundary condition is reached. Thus, from Eqs. (7.8) and (7.18),

$$1 + \left(1 + \frac{K_I^2 R}{Lf_s}\right)^{1/2} = \frac{2}{1-d} \tag{7.19}$$

Now, as we know that the mode $CCM_I$ is the same as that of mode $DCM_I$ i.e. $d$

$= K_I$. Therefore, the normalized time constant at the boundary conditions ($\xi_{Lb}$) for the inductors ($L_1$ and $L_2$) is shown by the following expression,

$$\xi_{Lb} = d \times \frac{1+d^2-2d}{4} \tag{7.20}$$

Fig. 7.5 illustrates the variation of ($\xi_{Lb}$) with the variation in duty cycle ($d$) for the proposed converter. It is important to note that, the proposed converter works in CCM for the values of ($\xi_L$) greater than ($\xi_{Lb}$).
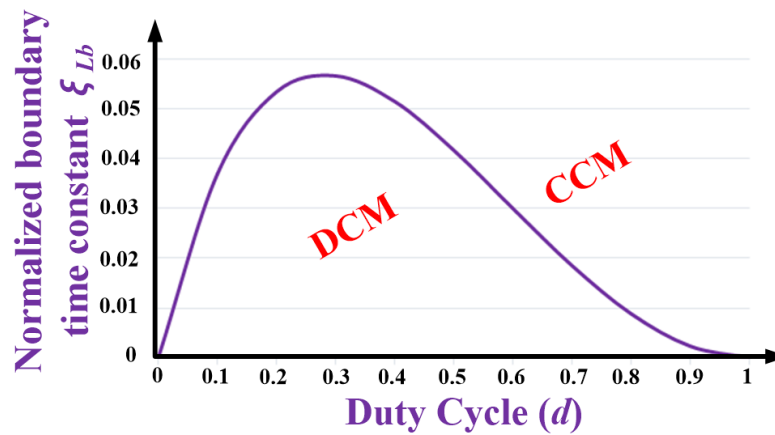


Figure 7.5. Normalized boundary condition.

### 7.5 Effects of Non-idealities on Voltage Gain

The proposed converter's power circuit with consideration of the non-idealities of the circuit elements to study their effect on voltage gain is shown in Fig. 7.6. The ESR of inductors $L_1$ and $L_2$ is denoted as $r_L$. The non-ideality of the diodes is represented by their internal resistance ($r_D$) and the threshold voltage ($V_{FD}$). Hence, the non-ideality of diodes $D_1$ and $D_2$ is represented with their respective internal resistance and forward voltage drop as shown in Fig. 7.6. Similarly, switches $S_1$ and $S_2$ are represented with their internal resistance $r_S$. The ESR for the capacitors $C_1$ and $C_2$ are represented with their internal resistance $r_C$.
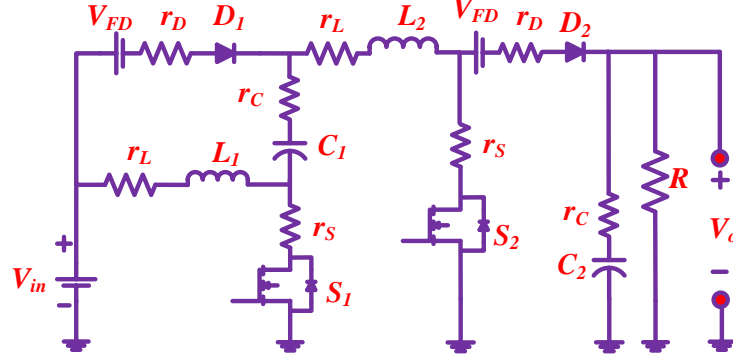
Figure 7.6. Proposed converter with non-ideality characteristics.

### 7.5.1. Effect of ESR of Inductors on Voltage Gain

The effect of the inductor's ESR on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the ESR of both the inductors is assumed to be equal i.e. $r_{L1} \approx r_{L2} \approx r_L$. Therefore, the inductors $L_1$ and $L_2$ voltages in $CCM_I$ and $CCM_{II}$ can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in} - I_{L1}r_L, V_{L2} \approx V_{in} - I_{L2}r_L \tag{7.21}$$

$$CCM_{II} : V_{L1} \approx V_{in} - I_{L1}r_L - \frac{V_o}{2}, V_{L2} \approx V_{in} - I_{L2}r_L - \frac{V_o}{2} \tag{7.22}$$

From (7.21) and (7.22),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - I_{L1}r_L - I_{L2}r_L \tag{7.23}$$

$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - I_{L1}r_L - I_{L2}r_L - V_o \tag{7.24}$$

Considering inductor volt second balance principle and small approximation technique,

$$2V_{in} - I_{L1}r_L - I_{L2}r_L \ d = - \ 2V_{in} - I_{L1}r_L - I_{L2}r_L - V_o \ (1-d) \tag{7.25}$$

The expression of voltage gain for the proposed converter with consideration of the effect of the inductor's ESR is expressed as,

$$\frac{V_o}{V_{in}}\bigg|_{r_L} = \frac{2 - \frac{r_L}{V_{in}} \quad I_{L1} + I_{L2}}{1-d} \tag{7.26}$$

Now, on the assumption of $V_{DL}$ as the ESR voltage drop across the inductors (i.e. $I_{L1}r_L$ and $I_{L2}r_L$ are equal to $V_{DL}$), (7.26) can be expressed as,

$$\frac{V_o}{V_{in}}\bigg|_{r_L} = \frac{2\left(1 - \frac{V_{DL}}{V_{in}}\right)}{1-d} = \frac{2}{1-d} - \frac{2}{V_{in}} \frac{V_{DL}}{1-d} \tag{7.27}$$

It is noticed from (7.26)–(7.27) that, with greater values of $V_{DL}$ and $d$ the voltage gain declines drastically. It indicates that the duty cycle and inductor's ESR should have a small value.

### 7.5.2. Effect of ESR of Diodes on Voltage Gain

The effect of the non-ideality of the diode on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the following non-idealities are assumed: $r_{D1} \approx r_{D2} \approx r_D$ and $V_{FD1} \approx V_{FD2} \approx V_{FD}$. Therefore, the voltages across the inductors $L_1$ and $L_2$ in $CCM_I$ and $CCM_{II}$ can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in}, V_{L2} \approx V_{in} - I_{D1}r_D - V_{FD} \tag{7.28}$$

$$CCM_{II} : V_{L1} \approx V_{L2} \approx V_{in} - \frac{I_{D2}r_D + V_{FD} + V_o}{2} \tag{7.29}$$

From (7.28) and (7.29),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - I_{D1}r_D - V_{FD} \tag{7.30}$$

$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - I_{D2}r_D - V_{FD} - V_o \tag{7.31}$$

Considering inductor-volt-second-balance principle and smallapproximation technique,

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$$\left(2V_{in} - I_{D1}r_D - V_{FD}\right) d = -\left(2V_{in} - I_{D2}r_D - V_{FD} - V_o\right) (1-d) \qquad (7.32)$$

The voltage gain expression for the proposed converter by considering the effect of diodes ($D_1$ and $D_2$) ESR can be obtained as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_D,\ V_{FD}} = \frac{2 - \dfrac{V_{FD}}{V_{in}} - d\dfrac{r_D}{V_{in}}I_{D1} - (1-d)\dfrac{r_D}{V_{in}}I_{D2}}{1-d} \qquad (7.33)$$

Now, on the assumption of $V_D$ as the forward resistance voltage drop across the diodes (i.e. $I_{D1}r_D$ and $I_{D2}r_D$ are equal to $V_D$), (7.33) can be shown as,

$$\left.\frac{V_o}{V_{in}}\right|_{r_D,\ V_{FD}} = \frac{2 - \dfrac{1}{V_{in}}\left(V_{FD} + V_D\right)}{1-d} = \frac{2}{1-d} - \frac{V_{FD} + V_D}{V_{in}}\frac{1}{1-d} \qquad (7.34)$$

It is noticed from (7.33)–(7.34) that, with greater values of $V_D$ and $d$ the voltage gain declines drastically. It indicates that the threshold voltage ($V_{FD}$) and the internal forward resistance of the diodes should have a small value.

### 7.5.3. Effect of ESR of Switches on Voltage gain

The effect of ESR of switches on voltage gain is analyzed by neglecting the parasitic irregularities caused by the other components. For the mathematical analysis, the internal forward resistance of switches is assumed to be equal i.e. $r_{S1} \approx r_{S2} \approx r_S$. Therefore, the voltages across the inductors $L_1$ and $L_2$ in $CCM_I$ and $CCM_{II}$ can be obtained by using the following expressions,

$$CCM_I : V_{L1} \approx V_{in} - I_{S1}r_S, V_{L2} \approx V_{in} - I_{S2}r_S \qquad (7.35)$$

$$CCM_{II} : V_{L1} \approx V_{in} - \frac{V_o}{2}, V_{L2} \approx V_{in} - \frac{V_o}{2} \qquad (7.36)$$

From (7.35) and (7.36),

$$CCM_I : V_{L1} + V_{L2} \approx 2V_{in} - \left(I_{S1} + I_{S2}\right)r_S \qquad (7.37)$$

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$$CCM_{II} : V_{L1} + V_{L2} \approx 2V_{in} - V_o \tag{7.38}$$

Considering inductor volt second balance principle and small approximation technique,

$$\left[ 2V_{in} - \left( I_{S1} + I_{S2} \right) r_S \right] d = -\left( 2V_{in} - V_o \right) \left( 1 - d \right) \tag{7.39}$$

The expression of voltage gain for the proposed converter with consideration of the effect of switches $S_1$ and $S_2$ ESR can be obtained as,

$$\left. \frac{V_o}{V_{in}} \right|_{r_S} = \frac{2 - \frac{r_S}{V_{in}} \left( I_{S1} + I_{S2} \right) d}{1 - d} \tag{7.40}$$

Now, on the assumption of $V_{DS}$ as the ESR voltage drop across the switches (i.e. $I_{S1}r_S$ and $I_{S2}r_S$ are equal to $V_{DS}$), (7.40) can be expressed as,

$$\left. \frac{V_o}{V_{in}} \right|_{r_S} = \frac{2 - \frac{2V_{DS}}{V_{in}} d}{1 - d} = \frac{2}{1 - d} - \frac{2V_{DS}d}{V_{in} \left( 1 - d \right)} \tag{7.41}$$

It is noticed from (7.40)–(7.41) that, with greater values of $V_{DS}/V_{in}$ and $d$ the voltage gain declines drastically. It indicates that the inductor's ESR should have a small value.

### 7.5.4. Effect of ESR of Capacitors

The voltage drop across the capacitor's internal resistance $r_C$ is assumed as $V_{DC}$.

*7.5.4.1 Effect of ESR of Intermediate Capacitor*

The input voltage supply ($V_{in}$) charges the capacitor $C_1$ in $CCM_I$. The capacitor $C_1$ is being discharged by the current $I_{L1}$ in $CCM_{II}$. Hence, it experiences a drop in voltage which is indicated by $\Delta V_{C1}$,

$$V_{C1} = V_{in} - V_{DC} - \Delta V_{C1} \approx V_{in} - \frac{t}{C_1} I_{L_1} \tag{7.42}$$

The voltage across the capacitor $C_1$ at the end of $CCM_{II}$ is expressed as,

$$V_{C1} = V_{in} - \frac{1}{C_1} \frac{T_S}{dT_S} \int I_{L_1} dt = V_{in} - \frac{1-d}{C_1} T_S I_{L1} \tag{7.43}$$

The current $I_{L1}$ during $CCM_{II}$ can be shown by the following expression,

$$I_{L1} = I_o + I_{C2} = \frac{I_o}{1-d} \tag{7.44}$$

From (7.43) and (7.44),

$$V_{C1} = V_{in} - \frac{1-d}{C_1} T_S \frac{I_o}{1-d} = V_{in} - \frac{V_o}{f_s R C_1} \tag{7.45}$$

As we know that the currents through the inductors in $CCM_I$ and $CCM_{II}$ modes increase and decrease, respectively. The comparison of the ripples in $CCM_I$ and $CCM_{II}$ shows that,

$$\frac{dT_S}{L_1} V_{in} = \frac{1-d}{L_1} \frac{T_S}{L_1} \quad V_o - V_{in} - V_{C1} \tag{7.46}$$

From (7.42), Eq. (7.46) can be written as

$$\frac{dT_S}{L_1} V_{in} = \frac{1-d}{L_1} \frac{T_S}{L_1} \quad V_o - 2V_{in} + \Delta V_{C1} \tag{7.47}$$

From (7.45)–(7.47), the voltage gain can be expressed as,

$$V_o \Big|_{C_1} = \frac{2V_{in}}{1-d \left( 1 + \dfrac{t}{1-d \ RC_1} \right)} \tag{7.48}$$

From (7.8), the output voltage at the beginning of $CCM_{II}$ is expressed as,

$$V_o = \frac{2V_{in}}{1-d} \tag{7.49}$$

Also, the output voltage at the end of $CCM_{II}$ is dropped down and expressed as,

$$V_o\Big|_{C_1} = \frac{2V_{in}}{1-d\left(1+\dfrac{1}{f_sRC_1}\right)} = \frac{2V_{in}}{1-d\left(\dfrac{f_sRC_1+1}{f_sRC_1}\right)} \tag{7.50}$$

Hence, the gain in voltage and the drop in output voltage is predictable for $f_sRC_1$

$\gg 1$,

$$\Delta V_o\Big|_{C_1} = \frac{2V_{in}}{1-d}\frac{}{f_sRC_1} = \frac{V_o}{f_sRC_1} \tag{7.51}$$

From (7.51), the gain in voltage gain can be expected as,

$$\frac{V_o}{V_{in}}\Bigg|_{C_1} = \frac{2}{1-d\left(1+\dfrac{1}{f_sRC_1}\right)} \tag{7.52}$$

From the above expression, the values of switching frequency, load, and capacitor $C_1$ can be selected appropriately.

*7.5.4.2 Effect of ESR of Output Capacitor*

The voltage drop across the capacitor $C_2$ due to internal resistance ($r_C$) is indicated as ($V_{DC}$). In $CCM_I$, the energy of capacitor $C_2$ is being released through ($R$). Therefore, the capacitor $C_2$ voltage being the same as the output voltage, also drops down and can be expressed as,

$$V_{C2} = V_o - V_{DC} - \frac{t}{C_2}I_o \approx V_o\left(1-\frac{t}{RC_2}\right) \tag{7.53}$$

The final expression at the end of $CCM_I$ is indicated by $(\Delta V_o)$ and can be written as,

$$\Delta V_o\big|_{C_2} = \frac{dV_o}{f_s R C_2} \qquad (7.54)$$

It indicates that the switching frequency $f_S$, load $R$, and capacitance $C_2$ should be selected appropriately. The variation in the output voltage caused by the combination of both the capacitors $C_1$ and $C_2$ is expressed as,

$$\Delta V_o\big|_{C_1+C_2} = \Delta V_o\big|_{C_1} + \Delta V_o\big|_{C_2} = \frac{V_o}{f_s R}\left(\frac{1}{C_1} + \frac{d}{C_2}\right) \qquad (7.55)$$

*7.5.5. Overall effect of Non-idealities on voltage gain*

The non-idealities associated with the inductors, diodes, the capacitors, and switches' ESR effect have been taken into account; the gain in voltage can be shown by using the following expression,

$$\frac{V_o}{V_{in}} \approx \frac{2}{1-d} - \frac{2}{V_{in}}\frac{V_{DL}}{1-d} - \frac{V_{FD}+V_D}{V_{in}}\frac{1}{1-d} - \frac{2V_{DS}d}{V_{in}}\frac{1}{1-d}$$

$$- \frac{2}{1-d}\frac{f_s R C_1 C_2}{f_s R C_1 C_2 + dC_1 + C_2} \qquad (7.56)$$

From Eq. (7.56), the gain in voltage is observed to be decreasing with the increasing values of voltage drop caused by each ESR and duty ratio. Therefore, for the proposed converter it is advisable to select semiconductor devices with the lower internal resistance and the duty ratio moderate values.

## 7.6 Evaluation of efficiency

The proposed converter's overall efficiency can be expressed as,

$$\eta = \frac{2 - \dfrac{2\,V_{DL}}{V_{in}} - \dfrac{2V_{DS}d}{V_{in}} - \dfrac{V_{FD}+V_D}{V_{in}} - \dfrac{V_{DC}}{V_{in}} - V_{DC}}{2 + \dfrac{R}{V_o \times V_{in}} \dfrac{1-d}{} P_{SW}} \qquad (7.57)$$

Where, $P_{SW}$ indicates the overall switching loss during switching; $P_{SW-S1}$ and

$P_{SW-S2}$ indicate the switching power losses for the switches $S_1$ and $S_2$, respectively. For

switch $S_1$ and switch $S_2$, the rising and falling times are indicated by $t_{RS1/2}$, and $t_{FS1/2}$,

respectively; $I_{S1}$ and $I_{S2}$ indicate the average currents through the switch $S_1$ and switch

$S_2$; $V_{S1}$ and $V_{S2}$ indicate the voltages across the switch $S_1$ and switch $S_2$, respectively.

The overall input/output power is obtained by using the following expressions,

$$P_{SW} = P_{SW-S1} + P_{SW-S2} = \frac{I_{S1}V_{S1}(t_{RS1}+t_{FS1})+I_{S2}V_{S2}(t_{RS2}+t_{FS2})}{T_s} \qquad (7.58)$$

### 7.7 Design of Circuit Components

A laboratory prototype of the proposed topology is developed to validate its

operating principle and performance, where the typical input and output parameters are

considered as follows: input voltage is 40 V, output voltage as 400 V, output power as

500 W, and the switching frequency as 100 kHz. The inductors are selected based on

the current through the inductors, whereas the selection of capacitors is done based on

the voltage across them. To obtain a better performance, the worst-case scenario has

been considered to design the inductors and capacitors. Table 7.2 shows the specific

values of various circuit components for the designed prototype.

### 7.7.1 Design of Inductors

The 90% worst efficiency $\eta$(worst) has been selected to calculate the duty cycle.

$$d\big|_{\eta(worst)=90\%} = 1 - \frac{2}{M_{CCM}}\eta(worst) = 1 - \left(\frac{2}{10} \times 0.90\right) \approx 82\% \qquad (7.59)$$

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Table 7.2. Experimental Parameters

| Parameters | Experimental Values |
|---|---|
| Power | 500 W |
| Input Voltage ($V_{in}$) | 36 V to 48 V |
| Duty ratio | 0.8 (for 40V to 400V conversion) |
| Output voltage ($V_0$) | 400 V |
| Load | 320 Ω |
| Switching frequency | 100 kHz |
| Inductor $L_1$ and $L_2$ | ≈ 1mH, 20A (ferrite E core) |
| Capacitor $C_1$, $C_2$ | ≈ 22 μF/100 V, 3.3μF/450V |
| Switches $S_1$, $S_2$ | $V_{DS} = 900$ V, $i_D = 36$ A, $R_{ON} = 65$ mΩ (C3M0065090) |
| Diodes ($D_1$, $D_2$) | $V_{RRM} = 400$ V, $i_F = 30$ A, $R_{ON} = 0.01$Ω, $V_F = 0.8$ V (STTH30R06) |

The critical values of the inductors $L_1$ and $L_2$ can be obtained as follows,

$$L_{1,C} = L_{2,C} = \frac{dV_{in}}{\Delta I_L f_s} = \frac{dV_{in}}{40\% \text{ of } I_L \times f_s} \qquad (7.60)$$

Therefore, using the given parameters, the critical values can be calculated as,

$$L_{1,C} = L_{2,C} = \frac{0.82 \times 40}{4.5A \times 100kHz} \approx 72.89 \ \mu H \qquad (7.61)$$

Therefore, both the inductor values are selected based on (7.61), where 20% to 40% of the inductor current (average value) is indicated by $\varDelta I_L$ and switching frequency for the switch control is indicated by $f_S$. The inductance values and the current rating of the inductors $L_1$ and $L_2$ should be more than the respective calculated values of input current and critical inductance. Therefore, inductors with the core of ferrite E-type rated at 1 mH/18 A have been selected for the designed prototype.

### 7.7.2 Design of Capacitors

The current flowing through the capacitor $C_1$ is observed to be maximum when the switches are turned ON. Thus, the value of critical capacitance for the capacitor $C_1$ can be calculated as follows,

$$C_{1,C} = \frac{I_{in}(1-d)}{f_s \Delta V_{C1}} = \frac{12 \times 0.18}{100kHz \times 2V} = 10.8\mu F \tag{7.62}$$

The capacitor $C_1$ voltage rating must be more than the input voltage value (40 V). Hence, a capacitor (film-type: rated at 22 μF/100 V) has been selected for the designed prototype. The value of critical capacitance for the capacitor $C_2$ can be calculated as follows,

$$C_{2,C} = \frac{dP_o}{V_o f_s \Delta V_{C_2}} = \frac{0.82 \times 500}{400 \times 100kHz \times 4} \approx 2.56\mu F \tag{7.63}$$

The capacitor $C_2$ voltage rating must be more than the output voltage value (i.e. 400 V). Hence, a capacitor (film-type: rated at 3.3 μF/450 V) has been selected for the designed prototype.

### 7.7.3 Diode Selection

The critical value of diode $D_1$ voltage rating can be calculated as,

$$V_{D1,C} = \frac{V_o}{2} \quad \text{or} \quad \frac{V_{in}}{1-d} \tag{7.64}$$

The critical value of diode $D_2$ voltage rating can be calculated as,

$$V_{D2,C} = V_o \quad \text{or} \quad \frac{2V_{in}}{1-d} \tag{7.65}$$

The voltage ratings of the diodes $D_1$ and $D_2$ should be more than 200 V and 400 V, respectively for the selected parameters. The current ratings of the diodes $D_1$ and $D_2$ should be more than the input current i.e. $I_{D1}$ and $I_{D2} > I_{in}$. Therefore, diodes STTH30R06 have been selected for the designed prototype.

### 7.7.4 Switch Selection

The critical values of switches $S_1$ and $S_2$ voltage ratings can be calculated as,

$$V_{S1,C} = \frac{V_o}{2} \quad \text{or} \quad \frac{V_{in}}{1-d}, \quad V_{S2,C} = V_o \quad \text{or} \quad \frac{2V_{in}}{1-d} \tag{7.66}$$

The voltage ratings of the switches should be more than 200 V and 400 V, respectively for the chosen parameters. The current ratings of switch $S_1$ and switch $S_2$ should be less than the input current value i.e. $I_{S1}$ and $I_{S2} < I_{in}$. Therefore, switches C3M0065090 have been selected for the designed prototype.

## 7.8 Simulation Results and Discussion

The theoretical characteristics waveforms represent the voltage and current behavior of the different circuit components. However, in practical or real conditions non-idealities in the circuit components does exist. Therefore, the experimental waveforms are slightly different than the theoretical waveforms. Some simulation results are shown below in Fig. 7.7 for the confirmation.

Initially, the design and circuitry of the proposed TBC is validated through simulation for 500W power, an output voltage of 400V, and an input voltage of 40V. The obtained voltage and current waveforms across/through each component is shown in Fig. 7.7(a)-(b), respectively. The obtained waveforms are matched with the typical waveforms discussed in Section 7.2. Fig. 7.7(a) displays the input voltage (40V), output voltage (400V), and diodes $D_1$ (200V) and $D_2$ (400V) voltages waveforms for the proposed converter. Both the inductors $L_1$ and $L_2$ are observed to be charging in ON-state with the average voltage value of 40V, and both the inductors $L_1$ and $L_2$ are discharging in OFF-state with the average voltage value of -150V. The maximum switch voltage across the switches $S_1$ and $S_2$ are observed as 200 V and 400 V, respectively. The voltage across the input capacitor $C_1$ is found to be nearly equal to the input voltage (i.e. 39 V). The average input current drawn by the proposed converter is nearly equal to 12A. However, the output current is nearly equal to the 1.25A as shown in Fig. 7.7(b). It is important to note that the values of the average currents flowing through the inductors $L_1$ and $L_2$ are observed as 6.5 A and 6.8 A, respectively.

The maximum value of switch current through each of the switches $S_1$ and $S_2$ is observed as 6A, which is approximately equal to half of the input current value.
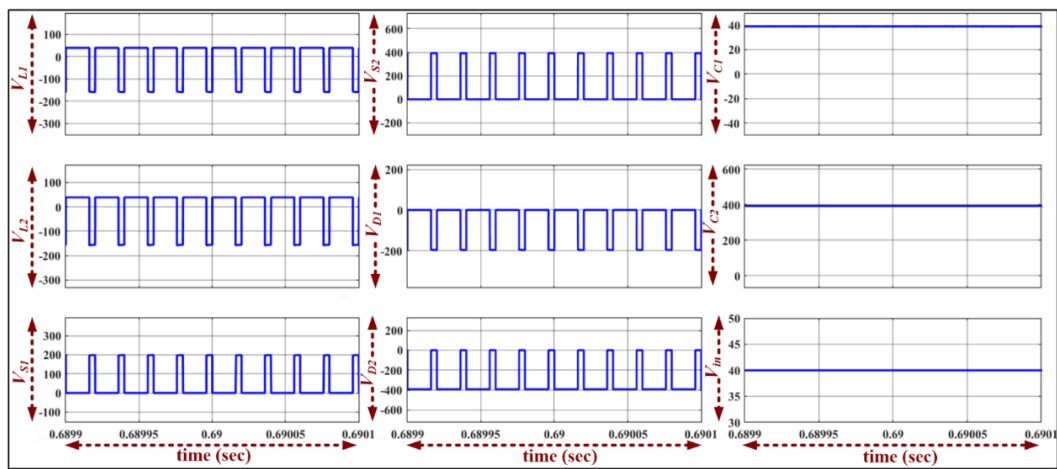


(a) Voltage waveforms
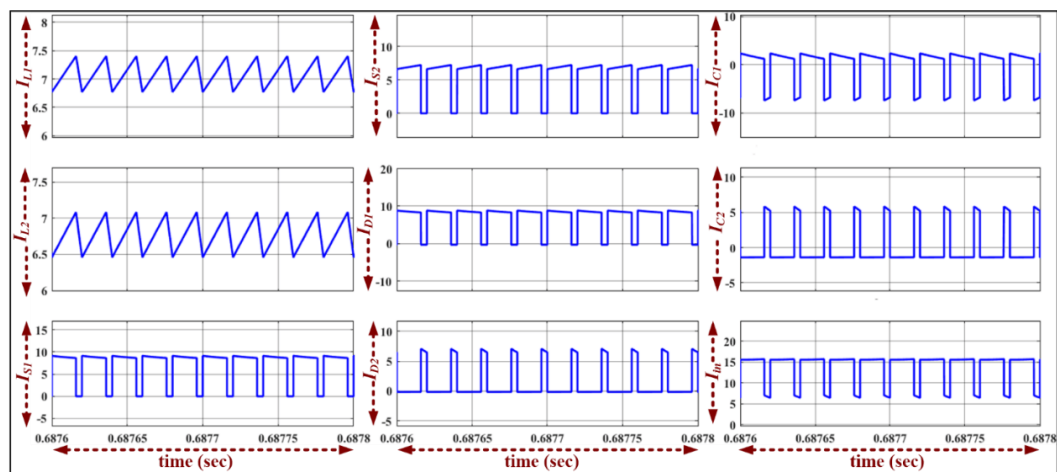


(b) Current waveforms

Figure 7.7. Simulation results

7.9 Hardware Implementation, Experimental Results, and Discussion

The working theory for the proposed converter is verified by developing a 500 W laboratory prototype. STTH30R06 is used for all the diodes, which is an ultra-fast recovery diode. To achieve higher efficiency and high switching operation, C3M0065090 silicon carbide MOSFET is used for the switches. The prototype of the proposed converter is implemented in the laboratory to validate the theoretical analysis and performance of the converter. The designed prototype is shown in Fig. 7.8.
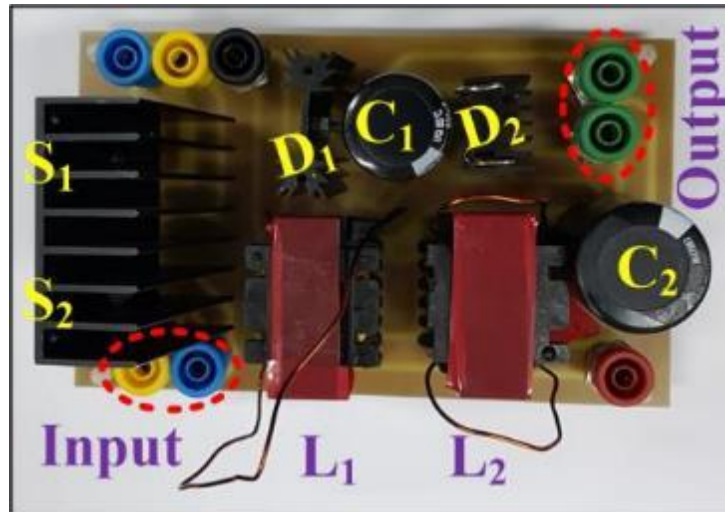
Figure 7.8. Designed 500 W laboratory prototype of the proposed converter.

Fig. 7.9(a) shows the output/input voltages and input/output currents waveforms obtained experimentally. It indicates that 400 V, 43 V, 1.25 A, and 12 A are the output voltage, input voltage, output current, and input current average values, respectively. It is important to note that the input current is continuous, and its slope is positive in the mode $CCM_I$ due to the charging of the inductors $L_1$ and $L_2$. While the input current slope is negative in mode $CCM_{II}$ due to the discharging of the inductor $L_1$ and inductor $L_2$. The peak value of efficiency for the proposed converter is observed as 96.9% at 500Wpower. The waveforms for the inductors $L_1$ and $L_2$ currents obtained experimentally are presented in Fig. 7.9(b). The output voltage and input current waveforms are also shown for reference and to validate. It is important to note that the values of the average currents flowing through the inductors $L_1$ and $L_2$ are 6.72 A and 6.63 A, respectively.
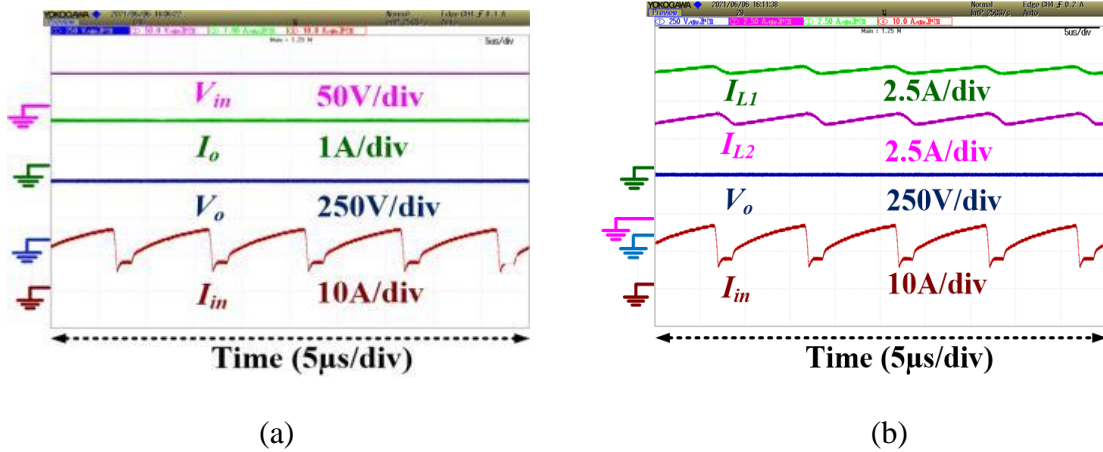
Figure 7.9. Experimental results for (a) input voltage, output current, output voltage, and input current (b) inductor $L_1$ and inductor $L_2$ currents, input current, and output voltage.

The diodes $D_1$ and $D_2$ voltage waveforms obtained experimentally are displayed in Fig. 7.10(a). The waveforms of input current and output voltage are also shown for reference and to validate. It is important to note that, during the mode $CCM_I$ the diode $D_1$ is forward biased whereas diode $D_2$ is reversed biased and vice-versa during the mode $CCM_{II}$. The diodes $D_1$ and $D_2$ PIV values are −200.1 V and −400.3 V, respectively. The fluctuations are observed in the PIV of diode $D_1$ and $D_2$ due to the parasitic capacitance of the switches and the practical mismatch of the inductor $L_1$ and inductor $L_2$. The waveform of the voltage for the capacitor $C_1$, and the voltages across both the switches $S_1$ and $S_2$, obtained experimentally are shown in Fig. 7.10(b); the input current waveform is also shown for reference and to validate. The voltage across the capacitor $C_1$ is found to be nearly equal to the input voltage (i.e. 42.4 V). The maximum switch voltage across the switches $S_1$ and $S_2$ are observed as 200.3 V and 399.4 V, respectively. The switch current waveforms of both the switches $S_1$ and $S_2$, obtained experimentally are shown in Fig. 7.10(c); the waveforms of the output voltage and input current are displayed for reference and to validate. The maximum value of switch current through each of the switches $S_1$ and $S_2$ are observed as 6.61 A and 6.41 A, which

is approximately equal to half of the input current value. Therefore, switches with a lesser current rating can be used in the proposed circuit. The utilization of lower rating components in the proposed circuit offers a lesser ON-state resistance and a low cost design as well. The mathematical analysis shows that the decrease in voltage gain is in reverse proportion to the input voltage. Therefore, as the input voltage increases, the drop in output voltage automatically decreases. The conduction loss of the proposed converter is directly proportional to the current through each of the components, and these currents are directly proportional to the input current. Therefore, at a constant value of power, as the input voltage increases the input current decreases. The efficiency of the developed prototype is analyzed by studying the converter's performance at different values of input voltage and power. The efficiency curve of the developed prototype with the values of power varying from 100 W to 500 W, and variation in input voltage from 20 V to 43 V when the load is set at 320 Ω is shown in Fig. 7.10(d). When the input voltage is at 43 V, and the output power value is 500 W, the efficiency achieved by the designed prototype is 96.9%.
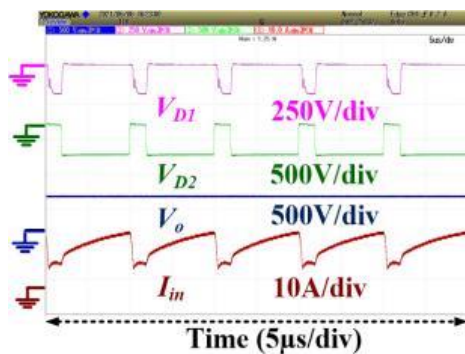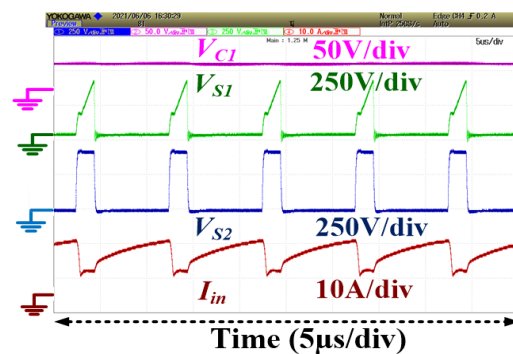


(a)                                                    (b)
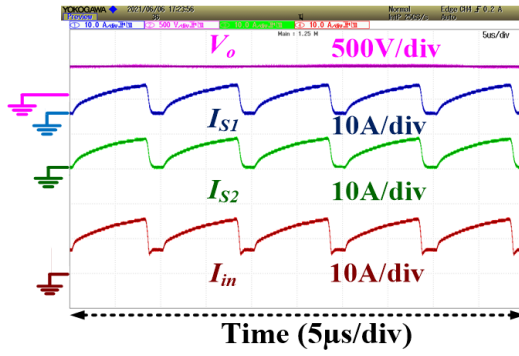
(c)
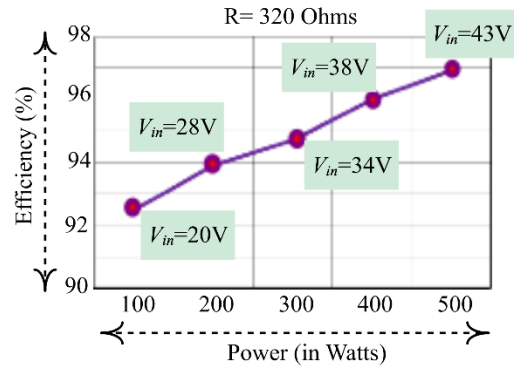


(d)

Figure 7.10. The experimentally obtained waveform for (a) the diodes $D_1$, and $D_2$ voltages, output voltage, and input current (b) switch voltage for $S_1$ and $S_2$, the voltage across capacitor $C_1$, and input current, (c) switch current for $S_1$ and $S_2$, output voltage, and input current (d) Efficiency curve.

Fig. 7.11(a) shows the experimentally obtained waveform for the dynamically varying input and output voltage/current with the duty cycle variation from 0.5 to 0.8. The output voltage values are observed as 172 V, 215 V, 286 V, and 400 V approximately at the duty cycle values of 0.5, 0.6, 0.7, and 0.8, respectively. The experimentally obtained waveform for dynamically varying input and output voltage/current with the load variation is shown in Fig. 7.11(b).
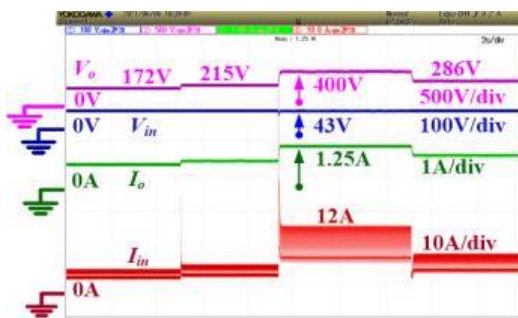


(a)
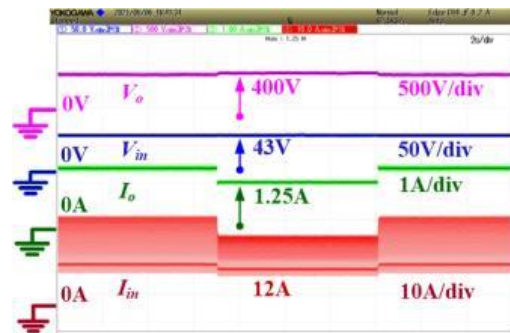


(b)

Figure 7.11. The experimental waveforms for (a) dynamically varying input and output voltage/current with the duty cycle variation from 0.5 to 0.8, and (b) dynamically varying input and output voltage/current with the load variation.

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The experimental results show that the converter topology proposed here can develop steady input and output voltages/currents values.

## 7.10 Comparison of different topologies

This section provides a detailed comparison of various high gain DC–DC converters with the proposed converter topology, like DDTM in [24], mSIBC in [29], converter in [42], Switched-Capacitor-Based Dual- Switch High-Boost DC–DC Converter (SCDS) [44], High Gain Switched-Inductor-Double-Leg Converter (HG-SIDL) [45], Non-isolated High-Step-Up DC–DC Converter Derived from Switched-Inductors and Switched-Capacitors (ASL-SU2C-VO) [46], Converter in [47], and H-SLCs in [149]. Table 7.3 presents the number of components, Voltage gain in CCM, switch current stress, normalized switch voltage stress, and efficiency for the various DC–DC converters being compared.

Only one switch is used in the classical boost converter. However, the switch voltage stress is higher, and the voltage conversion ratio is lesser than the proposed topology. The proposed converter utilizes fewer diodes than all the other converters except the converter proposed in [47] and the classical boost converter. It leads to lesser losses in the proposed circuit. Moreover, the total components count of the proposed converter is lesser than the converters proposed in [24], [44], [45], [46], and [149], leading to an overall cost reduction of the circuit. The proposed converter achieves a higher voltage conversion ratio at a small value of duty cycle as compared to the traditional boost converter and the converter topologies presented in [29], [42], [44], and [149]; while the gain in voltage is the same as the topology proposed in [45] and [47]. The source and load end of the converter in [29] and [42] are connected with the same ground, whereas all other converters are appropriate only for floating loads. It is observed from Table 7.3 that a lesser switch current stress is offered by the proposed

converter topology in comparison to the rest of the converters except [42] and [46], and its value is half of the input current value. Therefore, lower current rating switches can be incorporated into the proposed circuit. The utilization of lower rating components in the proposed circuit offers a lesser ON-state resistance and a low-cost design as well. The efficiency of the proposed converter is greater than the converters in [24], [42], [44], [45], [46], [47], and [149]. Several factors influence the efficiency of a converter, such as voltage/current ratings of the components, their count, and types. Commonly, the device's ON-state resistance increases with an increase in its rating.

The converter topology proposed here develops a design with low cost and improved efficiency due to the usage of lower rating components. It is observed from the detailed comparative study that a high voltage conversion ratio, reduced current stress through the switches, and improved efficiency can be attained by the proposed converter topology by using fewer components. Moreover, the source and load end of the proposed converter has a common ground connection. Suppose we do not have a common ground between the source and load. In that case, there will be a potential difference between load and source ground, which will initiate a circulating current that is not suitable for the PV application. Therefore, for the proposed converter to be used in PV systems, common-mode voltage and leakage current reduction techniques are not required, and hence making the proposed converter highly suitable for integration of solar PV panels with the DC Nanogrid system at the 400 V bus.

Table 7.3. Comparison Table

| Conv. | Number of Reactive components | | Semiconductor Components count | | Total | Voltage gain (M) | Normalized Switch voltage stress | Switch current stress | Efficiency | Output port |
|---|---|---|---|---|---|---|---|---|---|---|
| | Inductor | Capacitor | Switches | Diodes | | | | | | |
| A | 1 | 1 | 1 | 1 | 4 | $1/(1-d)$ | 1 | $I_{in}$ | 98.33% at 200W | Grounded |
| B | 2 | 2 | 3 | 3 | 10 | $(2-d_2)/(1-d_1-d_2)$ | 1/2, (M-1)/M | $I_{in}d_1/2, I_{in}d_2$ | 93.43% at 500W | Floating |
| C | 2 | 1 | 2 | 3 | 8 | $(1+d)/(1-d)$ | 1/2, 1/2 | $dI_{in}/2, dI_{in}$ | 97.17% at 500W | Grounded |
| D | 2 | 1 | 2 | 3 | 8 | $(1+d)/(1-d)$ | (1+M)/2M, 1 | $I_{in}/2, I_{in}/2$ | 93.12% at 500W | Grounded |
| E | 1 | 3 | 2 | 4 | 10 | $(3-2d)/(1-2d)$ | (1-M)/2 | $I_{in}/(3-2d)$ | 95.4% at 200W | Floating |
| F | 4 | 1 | 3 | 8 | 16 | $(1+3d_1+d_2)/(1-d_1-d_2)$ | (1+M)/2M, 1 | $2I_{in}d_1/((1+3d_1+d_2)),$ $2I_{in}d_2/((1+3d_1+d_2))$ | 94.69% at 500W | Floating |
| G | 2 | 3 | 2 | 3 | 10 | $(3+d)/(1-d)$ | M/(3+d) | $I_{in}/2, I_{in}/2$ | 94.53% at 200W | Floating |

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| Conv. | Number of Reactive components | | Semiconductor Components count | | Total | Voltage gain (M) | Normalized Switch voltage stress | Switch current stress | Efficiency | Output port |
|---|---|---|---|---|---|---|---|---|---|---|
| | Inductor | Capacitor | Switches | Diodes | | | | | | |
| H | 2 | 1 | 3 | 2 | 8 | $(1+d_1)/(1-d_1-d_2)$ | $(1+M)/2M$, 1 | $I_{in}/2, I_{in}$ | 93.60% at 100W | Floating |
| I | 2 | 1 | 2 | 4 | 9 | $(1+2d)/(1-d)$ | $(2+M)/3M$, $(1+2M)/3M$ | - | 93-95% at 200W | Floating |
| J | 4 | 1 | 2 | 7 | 14 | $(1+3d)/(1-d)$ | $(1+M)/2M$ | - | | Floating |
| K | 2 | 2 | 2 | 2 | 8 | $2/(1-d)$ | $(1+M)/2M$, 1 | $I_{in}/2$, $I_{in}/2$ | 96.9% at 500W | Grounded |

A: Traditional Boost Converter [26], B: DDTM Converter [24], C: modified SIBC (mSIBC) [29], D: converter in [42], E: SCDS converter [44], F: HG-SIDL converter [45], G: ASL-SU2C-VO converter [46], H: converter in [47], I: ASH-SLC in [149], J: SH-SLC in [149], K: proposed converter

## 7.11 Summary

A new double stage converter with low switch current stress for 400 V DC Nanogrid low to high voltage conversion has been presented in this chapter. One of the main advantages of the proposed converter is that the switch current stress is reduced, as the current through both the switches is approximately half of the input current. Therefore, the proposed converter topology incorporates low current rating switches leading to cost reduction. The proposed converter topology utilizes fewer components, achieves high voltage gain at a small value of duty ratio, and provides high efficiency. Also, the source and load end of the proposed converter circuit connected with a common ground makes it highly suitable for solar PV to be integrated with DC Nanogrid. The theoretical and mathematical analysis in both CCM and DCM is carried out for the proposed converter, and a formula for the voltage gain is obtained. Furthermore, a 500 W laboratory prototype is developed for the proposed converter and analyzed experimentally for its performance validation. With consideration of the physical constraints of the designed converter, the lower and upper limits of the duty cycle are set as 0.3–0.8. The direct connection of the pair of the diode and intermediate capacitor to the input supply and switch set a limitation on the proposed converter. Due to this direct connection of the diode and intermediate capacitor with the input supply, it will experience a high transient peak current at the starting of the converter. The converter operation at different duty cycles and turn-on delay effect on the performance of the converter can be analyzed as future research work. Furthermore, there are multiple ways to extend the proposed configuration by using multiple switched inductors.

CHAPTER 8: CONCLUSION AND FUTURE DIRECTION

In this research work, a new class of two switches, uni-directional, non-isolated, non-coupled step-up, high voltage conversion ratio DC-DC power converter configurations with reduced switch voltage/current stress based on switched inductor circuitry are articulated for Nanogrid Applications. In the Nanogrid applications, the DC-DC converter is an integral part of the energy conversion process due to its high voltage conversion capability before feeding to the grid. A general classification of the DC-DC converters with a brief discussion on isolated and non-isolated converters, uni-directional and bi-directional converters has been presented in the literature review. It was found that, a conventional DC-DC converter is not suitable for high voltage applications, which leads to the design of various new topologies of DC-DC converters that can achieve a high voltage conversion ratio. The various boosting techniques have been analyzed and explained in the literature survey to develop high-voltage capability DC-DC converters.

By adopting the feature of boosting techniques, five novel high voltage gain DC-DC converters namely modified Switched Inductor Boost Converter (mSIBC), Transformer-less Boost Converter (TBC), a Switched-Inductor based DC-DC converter with reduced switch current stress, a Novel High Gain Active Switched Network-Based Converter, and Double Stage Converter with low current stress for Nanogrid are developed. The key feature of these DC-DC Converters is reducing the switch voltage/current stress to achieve a high step-up DC voltage. Hence, the proposed converters are designed and developed by using low voltage/current rating switches and hence lead to cost reduction. The operating principle, theoretical/characteristic waveforms in CCM, and DCM including steady-state analysis are presented for each of these DC-DC Converter topologies. A comprehensive analysis discussing the effect

of non-idealities on the voltage gain of each of the proposed converter configurations, the design of their components, and a comparison considering the number of components, their CCM voltage gain, normalized switch voltage stress, switch current stress, and their efficiency with other converters are presented.

Each of the five proposed converters has its own drawbacks and advantages. The modified Switched Inductor Boost Converter (mSIBC) (Converter 1) is good for reduced voltage stress, but the drawback is unequal ratings of the switches. Whereas, the Transformer-less Boost Converter (TBC) (Converter 2) has a high voltage gain and equal switch ratings, but suffers from transients in the input current due to the presence of capacitor. Similarly, the Switched-Inductor-based DC-DC converter with reduced switch current stress (Converter 3) is good for reduced switch current stress and hence the same switch current ratings, while different voltage ratings of the two switches. On the other hand, the Double Stage Converter with low current stress (Converter 5) has a higher voltage gain and the same current ratings of the two switches. However, as the capacitor is directly connected with the input supply, it experiences a high transient peak current. As far as the Novel High Gain Active Switched Network-Based Converter (Converter 4) is concerned, it is good for reduced switch voltage/current stress. However, the number of components is higher than the other four converters.

Furthermore, for future work, this research opens up the path for several motivating tasks such as:

- Simulation of a full Nanogrid with active and reactive power control incorporating these DC-DC Converter topologies and implementation in RTDS.
- A complete closed-loop hardware realization by implementing MPPT control to these DC-DC Converter topologies for Solar PV application.

- Analyzing Smart features of these DC-DC Converter topologies by adding communications module to transfer data from one to the other converter like the voltage, current, etc.

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APPENDIX: RESEARCH CONTRIBUTION AND PUBLICATION DETAILS

In this section, the details of the student's research contribution and publication during the Ph.D. are provided.

*Transaction and Journal Articles*

1. S. Sadaf, M. S. Bhaskar, M. Meraj, A. Iqbal and N. Al-Emadi, "A Novel Modified Switched Inductor Boost Converter With Reduced Switch Voltage Stress," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 2, pp. 1275-1289, Feb. 2021, doi: 10.1109/TIE.2020.2970648.

2. S. Sadaf, M. S. Bhaskar, M. Meraj, A. Iqbal and N. Al-Emadi, "Transformer-Less Boost Converter With Reduced Voltage Stress for High Voltage Step-Up Applications," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 2, pp. 1498-1508, Feb. 2022, doi: 10.1109/TIE.2021.3055166.

3. S. Sadaf, N. Al-Emadi, P. K. Maroti and A. Iqbal, "A New High Gain Active Switched Network-Based Boost Converter for DC Microgrid Application," in *IEEE Access*, vol. 9, pp. 68253-68265, 2021, doi: 10.1109/ACCESS.2021.3077055.

4. S. Sadaf, N. Al-Emadi, A. Iqbal, M. S. Bhaskar, and M. Meraj, "Modelling, analysis, and implementation of a switched-inductor based DC/DC converter with reduced switch current stress," *IET power electron.*, vol. 14, no. 8, pp. 1504–1514, 2021.

5. S. Sadaf, N. Al-Emadi, A. Iqbal, and M. S. Bhaskar, "Double stage converter with low current stress for low to high voltage conversion in nanogrid," *Energy rep.*, vol. 7, pp. 5710–5721, 2021.

*Conference Proceedings*

1. S. Sadaf, N. A. Al-Emadi, A. Iqbal, M. S. Bhaskar and M. Meraj, "New High Gain 2LC-Y Multilevel-Boost-Converter (2LC-Y MBC) Topologies for Renewable Energy Conversion: Members of X-Y Converter Family," *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, 2019, pp. 2647-2652, doi: 10.1109/ISIE.2019.8781355.

2. S. Sadaf, N. Al-Emadi, M. S. Bhaskar, and A. Iqbal, "Triple-switch DC-to-DC converter for high-voltage boost application—Revista," in *Lecture Notes in Electrical Engineering*, Singapore: Springer Singapore, 2021, pp. 197–204.

*Patent*

1. A. Iqbal, S. Sadaf, N. Al-Emadi, M. S. Bhaskar and M. Meraj, "DC TO DC SWITCHED INDUCTOR BOOST CONVERTER". *US Patent*, US 2021-0313890 A1, 9 October 2021.