

# Modelling, analysis, and implementation of a switched-inductor based DC/DC converter with reduced switch current stress

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## Abstract

This paper proposes a technique for switch current stress reduction in a Switched Inductor DC-DC Boost Converter (SIBC). The proposed technique comes up with a low-cost design, high voltage conversion ratio with a less duty cycle value, and lower current stress without increasing the component count. This topology is basically a transformerless design where one diode of the traditional switched inductor configuration has been replaced with a switch, which is in parallel with the existing switch, resulting in a design that can incorporate active switches with a low current rating, since the total input current is equally shared by them. The detailed modes of operation in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) and steady-state analysis, the non-idealities' effect on voltage gain, design approach, and a comparative study with other DC-DC converters for some significant performance characteristics are provided. The experimental validations for the performance and working of the 500 W designed prototype are presented.

## 1 | INTRODUCTION

For various applications such as high-intensity discharge lamp ballast, uninterruptible power supply, photovoltaic and fuel cell energy conversion, LED and DC microgrid, high gain DC-DC converters are required for stepping up the voltage [1,2]. Theoretically, a high voltage conversion ratio can be achieved by using the traditional DC-DC boost converter with a large value of duty cycle, which in turn increases the current stress in the boost switch. Furthermore, the system efficiency is reduced and the maximum voltage gain is constrained due to serious reverse-recovery problems associated with the diode, inductor's and capacitor's parasitic resistance, semiconductor devices with a higher rating, and high switch conduction loss [3–6]. To overcome these issues, several power converter topologies have been introduced in the literature in the past decade to achieve a high voltage gain avoiding the duty cycle to be exceptionally high. The flyback, push-pull, SEPIC, and H-Bridge type topologies which are basically transformer-based converters, could be used to achieve a high voltage gain without working at extreme val-

ues of duty cycles. However, to minimize the component stress and effect of transformer leakage inductance, and recycle the leakage energy, extra energy restoration methods and voltage clamping practices are needed to incorporate in these converters [7–11]. A high gain in voltage with low switch current stress can be achieved by using coupled inductor based topologies [12]. Nevertheless, in the case of high-power applications, significant current stress is observed through the switch [13]. Also, the need of ripples reduction techniques and energy recovery schemes for leakage inductor by using input filter and additional clamped circuit increase the cost. Furthermore, the gain factor of these topologies is controlled by the coupling coefficient of the coupled inductors and these are complex in design too [14,15]. Although the quadratic boost and cascaded converter topologies can solve the above mentioned issues, the cascade structure is observed to be complex in design which leads to an increased cost. Furthermore, to reduce the circuit complexity, integrating the two switches into one, does not help much and the current stress continues to be high in that case too [7, 13, 16–18]. Some of the recently proposed solutions [3, 13, 19–22],

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such as switched inductor or switched capacitor based converters, hybrid switched inductor-capacitor converters, multiplier based or interleaved converter structures are able to solve the problems faced in the abovementioned converters. However, generally, the voltage gain is less in such converters, due to the presence of many power stages and the current stress through active switches is also high [17, 23]. Furthermore, the system size, complexity, and cost increase substantially due to the presence of several multiplier cells. Some new converter topologies are proposed to reduce the switch current stress and to increase the voltage gain without increasing the duty cycle [24–28]. However, a greater number of intermediate reactive components are needed for the proposed converters in [24, 25] and a high gain in voltage is attained by incorporating several stages. On the other hand, the circuits proposed in [26–30] are appropriate for floating load conditions only and the voltage gain improvement is not sufficient enough even by increasing the number of switches in the circuit. In [29–30], dual duty three mode converters with high gain are developed to improve the voltage gain with no coupled inductor, transformer, voltage lifting techniques, or voltage multiplier. These converters can attain a high voltage gain with a wide range of operations of the duty cycle. However, the control algorithm of these converters is complex due to the usage of three switches and two duty cycles, leading to an increase in complexity of the circuit, size, and cost. Furthermore, such converters are appropriate in the conditions of floating load only.

To achieve a high voltage gain, derived from the typical switched inductor boost converter (SIBC) design, this paper proposes an improved converter topology with reduced current stress for active switches to provide a stable constant boosted DC voltage. The proposed topology has the advantage of providing a high voltage gain, low current stress, and low conduction loss on the active switches, simplified control, and high efficiency. The current is equally shared by both the switches and thereby reducing the conduction loss. The proposed converter topology is a transformer-less design. Both the switches are connected in parallel and thereby reducing the switch current stress. Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. Furthermore, the solar PV panels can be integrated at 400-V bus of a DC microgrid system by incorporating the proposed converter because of the common ground connection of source and load. The proposed converter is more appropriate and a better option for PV application of 400 V DC microgrid because of its properties of achieving high voltage gain, operation in a wide duty range, and unidirectional power flow. As required for the PV applications, the proposed converter is able to draw a continuous input current with low ripples from the input source. The proposed converter is a viable solution for the integration of solar PV panels into a DC microgrid because of the abovementioned benefits where a high overall output voltage can be obtained by incorporating the proposed converter with each PV panel. The rest of the manuscript is arranged as follows. The power circuit and the characteristics in steady-state, and operating principle in different modes with analysis is explained in Section 2. Section 3 presents the effect of non-idealities of the

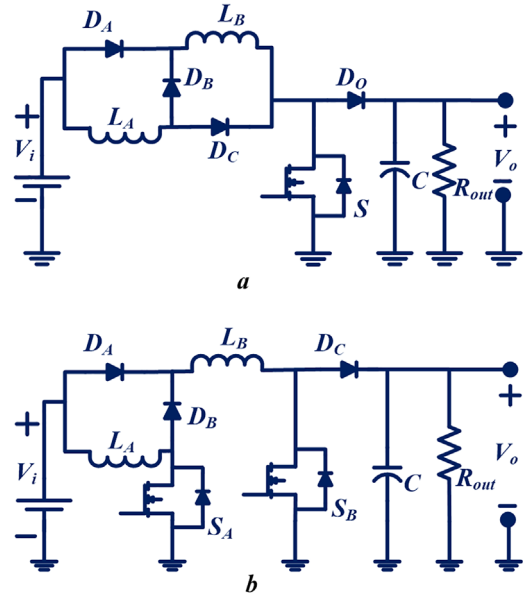


FIGURE 1 Power circuit: (a) typical SIBC [21], (b) proposed converter

circuit elements on voltage gain and the evaluation of efficiency. A comparative study of DC-DC converters is presented in Section 4. The method of design and experimentally obtained results are discussed in Section 5 and Section 6 gives the conclusion.

## 2 | PROPOSED CONVERTER TOPOLOGY

The power circuit of the typical SIBC [21] is shown in Figure 1(a). SI circuit is incorporated in the SIBC to attain a voltage gain higher than the conventional boost converter. Nonetheless, current stress on the switch increases significantly with voltage gain due to the total input current flowing through the switch. Hence, the power circuitry of the typical SIBC has been improved without increasing the component count to reduce the switch current stress. To attain a high voltage gain, the fundamental concept of switched inductor structures that is charging of inductors in parallel and discharging in series has been exploited. An extra switch is added in place of one diode, which reduces the switch current stress to half of the current stress on the active switch of the SIBC. The current is equally shared by both the active switches.

### 2.1 | Power circuitry

The power circuitry of the proposed converter is shown in Figure 1(b) comprising of diodes  $D_A$ ,  $D_B$ , and  $D_C$ , inductors  $L_A$  and  $L_B$ , active switches  $S_A$  and  $S_B$ ,  $C$  as capacitor, and  $R_{out}$  as load. The converter topology put forward is basically a transformer-less design and is originated from the typical Switched Inductor Boost Converter (SIBC) structure by substituting a diode with a switch in the switched inductor circuit. Both the switches are connected in parallel and thereby

reducing the switch current stress to half of the current stress on the active switch of the SIBC. Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. It is important to note that the components count of the proposed converter is the same as that of the typical SIBC and the voltage gain is improved. Firstly, all the circuit elements of the proposed converter topology are considered to be ideal for studying the CCM steady-state characteristics. The capacitance value is sufficiently large to achieve a ripple-free voltage, and the ON-state resistance voltage drop across semiconductor devices is ignored. The inductance value of the inductors  $L_A$  and  $L_B$  are considered to be equal in this section that is,  $L_A = L_B = L$  (superior case). Both the inductor  $L_A$  and  $L_B$  currents are equal as per the above circuit, and are expressed as,

$$I_L = I_{L_A} = I_{L_B} \quad (1)$$

Figure 2(a)-(b) presents the CCM and DCM characteristic waveforms of the proposed converter; where  $T_{on}$  being the Mode I time period (time interval between  $t_0$  and  $t_a$ ) and the overall time period is  $T$ .

## 2.2 | CCM—Principle of operation and analysis

There are two CCM operation modes of the proposed converter; both the switches  $S_A$  and  $S_B$  are kept ON in Mode I (between time  $t_0$  and  $t_a$ ) while switches  $S_A$  and  $S_B$  are kept OFF in Mode II (between time  $t_a$  and  $t_b$ ).

### 2.2.1 | Mode I (between time $t_0$ and $t_a$ )

Input voltage ( $V_i$ ) charges the Inductor  $L_A$  via switch  $S_A$ , while input voltage ( $V_i$ ) charges inductor  $L_B$  via diode  $D_A$  and switch  $S_B$ , and capacitor  $C$  is getting discharged via load  $R_{out}$ . Diode  $D_A$  is forward biased and diodes  $D_B$  and  $D_C$  are reversed biased. Figure 3(a) shows the equivalent circuit of the proposed converter for Mode I. Both the inductors are observed to be charged by the input voltage ( $V_i$ ) in parallel and with the same values of current. Inductors  $L_A$  and  $L_B$  voltages and currents are expressed as,

$$V_L = V_{L_A} = V_{L_B} = V_i, V_C = V_o \quad (2)$$

$$I_L = I_{L_A} = I_{L_B} = \frac{I_i}{2}, I_C = -I_o = -\frac{V_o}{R_{out}} \quad (3)$$

where  $I_i$  is the input current. The switches  $S_A$  and  $S_B$  voltages and currents are expressed as,

$$V_S = V_{S_A} = V_{S_B} = 0, I_S = I_{S_A} = I_{S_B} = \frac{I_i}{2} \quad (4)$$

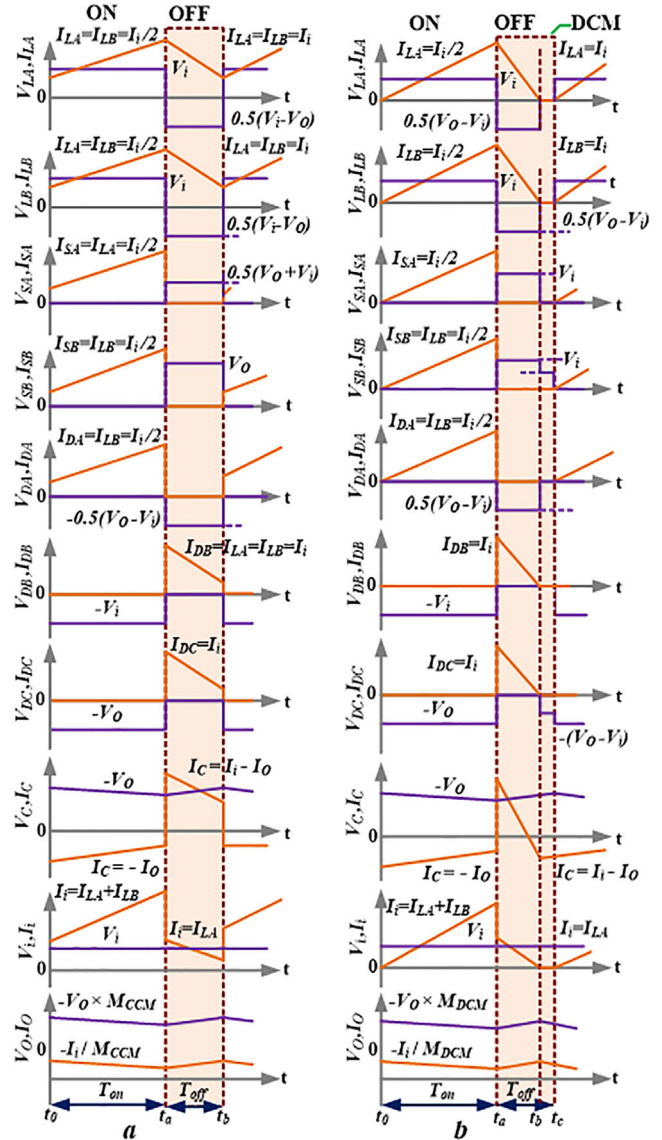


FIGURE 2 Characteristic plots of proposed converter. (a) Continuous conduction mode (CCM). (b) Discontinuous conduction mode (DCM)

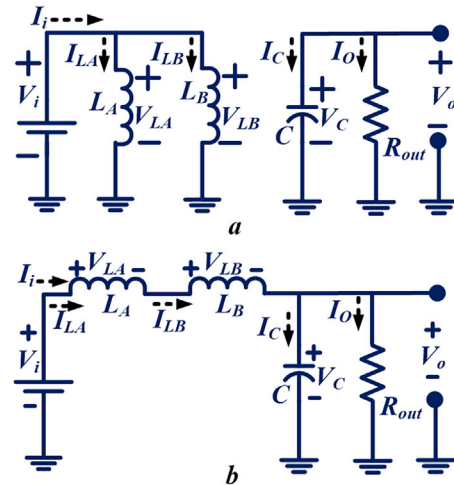


FIGURE 3 Diagram of equivalent circuitry. (a) Mode I, (b) Mode II

### 2.2.2 | Mode II (between time $t_a$ and $t_b$ )

Both the inductors  $L_A$  and  $L_B$  are discharging in series having the input supply  $V_i$  for charging capacitor  $C$  via diodes  $D_B$  and  $D_C$  and supplying energy to the load  $R_{out}$ . Diode  $D_A$  is reversed biased and diodes  $D_B$  and  $D_C$  are forward biased. Figure 3(b) displays the proposed converter equivalent circuitry for Mode II. The inductors  $L_A$  and  $L_B$  voltages and currents are expressed as,

$$V_L = V_{LA} = V_{LB} = \frac{V_i - V_o}{2}, V_C = V_o \quad (5)$$

$$I_L = I_{LA} = I_{LB} = I_i, I_C = I_L - \frac{V_o}{R_{out}} \quad (6)$$

The switches  $S_A$  and  $S_B$  voltages and currents are expressed as,

$$V_{SA} = \frac{1}{(1-D)} V_i, V_{SB} = \frac{(1+D)}{(1-D)} V_i, I_S = I_{SA} = I_{SB} = 0 \quad (7)$$

The voltage gain of the proposed converter can be expressed as,

$$M_{CCM} = V_o/V_i = (1+D)/(1-D) \quad (8)$$

where the duty cycle is denoted by  $D$  and the voltage gain is denoted by  $M_{CCM}$ . The proposed converter's voltage gain is observed to be equal to that of the typical SIBC.

## 2.3 | DCM—Principle of operation and analysis

There are three modes of operation of the proposed converter for DCM; switches  $S_A$  and  $S_B$  are kept ON in the first mode that is ON State, switches  $S_A$  and  $S_B$  are kept OFF in the second mode with a non-zero value of inductor currents and switches  $S_A$  and  $S_B$  are kept OFF with zero inductor currents during the third mode. Figure 2(b) shows that the inductor current comes to zero, let us say at time  $t_b$ . Figure 2(b) shows the characteristic waveform for DCM, where the time period for the first mode is indicated as  $Y_I T$  or  $T_{on}$  that is the time between  $t_0$  and  $t_a$ , the time period for the second mode is indicated as  $Y_{II} T$  or  $T_{off,I}$  that is the time between  $t_a-t_b$ , and the time period for the third mode is indicated as  $Y_{III} T$  or  $T_{off,II}$  that is the time between  $t_b-t_c$ .

### 2.3.1 | Mode I (between time $t_0$ and $t_a$ )—Both $S_A$ and $S_B$ are kept ON

The proposed converter's equivalent circuitry and working in this mode are the same as that of mode I of CCM. Both inductors  $L_A$  and  $L_B$  are charged in parallel by the input supply  $V_i$ . The currents through inductors  $L_A$  and  $L_B$  started from zero value at the beginning of this mode that is at the time  $t_0$  or  $t_0+T$

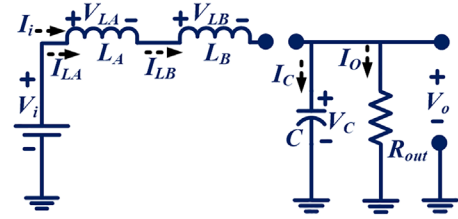


FIGURE 4 DCM mode III equivalent circuit

and attained the highest value at the end of this mode. Inductor  $L_A$  and  $L_B$  maximum currents can be expressed as,

$$I_{L,max} = I_{LA,max} = I_{LB,max} = V_i Y_I / L f \quad (9)$$

The maximum currents through inductor  $L_A$  and  $L_B$  are denoted by  $I_{LA,max}$  and  $I_{LB,max}$ , respectively, and the switching frequency is denoted by  $f = 1/T$ . The current ripples of inductors  $L_A$  and  $L_B$  can be expressed as,

$$\Delta I_L = \Delta I_{LA} = \Delta I_{LB} = V_i Y_I / L f \quad (10)$$

The inductor  $L_A$  and  $L_B$  current ripples are denoted by  $\Delta I_{LA}$  and  $\Delta I_{LB}$ , respectively.

### 2.3.2 | Mode II (between time $t_a$ and $t_b$ )—Both $S_A$ and $S_B$ are kept OFF with non-zero value of inductor currents

The equivalent circuit and working of the proposed converter for this mode are the same as that of mode II of CCM. Inductors  $L_A$  and  $L_B$  are discharged in series by the input supply  $V_i$ , and the capacitor  $C$  is charged to supply energy to load  $R_{out}$ . The currents through inductors  $L_A$  and  $L_B$  started from the maximum value at the beginning of this mode that is at time  $t_a$  or  $t_a+T$  and zero value is reached by the inductor currents at the end of this mode that is at the instant  $t_b$  or  $t_b+T$ . Inductor  $L_A$  and  $L_B$  maximum currents can also be expressed alternately as,

$$I_{L,max} = I_{LA,max} = I_{LB,max} = (V_o - V_i) Y_{II} / 2L f \quad (11)$$

The current ripples of inductors  $L_A$  and  $L_B$  are expressed as,

$$\Delta I_L = \Delta I_{LA} = \Delta I_{LB} = (V_o - V_i) Y_{II} / 2L f \quad (12)$$

### 2.3.3 | Mode III (between $t_b$ and $t_c$ )—Both $S_A$ and $S_B$ are kept OFF with zero value of inductor currents

Figure 4 shows the DCM mode III equivalent circuit. Both the switches  $S_A$  and  $S_B$  are kept OFF and currents through inductors  $L_A$  and  $L_B$  are zero. Hence, the energy accumulated by inductors  $L_A$  and  $L_B$  is also zero, capacitor  $C$  is discharged



through load  $R_{out}$ , and all the three diodes are reversed biased in this mode. Mode II time period which is denoted by  $Y_{II}T$  or  $T_{off,I}$  can be obtained from Equations (10) and (11), and is expressed as,

$$Y_{II}T \text{ or } T_{off,I} = 2V_i Y_I / (V_o - V_i) f \quad (13)$$

We know that,

$$T_{on} + T_{off,I} + T_{off,II} = T \quad (14)$$

The time periods for Mode I and III, respectively are expressed as,

$$T_{on} = \frac{Y_I}{f}, Y_{III}T \text{ or } T_{off,II} = 1 - \frac{1}{f} \left[ Y_I + \frac{2V_i Y_I}{(V_o - V_i)} \right] \quad (15)$$

The capacitor  $C$  average current can be obtained from Figure 2(b) and is expressed as,

$$\begin{aligned} I_C &= 0.5 (Y_{II} \times I_{L,max}) - I_o \\ &= 0.5 (Y_{II} \times I_{L,max}) - V_o / R_{out} \end{aligned} \quad (16)$$

From Equations (15) and (18),

$$I_C = 0.5 \left( \frac{2V_i Y_I}{V_o - V_i} \times \frac{V_i Y_I}{L f} \right) - \frac{V_o}{R_{out}} \quad (17)$$

The average current through a capacitor is always zero in a steady-state condition. Hence, Equation (17) can also be written as,

$$\frac{2V_i Y_I}{V_o - V_i} \times \frac{V_i Y_I}{L f} = \frac{2V_o}{R_{out}} \quad (18)$$

The quadratic equation obtained from Equation (18), is calculated by using the following expression,

$$\left( \frac{V_o}{V_i} \right)^2 - \frac{V_o}{V_i} - \frac{Y_I^2}{\lambda_L} = 0 \quad (19)$$

where inductors  $L_A$  and  $L_B$  normalized time constant is denoted by  $\lambda_L$  and has a value equal to  $fL/R_{out}$ . Hence,  $L$ ,  $f$ , and  $R_{out}$  values control the variation in  $\lambda_L$ . The voltage gain of the proposed converter for DCM denoted by  $M_{DCM}$  can be obtained by simplifying the Equation (19) and is expressed as,

$$\begin{aligned} M_{DCM} &= \frac{V_o}{V_i} = \frac{1}{2} + \left( \frac{0.25\lambda_L + Y_I^2}{\lambda_L} \right)^{1/2} \\ &= \frac{1}{2} + \left( \frac{1}{4} + \frac{Y_I^2 R_{out}}{L f} \right)^{1/2} \end{aligned} \quad (20)$$

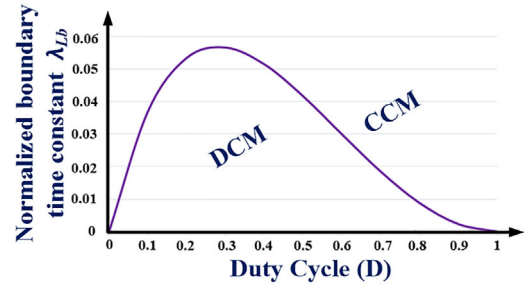


FIGURE 5 Normalized boundary condition w.r.t. duty cycle

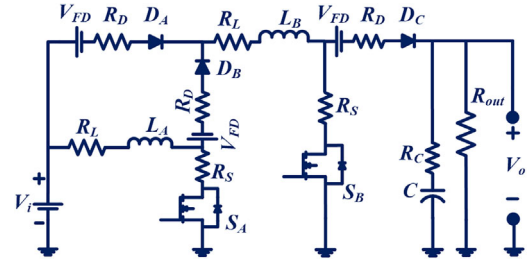


FIGURE 6 Equivalent circuit including non-idealities of the proposed topology

The CCM and DCM voltage gains are observed to be the same when the CCM and DCM boundary is considered as the proposed converter's operating point. Hence, from the Equations (8) and (20),

$$\frac{V_o}{V_i} = 0.5 + \left( \frac{0.25\lambda_{Lb} + Y_I^2}{\lambda_{Lb}} \right)^{1/2} = \frac{1+D}{1-D} \quad (21)$$

We know that the CCM and DCM mode I are the same. Hence,  $Y_I$  is the same as  $D$  and inductors  $L_A$  and  $L_B$  normalized boundary time constant which is denoted by  $\lambda_{Lb}$  can be expressed as,

$$\lambda_{Lb} = (D^3 - 2D^2 + D) / 2(1+D) \quad (22)$$

The plot of  $\lambda_{Lb}$  versus  $D$  is shown in Figure 5 indicating the DCM and CCM regions. It indicates that the proposed converter works in DCM mode when the value of  $\lambda_{Lb}$  is more than  $\lambda_L$ .

### 3 | NON-IDEALITIES EFFECTS ON VOLTAGE GAIN

Figure 6 displays the power circuitry of the proposed converter by taking into account the non-idealities of different circuit elements for analyzing their effect on the output voltage. Each of the inductors  $L_A$  and  $L_B$  Equivalent Series Resistance (ESR) is denoted by the resistances  $R_L$ . Each of the switches'  $S_A$  and  $S_B$  ON-state resistance is denoted by the resistances  $R_S$ . Each of the diodes  $D_A$ ,  $D_B$ , and  $D_C$  threshold voltage and forward

resistance are denoted by voltage  $V_{FD}$  and resistances  $R_D$ , respectively; for the capacitor  $C$ , ESR is denoted by  $R_C$ .

### 3.1 | Inductors $L_A$ and $L_B$ ESR effect on voltage gain

Other parasitic irregularities are neglected for analyzing the inductors  $L_A$  and  $L_B$  ESR effect on voltage gain that is by considering  $R_S = 0$ ,  $R_D = 0$ ,  $R_C = 0$ , and  $V_{FD} = 0$ . Hence, in this case, the voltages across the inductors  $L_A$  and  $L_B$  can be expressed as,

$$\begin{aligned} \text{onstate : } V_{L_A} &\approx V_i - I_{L_A}R_L, V_{L_B} \\ &\approx V_i - I_{L_B}R_L, V_o \approx V_C \end{aligned} \quad (23)$$

$$\text{offstate : } V_{L_A} + V_{L_B} \approx V_i - I_{L_A}R_L - I_{L_B}R_L - V_o \quad (24)$$

From Equation (23) and addition of voltages across inductors,

$$V_{L_A} + V_{L_B} \approx 2V_i - I_{L_A}R_L - I_{L_B}R_L \quad (25)$$

From the inductor volt second balance method and the method of small approximation,

$$\begin{aligned} (2V_i - I_{L_A}R_L - I_{L_B}R_L)D \\ = -(V_i - I_{L_A}R_L - I_{L_B}R_L - V_o)(1 - D) \end{aligned} \quad (26)$$

From Equation (26), the proposed converter voltage gain is calculated by using the following expression,

$$\left. \frac{V_o}{V_i} \right|_{R_L} = \frac{(1 + D) - \{(I_{L_A}R_L + I_{L_B}R_L) / V_i\}}{(1 - D)} \quad (27)$$

Both the inductors  $L_A$  and  $L_B$  currents have the same value that is  $I_L = I_{L_A} = I_{L_B}$  when  $L_A = L_B$ . If the inductor voltage drop because of ESR is denoted by  $V_{DL}$ , then  $V_{DL} = I_{L_A}R_L = I_{L_B}R_L$ . Therefore, Equation (27) can also be expressed alternately as,

$$\left. \frac{V_o}{V_i} \right|_{R_L} = \frac{(1 + D) - 2V_{DL}/V_i}{(1 - D)} \quad (28)$$

It is observed from (27) and (28) that for larger values of  $V_{DL}$  and  $D$ , the voltage gain is decreasing. Hence, moderate values of the duty cycle ( $D$ ) and the ESR of inductance ( $R_L$ ) should be considered.

### 3.2 | Diodes $D_A$ , $D_B$ , and $D_C$ effect on voltage gain

Other parasitic irregularities are neglected for analyzing the diodes  $D_A$ ,  $D_B$ , and  $D_C$  effect on voltage gain that is by consid-

ering  $R_{L_A} = 0$ ,  $R_{L_B} = 0$ ,  $R_C = 0$ , and  $R_S = 0$ . Hence, in this case, the voltages across the inductors  $L_A$  and  $L_B$  can be expressed as,

$$\text{ModeI : } V_{L_A} \approx V_i, V_{L_B} \approx V_i - I_{L_B}R_D - V_{FD} \quad (29)$$

$$\text{ModeII : } V_{L_A} + V_{L_B} \approx V_i - 2I_{L_B}R_D - 2V_{FD} - V_o \quad (30)$$

From Equation (29) and addition of inductor voltages,

$$V_{L_A} + V_{L_B} \approx 2V_i - I_{L_B}R_D - V_{FD} \quad (31)$$

From the inductor volt second balance method and the method of small approximation,

$$\begin{aligned} (2V_i - I_{L_B}R_D - V_{FD})D \\ = -(V_i - 2I_{L_B}R_D - 2V_{FD} - V_o)(1 - D) \end{aligned} \quad (32)$$

From Equation (32), the proposed converter voltage gain is calculated by using the following expression,

$$\left. \frac{V_o}{V_i} \right|_{R_D, V_{FD}} = \frac{(1 + D) - \{(I_{L_B}R_D + V_{FD})(2 - D) / V_i\}}{(1 - D)} \quad (33)$$

If the diode voltage drop because of the threshold voltage and forward resistance is denoted by  $V_{DD}$ , then  $V_{DD} = I_{L_B}R_D + V_{FD}$ . Therefore, Equation (33) can also be expressed alternately as,

$$\left. \frac{V_o}{V_i} \right|_{R_D, V_{FD}} = \frac{(1 + D) - \{V_{DD}(2 - D) / V_i\}}{(1 - D)} \quad (34)$$

It is observed from (33) and (34) that for larger values of  $V_{DD}/V_i$  and  $D$ , the voltage gain is decreasing. Hence, moderate values of threshold voltage and forward resistance should be considered.

### 3.3 | Switches $S_A$ and $S_B$ effect on voltage gain

Other parasitic irregularities are neglected for analyzing the switches  $S_A$  and  $S_B$  effect on voltage gain that is by considering  $R_{L_A} = 0$ ,  $R_{L_B} = 0$ ,  $R_C = 0$ ,  $R_D = 0$ , and  $V_{FD} = 0$ . Hence, in this case, the inductors  $L_A$  and  $L_B$  voltages can be expressed as,

$$\text{ModeI : } V_{L_A} \approx V_i - I_{S_A}R_S, V_{L_B} \approx V_i - I_{S_B}R_S \quad (35)$$

$$\text{ModeII : } V_{L_A} + V_{L_B} \approx V_i - V_o \quad (36)$$

From Equation (35) and addition of inductor voltages,

$$V_{L_A} + V_{L_B} \approx 2V_i - I_{S_A}R_S - I_{S_B}R_S \quad (37)$$

From the inductor volt second balance method and the method of small approximation,

$$(2V_i - I_{SA}R_S - I_{SB}R_S)D = -(V_i - V_o)(1 - D) \quad (38)$$

From Equation (38), the proposed converter voltage gain is calculated by using the following expression,

$$\left. \frac{V_o}{V_i} \right|_{R_S} = \frac{(1 + D) - \{D(I_{SA}R_S + I_{SB}R_S)/V_i\}}{(1 - D)} \quad (39)$$

The switches  $S_A$  and  $S_B$  voltage drops are considered to be the same, and hence  $V_{DS} = I_{SA}R_S = I_{SB}R_S$ . Therefore, Equation (39) can also be expressed alternately as,

$$\left. \frac{V_o}{V_i} \right|_{R_S} = \frac{(1 + D) - 2D(V_{DS})/V_i}{(1 - D)} \quad (40)$$

It is observed from (39)-(40) that for larger values of  $V_{DS}/V_i$  and  $D$ , the voltage gain is decreasing. Hence, moderate values of the switches ON-state resistance should be considered.

### 3.4 | Effect of capacitor C

Other parasitic irregularities are neglected for analyzing capacitor  $C$ , ESR effect on voltage gain that is by considering  $R_{LA} = 0$ ,  $R_{LB} = 0$ ,  $R_D = 0$ ,  $V_{FD} = 0$ , and  $R_S = 0$ . Here, the voltage drop across resistance  $R_C$  is denoted by  $V_{DC}$ . The capacitor  $C$  is being discharged via load  $R_{out}$  when the switches are kept at ON position. There is a decrement in voltage across the capacitor  $C$  which is the same as the output voltage and the instantaneous value of output voltage is obtained as follows,

$$v_{out} = V_o - V_{DC} - \frac{I_o}{C}t = V_o \left( 1 - \frac{1}{R_{out}C}t \right) - V_{DC} \quad (41)$$

Hence, output voltage variation ( $\Delta V_o$ ) at the end of ON-state is,

$$\Delta V_o|_C = \frac{V_o}{R_{out}Cf} \times D \quad (42)$$

### 3.5 | Non-idealities' integrated effect on voltage gain

The non-idealities associated with the inductors  $L_A$  and  $L_B$ , diodes  $D_A$ ,  $D_B$ , and  $D_C$ , switches  $S_A$  and  $S_B$ , and their ESR effects on voltage gain have been considered; the voltage gain is expressed as,

$$\frac{V_o}{V_i} \approx \frac{1 + D - \frac{2V_{DL}}{V_i} - (2 - D)\frac{V_{DD}}{V_i} - 2D\frac{V_{DS}}{V_i}}{1 - D} \quad (43)$$

### 3.6 | Evaluation of efficiency

For capacitor  $C$ , ON-state and OFF-state currents can be expressed as,

$$\begin{aligned} \text{ON-State : } I_C &= -V_o R_{out}^{-1}, \\ \text{OFF-State : } I_C &= I_i - V_o R_{out}^{-1} \end{aligned} \quad (44)$$

Inductors  $L_A$  and  $L_B$  currents are equal in the OFF state that is  $I_L = I_{LA} = I_{LB}$ . Now, considering the capacitor charge balance principle, and the method of small approximation, together with Equation (44),

$$\begin{aligned} \int_0^{DT} \left( \frac{V_o}{R_{out}} \right) dt &= \int_{DT}^T \left( I_L - \frac{V_o}{R_{out}} \right) dt \Rightarrow \frac{V_o}{R_{out}} D \\ &= \left( I_L - \frac{V_o}{R_{out}} \right) (1 - D) \end{aligned} \quad (45)$$

Inductor currents are calculated by using Equation (45) as,

$$I_L = I_{LA} = I_{LB} = \frac{V_o R_{out}^{-1}}{1 - D} \quad (46)$$

The switching power losses of switches  $S_A$  and  $S_B$  are denoted by  $P_{SW-SA}$  and  $P_{SW-SB}$ , respectively. The total switching loss during switching is denoted by  $P_{SW-TOT}$  and can be expressed as,

$$\begin{aligned} P_{SW-TOT} &= \sum_{i=A,B} P_{SW-i} \\ &= \frac{1}{T} \left\{ (I_{SA} \times V_{SA}) (t_{R-SA} + t_{F-SA}) \right. \\ &\quad \left. + (I_{SB} \times V_{SB}) (t_{R-SB} + t_{F-SB}) \right\} \end{aligned} \quad (47)$$

where,  $t_{R-SA}$ ,  $t_{F-SA}$ , and  $t_{R-SB}$ ,  $t_{F-SB}$  being the respective rising and falling times for the switches  $S_A$  and  $S_B$ ; the switches  $S_A$  and  $S_B$  average currents are  $I_{SA}$  and  $I_{SB}$ , and the average voltages across the switches  $S_A$  and  $S_B$  are  $V_{SA}$ , and  $V_{SB}$  respectively. The total input and output power can be expressed as,

$$\begin{cases} P_m = V_i \{ 2I_L D + I_{LA} (1 - D) \} + P_{SW-TOT} \\ = \frac{V_i V_o R_{out}^{-1}}{1 - D} (1 + D) + P_{SW-TOT} \end{cases}, P_{out} = \frac{V_o^2}{R_{out}} \quad (48)$$

The proposed converter's efficiency  $\eta_{PRO}$  is obtained from Equations (43)-(48), and is expressed as,

$$\eta_{PRO} = \frac{1 + D - \frac{2V_{DL}}{V_i} - \frac{(2-D)V_{DD}}{V_i} - \frac{2DV_{DS}}{V_i}}{(1 + D) + P_{SW-TOT} \frac{R_{out}(1-D)}{V_i V_i}} \quad (49)$$

**TABLE 1** Comparison of DC-DC Converters

Converter	Number of reactive components		Number of Semiconductor devices		Total components	CCM Voltage gain (M)	Switch current stress	Efficiency	Output port
	Inductor	capacitor	Control Switches	Diodes					
A	1	1	1	1	4	$1/1-D$	$I_i$	–	Grounded
B	2	1	1	4	8	$1+D/1-D$	$I_i$	95.2% at 50 W	Grounded
C	2	1	2	1	6	$1+D/1-D$	$2I_i / 1+D$	92.7% at 40 W	Floating
D	2	3	2	4	11	$1+D/D(1-D)$	$2I_i / 1+D$	–	Grounded
E	2	3	1	2	8	$2/1-D$	$I_i$	92.2% at 100 W	Grounded
F	6	1	3	12	22	$1+5D/1-D$	$I_i(1+D)/(1+5D)$	95.6% at 200 W	Floating
G	2	1	3	2	8	$1+D_1/1-D_1-D_2$	$I_i / 2, I_i$	93.6% at 100 W	Floating
H	2	2	3	3	10	$2-D_2/1-D_1-D_2$	$I_i D_1/2, I_i D_2$	93.43% at 500 W	Floating
I	2	1	2	3	8	$1+D/1-D$	$I_i / 2, I_i / 2$	93.12% at 500 W	Grounded

#### 4 | COMPARATIVE STUDY OF CONVERTERS

To achieve a high voltage gain and an improved efficiency several DC-DC boost converters have been proposed in the past decade. This section presents a comparison of the proposed converter with some similar high gain DC-DC converters. The converters are compared for the voltage gain, switch current stress, components count, and efficiency and presented in Table 1. The components count for the proposed converter is observed to be the same as that of the converters discussed in [21, 25], and [30], while the components count for the converter presented in [26] is lesser than the converter proposed here. However, the proposed converter's efficiency is more than the converter in [26]. Furthermore, the output and input of the proposed converter and the converters in [21, 24], and [25] are on common ground, while the rest of the converters are only suitable in the conditions of floating load. The converter's efficiency depends on different factors such as the components count, their types, and voltage/current ratings. The comparison with regards to switch current stress among the different converters indicates that the proposed converter has the lowest current stress across the active switches and is equal to half of the input current. The proposed topology is based on a transformer-less design and it is developed by substituting a diode of the traditional switched inductor configuration with a switch in parallel with the existing switch. Hence, low current rating switches can be incorporated, as the total input current is equally shared by the two switches. Generally, the increase in the rating of a device leads to an increment in its ON-state resistance. Components with lower rating are required for the proposed converter topology and hence it comes up with a low-cost design and generates a high efficiency with the same number of components used in the traditional SIBC. The efficiency of the proposed converter is 93.12%, which is higher than the efficiency of the converters presented in [25] and [26] which are 92.2% and 92.7%, respectively. The proposed converter's efficiency is nearly equal to the

converters in [29] and [30], while the proposed converter's efficiency is lesser than the converters in [19] and [21].

A: Traditional Boost Converter, B: Conventional switched inductor based boost converter [21], C: converter-I [26], D: Non-isolated voltage lift converter [24], E: modified SEPIC converter [25], F: Active-passive switched inductor converter [19], G: High gain converter [30], H: DDTM converter [29], I: proposed converter.

Therefore, the converter proposed is highly suitable for high voltage gain with reduced switch current stress and less duty cycle, high efficiency, and low-cost applications.

#### 5 | DESIGN AND RESULTS

To validate the operation and performance of the proposed converter it is designed by taking into account the typical values of input voltage as 100 V, output voltage as 400 V, power output as 500 W, and the switching frequency as 100 kHz.

##### 5.1 | Reactive components

The worst possible efficiency ( $\eta_{worst}$ ) has been taken into account for the design of the reactive components to obtain a good performance. Therefore, the required duty cycle can be calculated by considering the worst efficiency as 90%, and is expressed as,

$$D|_{\eta_{worst}=90\%} = \frac{M_{CCM} - 1}{(M_{CCM} + 1)\eta_{worst}} = \frac{4 - 1}{(4 + 1)0.90} \approx 66.67\% \quad (50)$$

The inductors  $L_A$  and  $L_B$  critical values are calculated as,

$$L_A|_{critical} = L_B|_{critical} = \frac{V_i}{\Delta I_L} DT = \frac{V_i}{40\%oI_L} DT \quad (51)$$



The ripple value of peak to peak inductor currents is considered as 1A to calculate the critical values of inductor  $L_A$  and  $L_B$  and are expressed as,

$$L_A|_{critical} = L_B|_{critical} = \frac{100V \times 0.67}{1A \times 100kHz} \approx 670\mu H \quad (52)$$

The inductors'  $L_A$  and  $L_B$  current rating and inductance value should be more than the value of input current and critical inductance values, respectively. Therefore, the prototype is designed by selecting 1 mH/10 A rated core inductors of ferrite E type having  $R_L = 75 \text{ m}\Omega$ .

The critical capacitance of capacitor  $C$  at the output side is calculated by,

$$C|_{critical} = \frac{P_{out}}{V_o \Delta V_C} DT \quad (53)$$

The peak to peak ripple value of the capacitor voltage is considered as 4 V to calculate the capacitor  $C$  critical capacitance and is obtained as,

$$C|_{critical} = \frac{500W \times 0.67}{400V \times 4V \times 100kHz} \approx 2.1\mu F \quad (54)$$

The capacitor  $C$  voltage rating should be more than the value of output voltage that is 400 V. Thus, the prototype is designed by selecting a  $2.2 \mu F/450 \text{ V}$  ( $R_C = 4 \text{ m}\Omega$ ) rated film type capacitor.

## 5.2 | Semiconductor devices

The switches  $S_A$  and  $S_B$  voltage stresses are calculated as,

$$V_{S_A}|_{stress} = \frac{V_o + V_i}{2}, V_{S_B}|_{stress} = V_o \quad (55)$$

The switches  $S_A$  and  $S_B$  minimum voltage rating can be calculated as,

$$V_{S_A} = \frac{400V + 100V}{2} = 250V, V_{S_B} = 400V \quad (56)$$

The selected switches  $S_A$  and  $S_B$  current ratings should be higher than the value of input current. Thus, FDP19N40-ND ( $R_s = 200 \text{ m}\Omega$ ) MOSFET and FDP18N20-ND ( $R_s = 140 \text{ m}\Omega$ ) MOSFET have been chosen.

The diodes  $D_A$ ,  $D_B$ , and  $D_C$  Peak Inverse Voltage (PIV) rating can be obtained as,

$$V_{D_A}|_{PIV} = \frac{V_i - V_o}{2}, V_{D_B}|_{PIV} = -V_i, V_{D_C}|_{PIV} = -V_o \quad (57)$$

The diodes  $D_A$ ,  $D_B$ , and  $D_C$  minimum PIV rating considering the given parameters can be obtained as,

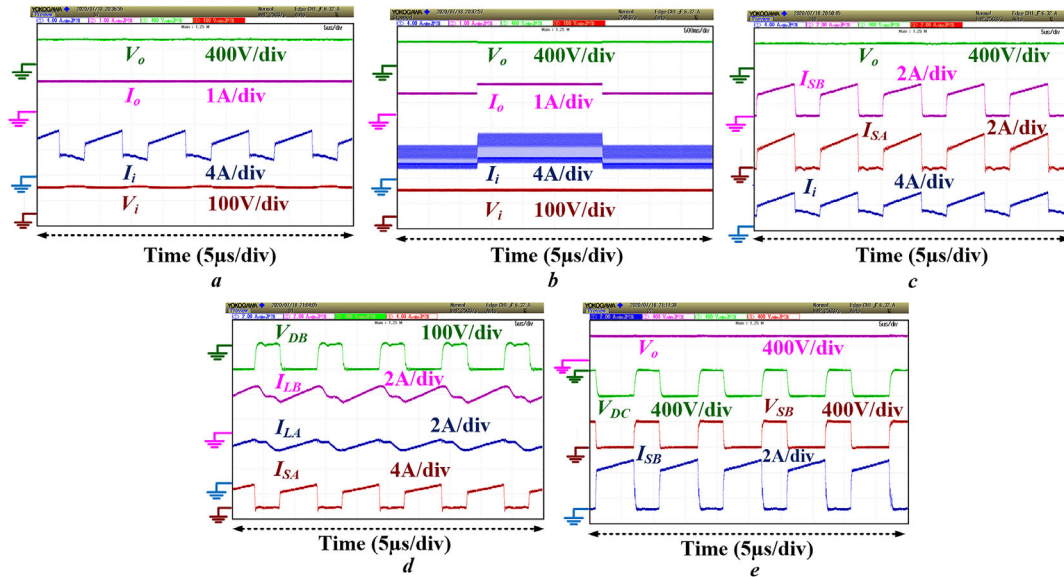
$$\begin{cases} V_{D_A}|_{PIV} = \frac{(100 - 400)}{2} = -150V, V_{D_B}|_{PIV} = -100V \\ V_{D_C}|_{PIV} = -400V \end{cases} \quad (58)$$

The selected diodes  $D_A$ ,  $D_B$ , and  $D_C$  current ratings should be higher than the value of input current. Thus, DPG10I400PM (400 V/10 A,  $R_D = 19.8 \text{ m}\Omega$ ,  $V_{FD} = 0.77 \text{ V}$ ) and C3D10060A-ND (600 V/14 A,  $R_D = 55.2 \text{ m}\Omega$ ,  $V_{FD} = 0.91 \text{ V}$ ) diodes have been chosen.

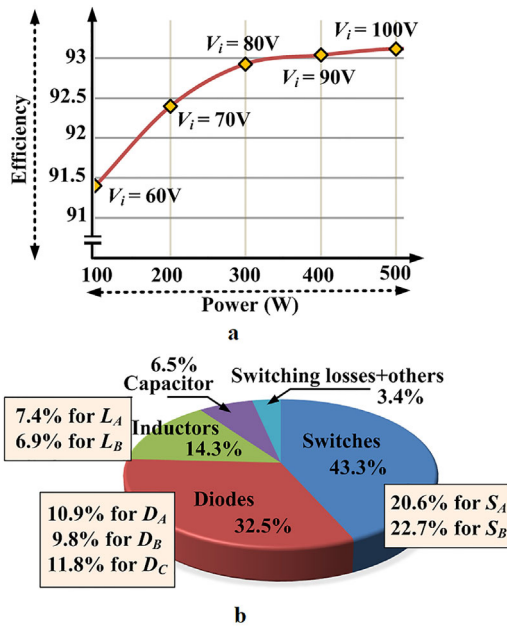
## 5.3 | Experimentally obtained results

The proposed converter's operation and performance have been experimentally verified. Figure 7(a) displays the input and output voltages and currents waveforms obtained experimentally. The output voltage, output current, input current, and input voltage average values are observed as 398 V, 1.2 A, 5.35 A, and 100 V, respectively. The input current is observed to be continuous in nature; charging and discharging of the inductors  $L_A$  and  $L_B$  during ON-state and OFF-state causes the input current slope to be increasing and decreasing, respectively. Figure 7(b) demonstrates the effect of the step change in load on input/output voltages and currents that is the dynamic behavior of the input/output voltages and currents for the proposed converter with a change in load at a constant duty ratio. It is observed from the experimentally obtained results, that the proposed system is developing stable input/output voltages and currents. The experimentally obtained waveforms of the currents through switches  $S_A$  and  $S_B$  are shown in Figure 7(c); where the output voltage and input current waveforms are included to refer and validate. The switches  $S_A$  and  $S_B$  average current values are observed as 1.54 and 1.62 A, respectively. Both the switches  $S_A$  and  $S_B$  current slopes are observed to be the same as the input current slope during the ON-state. Figure 7(d) shows the experimentally observed waveforms of currents through inductors  $L_A$  and  $L_B$ , and the voltage across the diode  $D_B$ ; where the switch  $S_A$  current waveform is shown for reference and validation. The inductors  $L_A$  and  $L_B$  average current values are observed as 2.99 and 3.1 A, respectively. The PIV across the diode  $D_B$  is observed as 100 V. Figure 7(e) shows the experimentally observed waveforms for the voltages across Switch  $S_B$  and the output diode  $D_C$ ; where the switch  $S_B$  current and the output voltage waveforms are shown to refer and validate. Both switches are observed to be turned ON and turned OFF together at the same time. The peak value of switch voltage across the switch  $S_B$  is observed as 399.4 V. When the switches are conducted, the output diode  $D_C$  is observed to be forward biased. The PIV across the diode  $D_C$  is observed as -399.2 V. The diodes  $D_A$  and  $D_B$  are observed to be forward biased in ON state and reversed biased in OFF state, respectively.

To study the efficiency of the developed prototype, the converter's performance is studied at different power levels and input voltage. Figure 8(a) shows the efficiency of the designed prototype with variation in power and input voltage. The efficiency of the developed prototype is 93.12% when the input voltage is 100 V and output power is 500 W. The power loss distribution is given in Figure 8(b) when load power is 500 W and the input voltage is 100 V. It is investigated that power loss across switches is high compared to other elements of the converter.



**FIGURE 7** Experimentally obtained results. (a) Output voltage, output current, input current, input voltage, (b) effect of step change in load: output voltage, output current, input current, input voltage, (c) output voltage, switches  $S_B$  and  $S_A$  currents, input current, (d) diode  $D_B$  voltage, inductors  $L_B$  and  $L_A$  currents, switch  $S_A$  current, (e) output voltage, diode  $D_C$  voltage, switch  $S_B$  voltage and current



**FIGURE 8** Plots. (a) Efficiency versus power for different input voltage. (b) Loss distribution at load power 500 W and input voltage 100 V

## 6 | CONCLUSION

A high gain DC-DC converter with reduced switch current stress has been successfully developed through this study. The proposed converter has a higher gain in voltage in comparison to the traditional boost converter and is equal to the gain in voltage of the conventional SIBC at a small duty cycle value. The proposed converter offers the advantage of common ground, continuous input current, and reduced current stress on the active switches using the same number of components as that

of a conventional SIBC. Therefore, low current stress active switches can be employed, leading to reduction in losses. Resulting in a low cost and highly efficient converter because of the use of active switches with lower current rating and eliminating a diode. Moreover, the common ground connection of source and load in the proposed converter circuit makes it highly suitable for DC Microgrid integrated with solar PV. The operating principle in both CCM and DCM including the boundary conditions, the voltage gain, and the effect of non-idealities have been discussed in detail. The comparison of the proposed converter with other similar converters has been presented, which indicates that the proposed converter is feasible to attain a high voltage gain by incorporating low current rating switches. The principle of operation and theoretical analysis have been validated by the experimental results of the developed laboratory prototype, the efficiency at 500 W load power was observed to be 93.12%. Hence, the proposed converter topology provides a viable solution for an efficient renewable energy conversion which can easily be extended further to other power conversion systems for applications where high voltage is required.

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