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Modeling and Control of Single-Stage Quadratic-Boost Split Source Inverters

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ABSTRACT This paper aims to develop the recently introduced Spilt-Source Inverter (SSI) topology to improve its boosting characteristics. New SSI topologies with high voltage gain are introduced in this paper. The proposed converters square the basic SSI's boosting factor by utilizing an additional inductor, capacitor, and two diodes. Thus, the proposed converters are called Quadratic-Boost (or Square-Boost) SSIs (QBIs or SBIs). Four different QBI topologies are presented. One with continuous input current (CC-QBI), and the other draws a discontinuous input current (DC-QBI) but with reduced capacitor voltage stresses. This paper also introduces the small-signal model of the CC-QBI using state variables perturbance. Based on this model, the closed-loop voltage and current control approach of the dc-boosting factor are designed. Moreover, a modified space vector modulation (MSVM) scheme is presented to reduce the input current ripples. To evaluate the performance of the proposed topologies, a comparative study between them and the other counterpart from different perspectives is introduced. It can be found that the CC-QBI topology has superior boosting characteristics when operating with low input voltage compared with their counterparts. It has a higher boosting capability, lower capacitor voltages, and semiconductor stresses, especially when high voltage gains are required. These merits make the proposed topologies convenient to the Photovoltaic and Fuel-Cell systems. Finally, the feasibility of the suggested topology and the introduced mathematical model is verified via simulation and experimental results, which show good accordance with the theoretical analysis.

INDEX TERMS Split-source inverters (SSI), quasi-z source inverters, dc-ac boost converter, space-vector PWM.

I. INTRODUCTION

Renewable Energy Sources (RES) have been rapidly growing in the past two decades to solve conventional power plants' problems and thus overwhelmed their negative impacts on the environment. Among RES, the Photovoltaic (PV) and fuel cell (FC) technologies are cleaner, and their penetration into the power system is continuously increasing [1], [2]. This growth has triggered the evolution of the dc-ac boost converter technologies, which are essential for interfacing the low voltage PV and FC modules (e.g., 20-40 Vdc) with the higher voltage grid or supplying isolated loads (e.g., 200-400 Vac) [3]–[5]. For this reason, the dc-ac boost converters undeniably represent an urgent research topic of

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continuously gaining interest in power electronics [6]. The possible solution to realize dc-ac conversions with high gains are classified into two-stage and single-stage converters.

The two-stage dc-ac converter has traditionally been used as the standard solution to interface RES with the loads/grids. In this topology, a dc-dc boost converter with high voltage gain is required to boost the low voltage of PV or FC panels [6]. After that, the Voltage Source Inverter (VSI) is used in the inversion process. There are two main types of dc-dc converters, namely isolated and non-isolated configurations [7]. In both, high voltage gains generally can be obtained using switched impedance (inductance and capacitance), voltage boost cells, cascading architecture, and coupled inductor [8]. Admittedly, this topology is functional. However, an additional switch is needed. This leads to many problems regarding the system complexities, controls, high costs, and low efficiency [9].

Alternatively, the basic Z-source inverter (ZSI) [10], which exploits an impedance network composed of two inductors, two capacitors, and one diode, has been proposed to surmount the problems caused by the two-stage architecture. It utilizes the shoot-through (ST) mode of the inverter bridge (B6) to boost the input dc voltage via the impedance network in a single stage. Accordingly, ZSI technology has facilitated the evolution of various single-stage topologies. These topologies have garnered considerable discussions among researchers to improve efficiency, boost capability, and compactness.

Several comprehensive reviews of the different ZSIs topologies and modulation techniques have been reported in the literature [11]–[17]. Among the plenteous structures of ZSIs, quasi-ZSI (qZSI) topology, shown in Fig. 1(a), is found to be more suitable for the PV, FC applications, multiport topologies, Electric-Vehicles (EVs), and electric drives applications due to its simple structure and continuous input current [17]–[19]. Notwithstanding this attractive utilization of the ZSI/qZSI in many applications, it suffers from common shortcomings that should be considered before utilizing these inverters in the industry. These shortcomings can be summarized as follows [11], [12]:

1) The ST intervals shrink the modulation region, give low voltage quality, and reduce the dc-bus utilization.
2) The dc-link voltage is pulsed with high dv/dt.
3) A long ST is needed to provide a high gain; hence, ZSIs would have to be operated under extreme conditions with a low output voltage quality. Also, in this case, the impedance network's parasitic effects become more dominant, and thus, the gain is significantly reduced.
4) More passive components should be used to form an extended impedance source network to accomplish a high voltage gain with a short ST duration.

With the accelerated development of modern technologies, ZSIs demerits limit further industrial applications in some areas that require high boosting and inversion functions.

Recently, the SSI topology, shown in Fig. 1(b), has been suggested to surmount the ZSIs problems [20]. As can be seen from Fig. 1(b), this topology was acquired by combining the canonical dc-dc boost converter into the VSI, by connecting the boost inductor, L to the midpoint of each inverter leg (a, b, and c) via diodes (D_a, D_b, and D_c). Contrary to ZSIs, it can perform the boosting and inversion functions for a wide modulation index range. Theoretically, SSI obtains a proportional relationship to infinity between the voltage gain and modulation index with fewer passive elements. Also, it does not require the ST mode.

As a research hotspot, the basic topology of SSI has been extended to single-phase applications [21]–[24], multiport inverters [25], [26], and multilevel technologies [27], [28]. Moreover, it was explored for a wide range of applications [20]–[28]. However, the parasitic effects of the passive elements in SSI topology, which is based on the canonical step-up converter, significantly impact its boosting and output voltage gain. Consequently, the output voltage gain does not reach infinity in practice. As a result, the developments for the basic SSI are thus essential to achieve higher voltage gain. To the best of the authors' knowledge, scarce research works have focused on developing the SSI topology [29]–[31]. For example, a split-Y-source inverter has been introduced in [29], [30]. This topology increases the boosting factor and the voltage gain. Moreover, the voltage spikes, commonly generated in the Y-source impedance network, are avoided in this work. However, this topology is complex in implementation and has more passive elements.

Addressing this concern, this paper aims to develop the SSI topology to improve its boosting capability with a simple circuit structure. The developed topologies combine ZSI [10], quadratic boost dc-dc converter [32], and SSI features in a single circuit to obtain a square boosting in the dc-side. The newly obtained SSI topology is called Quadratic-Boost

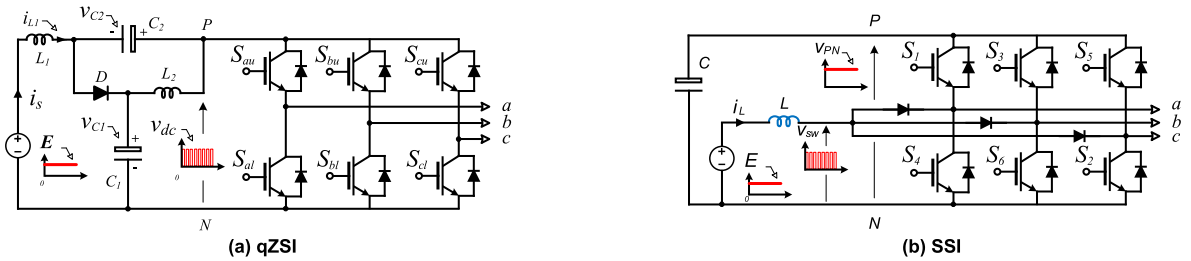


FIGURE 1. Traditional single-stage boosting three-phase inverter topologies.

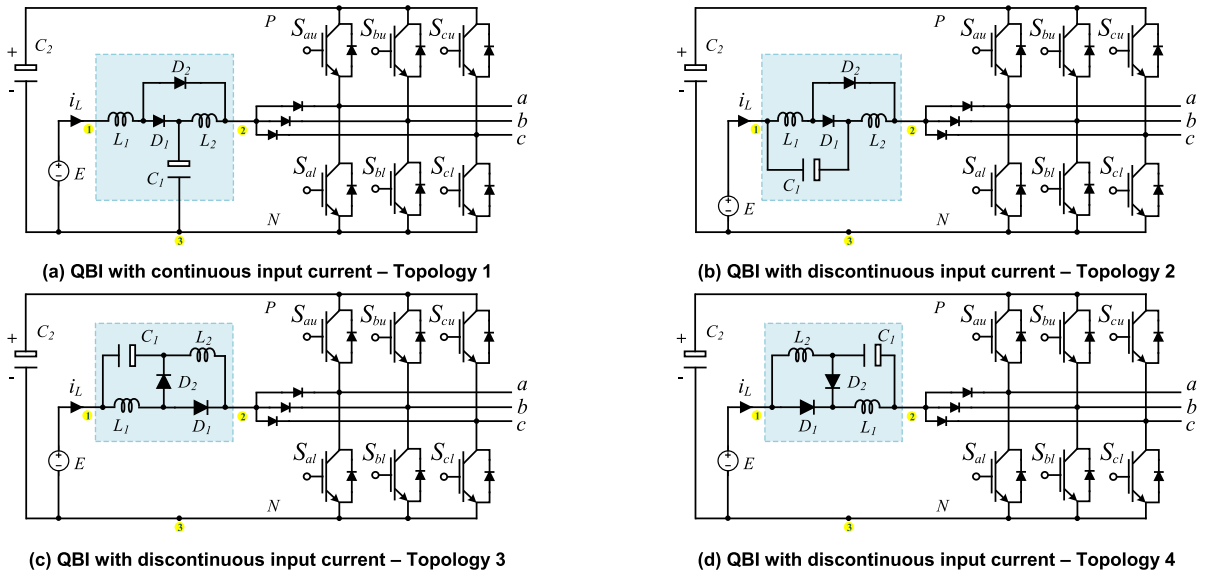


FIGURE 2. Proposed QBI topologies.

SSI and is then termed by QBI. Four different topologies of the proposed QBI are introduced, as shown in Fig. 2. One with continuous input current (CC-QBI), and the other draws a discontinuous input current (DC-QBI) but with reduced capacitor voltage stresses. All topologies are modulated by the modified SVPWM scheme of the basic SSI. The main characteristics of these topologies compared to the previous boost inverters can be summarized as follows:

1) The basic spilt-source structure is retained.
2) Both boost and buck operations can be achieved.
3) Higher boosting and voltage gains are obtained.
4) It uses the conventional modulation schemes of SSI.
5) The CC-QBI has a continuous dc-current, while other architectures have a lower capacitor voltage.

However, it corresponds to the following demerits:

1) Like the basic SSI, unequal switch current sharing and power distribution are found compared to qZSI.

Given its many merits, this paper first introduces the proposed topologies and operating principles. The boosting factor and voltage gain are analyzed in detail for both ideal and considering the nonlinearities cases.

A modulation technique to reduce the inductor current ripples is presented. Moreover, the performance of the proposed topologies is assessed and compared with their counterparts. Finally, simulation and experimental results are given to confirm the theoretical findings.

II. PROPOSED INVERTER TOPOLOGY AND ITS OPERATING MODES

A. TOPOLOGY

Four different topologies of the proposed QBI are shown in Fig. 2. In all topologies, the input inductance of the basic SSI, L_1, shown in Fig. 1(b) is replaced by an impedance cell. This cell is composed of two inductors, L_1, L_2, capacitor, C_1 and two diodes, D_1, D_2. This combination is used to perform a cascaded boosting without additional switching states. The QBI, shown in Fig. 2(a), has a continuous input current compared to the others shown in Figs. 2(b)-(d). This is owed to the presence of the input inductance L_1 in series with the supply, which buffers the supply current and reduces the supply stresses. Therefore, in the QBI with discontinuous input current (DC-QBI) of the Figs. 2(b)-(d), an additional input parallel capacitance with the supply is needed to mitigate input ripples' harmful effects. Nevertheless, the voltage stress on the capacitor C_1 in the DC-QBI is lower than that of the QBI with continuous input current (CC-QBI). Moreover, all topologies feature a common dc-rail between the supply and inverter bridge. This connection reduces common-mode noise effects. The features of the proposed topologies are summarized in Table-1.

B. OPERATING PRINCIPLES

1) MODES OF OPERATION

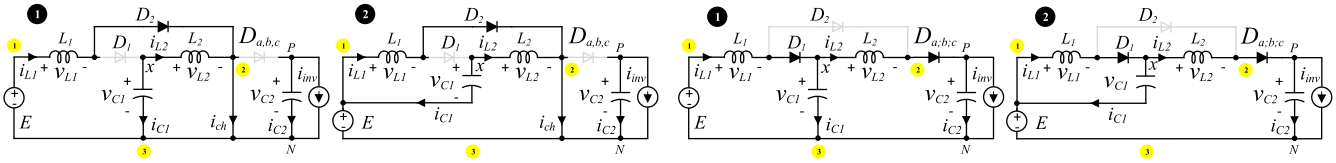
Inductive charging and discharging modes of operation can be observed in all QBI topologies. The ideal equivalent circuits during both modes are shown in Fig. 3. For the analysis's abridgment, the equivalent circuits of two different topologies are selected, the first one for the CC-QBI, shown in Fig. 2(a), and the other for the DC-QBI topology Fig. 2(b), as shown in Fig. 3.

2) STEADY-STATE ANALYSIS

In this section, the steady-state analysis of QBI topologies is reported. This analysis is simplified by considering an ideal case. In this analysis, the CC-QBI and DC-QBI topologies equations will be remarked by ❶, and ❷, respectively.

a: INDUCTIVE CHARGING MODE

The charging mode can be obtained by switching ON at least one of the lower switches in the inverter bridge. In this case,



(a) charging mode of both CC-QBI ❶ and DC-QBI ❷, respectively.

(b) discharging mode of both CC-QBI ❶ and DC-QBI ❷, respectively.

FIGURE 3. Modes of operations of the proposed QBIs.

TABLE 1. Comparison between QBI topologies.

Topologies	Supply Current	V_{C1}	Needs of Input Cap.	dc-rail
DC-QBI	Discontinuous	Low	√	Common
CC-QBI	Continuous	High	x	Common

the voltage at the output of the dc-side is zero due to the short-circuited. Besides, the diode D_1 is blocking, while the diode D_2 is conducting, as shown in Fig. 3(a). As a result, both inductors L_1 and L_2 are charged. By applying KVL, the following steady-state relationships during the charging duty cycle, D_{ch} can be observed.

$$\text{❶}\begin{cases} v_{L1} = E \\ v_{L2} = v_{C1} \\ i_{C1} = -i_{L2} \\ v_{D1} = -v_{L2} \\ i_{ch} = i_{L1} + i_{L2} \end{cases} \text{ and } \text{❷}\begin{cases} v_{L1} = E \\ v_{L2} = E + v_{C1} \\ i_{C1} = -i_{L2} \\ v_{D1} = -v_{L2} \\ i_{ch} = i_{L1} + i_{L2}. \end{cases} \tag{1}$$

b: INDUCTIVE DISCHARGING MODE

The discharging mode has only occurred when all the upper switches in the B6 are turned ON. In this case, the diode D_1 will conducting, while D_2 is in the blocking mode, as shown in Fig. 3(b), obtaining the following relation during a discharging duty cycle of $D_{dis} = 1 - D_{ch}$.

$$\text{❶}\begin{cases} v_{L1} = E - v_{C1} \\ v_{L2} = v_{C1} - v_{C2} \\ i_{C1} = i_{L1} - i_{L2} \\ v_{D2} = v_{L2} \end{cases} \text{ and } \text{❷}\begin{cases} v_{L1} = -v_{C1} \\ v_{L2} = E + v_{C1} - v_{C2} \\ i_{C1} = i_{L1} - i_{L2} \\ v_{D2} = v_{L2} \end{cases} \tag{2}$$

Based on the volt-second balance concept, the moving average voltage across the inductors over one switching period is zero (i.e., $\int_0^{T_s} v_L dt = 0$). From (1) to (2), we have

$$\text{❶}\begin{cases} V_{L1} = \tilde{v}_{L1} = ED_{ch} + (E - v_{C1})\, D_{dis} = 0 \\ V_{L2} = \tilde{v}_{L1} = v_{C1} D_{ch} + (v_{C1} - v_{C2})\, D_{dis} = 0, \end{cases}$$
$$\text{❷}\begin{cases} V_{L1} = \tilde{v}_{L1} = ED_{ch} - v_{C1} D_{dis} = 0 \\ V_{L2} = \tilde{v}_{L1} = v_{xN} D_{ch} + (v_{xN} - v_{C2})\, D_{dis} = 0 \\ v_{xN} = E + v_{C1}. \end{cases} \tag{3}$$

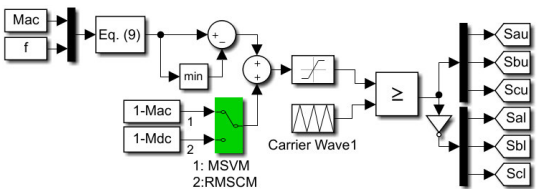


FIGURE 4. Block diagram of MSVM schemes for QBI.

Thus, the voltage across the capacitors of both topologies is

$$\text{❶}\begin{cases} V_{C1} = E/\left(1 - D_{ch}\right) = \beta_o E \\ V_{C2} = E/\left(1 - D_{ch}\right)^2 = \beta_o^2 E \end{cases}$$
$$\text{❷}\begin{cases} V_{C1} = ED_{ch}/\left(1 - D_{ch}\right) = \left(\beta_o - 1\right) E \\ V_{C2} = E/\left(1 - D_{ch}\right)^2 = \beta_o^2 E \end{cases} \tag{4}$$

where β_o is the dc-boosting factor of the basic SSI, and its value is defined by

$$\beta_o = 1/\left(1 - D_{ch}\right) \tag{5}$$

It can be observed from (4) that the capacitor C_1 voltage, V_{C1} in DC-QBI is much lower than that of CC-QBI as expected, while the voltage stress across the inverter switches, which is measured on the capacitor C_2 are equals for both topologies.

3) BOOSTING FACTOR AND AC VOLTAGE GAIN

Based on (4) the boosting factor, B of the QBI topologies, which is defined by the ratio of the average voltage across the inverter legs (V_{C2}) to the input voltage, E can be written as

$$B = 1/\left(1 - D_{ch}\right)^2 = \beta_o^2 \tag{6}$$

It is worth noting that the boosting factor of the proposed QBI gives a square relationship of the basic SSI topology.

Finally, the output ac voltage gain (G) is governed by

$$G = \frac{\hat{V}_{\phi 1}}{E} = \frac{BM_{ac}}{\sqrt{3}} = \frac{M_{ac}}{\left[\sqrt{3}\left(1 - D_{ch}\right)\right]^2} \tag{7}$$

where $\hat{V}_{\phi 1}$ is the fundamental peak output phase voltage. It is worth noting that $G \leq 1/\sqrt{3}$ for conventional VSI.

C. MODULATION

Although all PWM schemes of the standard VSI can be used to modulate the proposed QBI switches to obtain the boosting

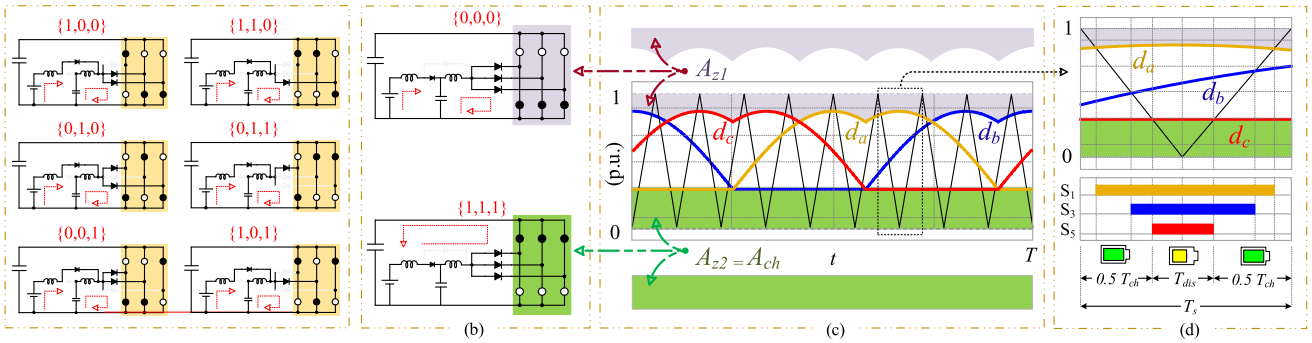


FIGURE 5. Modulation of quadratic-boost split-source inverter.

and inversion functions, modified unregulated and regulated SVPWM (MSVM and RMSVM) schemes, proposed in [20], and [33] represent the standard modulation approach of all extended-boost-based SSIs due to the following merits:

1) It successfully ensures inductor charging and discharging with constant duty cycles. Consequently, lower input current ripples and voltage stresses are obtained.
2) It can be used to obtain the same performance as the two-stage topology.

In the carrier-based implementation of this scheme, the per-phase duty cycles (d_a, d_b, d_c), which are compared with the triangular high-frequency carrier-wave to generate the gating pulses of the B6 switches, can be defined by

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \min(v_a, v_b, v_c) + (1-\gamma) \tag{8}$$

where M_{ac} is the modulation index and, v_a, v_b and v_c are the sinusoidal reference signals, which are governed by

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{M_{ac}}{\sqrt{3}} \begin{bmatrix} \cos(2\pi ft) \\ \cos(2\pi ft - 2\pi/3) \\ \cos(2\pi ft + 2\pi/3) \end{bmatrix} \tag{9}$$

The last term in (8) represents a constant upward shifting term of the duty cycles responsible for the boosting. In the MSVM scheme, γ, in (8) is equal to M_{ac} [20]. Therefore, both the dc-boosting factor, B, and the output voltage gains are controlled via the one control variable, M_{ac}. The RMSVM scheme give the inverter an additional control variable in the dc side by replacing γ in (8) by M_{dc} [33]. This yields to independent control between the dc and ac sides, which is necessary for the grid-connected applications and V/f control of the motor drives.

Figs. 4 and 5 show the implementation block diagram of the phase duty cycles generation and switching pattern of these modulation schemes, where the manual switch is used to select between the unregulated and regulated MSVM approach.

In the regulated modulation scheme, the QSI can be considered as two separate converters (i.e., quadratic boost dc-dc converter and VSI), and hence, the standard control modes can be implemented. Observing Fig. 5, the upper and lower switches for each leg of the B6 are commutated one per half switching cycle with variable duty cycles, like in the standard VSI.

Meanwhile, the overall inductive charging and discharging intervals (T_{ch} and T_{disch}) are fixed since the minimum envelope of the per phase duty cycles is kept constant at $(1-\gamma)$ where γ equals to M_{dc}. However, M_{dc} must be higher than M_{ac} to ensure that the per phase duty cycles (d_a, d_b, d_c) remain less than 1 (i.e.: the carrier amplitude) and hence maintaining in linear modulation region. Based on the volt-second balance concept, the inductor L is charged with

$$D_{ch} = M_{dc} \tag{10}$$

From (6), (7), and (10), the boosting factor, B, and ac-voltage gain of the proposed QBI using the RMSVM scheme are

$$\begin{cases} B = 1/(1-M_{dc})^2 \\ G = M_{ac}/\left\{\sqrt{3}(1-M_{dc})^2\right\} \end{cases} \tag{11}$$

It can be noticed from (10) that, when M_{dc} ranges from 0 to 1, the booting factor, B vary from 1 to infinity. However, due to the parasitic effects of the modulation deadtime and passive elements of the QSI, the boosting factor in practice is limited. On the other hand, the proposed topology can be used for the buck operating mode. This mode can be achieved by canceling the upward shifting term in (8) or by setting M_{dc} by one. In the following section, an analytical study of the proposed QBI topology considering the inverter nonlinearities is presented.

III. MODELING OF THE PROPOSED TOPOLOGY CONSIDERING THE NONIDEALITIES

For simplicity, the CC-QBI topology is only considered in the analysis due to its merits and the suitability of the applications. Fig. 6 shows the nonideal equivalent circuits of the CC-QBI by considering the effect of the inductor parasitic resistance and equivalent series resistance of the capacitors. In this section, the state-space averaging approach of the CC-QBI, assuming continuous condition mode, is described and used to derive the quiescent dc and small-signal ac equations of the analyzed topology.

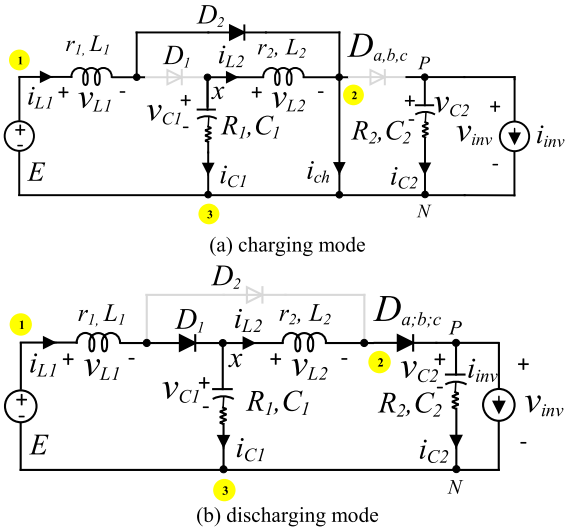


FIGURE 6. Equivalent circuit Of CC-QBI with nonlinearities.

A. STATE-SPACE AVERAGING MODEL

As in the ideal case analysis, the operation of QBI is divided into inductive charging and discharging modes. In both modes, the independent states of the inverter are the inductor currents, i_{L1}, i_{L2} and the capacitor voltages, v_{C1}, v_{C2}. Therefore, the state vector $x(t)$ can be defined as

$$x\left(t\right)=\left[\begin{array}{cccc} i_{L1} & i_{L2} & v_{C1} & v_{C2} \end{array}\right]^{T} \tag{12}$$

The input and output variables, $u(t)$ and $y(t)$ are defined by

$$u(t)=\left[\begin{array}{cc} e & i_{inv} \end{array}\right] \tag{13}$$

$$y\left(t\right)=v_{inv} \tag{14}$$

where e is the input-dc voltage, i_{inv} is the dc-link current, and v_{inv} is the output voltage of the dc-side, which can also be defined as the inverter bridge voltage.

During the charging mode of the duty cycle $d = d_{ch}$, the dc-side of the inverter is reduced to the linear circuit of Fig. 6(a), which the following state-space equations can describe:

$$\begin{cases} \dot{x}\left(t\right)=A_1x\left(t\right)+B_1u\left(t\right) \\ y\left(t\right)=C_1x\left(t\right)+D_1u\left(t\right) \end{cases} \tag{15}$$

where

$$A_1=\begin{bmatrix} -\frac{r_1}{L1} & 0 & 0 & 0 \\ 0 & -\frac{R_1+r_2}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},\quad B_1=[]$$

$$C_1=\begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix},\quad D_1=\begin{bmatrix} 0 & -R_2 \end{bmatrix} \tag{16}$$

With the zero-state, V_7, the inverter is in the discharging mode for the duty cycle of $d' = 1 - d_{ch}$. The equivalent linear circuit of this mode is shown in Fig. 6(b). It can be described by the following state-space equation

$$\begin{cases} \dot{x}\left(t\right)=A_2x\left(t\right)+B_2u\left(t\right) \\ y\left(t\right)=C_2x\left(t\right)+D_2u\left(t\right) \end{cases} \tag{17}$$

where

$$A_2=\begin{bmatrix} -\frac{R_1+r_1}{L_1} & \frac{R_1}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{R_1}{L_2} & -\frac{R_1+R_2+r_2}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix}$$

$$B_2=\begin{bmatrix} 1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}^{T}$$

$$C_2=\begin{bmatrix} 0 & R_2 & 0 & 1 \end{bmatrix},\quad D_2=\begin{bmatrix} 0 & 0 \end{bmatrix} \tag{18}$$

So, the matrices A_1, B_1, C_1, and D_1 for the charging mode and A_2, B_2, C_2, and D_2 for the discharging mode are defined. Given these matrices, the averaged state-space model (large-signal model) can be defined by

$$\begin{cases} \dot{x}\left(t\right)=\bar{A}x\left(t\right)+\bar{B}u\left(t\right) \\ y\left(t\right)=\bar{C}x\left(t\right)+\bar{D}u\left(t\right) \end{cases} \tag{19}$$

where the matrices $\bar{A}$, $\bar{B}$, $\bar{C}$ and $\bar{D}$ are evaluated by applying the state-space averaged equilibrium equations of (20),

$$\begin{cases} \bar{A}=A_1d+A_2d' \\ \bar{B}=B_1d+B_2d' \\ \bar{C}=C_1d+C_2d' \\ \bar{D}=D_1d+D_2d' \end{cases} \tag{20}$$

B. STEADY-STATE DC-MODEL

If the inverter is driven with the steady-state at the quiescent operating point, the duty cycle, d and input voltage, e in the state-space model of (19) and (20) are equal D_{ch} and E, respectively. The steady-state model can be derived from a large-signal model by setting $(\dot{x}\left(t\right)=0)$ and hence:

$$\begin{cases} 0=\bar{A}X+\bar{B}U \\ Y=\bar{A}X+\bar{B}U \end{cases} \tag{21}$$

where X, U, and Y are the state, input, and output variables at steady-state, respectively.

Solving (21) to find the equilibrium state and output vectors

$$\begin{cases} X=-\bar{A}^{-1}\bar{B}U \\ Y=\left(-C\bar{A}^{-1}\bar{B}+\bar{D}\right)U \end{cases} \tag{22}$$

This results in the following steady-state equations

$$\begin{cases} I_{L1}=\dfrac{1}{1-D_{ch}}I_{L2} \\ I_{L2}=\dfrac{D_{ch}}{1-D_{ch}}I_{INV}, \end{cases}$$

TABLE 2. System parameters and operating conditions used for the frequency analysis.

Parameter	*Value*	Parameter	*Value*	Parameter	*Value*
E	$100\,V$	R_L	$20\,\Omega$	$C_1 = C_2$	$120\,\mu F$
L_1	$1.25\,mH$	r_1	$0.05\,\Omega$	R_1	$0.1\,\Omega$
L_2	$1.25\,mH$	r_2	$0.05\,\Omega$	R_2	$0.1\,\Omega$

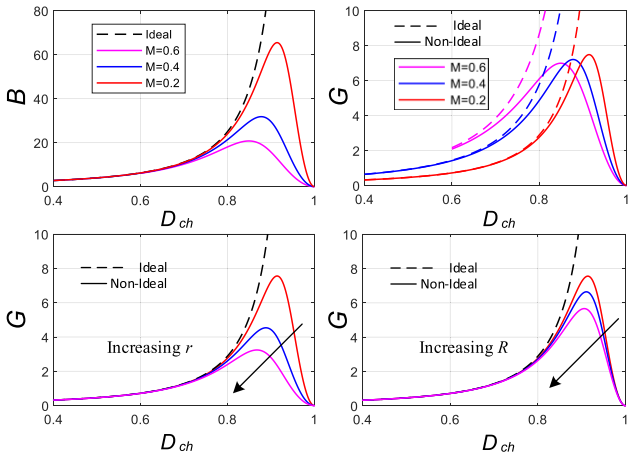


FIGURE 7. Nonideal dc-voltage boosting and ac-voltage gain of the proposed CC-QBI.

$$\begin{cases} V_{C1} = \dfrac{E}{1 - D_{ch}} - V_u \\ V_{C2} = V_{inv} = \dfrac{E}{(1 - D_{ch})^2} - V_w \end{cases} \tag{23}$$

where

$$\begin{cases} V_u = \left(D_{ch} R_1 + \dfrac{r_1}{1 - D_{ch}} \right) I_{L1} \\ V_w = \left(\dfrac{D_{ch} R_1}{1 - D_{ch}} + \dfrac{r_1}{(1 - D_{ch})^2} \right. \\ \qquad \left. + D_{ch} r_2 + (1 - D_{ch}) R_2 \right) I_{L1} \end{cases} \tag{24}$$

It is worth noting that the same steady-state equation in the ideal case can be obtained from (23) and (24) by neglecting the nonlinear effects of the parasitic resistance of the inductors and the ESR of the capacitors. Figs. 7 and 8 show the plot of dc-boosting, ac-voltage gain, and inverter efficiency considering the nonideal circuit parameters of Table 2 at different modulation indices. It is evident how the increase of the inductor's parasitic resistance and ESR of the capacitors reduce the boosting and ac-voltage gains to zero at high duty cycles, although ideally, it is supposed to obtain a quite large value. Moreover, it can be observed that the parasitic resistances significantly reduce the boosting factor than that of the ESRs. For these reasons, a very low impact of the parasitic resistances should be considered in the design to improve the boosting capability and inverter efficiency.

C. SMALL-SIGNAL AC-MODEL

The small-signal model can be obtained by linearizing all the variables in the state-space averaging model around the equilibrium (steady-state) point. This can be done by

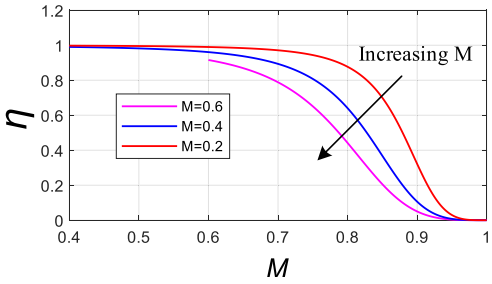


FIGURE 8. Nonideal dc-voltage boosting, and ac-voltage gain of the proposed CC-QBI.

assuming that any variable equals steady-state value plus a superimposed small, perturbed ac variable and neglecting the high-order nonlinear terms. Hence, the state equations of the small-signal ac model are

$$\begin{cases} \dot{\tilde{x}} = \bar{A}\tilde{x} + \bar{B}\tilde{u} + [(A_1 - A_2)\,X + (B_1 - B_2)\,U]\,\tilde{d} \\ \tilde{y} = \bar{C}\tilde{x} + \bar{D}\tilde{u} + [(C_1 - C_2)\,X + (D_1 - D_2)\,U]\,\tilde{d} \end{cases} \tag{25}$$

where $\tilde{x}$, $\tilde{u}$, $\tilde{d}$, and $\tilde{y}$ are the small-perturbed ac variations about the steady-state solution or the quiescent operating point defined by (20)-(24).

Therefore, the linearized ac small-signal state-space model of the proposed topology can be written as

$$\begin{cases} \dot{\tilde{x}} = \mathcal{A}\tilde{x} + \mathcal{B}\tilde{u} \\ \tilde{y} = \mathcal{C}\tilde{x} + \mathcal{D}\tilde{u} \end{cases} \tag{26}$$

where $u = \begin{bmatrix} e & i_{inv} & d \end{bmatrix}^T$

D. CC-QBI TRANSFER FUNCTION

This section uses the small-signal model of the CC-QBI derived in the previous section to obtain the system transfer functions. Using Laplace Transformation of (26) yields

$$\begin{cases} x(s) = [sI - \mathcal{A}]^{-1}\,\mathcal{B}u(s) \\ y(s) = \left(\mathcal{C}\,[sI - \mathcal{A}]^{-1}\,\mathcal{B} + D \right) u(s) \end{cases} \tag{27}$$

Consequently, it is possible to express the dc-link voltage of the CC-QBI, $v_{inv}(s) = y(s)$ as follows

$$v_{inv}(s) = G_{dv}(s)\,d(s) + G_{ev}(s)\,e(s) + G_{iv}(s)\,i_{inv}(s) \tag{28}$$

Moreover, the input current, i_1 can be expressed as

$$i_1(s) = \left(\acute{\mathcal{C}}\,[sI - A]^{-1}\,\mathcal{B} + \acute{\mathcal{D}} \right) u(s) \tag{29}$$

where $\acute{\mathcal{C}} = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix}$ and $\acute{\mathcal{D}} = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix}$.

This yields to

$$i_1(s) = G_{di}(s)\,d(s) + G_{ei}(s)\,e(s) + G_{ii}(s)\,i_{inv}(s) \tag{30}$$

where G_{dv}, G_{ev}, and G_{iv} are the duty, input voltage, and input current to dc-link voltage transfer functions. Also, G_{di}, G_{ei}, and G_{ii} are the transfer functions of duty, input voltage, and output dc-link current to the input current.

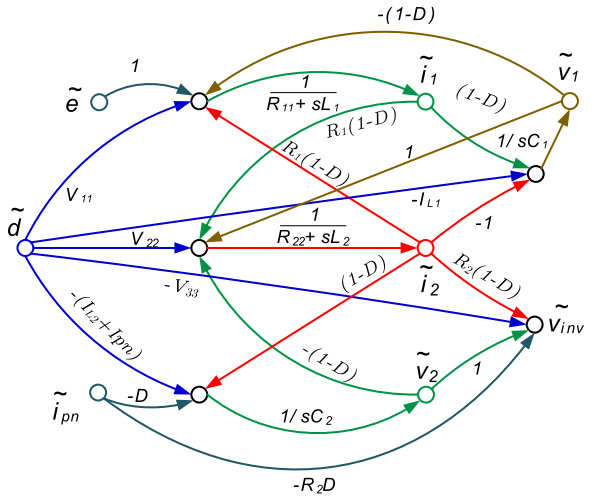


FIGURE 9. Signal flow graph of the CC-QBI.

From (28) and (30), the signal flow graph (SFG) of the proposed QBI can be obtained, as shown in Fig. 9, where

$$\begin{cases} V_{11} = R_1 I_1 - R_1 I_2 + V_1 \\ V_{22} = R_2 I_2 - R_1 I_1 + V_2 \\ V_{33} = R_2 I_2 + R_2 I_{pn} \\ R_{11} = r_1 + (1-D)\, R_1 \\ R_{11} = r_2 + (1-D)\, R_2 + R_1 \end{cases} \tag{31}$$

As observed from the SFG of Fig. 9, the sources of disturbances and variations in the proposed inverter are many. The following section desires to obtain the frequency domain analysis despite the disturbance of the duty cycle.

E. FREQUENCY DOMAIN ANALYSIS

The transfer functions of (24) and (26) describe how the disturbances in the input variables lead to disturbances in the output variables of the dc-side of the proposed topology. For the sake of illustration, if the proposed topology is used for grid-connected PV systems, the dc-link voltage, v_{inv} will be controlled via the inverter bridge and, the input voltage variation held to zero due to the MPPT regulator, then the perturbation of v_{inv} and e are neglected. This yields to

$$\begin{cases} i_{pn}(s) = -\dfrac{G_{dv}(s)}{G_{iv}(s)} d(s) \\ G(s) = \left.\dfrac{i_1(s)}{d(s)}\right|_{\substack{v_{inv}=0 \\ e=0}} = G_{di}(s) - \dfrac{G_{ii}(s)\, G_{dv}(s)}{G_{iv}(s)} \end{cases} \tag{32}$$

The transfer function G of (28) describes how the variation of the duty cycle input influence the input current of the inverter. It is worth noting that in the grid-connected PV systems, G is the key component of the control system and has a significant effect on the grid-tie inverter performance.

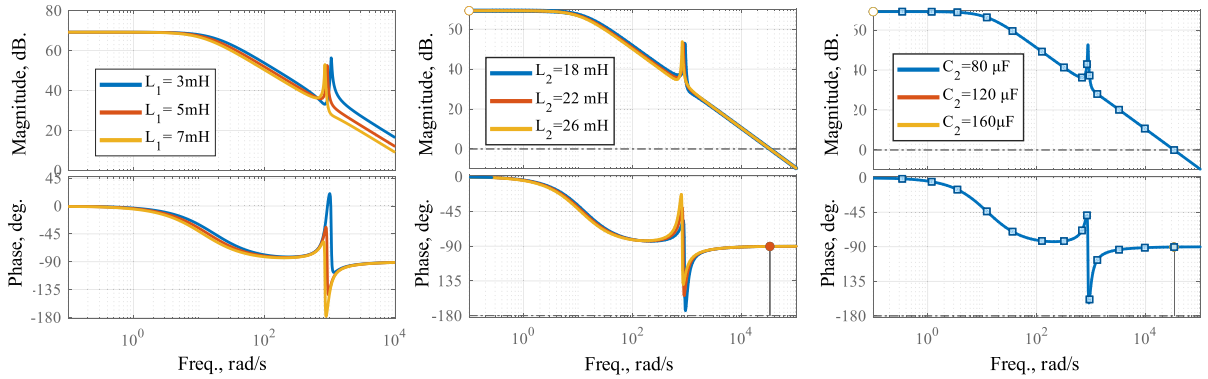
The Bode plot of Fig. 10 and the time responses of Fig. 11 for the transfer function in (32) are used to optimize the design parameters. Fig. 10(a) shows the Bode diagram under changing of L_1 and L_2 for specific parameters and steady-state operating conditions indicated in Table 2. It can be observed that as L_1 decreases, the cutoff frequency and hence the bandwidth increases, which results in a faster response, as indicated in Fig. 11(a), which shows the time response for a step-change in the duty cycle. However, a lower L_1 results in higher input current ripples. Therefore, a comprise between dynamic response and current ripples should be achieved. On the other hand, variation of L_2 has a slight effect on the dynamic response (as L_2 decrease the response goes slightly faster) as shown in Fig. 10(b) and Fig. 11(b), while the variation C_2 do not affect the response speed. However, a higher value of C_2 results in a lower ripple in the dc-link voltage. Also, variation of C_1 do not affect the speed of response.

$$\mathcal{A} = \begin{bmatrix} -\dfrac{1}{L_1}[r_1 + (1-D)R_1] & R_1\dfrac{1-D}{L1} & -\dfrac{1-D}{L1} & 0 \\ R_1\dfrac{1-D}{L_2} & -\dfrac{1}{L_2}[R_1 + r_2 + (1-D)r_2] & \dfrac{1}{L_2} & -\dfrac{1-D}{L_2} \\ \dfrac{(1-D)}{C_1} & -\dfrac{1}{C_1} & 0 & 0 \\ 0 & \dfrac{1-D}{C_2} & 0 & 0 \end{bmatrix}$$

$$\mathcal{B} = \begin{bmatrix} \dfrac{1}{L_1} & 0 & \dfrac{1}{L_1}[R_1.I_{L1} - R_1.I_{L2} + V_{C1}] \\ 0 & 0 & \dfrac{1}{L_2}[-R_1 I_{L1} + R_2.I_{L2} + V_{C2}] \\ 0 & 0 & -\dfrac{I_{L1}}{C_1} \\ 0 & -\dfrac{D}{C_2} & -\dfrac{I_2}{C_2} - \dfrac{I_{INV}}{C_2} \end{bmatrix}$$

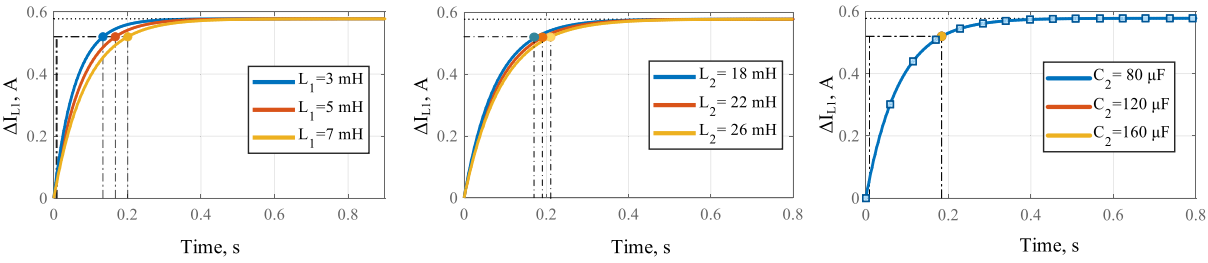
$$\mathcal{C} = \begin{bmatrix} 0 & R_{C2}(1-d) & 0 & 1 \end{bmatrix}$$

$$\mathcal{D} = \begin{bmatrix} 0 & -R_2 d & -R_2 I_{L2} - R_2 I_{INV} \end{bmatrix}$$



(a) different values of L_1. (b) different values of L_2. (c) different values of C_2.

FIGURE 10. Bode plots foR $G(s)$.



(a) different values of L_1. (b) different values of L_2. (c) different values of C_2.

FIGURE 11. Time response of the source current due to a small step increase of the duty cycle ($\Delta d = 0.0002$).

IV. COMPARATIVE ASSESSMENT

This section introduces a detailed comparative assessment between the presented single-stage inverter topologies, including qZSI, SSI, and proposed QBI. This assessment covers the following aspects: modulations complexity, steady-state analysis, current and voltage stresses, and the passive components requirements. The losses and inverter efficiency are explored in the simulation study using PLECS.

Table 3 summarizes the comparison results between the analyzed topologies regarding the duty cycles, boosting factors, voltage stresses on capacitors and semiconductors, and the ac-voltage gain of different topologies. Moreover, Figs. 12-14 give better representations of the boosting and performance characteristics of these topologies.

Note that all topologies are controlled by the MSVM technique, presented in [34] for qZSI and in [20] for SSI topology to obtain a fair comparative study.

A. IMPLEMENTATIONS

The implementation procedure of power converters' modulation techniques represents an important issue that should be considered in comparing the different topologies.

The modulation technique complexity can be determined based on different factors such as the number of duty cycles and the possibility of utilizing the enhanced PWM (ePWM) modules of modern DSPs in the implementation. Table 2 compares the analyzed topologies regarding the required number of duty cycles and the complexity of utilizing the ePWM modules used in the implementation aspects. The modulation of basic SSI and proposed QBI is more straightforward than that of qZSI, which requires more duty cycles in addition to the high specifications of DSP controllers due to its complexity.

B. VOLTAGE GAINS AND BOOSTING ABILITY

Table 3 lists more evident steady-state comparisons among the analyzed topologies in terms. To be fair, these relations are plotted for the same gain range. Considering limitations due to parasitic elements, the voltage gain range is chosen as $G \leq 5$. The relations between the boosting factor, charging duty cycles, and the voltage gains for the analyzed topologies are shown in Fig. 12, and the following conclusions can be made:

1) The boosting action of qZSI is valid for $D_{ch} < 1/2$, while in SSI and QBI, D_{ch} has a broader range with $D_{ch} < 1$.
2) The SSI and proposed QBI topologies have more voltage gain capability compared to qZSI.
3) The boosting ability of the QBI is significantly higher than that of the basic SSI for the exact charging duty cycle. This is owed to the squaring feature of the dc-boost factor.
4) SSI has the lowest boosting factor compared with the other topologies for the same voltage gains. Thus, SSI

TABLE 3. Comparisons of the proposed QBI with For qZSI and SSI.

Topology		qZSI (*) [34]	SSI (‡) [20]	CC-QBI (‡)	DC-QBI (‡)
Number of duty cycles		5	3	3	3
Utilizing ePWM		Complex	Simple	Simple	Simple
Charging duty cycle, D_{ch}		$1-M$	M	M	M
Number of inductors		2	1	2	2
Number of capacitors		2	1	2	2
Boosting factor, B		$\frac{1}{1-2D_{ch}}$	$\frac{1}{1-D_{ch}}$	$\frac{1}{(1-D_{ch})^2}$	
dc-voltage, V_{dc}		Pulsed	Continuous		
Voltage gain, G		$\frac{M}{\sqrt{3}(2M-1)}$	$\frac{M}{\sqrt{3}(1-M)}$	$\frac{M}{\sqrt{3}(1-M)^2}$	
Capacitor voltage	$\frac{V_{C_1}}{E}$	$\frac{1-D_{ch}}{1-2D_{ch}}$	-	$\frac{1}{1-D_{ch}}$	$\frac{D_{ch}}{1-D_{ch}}$
	$\frac{V_{C_2}}{E}$	$\frac{D_{ch}}{1-2D_{ch}}$	$\frac{1}{1-D_{ch}}$	$\frac{1}{(1-D_{ch})^2}$	$\frac{1}{(1-D_{ch})^2}$
Efficiency (‡)		89%	93%	91%	91%

(*) qZSI, in this study, is controlled using the MSVM scheme given in [34].
(‡) SSI and QBI are controlled using the MSVM scheme given in [20].
(‡) Efficiency is determined by PLECS for 1kVA, and voltage gains.

will produce lower voltage stresses on the B6 semiconductors. However, qZSI produces a higher boosting factor for $G > 2$. Therefore, it has higher voltage ratings than B6 devices.

5) Low modulation indexes are required to obtain high voltage gains in the qZSI. Hence, the distorted output voltage is expected in the qZSI than the other topologies.

C. CAPACITOR VOLTAGES AND INDUCTOR CURRENT RIPPLES

The voltage stress and input current ripples are essential factors that should be carefully considered in any converter design. It determines the cost, weight, and volume of the converter. Table 3 lists the capacitor voltages of the analyzed topologies. Besides, Figs. 13(a) and 13(b) sketch the variations of these voltages versus gain, G.

1) CAPACITOR VOLTAGES

Regarding the voltage stress on the capacitor C_1. It can be seen from Fig. 13(a) that, qZSI has the highest voltage stress. Meanwhile, the CC-QBI topology has slightly higher voltage stress on the capacitor C_1. However, the DC-QBI introduces much lower voltage stress on C_1. From Fig. 13(b), qZSI has the minimum voltage stress on the capacitor C_2.

2) INPUT CURRENT RIPPLES

As far as the input current ripples of the analyzed topologies are concerned, the instantaneous current ripples ΔI_i in each topology is investigated. The focus will be on the same input and output conditions. By applying Kirchhoff's voltage law for the equivalent circuits of the analyzed topologies in the inductive charging modes and after some derivation's steps, the normalized input current ripples, r_i can be given by

$$r_i = \frac{\Delta I_i}{k} = \begin{cases} D_S, & \Rightarrow \text{SSI} \\ D_q\left(1-D_q\right)/\left(1-2D_q\right), & \Rightarrow \text{qZSI} \\ D_{QB}, & \Rightarrow \text{CC-QBI} \end{cases} \quad (33)$$

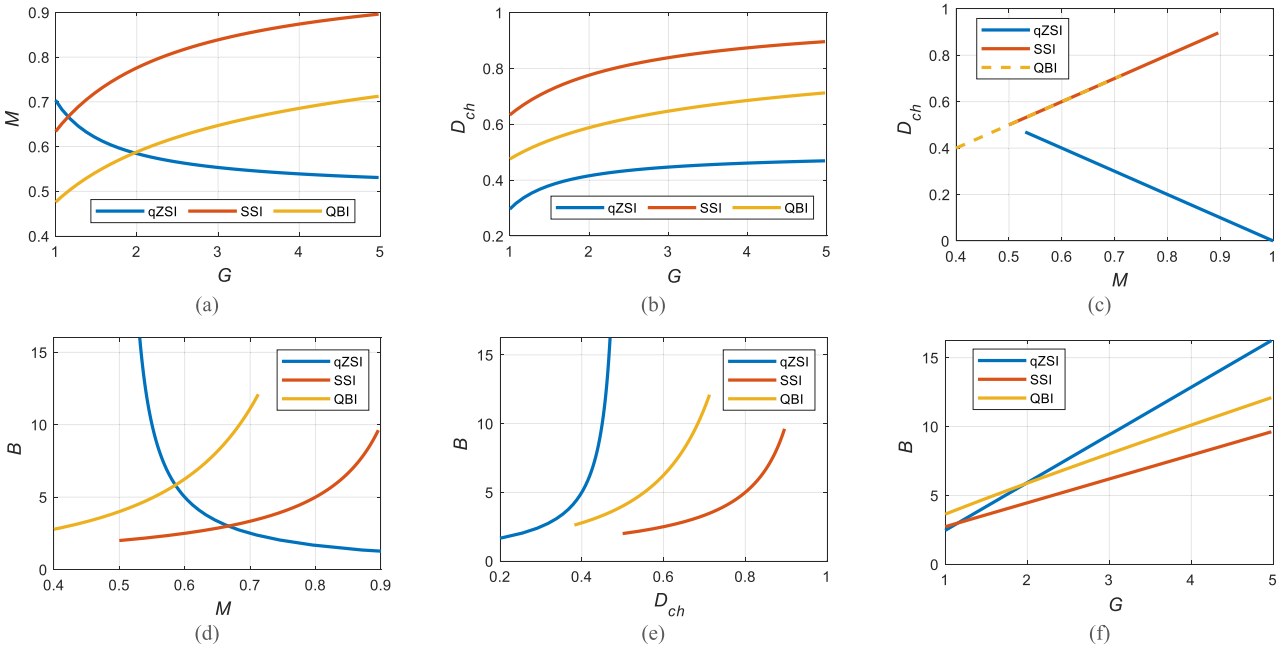


FIGURE 12. Voltage gain and the boosting ability of the analyzed topology.

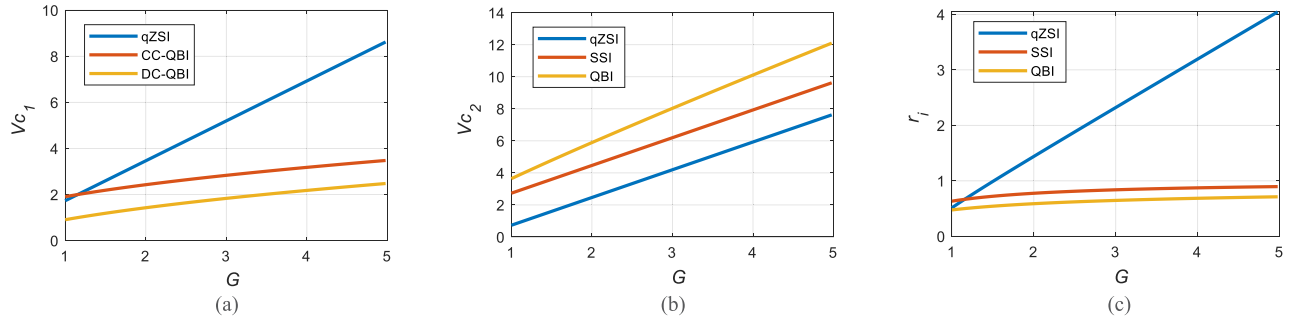


FIGURE 13. Capacitor voltages and input current ripples of the analyzed topologies.

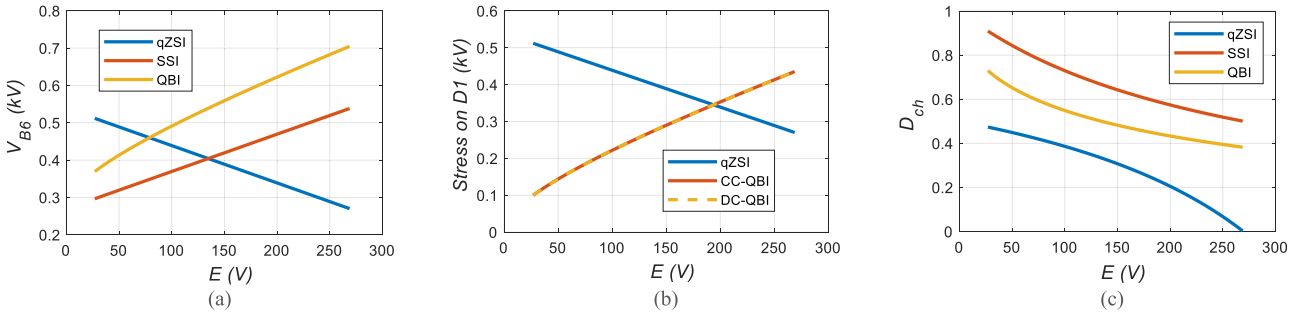


FIGURE 14. Semiconductor stresses analysis of the analyzed topologies versus E for a constant output voltage of 110V/phase.

where k is a constant ($k = ET_s/L_1$) and D_q, D_S and D_{QB} are charging duty cycles of the qZSI, SSI, and QBI, respectively.

Fig. 13(c) shows input current ripples dependency, r_i of the analyzed topologies versus the output gain. It can be observed that the proposed QBI has lower input current ripple than the other topologies, while the ripple of qZSI is high.

D. REQUIRED INDUCTANCES

Applying the volt-second balanced concept on the QBI dc-side with the MSVM scheme, it can be found that the input inductance, L_1 for CC-QBI can be determined from

$$L_1 = EM_{QB}/\left(f_s \cdot \Delta I_1\right) \tag{34}$$

where I_1 is the current in the inductor L_1, f_s is the effective switching frequency, which equals the carrier frequency in the MSVM scheme, and ΔI_1 is the input current variation. The relation between currents flowing in the two inductors (I_1 and I_2) at the dc-side of QBI is governed by

$$I_1 = I_2/\left(1 - M_{QB}\right) \tag{35}$$

Thus, to obtain the same current ripple of the two inductors, the required inductance L_2 should be evaluated from

$$L_2 = L_1/\left(1 - M_{QB}\right) \tag{36}$$

On the other hand, the inductances of the SSI and qZSI topologies can be determined from [20], [34]

$$\begin{cases} L = \dfrac{E}{f_s \cdot \Delta I_1} M_S, & \text{for SSI} \\ L = \dfrac{E}{f_s \cdot \Delta I_1} \dfrac{M_q\left(1 - M_q\right)}{2M_q - 1}, & \text{for qZSI} \end{cases} \tag{37}$$

For a fair comparison between the analyzed topologies, the modulation indexes (M_q, M_S, and M_{QB}) should be determined for the same output voltage gain. Based on (33)-(36), to obtain the same current ripples in the analyzed topologies, the qZSI requires larger inductance than SSI and the proposed QBI, which requires the lower one.

E. INVERTER VOLTAGE STRESSES

1) VOLTAGE STRESS

Considering the circuits of the analyzed topologies, it can be found that the voltage stress on all switches of the inverter bridges is equal to the peak dc-link voltage or the voltage across the capacitor C_2, $\hat{v}_{C2}$. Therefore, for the same gain, the switch voltage stress, v_{B6} normalized to the input voltage of the analyzed topologies can be determined from

$$\frac{v_{B6}}{E} = \begin{cases} \left(2\sqrt{3}\,G - 1\right), & \Rightarrow \text{qZSI} \\ \left(\sqrt{3}\,G + 1\right), & \Rightarrow \text{SSI} \\ \dfrac{6G^2}{1 + 2\sqrt{3}\,G + \sqrt{1 + 4\sqrt{3}\,G}}, & \Rightarrow \text{QBI} \end{cases} \tag{38}$$

Fig. 12(f) shows the dependency of the boosting factor, B, versus output gain, G, whereas Fig. 14 shows the variation of common semiconductor voltage stresses, with E for a constant output voltage of 110Vrms/phase.

From these results, it can be observed that

1) The SSI has the minimum voltage stress on B6 and the front-end diode when a high voltage gain is required.
2) The qZSI has the minimum voltage stress on B6 and the front-end diode for the high input voltage region, which requires low gains to obtain the same output voltage.

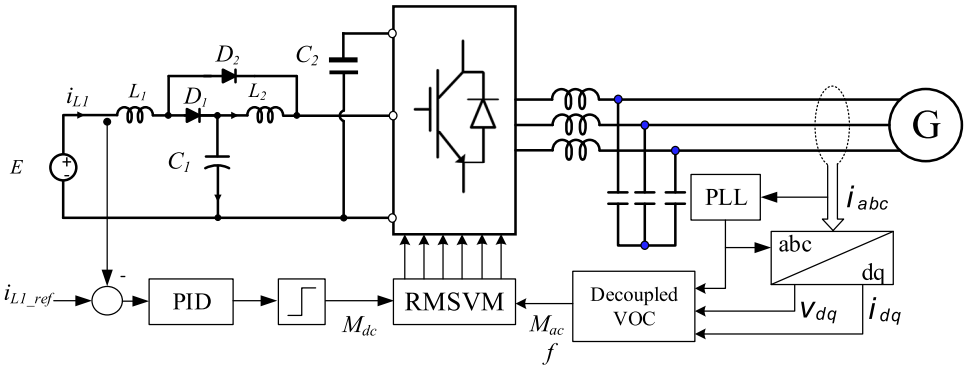


FIGURE 15. Closed-loop control of the proposed QBI.

TABLE 4. Measurements of the analyzed topologies for the case study.

Topology			qZSI	SSI	QBI
DC-Link Voltage			492V	319.5V	413.2V
Input Current			20A	20A	20A
Input Current ripples			5.6A	2A	1.48A
Output Voltage THD			114.4%	71.3%	97.99%
Average dc-Link voltage			269.6V	319.5V	413.2V
Capacitor Voltage, C_1			219.8V	-	143.7V
B6 Current stress	Max.	Upper	44A	7A	8A
		Lower	40A	25A	33A
	Average	Upper	6.7A	1.3A	0.9A
		Lower		6.8A	6.3A
	RMS	Upper	15A	2.2A	1.8A
		Lower		12.5	14A

3) Meanwhile, the SSI employs slightly higher voltage stress, especially for high input voltage regions.

2) CURRENT STRESS

In practice, the presented topologies' current stresses are different under different modulation schemes and load conditions. For comparisons, evaluating the current stress on the inverter bridge's switching devices will be presented in the simulation study.

F. DISCUSSION

Based on the preceding theoretical analyses, a study of four different topologies of quadratic boost split-source inverters is introduced, displaying the main characteristics. Based on the comparative study given in this paper, it can be concluded that among these topologies, the CC-QBI has superior characteristics. It has a good performance compared with the other QBI topologies, SSI and qZSI when operating with a low input voltage. This means that the proposed topology is suitable for PV, FC, and Electric Vehicle (EV) applications.

V. CLOSED-LOOP CONTROL OF QBI TOPOLOGY

The block diagram of the closed-loop control of the QBI for the grid-connected system is shown in Fig. 15. In this technique, the regulated MSVM presented in section II is used. The dc-link voltage is controlled via decoupled voltage-oriented control (VOC) through output current controllers and the dc-link voltage controller with the modulation index of the standard VSI as the manipulating variable. The input current, i_{L1} is adopted by controlling M_{dc} value as shown in Fig. 15. It should be noticed that the input current can be controlled to control the power required to supply the load in case of a constant voltage source or can be used to track the maximum available power in case of a PV source.

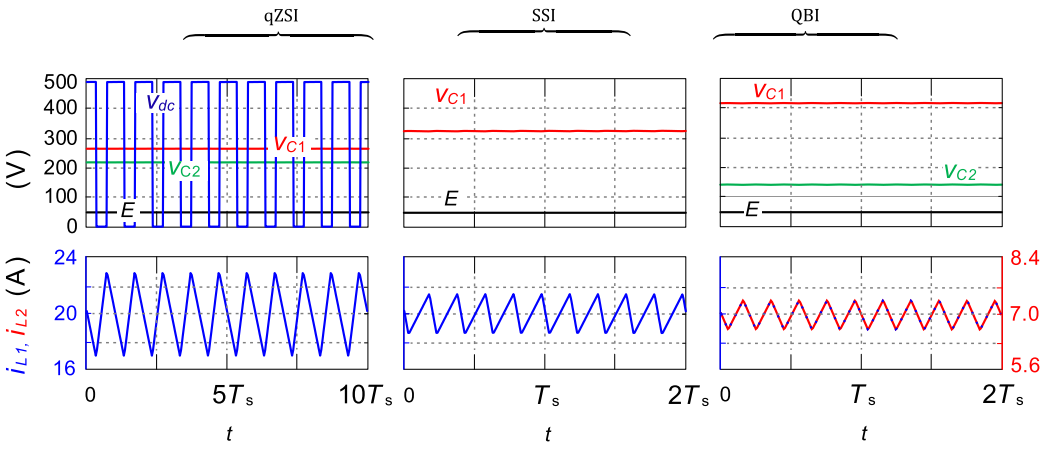
VI. SIMULATION RESULTS

A. CASE-I: STEADY-STATE ANALYSIS

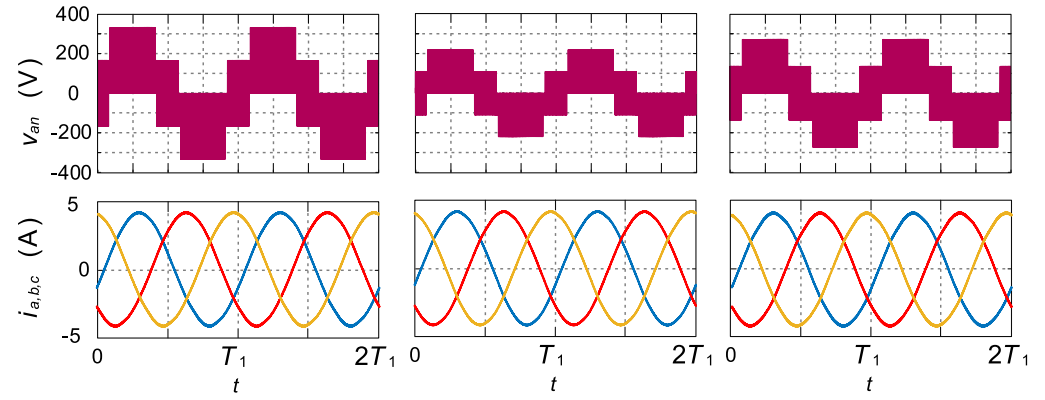
Three-phase qZSI, SSI, and CC-QBI topologies using MSVM techniques are modeled via MATLAB and PLECS platforms to investigate their functionality and verify the comparative study analysis. A dc-supply of 50V is used in all topologies, while three-phase loads of 1kVA, 50Hz, 0.95 lagging power factor at 110V/phase are connected at the output. Figs. 16-18 and Table 4 show the simulation results.

The modulation indices in the qZSI, SSI, and CC-QBI topologies are set at 0.5511, 0.8435, and 0.6521, respectively, to generate the same output phase voltages of 110V from the 50V dc-supply. The same inductance and capacitances of 1.25mH and 120μF, respectively, are used in all topologies to show these effects on the input current and dc-voltage ripples. Table 4 shows the measured voltage and current from the presented topologies' simulation models, where Fig. 16 shows the obtained results, which compares the proposed QBI with that of basic SSI and qZSI. Fig. 16(a) illustrates the voltage and current waveforms of the dc-side of the analyzed inverters, while Fig. 16(b) shows the output voltage, current waveforms, and the FFT analysis of the voltage. The current stress on the upper and lower switch in one leg of the analyzed topologies is shown in Fig. 16(c) at the same operating conditions. From these results, it can be observed that,

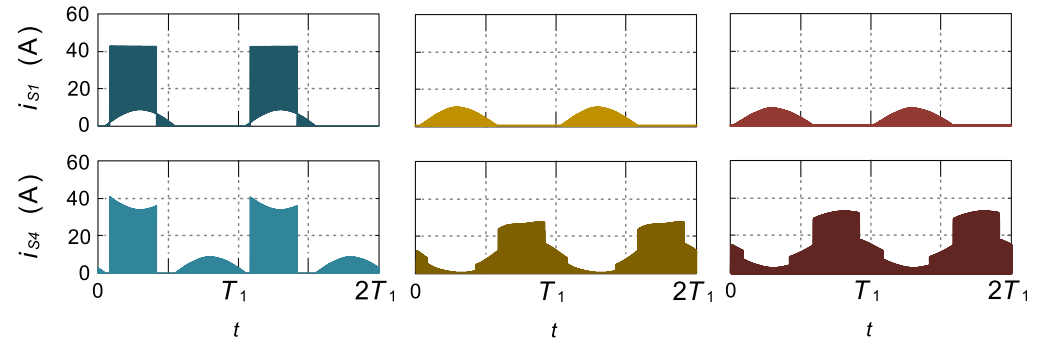
1) The measured values of Table 4 show a good agreement with that estimated from the analysis.
2) In all topologies, the output phase currents, as well as the average values of input current are very close. Moreover, the load currents exhibit near sinusoidal waveforms.



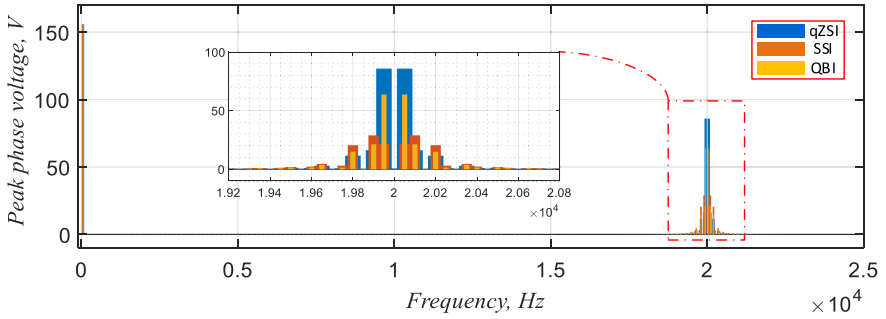
(a) dc-side waveforms.



(b) output-side voltage and current waveforms.



(c) the current stresses of the switching transistors of B6.



(d) output- voltage FFT analysis.

FIGURE 16. Simulation results of the one kVA qZSI, SSI, and QBI using the modified SVPWM techniques.

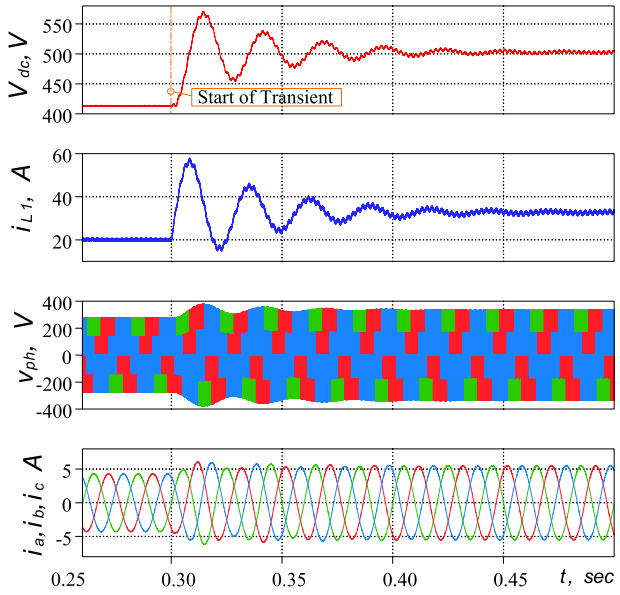


FIGURE 17. Simulation results of a step change of the output voltage.

3) The proposed QBI has a lower input current ripple than the other topologies, as shown in Fig. 16(a). Its current ripple is reduced by about 74% and 26% compared with qZSI and SSI values, respectively.
4) The dc-link voltage of the qZSI is pulsed with the highest value of 492V compared with the other topology. This leads to higher voltage stresses on the inverter bridge.
5) The same output voltage magnitude with a peak of $110\sqrt{2}$2V is obtained, as shown in the FFT analysis of Fig. 16(b). Moreover, the output voltage of the proposed QBI has a lower THD than qZSI, while the SSI has the least THD value. This is owed to using different modulation indexes to give the same output voltage in all topologies.
6) From the viewpoint of active switch current stress in the analyzed topology, the switch currents are determined by the output current, average input current, the peak-to-peak inductor current ripple, and the inductive charging and discharging methods. Since the same input and output conditions are considered in this study, the switch currents are significantly affected by the method of charging and discharging, as shown in Fig. 16(c). Due to the utilization of both switches in the inverter leg for ST state in the qZSI, the switch current is increased simultaneously. Hence, it is worth comparing the current stress of qZSI topology with that of the SSI and proposed QBI.

With the selected case study, Fig. 17 shows the simulation results of dc-link voltage, input current and output phase voltage, and currents of the QBI around the instant of step transition of the modulation index, which affect the output voltage. In $t = 0.3$ sec., the modulation index is increased by 5% from its initial value (i.e., it changed from 0.652 to 0.684). The captured waveform clearly illustrates the smooth dynamic transition between the two cases as can be theoretically predicted. Some overshoot with low-frequency transient is observed and it will be damped via the closed-loop operation.

TABLE 5. Parameters for power loss calculation.

Parameters	Values	Parameters	Values
MOSFETs	IPW60R280P6	ESR at 650V	50e-3
Diodes	IDW75E60	Output Voltage	220Vrms
Parasitic Resistances	0.12	Input Voltage	100V

Moreover, the inverter losses including switching and condition losses of the analyzed topologies are studied using PLECS and the results are shown in Fig. 18. Since the semiconductor loss analysis depends on the characteristics of the employed devices, Table 5 lists the parameters of the utilized modules in the PLECS thermal analysis. The used modules are the Infineon-MOSFET of IPW60R280P6 and the fast-switching diode of IDW75E60. Only the copper loss in the inductors is considered and determined based on the RMS current through the inductor as

$$\begin{cases} P_{cu} = r_L \cdot I_{L,rms}^2 \\ P_{cu} = R_C \cdot I_{C,rms}^2 \end{cases} \tag{39}$$

where r_L and R_C are the inductor's and ESR resistances, and I_L and I_C are the RMS inductor and capacitor currents, which are determined using PLECS.

Fig. 18 shows the losses distribution of 1kVA QBI. It can be observed that the switching and conduction losses in the B6 switches are significant. This is owed to the utilization of the inverter switches in the inductive charging and discharging processes. Also, Fig. 19 compares the efficiency of the proposed QBI and the qZSI considering the same operating conditions and losses in passive elements. It can be found that the proposed QBI has a larger efficiency profile than the qZSI.

It is important to note that the simulation results validate and verify the functionality and detailed comparative analysis and discussions of the presented inverters.

B. CASE-II: CLOSED-LOOP ANALYSIS

In this case study, the parameters of the grid-connected QBI system are summarized in Table 6. Fig. 20 shows the voltage and current responses of the system for a step decrease in the input current. It can be observed from Fig. 20 that, when the input current is reduced at the time 0.3 sec, the dc-link voltage decreases until the dc-link voltage controller acts to restore its value to the reference value by decreasing the d-axis current, and hence the line currents decrease.

Finally, the results of both case studies for steady-state and transient response in the closed-loop operation confirm the viability of the proposed QBI topology with the modulation and control scheme.

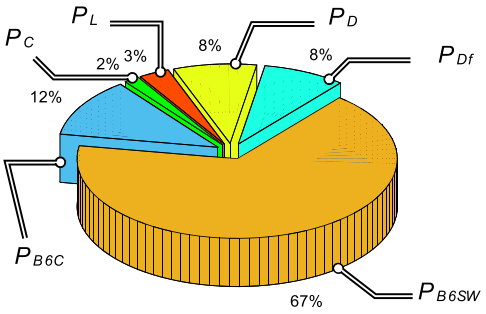


FIGURE 18. Simulated losses distribution in the 1 kVA three-phase QBI for B6 switches, input, and forward diodes, and passive components at full-load using PLECS. P_C: Power Loss in ESR of the capacitors, P_L: Power Loss in the inductors parasitic resistances, P_D: Loss in the diodes 1,2,3, P_{Df}: Loss in the forward diodes, P_{B6sw} and P_{B6C} are the switching and condition losses in the B6 switches.

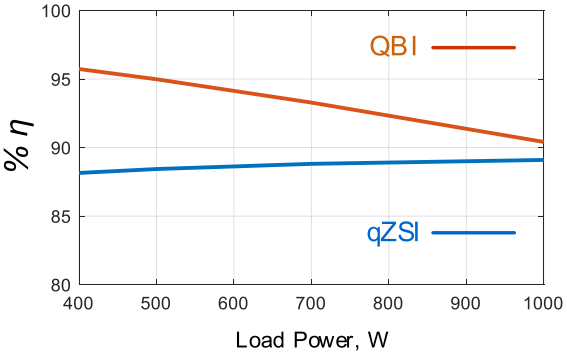


FIGURE 19. Simulated efficiency of 1kVA QBI and qZSI.

TABLE 6. Parameters for closed-loop case study.

Parameters	Values	Parameters	Values
Filter inductance	7mH	Filter resistance	2 Ω
Ref. input current	10A	Ref. dc-link voltage	950V
Parasitic Resistances	0.12	Input Voltage	100V

VII. EXPERIMENTAL RESULTS

This section describes the experimental work and measurements taken on a downscaled QBI prototype, which is based on a custom-designed and configurable power electronics development kit from PEModule® [35]. The photograph of the experimental setup is shown in Fig. 21. The dc-side's passive elements are selected as in the simulation study, while the inverter output terminals are connected to a star-connected inductive load. The main system parameters are listed as follows:

1) The dc-side passive elements: $L_1 = L_2 = 1.25$mH, $C_1 = C_2 = 120\mu F$.
2) The three-phase load: $R = 10\Omega$, $L = 5$mH.
3) The supply voltage: 15V.
4) Output voltage: 45V/Line at 50Hz.
5) Switching frequency: 10kHz.

The low-cost LAUNCHXL-F28379D development kit is used to implement the modulation strategy of the QBI to obtain an output line voltage of 45V at 50Hz. A deadtime of 5usec is inserted between the gating pulses. The experimental results

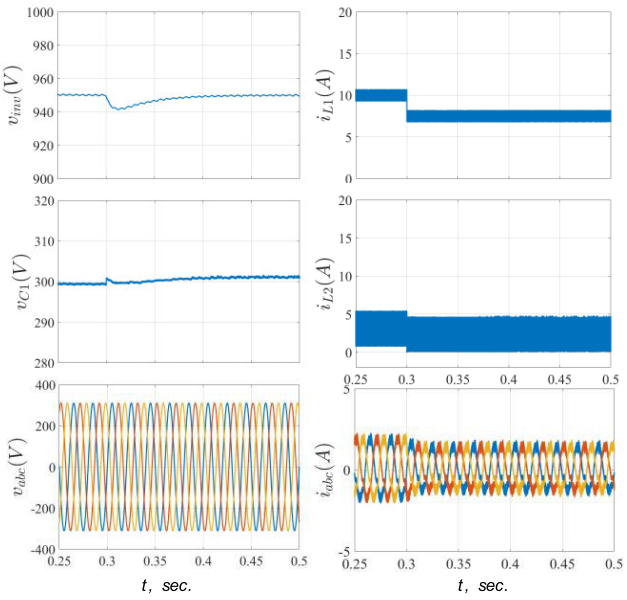


FIGURE 20. Simulated results for the closed-loop operation, the input current is reduced from 10A to 7.5A at 0.3 sec.

are captured by the DPO2024 Tektronics Oscilloscope, while the current sensors are used to measure the input, and output currents as well as the device's current stresses. The experimental results are shown in Figs. 22-28.

Fig. 22 shows the output voltage and current waveforms for the case study. The output current is near the sinusoidal waveform with low distortion, and the waveforms sound close to the theoretical.

The inductor currents, i_{L1}, i_{L2} and the load current waveforms are experimentally measured, and the results are shown in Fig. 23. As can be observed the current of the inductor L_1 is larger than the inductor L_2, while both waveforms shed light on low-frequency components. This is owed to utilizing the MSVM schemes. Moreover, the zooming of the inductor currents is shown in Fig. 23, which illustrates the charging and discharging operations.

To confirm the theoretical study about the current stresses on the inverter devices, Figs. 24-26 show the current of inverter upper and lower switches as well as on the forward diodes.

It can be noticed from the results of Figs. 24-26 that; the experimental results confirm the theoretical study about the current stresses on the semiconductor devices. The lower switches and the forward diodes of the proposed topology suffer from higher current stresses than the upper switches of the inverter bridge. It is worth noting that in Figs. 24-26, the input current is displayed to show the current stresses during the charging and discharging intervals in the zooming figures.

To confirm the feasibility of using the proposed topology with the motor drive systems, Fig. 27 shows the experimental results of the output voltage, and current as well as the inductor currents for a step-change in the output frequency and output voltage. The frequency is changed in Fig. 27 from

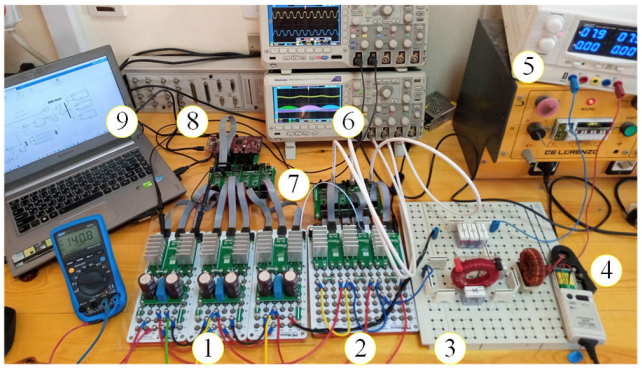


FIGURE 21. Experimental Setup Photograph. ① Three-Phase Inverter bridge with Current Sensors, ② Forward diodes with Current sensors, ③ Impedance network, ④ Current probe, ⑤ Power supply, ⑥ Oscilloscope, ⑦ Current measurement boards, ⑧ LAUNCHXL-F28379D kit, ⑨ Laptop.

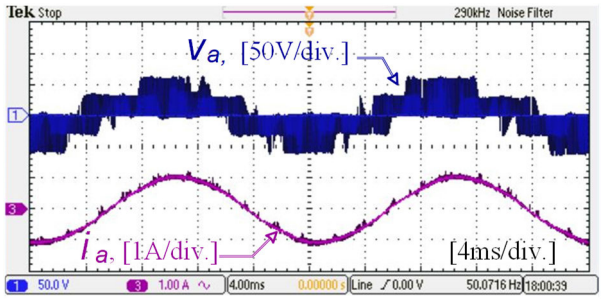


FIGURE 22. Experimental results for output phase voltage (upper trace, 50V/div.), current (lower trace, 2A/div).

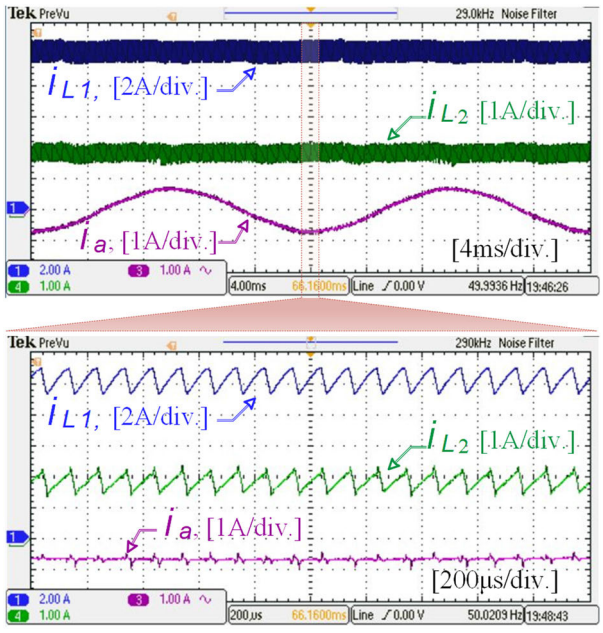


FIGURE 23. Experimental results for the inductor currents and output phase current waveforms.

50Hz to 25Hz. As can be observed from the results, a smooth dynamic transition is achieved.

The capacitors voltages, v_{dc} and v_{c1} are experimentally measured and the results are shown in Fig. 28. The proposed QBI boosts the input voltage from 15V to 95V at the dc-link

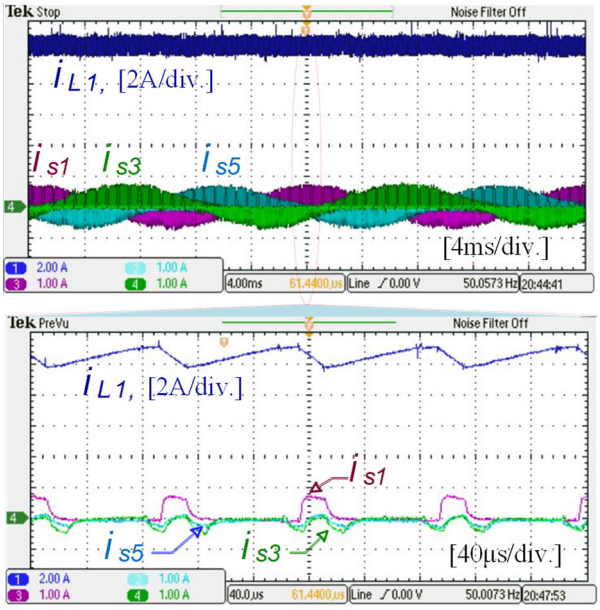


FIGURE 24. Experimental results for the current stresses of the upper switches.

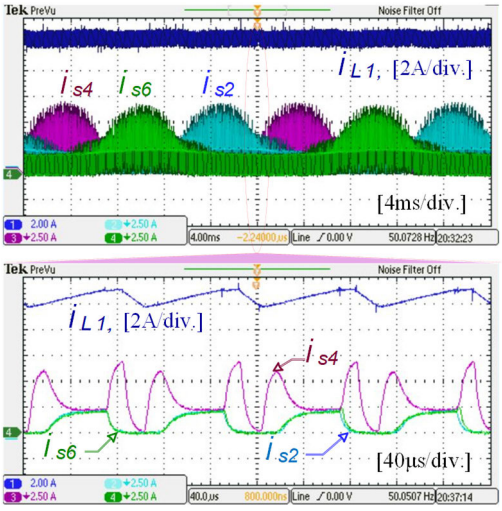


FIGURE 25. Experimental results for the current stresses of the lower switches.

TABLE 7. Measured booting factor from the experimental results.

M	0.2	0.4	0.6	0.8	0.9
B	1.51	2.64	4.72	5.6	2.28

(capacitor C_2) while the average voltage across the capacitor C_1 is lower with a value of 25V. It can be observed from Fig. 28 that, the trend of the capacitor voltage v_{c1} is opposite to that of the inductor current. This confirms the charging and discharging mode of operation of the proposed topology.

Table 7 lists the boosting factor of the experimental study versus the modulation index of the inverter under the same operating conditions. Fig. 29 shows a comparison between the experimental results and the results of the analytical study of the boosting factor of the QBI for ideal and non-ideal

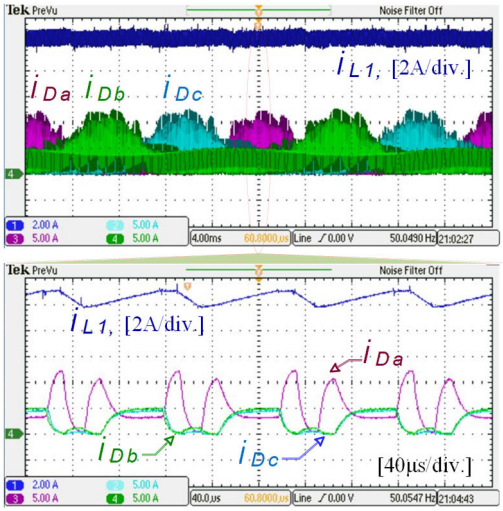


FIGURE 26. Experimental results for the current stresses of the forward diodes.

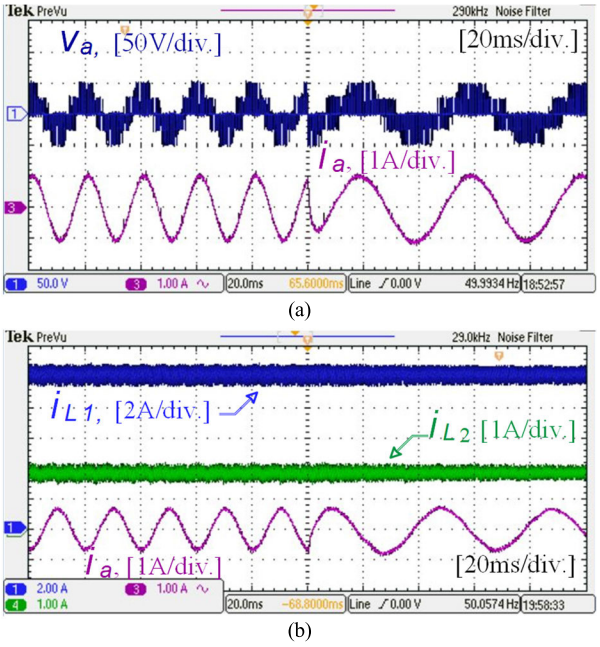


FIGURE 27. Experimental results of a step change of the output frequency from 50Hz to 25Hz.

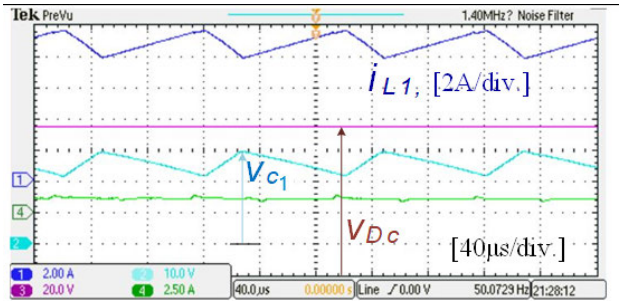


FIGURE 28. Experimental results of the capacitor voltage and input current of the proposed topology.

cases. it can be observed that a good agreement between the experimental and the analytical study is achieved.

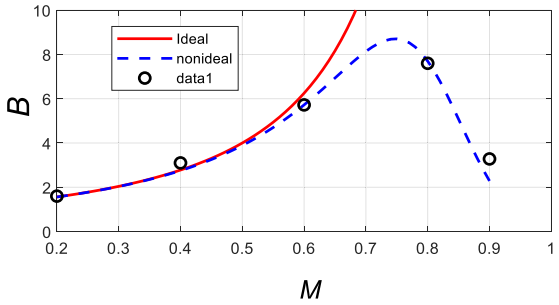


FIGURE 29. Boosting factor versus the modulation index for both experimental and analytical study at the same operating conditions.

Finally, it can be mentioned that the presented theory, concepts, and analysis of the proposed QBI with the presented modulation scheme are confirmed using the simulation results given and the experimental work in this section.

VIII. CONCLUSION

In this paper, four modified Split Source Inverter (SSI) topologies with high voltage gains are proposed. These topologies square the boosting ability of the basic SSI. Therefore, it is called Quadratic-Boost Inverters (QBIs) in this paper. In all topologies, the dc-boosting factor and the ac-voltage gain are increased significantly by utilizing auxiliary inductors, capacitors, and diodes. In this paper, the modified SVM approach is selected to reduce the dc-side ripples. The steady-state and small-signal models of the analyzed topologies are introduced. Moreover, a closed-loop controller design guideline is presented. In addition, a comprehensive analysis and comparisons study with the conventional single-stage boosting inverter topologies such as SSI and qZSI are presented to bring out the merits of the proposed topologies. This analysis includes the boosting factor, output voltage gain, voltage, and current stresses on the semiconductors and passive components. Finally, the effectiveness of the proposed QBI architecture is verified via simulation and experimental results. According to this paper, it can be concluded that the proposed topologies are more suitable than the other counterparts (basic SSI and qZSI) for renewable energy applications and could be widely used for the PV and FC applications where high voltage gain is required from a low input voltage.

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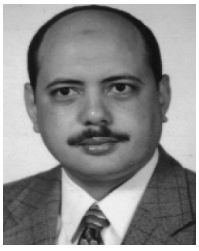

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