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ORIGINAL RESEARCH PAPER

A modular multilevel DC-DC converter with self-energy equalization for DC grids

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Abstract

Medium-/High Voltage DC grids are interesting for the integration of renewable energy sources. DC-DC conversion systems are highly needed for the development of DC grids. Recently, Modular Multilevel Converter (MMC) is the most promising technology for medium-/high-voltage applications, but employing the conventional MMC with DC output voltage leads to diversion in the Submodule (SM) capacitor voltages, that is energy drift. This paper proposes a modified modular multilevel DC-DC converter with self-energy equalization, which ensures successful DC-DC conversion with balanced capacitors voltages. In the modified topology, clamping Insulated Gate Bipolar Transistors (IGBTs) are employed in each arm to enable parallel-connection of the capacitors in the same arm. During the operation (equalization period), the parallel-connected upper capacitors are connected to the parallel-connected lower capacitors in each leg through a small limiting inductor to transfer energy between the arms to ensure balanced capacitor voltages. The proposed configuration, along with the operational concepts, mathematical analysis, and design, are presented. Finally, simulation and experimental results are presented for validation.

1 | INTRODUCTION

The high-voltage high-power DC-DC converter is a main component in the medium-/high-voltage DC grids [1]. The DC-DC converter can be used as a DC collector converter or an offshore converter in the DC collection scheme of offshore windfarm as shown in Figure 1(a) [2], or generally to interconnect between two voltage levels in the DC grids as shown in Figure 1(b).

Recently, the Modular Multilevel Converter (MMC) is the most commonly-promoted architecture in DC-DC connections due to its modularity, scalability, redundancy, and hot-swapping ability [3–8]. The modular design of the converter is achieved using series-connected Sub-Modules (SMs) in each arm. The series-connected SMs have the capability of generating voltage, where each SM contributes with a small voltage compared to the highest arm voltage, that is smoothed voltage waveforms can be generated successfully.

In [9], a review for different types of front-to-front dual active bridge (DAB)-based modular DC-DC converters were presented and discussed. The DAB-based modular DC-DC converter uses intermediate medium-/high-frequency ac link for the power transfer between the two involved sides via controlling the phase shift difference between the generated AC voltages at both sides [9].

Different techniques have been presented in literature to ensure balanced capacitor voltages during DC-DC operation of modular multilevel converters, such as AC circulating current injection [10]. Although AC circulating current injection can be employed to avoid arms' energy drift, it affects the converter efficiency negatively, that is the AC circulating current should be minimized to improve converter efficiency [10]. In [11], a modular DC-DC converter based on the boost converter circuit was presented, where boost converter valves have been implemented via several series-connected half-Bridge (HB) SMs. In this circuit structure, the SM capacitances are appropriately selected to ensure resonant condition, which leads to high AC current in the SMs.

In [12] and [13], cross-connected capacitances and cross-connected arms DC-DC converters were suggested, respectively, where AC voltage injection is used in both structures to ensure balanced capacitors voltages during the DC-DC conversion process. The employed IGBTs count in these structures

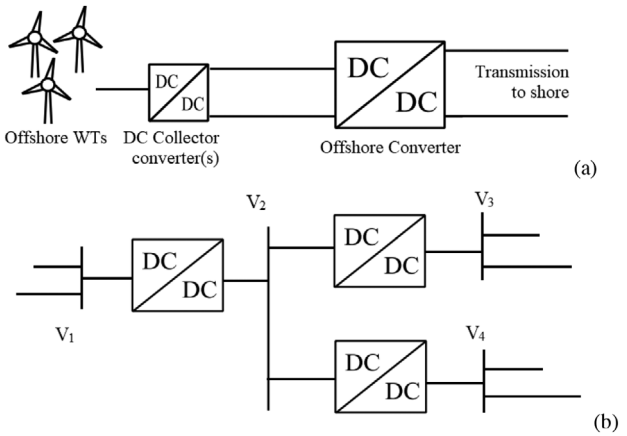

FIGURE 1 DC-DC converter applications in DC grids [1]. (a) Offshore wind turbines (WTs) DC collector collection scheme, (b) grid interconnection

is relatively high and circulating current increases the current stresses on the involved IGBTs.

In [14–18], hybrid modular DC-DC converters were presented, where high-voltage valves and SMs are used for DC-DC conversion in HVDC applications. The high-voltage valve is implemented via series-connected IGBTs. The main challenge is to ensure static and dynamic voltage sharing among the series-connected IGBTs in hard switching operations. On the other hand, soft-switching can be used to avoid dynamic voltage sharing complications.

In [19], arm interchange concept-based two-stage modular DC-DC converter is presented, where the arm condition is changed continuously with the operation to ensure charging and discharging of all involved capacitors to maintain the capacitor voltage balance. This structure requires a relatively high number of IGBTs.

Alternatively, Energy Equalizing Modules (EEMs) concept can be employed along with the conventional MMCs [20–22]. In [20], EEMs are employed to maintain the energy balance between the upper and lower submodules. In [21, 22], EEMs have also been employed with the HB-based MMC configuration to maintain energy balance between the two adjacent upper/lower arms. The presented EEMs in [20–22] are based on Dual HBs (DHBs), where the power flow between the two involved HBs in each EEM is controlled via phase shift control to ensure balanced capacitor voltages [21], that is the energy is transferred between arms through the energy equalizing modules to ensure arms energy balance.

The employed EEMs require a large number of additional semiconductor devices and isolating transformers, which negatively affects converter cost.

In this paper, the conventional MMC configuration is modified by adding additional balancing branches per converter leg to ensure a successful DC-DC conversion process. The main contributions of the presented work can be summarized as follows;

- A modular multilevel DC-DC converter with self-energy equalization is proposed for DC grids applications.

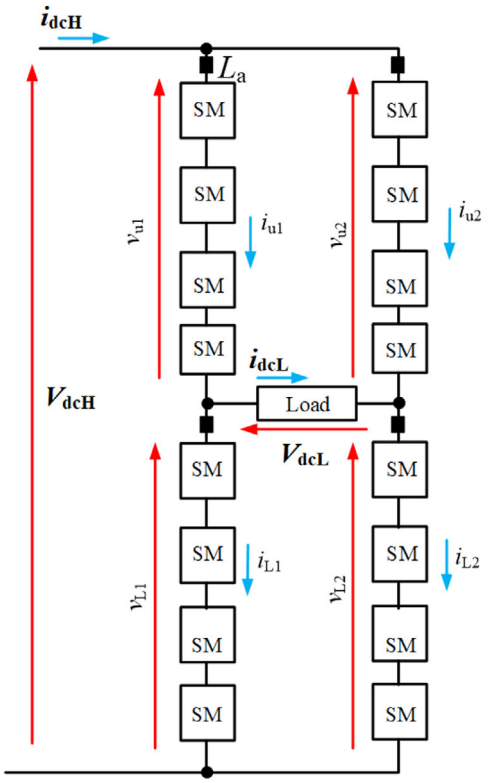

FIGURE 2 The conventional single-phase H-bridge MMC with Half-Bridge (HB)-SMs with arms voltages and currents during DC-DC conversion

- The self-energy equalization is done by employing an additional balancing branch per leg of the conventional half-bridge SM-based MMC.
- The suggested solution requires a lower number of IGBTs compared to the EEMs method, which has a positive effect on the converter cost and efficiency.
- The introduced modification enables energy transfer between arms to ensure energy balance and avoid energy drift.

In the presented work, a detailed illustration of the proposed configuration and its operational concept are presented. Full mathematical analysis and parameters design are presented as well. A simulation model for the proposed configuration is built using MATLAB/SIMULINK software to validate the proposed concept. Finally, a scaled-down prototype has been built for experimental validation. Simulation and experimental results showed satisfactory performance of the modular converter with balanced capacitor voltages during DC-DC conversion.

2 | OPERATIONAL CONCEPTS OF THE CONVENTIONAL MMC

In the presented work, a single-phase HB-based MMC shown in Figure 2 is considered. It consists of two legs, and each leg has two arms, namely, upper (u) and lower (L) arms. Each arm

consists of series-connected pre-charged HB-SMs, where each capacitor is pre-charged with V_{dc}/N, where N is the number of SMs per arm.

Based on the defined upper arms' voltages, the variation of the number of SMs to be included in each upper arm with the operation (N_{ui}) can be generated using one of the multilevel modulation techniques such as Phase Disposition (PD) [3]. To ensure that the sum of upper and lower arm voltages in each leg equals V_{dc}, the number of SMs to be activated in the lower arms (N_{Li}) should equal (N-N_{ui}).

Knowledge of the extracted number of SMs along with arm currents' directions allows proper SM selection for activation while bypassing others to ensure operating with balanced capacitor voltages [3].

Based on Figure 2, the arm voltages are defined by;

$$v_{u1} = v_{L2} = 0.5\,(V_{dcH} - V_{dcL}) \tag{1}$$

$$v_{L1} = v_{u2} = 0.5\,(V_{dcH} + V_{dcL})\,, \tag{2}$$

where V_{dcL} is the desired DC output voltage generated with a value up to V_{dcH} as in (3);

$$V_{dcL} = \alpha V_{dcH}, \tag{3}$$

where α is a bucking factor, that is $\alpha \leq 1$. Based on the power invariance concept, the DC input current is given by (4);

$$i_{dcH} = \frac{i_{dcL} V_{dcL}}{V_{dcH}} = \alpha i_{dcL}. \tag{4}$$

The corresponding arm's currents are given by (5) and (6).

$$i_{u1} = i_{L2} = 0.5\ (i_{dcH} + i_{dcL}) = 0.5 i_{dcL}\,(\alpha + 1) \tag{5}$$

$$i_{L1} = i_{u2} = 0.5\ (i_{dcH} - i_{dcL}) = 0.5 i_{dcL}\,(\alpha - 1)\,. \tag{6}$$

Based on (5) and (6), i_{u1} and i_{L2} are positive, while $i_{L1}$and i_{u2} are negative (unipolar arm currents are associated with the DC-DC operation). This means either charging or discharging is available for arm capacitors, which results in energy drift and capacitor voltage diversion [8]. During DC-DC operation of the conventional H-bridge MMC with HB-SMs (Figure 2), capacitors of the upper arm in leg 1 and capacitors of the lower arm in leg 2 will be charged, and their voltages continuously increase with the operation (an increase of stored energy). The opposite situation occurs for the other arms (decrease of stored energy). To ensure operating with balanced capacitor voltages, the energy balance between arms should be fulfilled. This can be done by finding a way to transfer the energy between arms to keep the energy balance and avoid energy drift. This paper presents a new approach to ensure arm energy balance for MMC's DC-DC operation. The details of the proposed approach are given in the following sections.

3 | PROPOSED MODIFIED MMC FOR DC-DC POWER CONVERSION WITH ENERGY SELF-EQUALIZATION

The proposed modular DC-DC converter/transformer is shown in Figure 3, where it is used to interconnect two different DC voltages levels in DC grids, namely, the high-voltage level (V_{dcH}) and the low-voltage side (V_{dcL}). For simplicity, the concept is illustrated, assuming four SMs per each arm ($N = 4$). With the same concept, a higher number of SMs per arm can be employed for higher voltages.

The proposed architecture consists of conventional single-phase HB-based MMC with some modifications to ensure balanced and bounded capacitor voltages during DC-DC operation via enabling energy transfer between arms (verifying energy balance condition).

The modifications over the conventional MMC topology are drawn in blue colour in Figure 3. The proposed configuration has two sequential modes of operation, namely, mode I and mode II, where swapping between them during the DC-DC conversion guarantees operating with balanced and bounded capacitor voltages. These modes are enabled sequentially during operation. During mode I, the proposed configuration is treated similar to a conventional MMC, and clamping IGBTs (S_{x1}: S_{x12}) are disabled (Figure 4(a)). This mode results in an energy difference between upper and lower arms in each leg. Then to restore the energy balance between arms in the same leg, mode II is activated, where clamping IGBTs (S_{x1}: S_{x12}) are enabled for parallel connection of arm capacitors (Figure 4(b)).

It has to be noted that with the help of S_1: S_{16} IGBTs, upper clamping IGBTs enable parallel-connection of upper arm capacitors, while lower clamping IGBTs enable parallel-connection of lower arm capacitors. The proposed configuration enables the parallel connection between two groups in each leg to transfer energy between arms through a limiting inductor (L_m). The first group represents the parallel-connected upper capacitors, while the second group represents the parallel-connected lower capacitors.

The limiting inductor is employed to limit the inrush current that emanates from the parallel connection of the aforementioned two groups with voltage mismatch between upper and lower capacitors. Two complementary bidirectional switches are employed with the limiting inductor to ensure successful operation and avoid high-voltage stresses due to di/dt effect. The switch (S_p) has the responsibility of inductor bypassing to freewheel its current when the parallel connection between the upper and lower capacitors is deactivated while the other switch (S_p) is turned-on during the parallel-connection period.

It has to be noted that mode I is enabled for the DT period where $D < 1$, and T is the pre-defined periodic time, which equals β/f_s, where β is an integer higher than 1, and f_s is the frequency of carriers in the PD modulation technique. The value of β should be appropriately selected to ensure operating with limited capacitor voltage ripple and limited switching losses of the additional balancing branch. On the other hand, mode II is

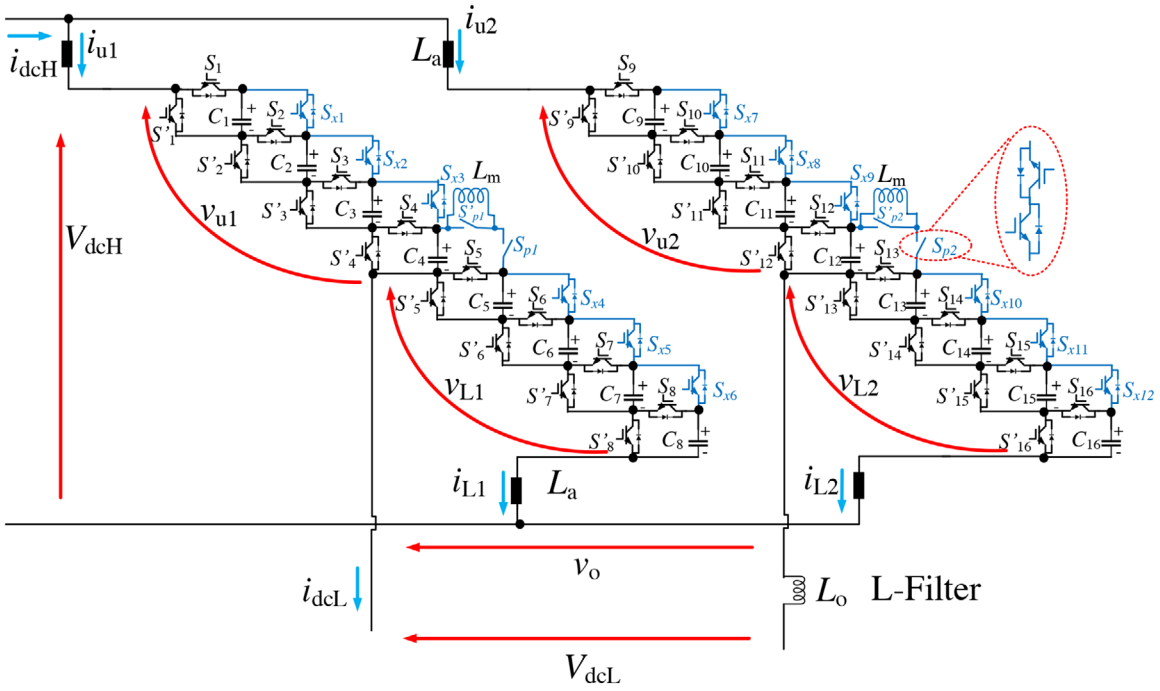

FIGURE 3 The proposed HB-based modular DC-DC converter with clamping IGBTs for $N = 4$ (where S' is complementary of S)

enabled for (1-D)T. The details of each mode are summarized in the following section.

4 | MODES OF OPERATION OF THE PROPOSED ARCHITECTURE

4.1 | Mode I ($0 < t <$ DT)

During mode I, the circuit is operated similar to a conventional MMC, as shown in Figure 4(a), where the clamping IGBTs are disabled, and the limiting inductors are bypassed (S_{x1}: $S_{x12} = 0$, S_{p1} and $S_{p2} = 0$, and S'_{p1} and $S'_{p2} = 1$). In this mode, the per-unit reference of upper arm voltage in leg 2 is given by;

$$v^*_{u2\,pu} = 1 - v^*_{u1\,pu}, \tag{7}$$

where $v^*_{u1\,pu}$ is the per-unit reference of upper arm voltage in leg 1. The proper value of $v^*_{u1\,pu}$ will be extracted from closed-loop current control at the low voltage DC side. This part will be addressed in the following section. The upper arm voltage references are used to generate a number of SMs to be activated in each upper arm (N_{u1} and N_{u2}) using the PD modulation technique, as shown in Figure 5. The number of SMs to be activated in the lower arms is then extracted as $N_{L1} = (N\text{-}N_{u1})$ and $N_{L2} = (N\text{-}N_{u2})$.

Finally, with the help of the extracted number of SMs in each arm and arm current directions, gate pulses of the involved SMs can be generated, as shown in Figure 5, where the basic voltage balancing technique presented in [3] has been employed in this work.

During mode I, the capacitor voltages of the arms (u_1 and L_2) increase due to the flow of positive arm current through them, as shown in (5), that is an increase in the stored energy of these arms. On the other hand, the capacitor voltages of the arms (u_2 and L_1) decrease due to the flow of negative arm current through them, as shown in (6), which means there is a decrease in the stored energy in these arms. As a result, if mode I is left for a long time, energy drift occurs, which leads to unsuccessful DC-DC operation. So the circuit is switched to mode II to ensure energy balance between arms, where the capacitors with higher energy stored (in $u1$ and L_2 arms) are transferring their extra energy to the capacitors with lower energy stored (in L_1 and u_2 arms).

4.2 | Mode II (DT $< t <$ T)

Restoration of arms energy balance can be achieved in mode II with the help of the added components, as illustrated in this subsection. It has to be noted that mode II is enabled for a time period of (1-D)T, then the circuit is re-switched to mode I, and so on periodically, that is successful DC-DC conversion of the proposed architecture depends on continuous swapping between the two defined modes during the operation.

To transfer energy between the upper and lower arms in both legs during mode II, zero upper and lower arm voltages are enabled, as shown in Figure 4(b) via turning on (S'_1:S'_{16}), turning-on clamping IGBTs (S_{x1}:S_{x12}), and turning-on (S_{p1}, S_{p2}). The equivalent circuits during mode II are shown in Figure 6.

Due to operating with zero upper and lower arm voltages during mode II, Figure 6(a) shows that the arm inductors

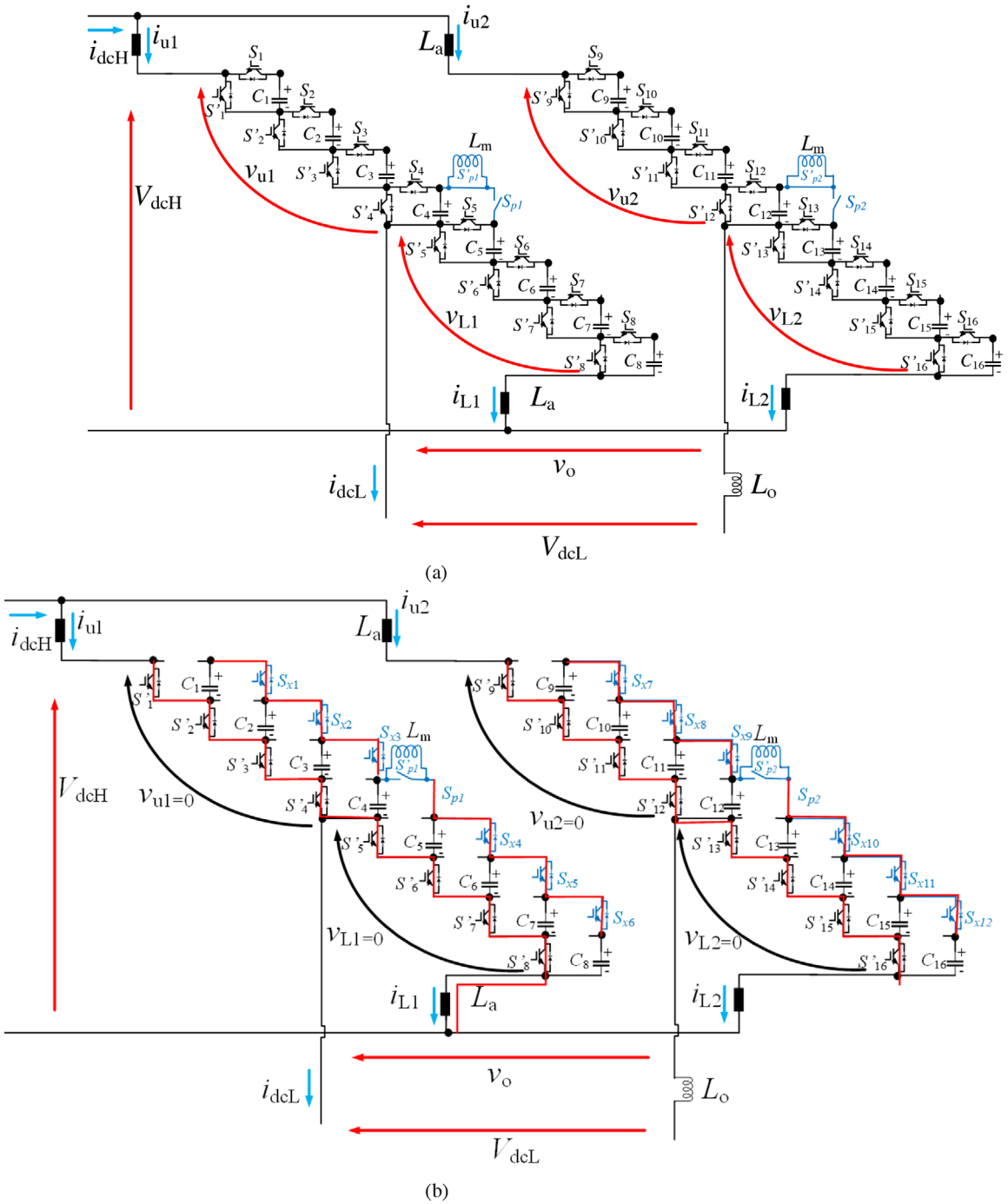

FIGURE 4 Modes of operation of the proposed architecture for $N = 4$ (a) Mode I, and (b) Mode II

are charged up from the high-voltage level (V_{dcH}) for a time interval of (1-D)T, which results in operating with boosting action for SMs capacitor voltages with continuous swapping between modes I and II. As a result, the SMs capacitor voltages are higher than the conventional MMC voltage level (i.e. $> V_{dcH}/N$).

For a boosting factor B, the SMs capacitor voltages are defined by (BV_{dcH}/N). The value of the boosting factor depends on the value of (D). So the duty cycle (D) should be appropriately selected to ensure a limited boosting factor. It has to be noted that an output L-filter (L_o) at the low-voltage side is employed to ensure operating with a continuous output DC current (i_{dcL}).

On the other hand, each leg's circuit is shown in Figure 6(b), where the parallel-connected upper capacitors are connected across the parallel-connected lower capacitors through the limiting inductor (L_m). As the upper and lower groups have different voltages, the employment of a limiting inductor is necessary to

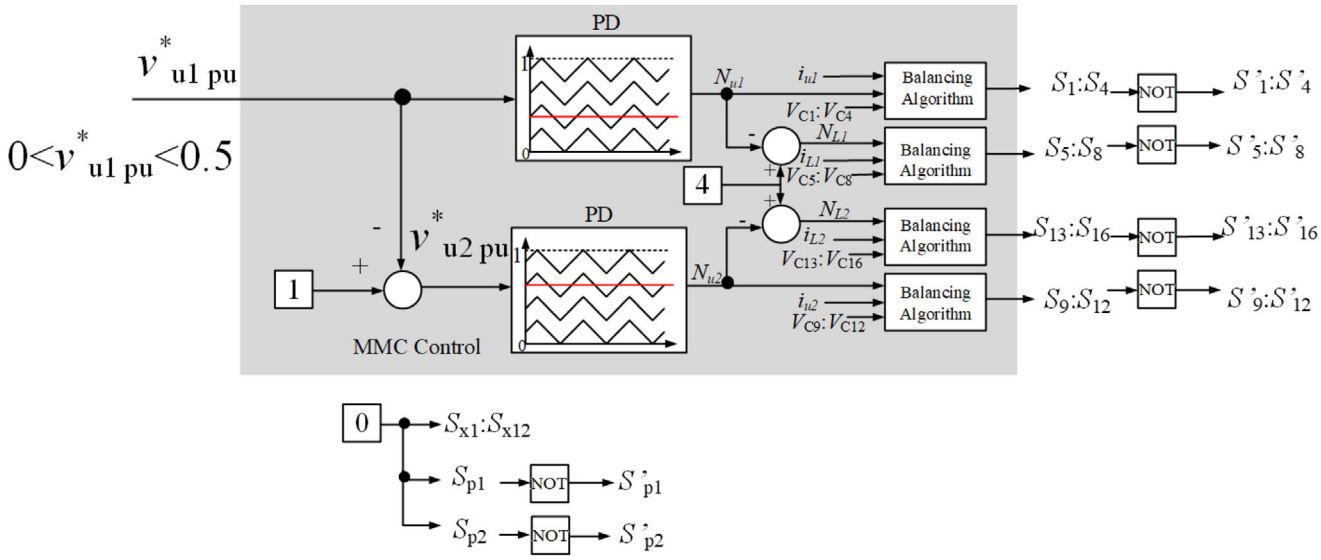

FIGURE 5 Gate pulses generation during mode I for $N = 4$

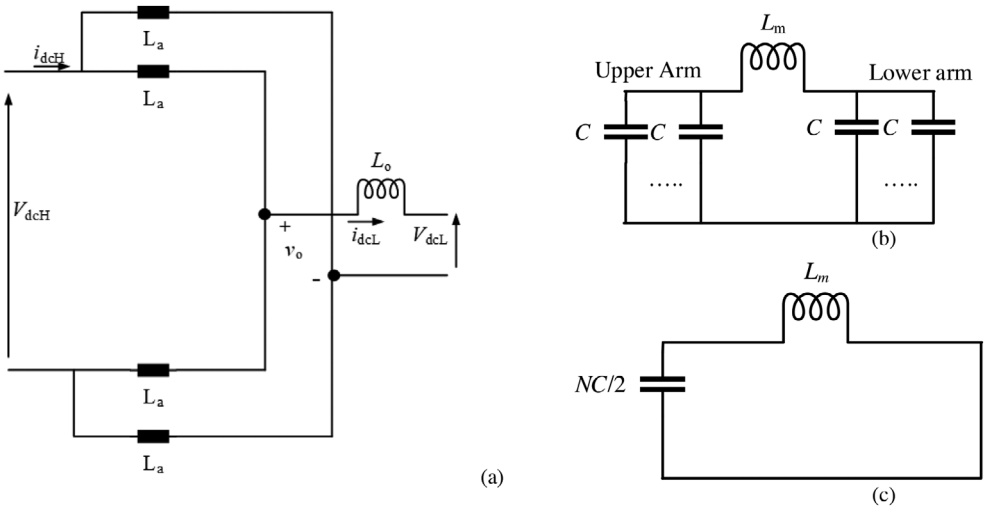

FIGURE 6 Equivalent circuits during mode II (a) charging arm inductors, (b) energy transfer between upper and lower arms in the same leg, and (c) equivalent circuit of Figure 6b

limit the inrush current that emanates from the parallel connection of both groups.

The parallel connection of the two aforementioned groups in each leg through a limiting inductor enables energy transfer between the arms in the same leg, where the arm with higher energy stored discharges into the other arm, which ensures energy balance condition. The direction of energy (or direction of limiting inductor current) depends on which arm has higher energy. For example, for positive i_{dcL}, in the first leg, the upper arm discharges into the lower arm, while in the second leg, the lower arm discharges into the upper arm. The opposite occurs in the case of negative i_{dcL}, which necessitates the employment of bidirectional switches (S_p and S'_p). The equivalent circuit of Figure 6(b) is shown in Figure 6(c), which is a second-order LC circuit.

5 | CLOSED-LOOP CONTROL

The overall controller for the proposed architecture is shown in Figure 7, where the current at the low-voltage side (i_{dcL}) is controlled to track a desired current reference. This can be done by comparing the actual and reference currents, then feeding the current error to a suitable controller, that is $G(s)$, such as the Proportional-Integral-Derivative controller (PID-controller) to extract the proper voltage reference for the upper arms, as shown in Figure 7. The current reference may be positive or negative, depending on the power flow direction.

If the current i_{dcL} is positive, the power is transferred from V_{dcH} side into V_{dcL} side and vice versa. It has to be noted that a square wave signal (En) with a duty cycle of D and periodic time of T is employed as a selector to swap

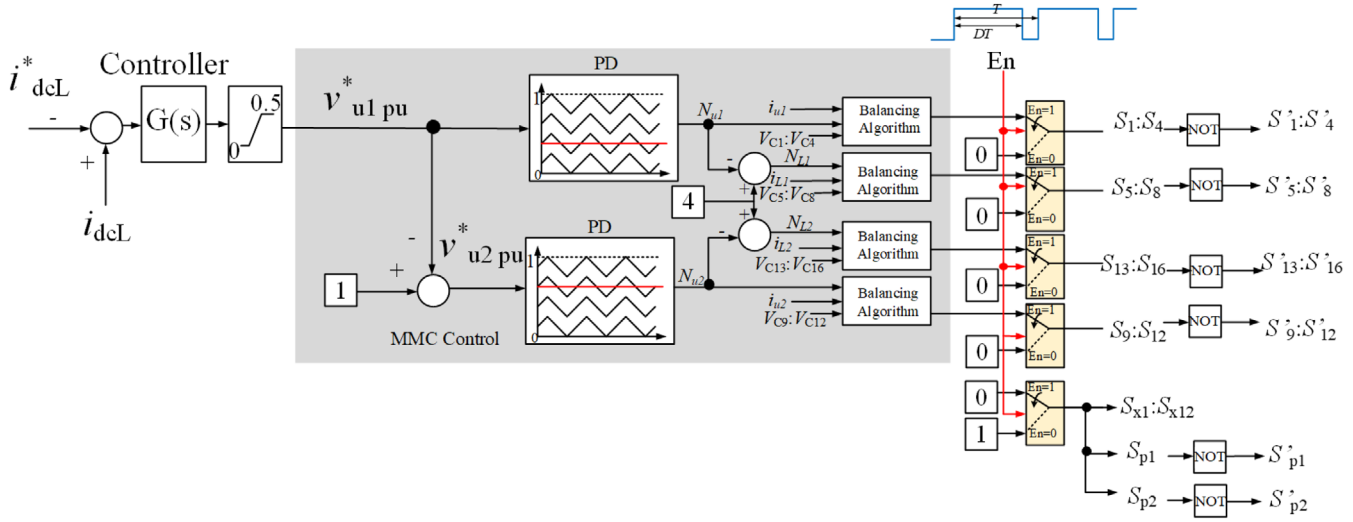

FIGURE 7 Closed-loop controller of the proposed architecture for $N = 4$

the operation between mode I and mode II, as shown in Figure 7. The periodic time T is selected such that $T = \beta/f_s$ where β is an integer higher than 1, and f_s is the frequency of PD carriers. The value of the duty cycle (D) should be selected to ensure operating with acceptable voltage and current stresses. The governing equations are presented in the following section.

6 | MATHEMATICAL ANALYSIS AND DESIGN

In this section, mathematical analysis and assessment of the proposed DC-DC converter along with its main components' design are presented.

6.1 | Arm inductor (L_a)

Based on Figure 6(a), the relation between the rate of increase of arm inductor current and V_{dcH} during mode II is given by;

$$V_{dcH} = 2L_a \frac{di}{dt} = 2L_a \frac{\Delta i}{(1-D)\,T} \tag{8}$$

For a defined current ripple of the arm currents (Δi), the proper arm inductance is given by;

$$L_a = V_{dcH}\ (1-D)\,T/2\Delta i \tag{9}$$

To ensure a limited arm current ripple, proper arm inductance should be selected. In the proposed approach, it has to be noted that the arm inductor should be designed to withstand a relatively high voltage, where during mode II, the voltage at the high-voltage side V_{dcH} is applied across the arm inductors of each converter leg as shown in Figure 6(a).

6.2 | Submodule capacitors (C)

During mode I, the capacitors are charged/discharged during the DT time duration. The relation between the current and voltage of the capacitor (i_c and v_c) is given by;

$$i_c = C dv_c/dt \tag{10}$$

$$i_{arm}\ \ v^*_{arm\ pu} = C\Delta v/DT, \tag{11}$$

where i_{arm} and $v^*_{arm\ pu}$ are the arm current and the per-unit arm voltage reference, respectively.

Based on the desired capacitor voltage ripple, Δv, proper submodule capacitance is given by;

$$C = i_{arm}\ \ v^*_{arm\ pu} DT/\Delta v \tag{12}$$

6.3 | Limiting inductor (L_m)

During mode II, based on Figure 6(c), the natural frequency (rad/s) for the second-order LC circuit is given by;

$$\omega_o = 1/\sqrt{L_m NC/2}. \tag{13}$$

In order to ensure unipolar current through the limiting inductor (L_m) during mode II, the time duration of mode II should be less than the periodic time of the second-order circuit ($2\pi/\omega_o$).

$$(1-D)\,T \ll \frac{2\pi}{\omega_o}. \tag{14a}$$

$$L_m \gg \frac{2}{NC}\left(\frac{(1-D)\,T}{2\pi}\right)^2 \tag{14b}$$

TABLE 1 Comparison between the proposed approach versus the EEMs approach

	H-bridge modular multilevel DC-DC converter with EEMs approach presented in [20] and [21]	The proposed approach
Voltage at high-voltage side	V_{dcH}	V_{dcH}
Number of employed legs	2	2
Number of employed SMs per arm	N	N
Voltage rating of SMs/IGBTs	V_{dcH}/N	BV_{dcH}/N
Number of employed IGBTs	8N IGBTs for SMs + 8N IGBTs for EEMs = 16N IGBTs	8N IGBTs for SMs +4(N–1) clamping IGBTs +8 IGBTs (limiting inductor) = 4(3N+1) IGBTs
Number of isolating transformers	2N	–
Number of arm inductors	4	4
Voltage rating of arm inductor	Low	High
Inductance of arm inductor	Low	High
Number of limiting inductors	–	2
Number and voltage rating of SMs capacitors	Two capacitors per SM, Total = $8N$ (voltage rating = $V_{dcH}/2N$)	one capacitor per SM, Total = 4N (voltage rating = BV_{dcH}/N)

6.4 | Boosting factor (B)

In the proposed architecture, each arm inductor has a continuous bounded current. The average voltage of each arm inductor is zero. During mode I, the sum of upper arm voltage and lower arm voltage equals $BV_{dcH,}$ where B is the defined boosting factor ($B > 1$) due to the aforementioned boosting effect of arm inductors. As a result, the voltage across each arm inductor during mode I is given by $-0.5(B-1)V_{dcH}$. On the other hand, the voltage across each arm inductor during mode II (Figure 6(a)) approximately equals $0.5V_{dcH}$. For zero average voltage across the arm inductor, the following equation can be written.

$$0.5\,(B-1)\,V_{dcH}\,D\,T = 0.5V_{dcH}\,(1-D)\,T \tag{15}$$

$$B = 1/D \tag{16}$$

Based on (16), as D increases, the boosting factor decreases.

6.5 | Number of SMs per arm (N)

For a given boosting factor (B), high-voltage level (V_{dcH}), and voltage rating of available SMs, the proper number of SMs per arm can be estimated. Moreover, the voltage rating of each submodule is given by BV_{dcH}/N.

6.6 | Assessment of the proposed converter

To demonstrate the effectiveness of the proposed converter, Table 1 shows the comparison between the proposed H-bridge DC-DC MMC the conventional DC-DC MMC with DHB-based EEMs [20], [21] connected between the upper and lower arms. The comparison has been held in terms of the number of employed capacitors/IGBTs and their voltage ratings, isolating transformers, and inductors. The comparison shows the effectiveness of the proposed approach over the EEMs approach, where no need for isolating transformer, as well as a lower number of IGBTs is required in the proposed approach. Figure 8 shows the number of employed IGBTs in both types for (N) number of SMs per arm. It is clear that as N increases, the saving in employed IGBTs is significant.

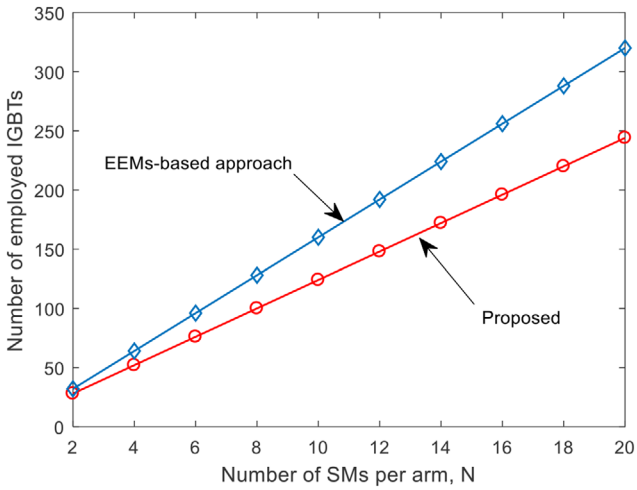

FIGURE 8 The comparison between the proposed approach versus the EEMs-based approach

7 | SIMULATION

A simulation model for a 10 kV/4 kV 800 kW DC-DC converter has been built for validation, assuming four SMs per arm ($N = 4$), as shown in Figure 3. The PD modulation technique with 2.4 kHz carriers is employed ($f_s = 2400$ Hz).

TABLE 2 Simulation and experimental parameters

Parameter	Simulation	Experimental
High-voltage side, V_{dcH}	10 kV	150 V
Number of SMs per arm, N	4	2
Low-voltage side, V_{dcL}	4 kV	110 V
Converter rated power	800 kW	1.5 kW
Rated current at low-voltage	+/− 200A	10 A (11 Ω load)
Carrier frequency	2400 Hz	2400 Hz
Enable signal (En)	$D = 0.8$, $T = 1/600$	$D = 0.9$, T = 1/240
Output filter, L_o	3 mH	11 mH
SM capacitance	1 mF	470 μF
Arm/limiting inductor	40 mH/90 μH	5 mH/10 μH

The system parameters are tabulated in Table 2, where components design is as follows; Based on (16), for $D = 0.8$, the boosting factor equals 1.25. The voltage rating of the involved SMs equals 1.25(10 kV)/4 = 3125 V. The rated current at the low-voltage side (i_{dcL}) equals 800 kW/4 kV = 200A. Based on (5), (6), and for i_{dcL} of +200A, the corresponding arm currents $i_{u1} = i_{L2} = 140$A, while $i_{L1} = i_{u2} = -60$A (where $\alpha = 4$ kV/10 kV = 0.4). The approximate per-unit reference voltage of upper arm in leg1 (v^*_{u1pu}) equals 0.5(10 kV−4 kV)/(10 kV) = 0.3, $v^*_{u2\,pu} = 1-0.3 = 0.7$.

Based on (12), for $\Delta v = 2\%$ (62.5V) and $T = 1/600$ ($\beta = 4$), based on upper arm (u_1) voltage and current, the submodule capacitance C = (140*0.3*0.8*(1/600))/62.5∼ = 1 mF. Based on (9), for $\Delta i = 40$A, the proper arm inductance L_a = (10 kV(1−0.8)*(1/600))/(2*40A); which results in L_a∼ = 40 mH. In the presented case study, a 40 mH inductor with an equivalent series resistance (ESR) of 0.25 Ω is considered. The value of duty cycle D is selected to be 0.8 as, during the equalization period (during $(1-D)T$ period), the converter output voltage is dropped. So to ensure a smooth output current, the duty cycle D should be kept high. The associated boosting action ($B = 1/D$) should be limited to avoid overvoltage of the involved DC capacitors and IGBTs. Based on (14b), a limiting inductor (L_m) = 90 μH is selected.

An output inductor filter (or smoothing reactor) is connected in series at the low-voltage terminals to ensure operating with a smooth current at the low-voltage side. Its inductance should be appropriately-selected to have attenuated output current ripple. The reactance of the output inductor at the swapping frequency is given by $X_L = 2\pi(1/T)L_f$.

The (X_L/R_{eq}) ratio should be appropriately-selected to ensure a smooth output current, where R_{eq} is the equivalent resistance seen by the converter low-voltage terminals.

In the presented simulated case study, $V_{DCL} = 4$ kV, $T = 1/600$ s, $P_o = 800$ kW, so for X_L/R_{eq} ratio of ½, the suitable reactance $X_L = 0.5R_{eq} = V^2_{DCL}/2\,P_o = 10\Omega$, that is suitable inductance = $10T/(2\pi) = 2.65$mH, so 3mH is selected.

In the presented case study, the current reference at the low-voltage side (i^*_{dcL}) is changed from +200 to −200 A to validate the bidirectional DC-DC operation.

The corresponding simulation results are shown in Figure 9, where a PID controller is employed to regulate the current at the low-voltage side (i_{dcL}). Figure 9(a) shows the grid currents at both sides. The current at the low-voltage side (i_{dcL}) tracks its reference successfully.

Based on the power invariance condition, it is expected that the high voltage side DC current (i_{dcH}) has an average value of 80A, which is validated in the presented results. Figures 9(b) and 9(c) show the voltages of the SMs' capacitors in the first and second legs, respectively. The capacitor voltages are well balanced and bounded thanks to the suggested modes of operation (mode I and mode II), where mode II allows the transfer of energy between arms of the same leg (energy drift is avoided). As a result, the voltages of the capacitors are kept balanced and bounded during the DC-DC conversion.

Figures 9(b) and 9(c) show that the level of capacitor voltages is approximately 3125 V, as extracted before in the design steps, which validates the presented aforementioned analysis. They also show that the desired magnitude of capacitor voltage ripples (Δv) is also achieved.

The arm currents of leg 1 are shown in Figure 9(d), where their average levels are 140A and 60A, as mentioned in the aforementioned design steps. On the other hand, the current of the limiting inductor is shown in Figure 9(e). The inductor current level is approximately 670A, which can be extracted merely assuming a zero average current of the involved SM capacitors. Finally, the zoomed-in view of the converter output voltage (v_o) is shown in Figure 9(f), where based on the magnitude and polarity of the desired current at the low-voltage side, the generated voltage supports injecting/absorbing the desired current to/from the low-voltage DC bus (V_{dcL}) through the inductive filter at the low-voltage side. It has to be noted that although all converter arms are short-circuited in mode II (during equalization period), the converter output voltage (v_o) is not zero during mode II in the presented results (Figure 9(f)), that is due to the unequal voltage distribution across the involved upper/lower arm inductors.

To check the proposed converter's efficiency for the presented simulation case study, the conduction and switching power loss calculations presented in [23] are adopted for the simulated case study. A 4.5 kV, 800 A (5SNA 0800J450300) IGBT module [24] is selected. The corresponding converter efficiency versus loading is shown in Figure 10, where it is clear that, as with other MMC-based topologies, the proposed converter's efficiency is high, which approximately equals 98%.

8 | EXPERIMENTAL VALIDATION

A 1.5 kW scaled-down prototype of the proposed modular DC-DC converter has been implemented, as shown in Figure 11, assuming the experimental parameters given in Table 2.

Based on (16), for $D = 0.9$, the boosting factor equals 1.11, the voltage rating of the involved SMs equals 1.11(150)/2 ∼ = 85 V. The rated current at the low-voltage side (i_{dcL}) equals 10 A.

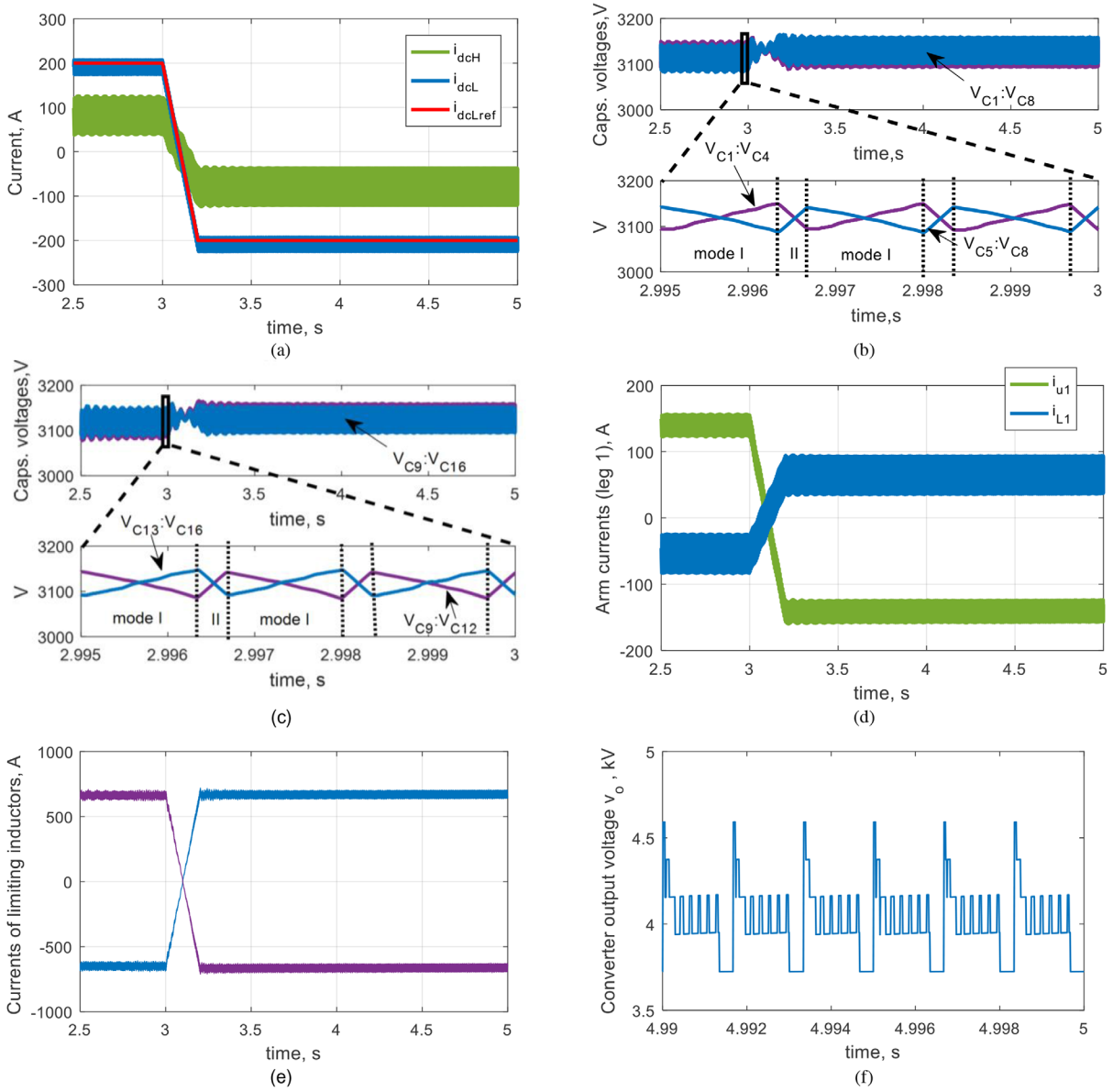

FIGURE 9 Simulation results. (a) DC currents at high and low voltage DC sides, (b) capacitor voltages of leg 1, (c) capacitor voltages of leg 2, (d) arm currents of leg 1, (e) currents of the involved limiting inductors assuming ideal bidirectional switches, and (f) the generated voltage at the low-voltage side of the converter

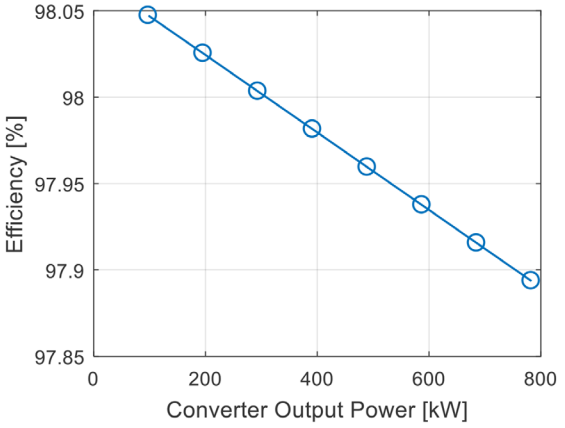

FIGURE 10 The converter efficiency versus loading for the simulated case study

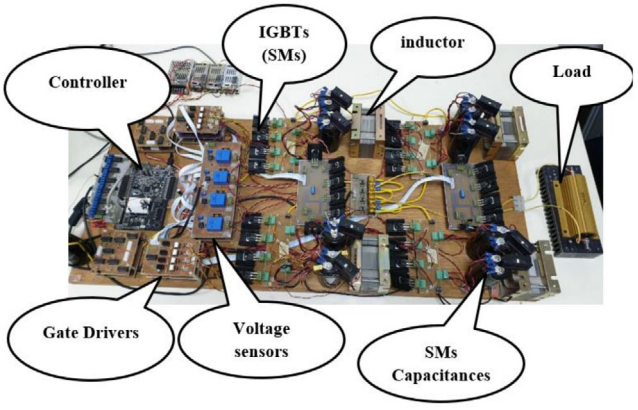

FIGURE 11 Experimental rig

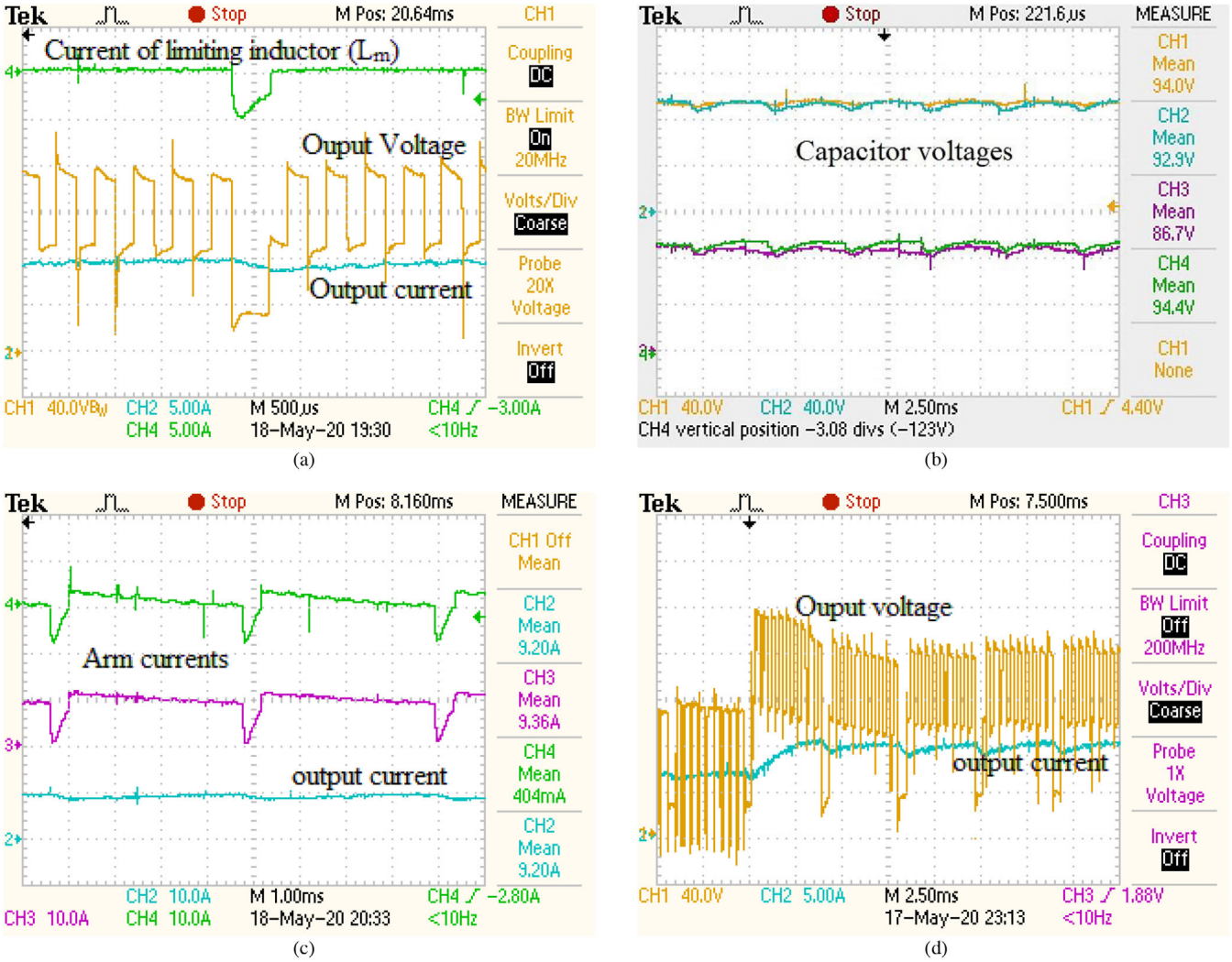

FIGURE 12 Experimental results. (a) limiting inductor current, output voltage, v_o, and output current,i_{dcL}, at 110 V output voltage, (b) capacitor voltages, v_{Ci}, at 110 V output voltage, (c) arm currents at the mid-leg point and the output currents, i_{dcL}, at 110 V output voltage, and (d) dynamic behaviour of the proposed converter when the output voltage,v_o, is changed from 75 to 110 V (step change)

For 110 V at the low-voltage side, the upper arm's per-unit reference voltage in leg1 ($v^*_{u1\,pu}$) equals 0.133 pu, and i_{u1} approximately equals 9A. Based on (12), for $\Delta v = 10\%$ and $T = 1/240$, based on upper arm voltage and current in the first leg, the proper submodule capacitance $C = 500$ µF, so 470 µF capacitance is employed. Also, 5 mH arm inductors and 10 µH limiting inductors are used to ensure operation with acceptable arm inductor current ripples and limited inrush current during the parallel-connection period. Finally, for $V_{DCL} = 110$ V, $T = 1/240$ s, $P_o = 1$ kW, and X_L/R_{eq} ratio of 1, the suitable smoothing reactance at the output terminal $X_L = R_{eq} = 12\Omega$, that is suitable series inductance at the low-voltage side is equal to 8 mH, so 11 mH is employed.

An open-loop control is applied to generate the desired DC output voltage (110 V). The corresponding experimental results are shown in Figure 12. Figure 12(a) shows output voltage, output current, and limiting inductor current at 110 V average output voltage (10 A load current). At the instant of parallel connection between upper and lower capacitances, inrush current passes through the limiting inductor from the higher voltage capacitances to the lower voltage capacitances, which leads to capacitor voltages equalization.

During the equalization interval, the upper arm's capacitors are connected in parallel (upper group), and the capacitors of the lower arm are connected in parallel as well (lower group). Since the upper group's voltage is different from the lower group's voltage, consequently, when the upper group is connected to the lower group through the limiting inductor, the shown inrush current is introduced through the limiting inductor. The rate of change of current depends on the limiting inductor value and the voltage difference between the upper and lower groups.

Figure 12(b) shows the voltages of the capacitors at the upper as well as lower arms. The capacitor voltages are well balanced with the operation, which is necessary for the successful DC-DC conversion process. It has to be noted that the capacitor

voltage is higher than the nominal voltage level in conventional MMC (i.e. 150 V/2 = 75 V) due to the associated boosting action in the presented topology where the boosting factor (B) is equal to 1.11 in the presented experimental results.

The corresponding arm currents at the mid-leg point with the operation are shown in Figure 12(c), where their subtraction equals the load current. To check the proposed circuit's dynamic performance, the output voltage is changed from 75 to 110 V. The corresponding results are shown in Figure 12(d), where the output voltage changes successfully as desired.

9 | CONCLUSION

In this paper, a modified modular DC-DC converter has been proposed for DC grids applications. The proposed configuration depends on the conventional single-phase H-bridge MMC along with an additional balancing branch per each leg. The additional balancing branch consists of 4(N−1) clamping IGBTs for N-level HB-SM based MMC, two limiting inductors, along with four bidirectional switches. Similar to the energy equalization modules (EEMs) concept, the additional balancing branches provide channels to transfer energy between upper capacitors and lower capacitors during the equalization period. The main advantage of the proposed approach over the EEMs concept is that the proposed approach needs no isolating transformers, and it requires a lower number of IGBTs, that is 4(3N+1) instead of 16N IGBTs, which positively affects the converter cost and efficiency. A detailed illustration of the proposed concept, along with mathematical analysis, design equations, and closed-loop controller, have been presented. Finally, simulation and experimental results have been presented for validation. The results show the promising performance of the proposed modular DC-DC converter with self-energy equalization.

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