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Hybrid Multimodule DC-DC Converters for Ultrafast Electric Vehicle Chargers

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Abstract: To increase the adoption of electric vehicles (EVs), significant efforts in terms of reducing the charging time are required. Consequently, ultrafast charging (UFC) stations require extensive investigation, particularly considering their higher power level requirements. Accordingly, this paper introduces a hybrid multimodule DC-DC converter-based dual-active bridge (DAB) topology for EV-UFC to achieve high-efficiency and high-power density. The hybrid concept is achieved through employing two different groups of multimodule converters. The first is designed to be in charge of a high fraction of the total required power, operating at a relatively low switching frequency, while the second is designed for a small fraction of the total power, operating at a relatively high switching frequency. To support the power converter controller design, a generalized small-signal model for the hybrid converter is studied. Also, cross feedback output current sharing (CFOCS) control for the hybrid input-series output-parallel (ISOP) converters is examined to ensure uniform power-sharing and ensure the desired fraction of power handled by each multimodule group. The control scheme for a hybrid eight-module ISOP converter of 200 kW is investigated using a reflex charging scheme. The power loss analysis of the hybrid converter is provided and compared to conventional multimodule DC-DC converters. It has been shown that the presented converter can achieve both high efficiency (99.6%) and high power density (10.3 kW/L), compromising between the two other conventional converters. Simulation results are provided using the MatLab/Simulink software to elucidate the presented concept considering parameter mismatches.

Keywords: ultra-fast chargers; input-series input-parallel output-series output-parallel multimodule converter; cross feedback output current sharing; reflex charging

1. Introduction

Despite the fact that internal combustion engines (ICEs) have been a mature technology for the past 100 years, it is expected that electric vehicles (EVs) will break the monopoly of conventional vehicles using only ICEs because of their performance and superior fuel economy [1]. Due to the strict regulations on global warming and energy resources constraints, and on reducing fossil fuel prices as well as gas emissions, environmental awareness has led to a high interest in EVs as an alternative solution for further improvement compared to ICEs [2,3]. To increase the adoption of EVs, significant efforts in terms of reducing the charging time are required. Consequently, to allow massive market penetration of EVs, the concept of ultrafast charging (UFC) requires more investigation. In this regard, several research studies targeting fast chargers and UFC for EVs have been provided in the literature [4–8]. UFC technology is a high power charging technology ($\geq$ 400 kW) that can replace or substitute the ICE technology and can charge EVs' battery packs in $\leq$ 10 min [9–11].

Advanced power electronics converters are considered as key enabling technologies for realizing EV UFC, where high-power DC-DC converters are needed. The critical requirements for designing EV battery chargers are high efficiency, low cost, high power density, and galvanic isolation [12].

Furthermore, one of the UFC stations' requirements is to design the DC-DC converters in a modular manner to offer easy maintenance, as well as scalability, redundancy, and fault ride-through capability [13–15]. In modular power converters, each unit handles a small portion of the total input power. Accordingly, the selected power switches are of lower voltage and/or current ratings; therefore, higher switching frequency capability, consequently, reduced weight and size [16–18]. Multimodule DC-DC converters can provide a bidirectional power flow through employing submodules that are based on dual active bridge (DAB), dual half bridge (DHB), or series resonant topologies [19,20].

The DAB configuration, shown in Figure 1, consists of two active bridges that are connected via a medium/high-frequency AC transformer. DAB can be constructed using a single-phase bridge or a three-phase bridge depending on the design criteria. The 2L-DAB, shown in Figure 1, usually operates in a square wave mode. The intermediate transformer leakage inductance limits the maximum power flow and is used as the energy transferring element. This topology is capable of bidirectional power flow that can be achieved by controlling the phase shift between the two bridges and the magnitude of the output voltage per bridge. The switches can be switched at zero voltage switching (ZVS) and/or zero current switching (ZCS). Accordingly, switching losses are reduced, and the power efficiency is increased.

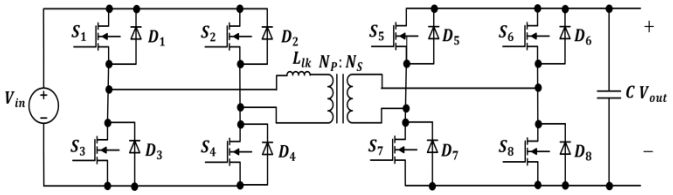

Figure 1. DAB converter circuit diagram.

Figure 2 presents a block diagram for a typical EV UFC that involves an AC-DC stage and a DC-DC stage. This paper will focus on the DC-DC stage employed in EV UFC applications. In the literature, many research studies have been introduced the two stages. In [21], to realize medium-voltage EV UFC stations, a multiport power converter has been proposed. In [22], a bidirectional fast charging system control strategy consisting of two cascaded stages has been proposed, where two DABs are connected in parallel at the battery side. However, in [23], an isolated DAB-based single-stage AC-DC converter has been presented. The charger in [23] contains a single stage that includes the PFC and ensures ZVS over the full load range. In [24,25], a frequency modulated CLLC-R-DAB has been proposed. In this topology, the converter operates over a considerable variation of the input voltage while maintaining soft-switching capability. A smaller switching frequency range is used to modulate the CLLC-R-DAB converter when compared to SR-DAB. In [26], a full-bridge phase-shifted DC-DC converter that combines the characteristics of the double inductor rectifier and the conventional hybrid switching converter is introduced for EV fast chargers. In [27], a medium-voltage high-power isolated DC-DC converter for EVs fast chargers is presented. In [28], the AC-DC and DC-DC stages of an EV charger are studied where the DC-DC stage utilizes interleaved DC-DC converters.

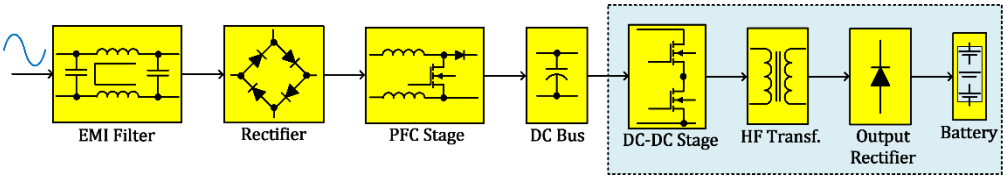

Figure 2. Block diagram for a typical EV UFC.

Multimodule converters are considered a suitable choice for realizing the high power and high voltage requirements of the UFC charger. However, an increased number of modules with low power would increase system complexity, cost and losses, which reduces the cooling requirements and

consequently the weight, volume, and cost. However, reduced switching losses can be achieved via soft-switching [29–35]. Nonetheless, introducing a low number of modules with high power would reduce the switching frequency capabilities; therefore, reducing the power density, which increases size and weight.

Accordingly, the main contribution of this work is to introduce a hybrid multimodule DC-DC converter-based DAB topology as the DC-DC stage for EV UFC to achieve high efficiency, high power density, and reduced weight and cost. The hybrid concept is achieved through employing two different groups of multimodule converters. The first group is designed to be in charge of a high fraction of the total required power while operating relatively at a low switching frequency. Nevertheless, the second group is designed for a low fraction of the total power operating relatively at a high switching frequency. The work presented in this paper includes a generalized small-signal model for the presented converter as well as the control strategy required in achieving uniform power-sharing between the employed modules. Besides, a power loss evaluation has been conducted to compare the proposed converter with the other two options.

To verify the presented concept, the number of modules needed to achieve the required ratings is calculated for both; conventional multimodule DC-DC converters and hybrid multimodule DC-DC converters. In addition, the power loss analysis of the hybrid multimodule converter is provided. To support the power converter controller design, a generalized small-signal model for the hybrid multimodule DC-DC converter is studied in detail. Besides, to ensure equal power-sharing among the employed modules, the control scheme for the hybrid multimodule DC-DC converter with the aforementioned specifications is studied. The main contribution of the paper can be summarized as follows:

- Development of a hybrid multimodule DC-DC converter-based DAB topology for EV UFC along with providing generalized small-signal modeling to support the design of the power converter controller. The presented generalized small-signal model of the hybrid multimodule DC-DC converter-based DAB is considered as the primary contribution of this paper.
- Examining the cross feedback output current sharing (CFOCS) for the hybrid Input-series output-parallel (ISOP) multimodule power converters to ensure uniform power-sharing among the employed modules and ensure the desired fraction of power handled by each multimodule group.

This paper is structured as follows: Section 2 presents the hybrid input-series input-parallel output-series output-parallel (ISIP-OSOP) multimodule power converter and the generalized small-signal modeling. Section 3 presents a 200 kW hybrid eight-module ISOP converter. In Section 3, the small-signal model of the presented converter is derived using the analysis provided in Section 2. Section 4 presents the number of modules needed to achieve the required ratings for both; conventional multimodule DC-DC converters and hybrid multimodule DC-DC converters. In addition, the power loss analysis of the conventional and hybrid multimodule converters is provided. Section 5 discusses the control strategy for the proposed hybrid ISOP multimodule DC-DC converters. Section 6 discusses the MatLab/Simulink model and the simulation results. Finally, Section 7 summarizes the key findings of this paper.

2. Generalized Small-Signal Analysis for Dual Series/Parallel Input-Output (ISIP-OSOP) Hybrid Multimodule Converters

In this section, the generalized small-signal modeling for dual series/parallel ISIP-OSOP hybrid multimodule DC-DC converter is introduced.

2.1. Hybrid ISIP-OSOP Generic DC-DC Converter Circuit Configuration

The hybrid ISIP-OSOP generic DC-DC converter configuration, shown in Figure 3, consists of n modules that are connected in series and/or parallel at the input side and in series and/or parallel at the output side. These n modules consist of two different multimodule groups. The primary group consists of L isolated DC-DC converters that are in charge of a high fraction of the total required power operating relatively at a low switching frequency. The secondary group consists of M isolated DC-DC converters that are designed for a small fraction of the total power operating relatively at a high switching frequency. Accordingly, it can be said that the summation of L and M power converters results in a total of n DAB units. To differentiate between the primary and secondary multimodule DC-DC converter in the small signal analysis, the set of equations representing the primary group is black colored while the set of equations representing the secondary group is blue colored. In addition, the red colored symbols reflect the parameters defined for the input side, while the blue colored symbols reflects the parameters defined for the output side, as presented in the following.

By ensuring input current sharing (ICS) and input voltage sharing (IVS) for the primary group, the input current for each module in the primary group is reduced to $\frac{I_{inL}}{\alpha_{L1}}$, and the input voltage for each module in the primary group is reduced to $\frac{V_{inL}}{\beta_{L1}}$. However, by ensuring ICS and IVS for the secondary group, the input current for each module in the secondary group is reduced to $\frac{I_{inM}}{\alpha_{M1}}$, and the input voltage for each module in the secondary group is reduced to $\frac{V_{inM}}{\beta_{M1}}$ group is reduced to $\frac{V_{inM}}{\beta_{M1}}$, in which, I_{inL} and V_{inL} are the input current and the input voltage for the primary group that consists of L number of modules, respectively. I_{inM} and V_{inM} are the input current and the input voltage for the secondary group that consists of M number of modules, respectively. α_{M1} represents the number of modules connected in parallel in the secondary group at the input side. β_{M1} represents the number of modules connected in series the secondary group at the input side.

Similarly, by ensuring output current sharing (OCS) and output voltage sharing (OVS) for the primary group, the output current per module in the primary group is $\frac{I_{oL}}{a_{L1}}$, and the output voltage per module in the primary module is reduced to $\frac{V_{oL}}{b_{L1}}$. However, by ensuring OCS and OVS for the secondary group, the output current per module is $\frac{I_{oM}}{a_{M1}}$, and the output voltage for each module in the secondary group is reduced to $\frac{V_{oM}}{b_{M1}}$. In which, I_{oL} and V_{oL} are the output current and the output voltage for the primary group that consists of L number of modules, respectively. I_{oM} and V_{oM} are the output current and the output voltage for the secondary group that consists of M number of modules, respectively. a_{M1} represents the number of modules connected in parallel in the secondary group at the output side. b_{M1} represents the number of modules connected in series in the secondary group at the output side.

The L isolated modules are responsible for delivering a portion of K_L of the total required power, while the M isolated modules are responsible for delivering a portion of K_M of the total required power, where $K_L + K_M = 1$ pu. The input voltages, input currents, output currents, and output voltages are represented in terms of the total input voltage, total input current, total output voltage, and total output current would result in Table 1.

Table 1. Individual module system parameters representation in terms of the overall system ratings.

Parameters	Representation	Value
	Primary group	
Input current	$\frac{\alpha_{L2}\ I_{in}}{\alpha_{L1}}$	$\alpha_{L2} = K_L$ if the two groups are connected in parallel at the input side, otherwise $\alpha_{L2} = 1$
Input voltage	$\frac{\beta_{L2}\ V_{in}}{\beta_{L1}}$	$\beta_{L2} = K_L$ if the two groups are connected in series at the input side, otherwise $\beta_{L2} = 1$
Output current	$\frac{a_{L2} I_o}{a_{L1}}$	$a_{L2} = K_L$ if the two groups are connected in parallel at the output side, otherwise $a_{L2} = 1$
Output voltage	$\frac{b_{L2} V_o}{b_{L1}}$	$b_{L2} = K_L$ if the two groups are connected in series at the output side, otherwise $b_{L2} = 1$
	Secondary group	
Input current	$\frac{\alpha_{M2}\ I_{in}}{\alpha_{M1}}$	$\alpha_{M2} = K_M$ if the two groups are connected in parallel at the input side, otherwise $\alpha_{M2} = 1$
Input voltage	$\frac{\beta_{M2}\ V_{in}}{\beta_{M1}}$	$\beta_{M2} = K_M$ if the two groups are connected in series at the input side, otherwise $\beta_{M2} = 1$
Output current	$\frac{a_{M2} I_{oL}}{a_{M1}}$	$a_{M2} = K_M$ if the two groups are connected in parallel at the output side, otherwise $a_{M2} = 1$
Output voltage	$\frac{b_{M2} V_o}{b_{M1}}$	$b_{M2} = K_M$ if the two groups are connected in series at the output side, otherwise $b_{M2} = 1$

2.2. Hybrid ISIP-OSOP DC-DC Converter Small-Signal Modeling

Using the model in [36], and expanding the study of the multimodule DC-DC converters in [37–41], the small-signal model for the hybrid multimodule ISIP-OSOP converter shown in Figure 4 is derived. Since each group is responsible for delivering a particular portion of the overall required power, where this portion is defined according to the overall system power ratings. Accordingly, it is worth mentioning that the equivalent load resistance seen by each group of multimodule converters is different.

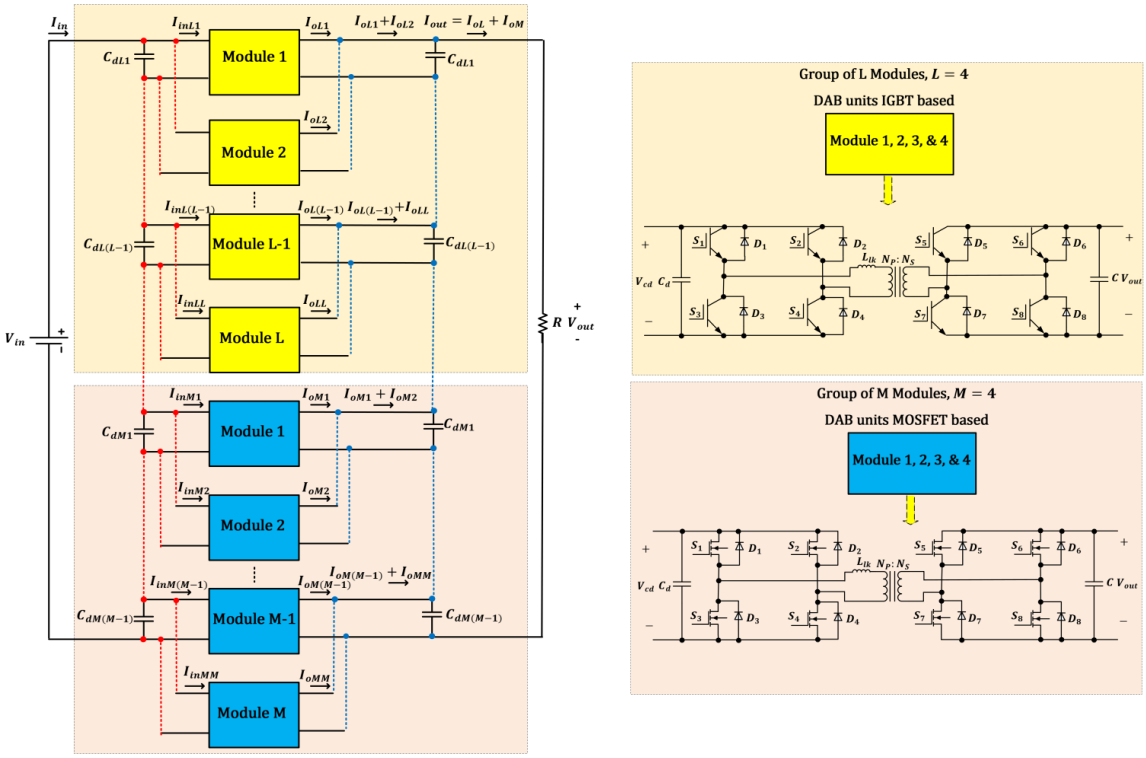

Figure 3. Generalized hybrid multimodule DC-DC converter configuration.

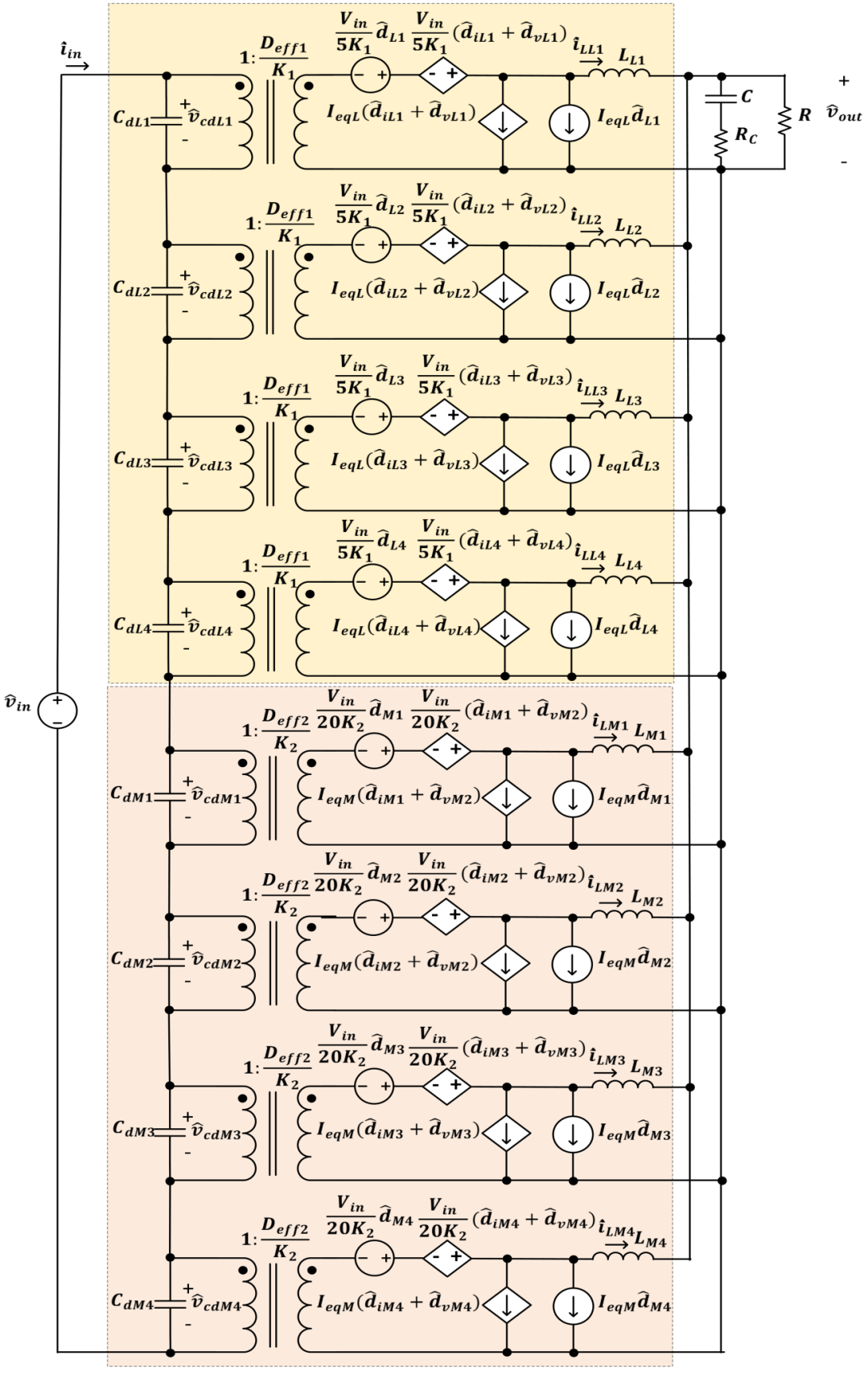

Figure 4. Small signal model for the generalized hybrid ISIP-OSOP multimodule DC-DC converter.

Since the input current and input voltage for each module in the primary group are $\frac{\alpha_{L2}\, I_{in}}{\alpha_{L1}}$ and $\frac{\beta_{L2}\, V_{in}}{\beta_{L1}}$, respectively, and the output current and output voltage for each module in the primary group are $\frac{a_{L2} I_o}{a_{L1}}$ and $\frac{b_{L2} V_o}{b_{L1}}$, respectively. Therefore, the load resistance for each module in the primary group is $\frac{a_{L1} b_{L2}}{a_{L2} b_{L1}} R$. Accordingly, $\hat{d}_{ijL}$, $\hat{d}_{vLj}$ which are the effect of changing the filter inductor current and the effect of changing the input voltage on the duty cycle modulation for the primary group and I_{eqL} presented in Figure 4 can be defined as:

$$\hat{d}_{iLj} = -\frac{4\beta_{L1} L_{lkL} f_{sL}}{\beta_{L2}\, K_1 V_{in}} \hat{i}_{LLj},\ j = 1, 2, \ldots, L \tag{1}$$

Equation (1) can be written as:

$$\hat{d}_{iLj} = -\frac{\beta_{L1} K_1 R_{dL}}{\beta_{L2}\, V_{in}} \hat{i}_{LLj},\ j = 1, 2, \ldots, L \tag{2}$$

where $R_{dL} = \frac{4 L_{lkL} f_{sL}}{K_1^2}$.

$$\hat{d}_{vLj} = \frac{4 a_{L2} b_{L1} \beta_{L1} L_{lkL} f_{sL} D_{eff1}}{a_{L1} b_{L2} \beta_{L2}\, K_1^2 R V_{in}} \hat{v}_{cdLj},\ j = 1, 2, \ldots, L \tag{3}$$

Equation (3) can be written as:

$$\hat{d}_{vLj} = \frac{a_{L2} b_{L1} \beta_{L1} R_{dL} D_{eff1}}{a_{L1} b_{L2} \beta_{L2}\, R V_{in}} \hat{v}_{cdLj},\ j = 1, 2, \ldots, L \tag{4}$$

$$I_{eqL} = \frac{a_{L2} b_{L1} \beta_{L2} V_{in}}{a_{L1} b_{L2} \beta_{L1}\, K_1 R} \tag{5}$$

Since the input current and input voltage for each module in the primary group is $\frac{\alpha_{M2}\, I_{in}}{\alpha_{M1}}$ and $\frac{\beta_{M2}\, V_{in}}{\beta_{M1}}$, respectively, and the output current and output voltage for each module in the primary group is $\frac{a_{M2} I_o}{a_{M1}}$ and $\frac{b_{M2} V_o}{b_{M1}}$, respectively. Therefore, the load resistance for each module in the primary group is $\frac{a_{M1} b_{M2}}{a_{M2} b_{M1}} R$. Accordingly, $\hat{d}_{ijM}$, $\hat{d}_{vMj}$ which are the effect of changing the filter inductor current and the effect of changing the input voltage on the duty cycle modulation for the primary group and I_{eqM} presented in Figure 4 can be defined as:

$$\hat{d}_{iMj} = -\frac{4\beta_{L1} L_{lkM} f_{sM}}{\beta_{L2}\, K_2 V_{in}} \hat{i}_{LMj},\ j = 1,2,\ldots, M \tag{6}$$

Equation (6) can be written as:

$$\hat{d}_{iMj} = -\frac{\beta_{L1} K_2 R_{dM}}{\beta_{L2}\, V_{in}} \hat{i}_{LMj},\ j = 1,2,\ldots,M \tag{7}$$

where; $R_{dM} = \frac{4 L_{lkM} f_{sM}}{K_2{}^2}$.

$$\hat{d}_{vMj} = \frac{4 a_{L2} b_{L1} \beta_{L1} L_{lkM} f_{sM} D_{eff2}}{a_{L1} b_{L2} \beta_{L2}\, K_2{}^2 R V_{in}} \hat{v}_{cdMj},\ j = 1,2,\ldots, M \tag{8}$$

Equation (8) can be written as:

$$\hat{d}_{vMj} = \frac{a_{L2} b_{L1} \beta_{L1} R_{dM} D_{eff2}}{a_{L1} b_{L2} \beta_{L2}\, R V_{in}} \hat{v}_{cdMj},\ j = 1,2,\ldots, M \tag{9}$$

$$I_{eqM} = \frac{a_{L2} b_{L1} \boldsymbol{\beta}_{L2} V_{in}}{a_{L1} b_{L2} \boldsymbol{\beta}_{L1} K_2 R} \tag{10}$$

Based on the feature of modularity and to simplify the analysis, it is assumed that all modules in the primary group and all modules in the secondary group have an equal effective duty cycle, transformer turns ratio, capacitor, and inductor values. Accordingly, $K_{L1} = K_{L2} = \cdots = K_{LL} = K_1$, $K_{M1} = K_{M2} = \cdots = K_{MM} = K_2$ $C_{L1} = C_{L2} = \cdots = C_{LL} = C_L$, $C_{M1} = C_{M2} = \cdots = C_{MM} = C_M$, $C_{dL1} = C_{dL2} = \cdots = C_{dLL} = C_{dL}$, $C_{dM1} = C_{dM2} = \cdots = C_{dMM} = C_{dM}$, $L_{L1} = L_{L2} = \cdots = L_{LL} = L_L$ and $L_{M1} = L_{M2} = \cdots = L_{MM} = L_M$. In addition, it is also assumed that all modules in the primary group share the same input voltage and that all modules in the secondary group share the same input voltage. Accordingly, the DC input voltage of each module in the primary group is $\frac{\beta_{L2} V_{in}}{\beta_{L1}}$ and the DC input voltage of each module in the secondary group is $\frac{\beta_{M2} V_{in}}{\beta_{M1}}$. Although each module has a different duty cycle perturbation, it is assumed that all the DAB units have an equal normalized time shift. Besides, the ESR of the output capacitance is considered in this model. However, the ESR can be neglected compared to the load.

The following equations are obtained from Figure 4:

$$\begin{cases} \frac{D_{eff1}}{K_1}\hat{v}_{cdL1} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_1}\left(\hat{d}_{iL1} + \hat{d}_{vL1} + \hat{d}_{L1}\right) = sL_L\hat{i}_{LL1} + \hat{v}_{outL1} \\ \frac{D_{eff1}}{K_1}\hat{v}_{cdL2} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_1}\left(\hat{d}_{iL2} + \hat{d}_{vL2} + \hat{d}_{L2}\right) = sL_L\hat{i}_{LL2} + \hat{v}_{outL2} \\ \vdots \\ \frac{D_{eff1}}{K_1}\hat{v}_{cdLL} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_1}\left(\hat{d}_{iLL} + \hat{d}_{vLL} + \hat{d}_{LL}\right) = sL_L\hat{i}_{LLL} + \hat{v}_{outLL} \\ \frac{D_{eff2}}{K_2}\hat{v}_{cdM1} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_2}(\hat{d}_{iM1} + \hat{d}_{vM1} + \hat{d}_{M1}) = sL_M\hat{i}_{LM1} + \hat{v}_{outM1} \\ \frac{D_{eff2}}{K_2}\hat{v}_{cdM2} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_2}(\hat{d}_{iM2} + \hat{d}_{vM2} + \hat{d}_{M2}) = sL_M\hat{i}_{LM2} + \hat{v}_{outM2} \\ \vdots \\ \frac{D_{eff2}}{K_2}\hat{v}_{cdMM} + \frac{\beta_{L2} V_{in}}{\beta_{L1} K_2}(\hat{d}_{iMM} + \hat{d}_{vMM} + \hat{d}_{MM}) = sL_M\hat{i}_{LMM} + \hat{v}_{outMM} \end{cases} \tag{11}$$

$$\begin{cases} \hat{i}_{LL11} + \hat{i}_{LL21} + \cdots + \hat{i}_{LLa_{L1}1} = \frac{sC_L}{sR_{cL}C_L+1}\hat{v}_{outL1} + \frac{\hat{v}_{outL}}{R} \\ \hat{i}_{LL12} + \hat{i}_{LL22} + \cdots + \hat{i}_{LLa_{L1}2} = \frac{sC_L}{sR_{cL}C_L+1}\hat{v}_{outL2} + \frac{\hat{v}_{outL}}{R} \\ \vdots \\ \hat{i}_{LL1b_{L1}} + \hat{i}_{LL2b_{L1}} + \cdots + \hat{i}_{LLa_{L1}b_{L1}} = \frac{sC_L}{sR_{cL}C_L+1}\hat{v}_{outLL} + \frac{\hat{v}_{outL}}{R} \\ \hat{i}_{LM11} + \hat{i}_{LM21} + \cdots + \hat{i}_{LMa_{M1}1} = \frac{sC_M}{sR_{cM}C_M+1}\hat{v}_{outM1} + \frac{\hat{v}_{outM}}{R} \\ \hat{i}_{LM12} + \hat{i}_{LM22} + \cdots + \hat{i}_{LMa_{M1}2} = \frac{sC_M}{sR_{cM}C_M+1}\hat{v}_{outM2} + \frac{\hat{v}_{outM}}{R} \\ \vdots \\ \hat{i}_{LM1b_{L1}} + \hat{i}_{LM2b_{L1}} + \cdots + \hat{i}_{LMa_{M1}b_{L1}} = \frac{sC_M}{sR_{cM}C_M+1}\hat{v}_{outMM} + \frac{\hat{v}_{outM}}{R} \end{cases} \tag{12}$$

Adding equations representing the primary multimodule group in (12):

$$\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij} = \frac{sC_L}{sR_{cL}C_L+1}\hat{v}_{outL} + \frac{b_{L1}\hat{v}_{outL}}{R} \tag{13}$$

Equation (13) can be written as:

$$\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij} = \hat{v}_{outL}\left(\frac{sRC_L + sb_{L1}R_{cL}C_L + b_{L1}}{R(1+sR_{cL}C_L)}\right) \tag{14}$$

Adding equations representing the secondary multimodule group in (12):

$$\sum_{i=1}^{\boldsymbol{a_{M1}}}\sum_{j=1}^{\boldsymbol{b_{M1}}}\hat{\imath}_{LMij} = \hat{v}_{outM}\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right) \tag{15}$$

Equation (15) can be written as:

$$\sum_{i=1}^{\boldsymbol{a_{M1}}}\sum_{j=1}^{\boldsymbol{b_{M1}}}\hat{\imath}_{LMij} = \hat{v}_{outM}\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right) \tag{16}$$

Defining the summation terms of the module's input and output voltage appearing after summing up equations representing the primary multimodule group in (11):

$$\sum_{j=1}^{L}\hat{v}_{cdLj} = \gamma_L\hat{v}_{inL} = \gamma_L\beta_{L2}\hat{v}_{in} \tag{17}$$

where:

- $\gamma_L = 1$, if all the modules in the primary group at the input side are connected in series.
- $\gamma_L = \alpha_{L1}$, if all the modules in the primary group at the input side are connected in parallel or connected in both series and parallel.

$$\sum_{j=1}^{L}\hat{v}_{outLj} = c_L\hat{v}_{outL} = c_Lb_{L2}\hat{v}_{out} \tag{18}$$

where:

- $c_L = 1$, if all the modules in the primary group at the output side are connected in series.
- $c_L = a_{L1}$, if all the modules in the primary group at the output side are connected in parallel or connected in both series and parallel.

Defining the summation terms of the module's input and output voltage appearing after summing up equations representing the secondary multimodule group in (11):

$$\sum_{j=1}^{M}\hat{v}_{cdMj} = \boldsymbol{\gamma_M}\hat{v}_{inM} = \boldsymbol{\gamma_M\beta_{M2}}\hat{v}_{in} \tag{19}$$

where:

- $\gamma_M = 1$, if all the modules in the secondary group at the input side are connected in series.
- $\gamma_M = \alpha_{L1}$, if all the modules in the secondary group at the input side are connected in parallel or connected in both series and parallel.

$$\sum_{j=1}^{M}\hat{v}_{outMj} = \boldsymbol{c_M}\hat{v}_{outL} = \boldsymbol{c_Mb_{M2}}\hat{v}_{out} \tag{20}$$

where:

- $c_M = 1$, if all the modules in the secondary group at the output side are connected in series.

- $c_M = a_{M1}$, if all the modules in the secondary group at the output side are connected in parallel or connected in both series and parallel.

2.2.1. Control-to-Output Voltage Transfer Function

The relation between the output voltage and the duty cycle is obtained by performing two steps. The first step is by adding the L equations in (11) to obtain the relation between $\hat{v}_{outL}$ and $\hat{d}_{Lj}$, assuming $\hat{v}_{inL} = 0$, and $\hat{d}_{Lk} = 0$, where $k = 1, 2, \ldots, L$ and $k \neq j$, and substituting (2), (4), (14), (17) and (18). However, the second step is by adding the M equations in (11) to obtain the relation between $\hat{v}_{outM}$ and $\hat{d}_{Mj}$, assuming $\hat{v}_{inM} = 0$, and $\hat{d}_{Mk} = 0$, where $k = 1, 2, \ldots, L$ and $k \neq j$, and substituting (7), (9), (16), (19) and (20).

Adding the L equations in (11) would result in:

$$\frac{D_{eff1}}{K_1}\sum_{j=1}^{L}\hat{v}_{cdLj} + \frac{\beta_{L2}\,V_{in}}{\beta_{L1}\,K_1}\left(\sum_{j=1}^{L}\hat{d}_{iLj} + \sum_{j=1}^{L}\hat{d}_{vLj} + \sum_{j=1}^{L}\hat{d}_{Lj}\right) = sL_L\sum_{j=1}^{L}\hat{i}_{LLj} + \sum_{j=1}^{L}\hat{v}_{outLj} \tag{21}$$

Substituting (2), (4) and (14) would result in:

$$\begin{aligned}\frac{D_{eff1}}{K_1}\sum_{j=1}^{L}\hat{v}_{cdLj} + \frac{\beta_{L2}\,V_{in}}{\beta_{L1}\,K_1}&\left(\begin{array}{c} -\frac{\beta_{L1}K_1R_{dL}}{\beta_{L2}\,V_{in}}\hat{v}_{outL}\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)+ \\ \sum_{j=1}^{L}\frac{a_{L2}b_{L1}\beta_{L1}R_{dL}D_{eff1}}{a_{L1}b_{L2}\beta_{L2}\,RV_{in}}\hat{v}_{cdLj} + \hat{d}_{L1}\end{array}\right) \\ &= sL_L\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL} + \sum_{j=1}^{L}\hat{v}_{outLj}\end{aligned} \tag{22}$$

Substituting (17) and (18) in (22) results in:

$$\begin{aligned}\frac{D_{eff1}}{K_1}\gamma_L\hat{v}_{inL} + \frac{\beta_{L2}\,V_{in}}{\beta_{L1}\,K_1}&\left(\begin{array}{c} -\frac{\beta_{L1}K_1R_{dL}}{\beta_{L2}\,V_{in}}\hat{v}_{outL}\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)+ \\ \frac{a_{L2}b_{L1}\beta_{L1}R_{dL}D_{eff1}}{a_{L1}b_{L2}\beta_{L2}\,RV_{in}}\gamma_L\hat{v}_{inL} + \hat{d}_{L1}\end{array}\right) \\ &= sL_L\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL} + c_L\hat{v}_{outL}\end{aligned} \tag{23}$$

Simplifying (23) results in (24):

$$\begin{aligned}G_{vdL} &= \frac{\hat{v}_{outL}}{\hat{d}_{Lj}} \\ &= \frac{\frac{\beta_{L2}\,V_{in}}{\beta_{L1}\,K_1}(1+sR_{cL}C_L)}{s^2L_LC_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+s\left(\frac{b_{L1}L_L}{R}+R_{dL}C_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+c_LR_{cL}C_L\right)+\frac{b_{L1}R_{dL}}{R}+c_L}\end{aligned} \tag{24}$$

Performing the second step which is adding the M equations in (11) to obtain the relation between $\hat{v}_{outM}$ and $\hat{d}_{Mj}$, assuming $\hat{v}_{inM} = 0$, and $\hat{d}_{Mk} = 0$, where $k = 1, 2, \ldots, M$, and $k \neq j$, and substituting (7), (9), (16), (19) and (20) would result in:

Adding the M equations in (11) would result in:

$$\frac{D_{eff2}}{K_2}\sum_{j=1}^{M}\hat{v}_{cdMj} + \frac{\boldsymbol{\beta_{M2}}\,V_{in}}{\boldsymbol{\beta_{M1}}\,K_2}\left(\sum_{j=1}^{M}\hat{d}_{iMj} + \sum_{j=1}^{M}\hat{d}_{vMj} + \sum_{j=1}^{M}\hat{d}_{Mj}\right) = sL_M\sum_{j=1}^{M}\hat{i}_{LMj} + \sum_{j=1}^{M}\hat{v}_{outMj} \tag{25}$$

Substituting (7), (9) and (16) would result in:

$$\begin{aligned}\frac{D_{eff2}}{K_2}+\frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2}\Bigg(&-\frac{\boldsymbol{\beta_{M1}}K_2R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}}\hat{v}_{outM}\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\\&+\sum_{j=1}^{M}\frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\hat{v}_{cdMj}+\hat{d}_{M1}\Bigg)\\&=sL_M\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM}+\sum_{j=1}^{M}\hat{v}_{outMj}\end{aligned}\tag{26}$$

Substituting (19) and (20) results in:

$$\begin{aligned}\frac{D_{eff2}}{K_2}\boldsymbol{\gamma_M}\hat{v}_{inM}+\frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2}\Bigg(&-\frac{\boldsymbol{\beta_{M1}}K_2R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}}\hat{v}_{outM}\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\\&+\frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\boldsymbol{\gamma_M}\hat{v}_{inM}+\hat{d}_{M1}\Bigg)\\&=sL_M\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM}+\boldsymbol{c_M}\hat{v}_{outM}\end{aligned}\tag{27}$$

Simplifying (27) would result in (28).

$$\begin{aligned}G_{vdM}&=\frac{\hat{v}_{outM}}{\hat{d}_{Mj}}\\&=\frac{\frac{\beta_{M2}V_{in}}{\beta_{M1}K_2}(1+sR_{cM}C_M)}{s^2L_MC_M\left(1+\frac{b_{M1}R_{cM}}{R}\right)+s\left(\frac{b_{M1}L_M}{R}+R_{dM}C_M\left(1+\frac{b_{M1}R_{cM}}{R}\right)+c_MR_{cM}C_M\right)+\frac{b_{M1}R_{dM}}{R}+c_M}\end{aligned}\tag{28}$$

By adding G_{vdL} and G_{vdM} the control-to-output voltage transfer function can be found.

2.2.2. Control-to-Filter Inductor Current Transfer Function

The relation between the filter inductor current and the duty cycle is derived by performing two steps, where the first step considers the L modules in (11) while the second step considers the M modules in (11). The first step is by substituting $\hat{v}_{outL}$ in terms of $\hat{i}_{LLj}$ using (14) in (23) and assuming $\hat{v}_{inL}=0$, and $\hat{d}_{Lk}=0$, where $k=1,\ 2,\ldots,\ L$ and $k\neq j$. However, the second step is by substituting $\hat{v}_{outM}$ in terms of $\hat{i}_{LMj}$ using (16) in (27) and assuming $\hat{v}_{inM}=0$, and $\hat{d}_{Mk}=0$, where $k=1,\ 2,\ldots,\ M$ and $k\neq j$.

Substituting $\hat{v}_{outL}$ in terms of $\hat{i}_{LLj}$ using (14) in (23):

$$\begin{aligned}\frac{D_{eff1}}{K_1}\gamma_L\hat{v}_{inL}+\frac{\beta_{L2}V_{in}}{\beta_{L1}K_1}\Bigg(&-\frac{\beta_{L1}K_1R_{dL}}{\beta_{L2}V_{in}}\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij}+\\&\frac{a_{L2}b_{L1}\beta_{L1}R_{dL}D_{eff1}}{a_{L1}b_{L2}\beta_{L2}RV_{in}}\gamma_L\hat{v}_{inL}+\hat{d}_{L1}\Bigg)\\&=sL_L\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij}+c_L\left(\frac{R(1+sR_{cL}C_L)}{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}\right)\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij}\end{aligned}\tag{29}$$

$$\frac{\beta_{L2}V_{in}}{\beta_{L1}K_1}\hat{d}_{L1}-R_{dL}\sum_{j=1}^{L}\hat{i}_{LLj}=sL_L\sum_{j=1}^{L}\hat{i}_{LLj}+c_L\left(\frac{R(1+sR_{cL}C_L)}{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}\right)\sum_{j=1}^{L}\hat{i}_{LLj}\tag{30}$$

Simplifying (30) would result in (31).

$$G_{idL} = \frac{\sum_{j=1}^{L} \hat{i}_{LLj}}{\hat{d}_{Lj}} = \frac{\frac{\beta_{L2}}{\beta_{L1}} \frac{V_{in}}{K_1} (sRC_L + sb_{L1}R_{cL}C_L + b_{L1})}{R\left(s^2 L_L C_L \left(1 + \frac{b_{L1}R_{cL}}{R}\right) + s\left(\frac{b_{L1}L_L}{R} + R_{dL}C_L\left(1 + \frac{b_{L1}R_{cL}}{R}\right) + c_L R_{cL} C_L\right) + \frac{b_{L1}R_{dL}}{R} + c_L\right)} \quad (31)$$

Performing the second step which is substituting $\hat{v}_{outM}$ in terms of $\hat{i}_{LMj}$ using (16) in (27) and assuming $\hat{v}_{inM} = 0$, and $\hat{d}_{Mk} = 0$, where $k = 1, 2, \ldots, M$ and $k \neq j$ would result in:

$$\frac{D_{eff2}}{K_2}\boldsymbol{\gamma_M}\hat{v}_{inM} + \frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2}\left(\begin{array}{c} -\frac{\boldsymbol{\beta_{M1}}K_2 R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}} \sum_{i=1}^{\boldsymbol{a_{M1}}}\sum_{j=1}^{\boldsymbol{b_{M1}}} \hat{i}_{LMij} + \\ \frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\boldsymbol{\gamma_M}\hat{v}_{inM} + \hat{d}_{M1} \end{array}\right) = sL_M \sum_{i=1}^{\boldsymbol{a_{M1}}}\sum_{j=1}^{\boldsymbol{b_{M1}}} \hat{i}_{LMij} + \boldsymbol{c_M}\left(\frac{R(1 + sR_{cM}C_M)}{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}\right)\sum_{i=1}^{\boldsymbol{a_{M1}}}\sum_{j=1}^{\boldsymbol{b_{M1}}} \hat{i}_{LMij} \quad (32)$$

$$\frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2}\hat{d}_{M1} - R_{dM}\sum_{j=1}^{M}\hat{i}_{LMj} = sL_M\sum_{j=1}^{M}\hat{i}_{LMj} + \boldsymbol{c_M}\left(\frac{R(1 + sR_{cM}C_M)}{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}\right)\sum_{j=1}^{M}\hat{i}_{LMj} \quad (33)$$

Simplifying (33) would result in (34). By adding G_{idL} and G_{idM}, the control-to-filter inductor current transfer function can be found.

$$G_{idM} = \frac{\sum_{j=1}^{M}\hat{i}_{LMj}}{\hat{d}_{Mj}} = \frac{\frac{\beta_{M2}}{\beta_{M1}}\frac{V_{in}}{K_2}(sRC_M + sb_{M1}R_{cM}C_M + b_{M1})}{R\left(s^2 L_M C_M\left(1 + \frac{b_{M1}R_{cM}}{R}\right) + s\left(\frac{b_{M1}L_M}{R} + R_{dM}C_M\left(1 + \frac{b_{M1}R_{cM}}{R}\right) + c_M R_{cM} C_M\right) + \frac{b_{M1}R_{dM}}{R} + c_M\right)} \quad (34)$$

By adding G_{idL} and G_{idM} the control-to-output filter inductor current transfer function can be found.

2.2.3. Output Impedance

The generalized converter output impedance for the hybrid ISIP-OSOP multimodule DC-DC converter can be found by considering two groups of equations. The primary group is the L number of KCL equations presented in (12). However, the secondary group is the M number of KCL equations presented in (12).

To find the generalized converter output impedance, the KCL equation in (12) can be rewritten as follows:

$$\begin{cases} \hat{i}_{LL11}+\hat{i}_{LL21}+\cdots+\hat{i}_{LLa_{L1}1}+\hat{i}_{outL}=g_L\hat{v}_{outL1}+\frac{\hat{v}_{outL}}{R} \\ \hat{i}_{LL12}+\hat{i}_{LL22}+\cdots+\hat{i}_{LLa_{L1}2}+\hat{i}_{outL}=g_L\hat{v}_{outL2}+\frac{\hat{v}_{outL}}{R} \\ \vdots \\ \hat{i}_{LL1b_{L1}}+\hat{i}_{LL2b_{L1}}+\cdots+\hat{i}_{LLa_{L1}b_{L1}}+\hat{i}_{outL}=g_L\hat{v}_{outLL}+\frac{\hat{v}_{outL}}{R} \\ \hat{i}_{LM11}+\hat{i}_{LM21}+\cdots+\hat{i}_{LMa_{M1}1}+\hat{i}_{outM}=g_M\hat{v}_{outM1}+\frac{\hat{v}_{outM}}{R} \\ \hat{i}_{LM12}+\hat{i}_{LM22}+\cdots+\hat{i}_{LMa_{M1}2}+\hat{i}_{outM}=g_M\hat{v}_{outM2}+\frac{\hat{v}_{outM}}{R} \\ \vdots \\ \hat{i}_{LM1b_{L1}}+\hat{i}_{LM2b_{L1}}+\cdots+\hat{i}_{LMa_{M1}b_{L1}}+\hat{i}_{outM}=g_M\hat{v}_{outMM}+\frac{\hat{v}_{outM}}{R} \end{cases} \tag{35}$$

where; $g_L=\frac{sC_L}{sR_{cL}C_L+1}$ and $g_M=\frac{sC_M}{sR_{cM}C_M+1}$.

Accordingly, the KCL equation in (14) can be modified as follows:

$$\sum_{i=1}^{a_{L1}}\sum_{j=1}^{b_{L1}}\hat{i}_{LLij}+\hat{i}_{outL}=\hat{v}_{outL}\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right) \tag{36}$$

The relationship between the output voltage and the output current for the L modules is obtained by adding the L equations in (11), assuming $\hat{v}_{inL}=0$, and $\hat{d}_{Lj}=0,\ j=1,2,\ldots,L$, and substituting (2), (4), (17), (18) and (36).

$$\begin{aligned} &\frac{D_{eff1}}{K_1}\gamma_L\hat{v}_{inL}+\frac{\beta_{L2}}{\beta_{L1}}\frac{V_{in}}{K_1}\left(\begin{array}{l} -\frac{\beta_{L1}}{\beta_{L2}}\frac{K_1R_{dL}}{V_{in}}\left(\hat{v}_{outL}\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)-\hat{i}_{outL}\right)+ \\ \frac{a_{L2}b_{L1}\beta_{L1}}{a_{L1}b_{L2}\beta_{L2}}\frac{R_{dL}D_{eff1}}{RV_{in}}\gamma_L\hat{v}_{inL}+\hat{d}_{L1} \end{array}\right) \\ &\quad=sL_L\left(\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL}-\hat{i}_{outL}\right)+c_L\hat{v}_{outL} \end{aligned} \tag{37}$$

$$\begin{aligned} &-R_{dL}\left(\hat{v}_{outL}\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)-\hat{i}_{outL}\right) \\ &\quad=sL_L\left(\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL}-\hat{i}_{outL}\right)+c_L\hat{v}_{outL} \end{aligned} \tag{38}$$

Simplifying (38) would result in (39).

$$\begin{aligned} Z_{outL}&=\frac{\hat{v}_{outL}}{\hat{i}_{outL}} \\ &=\frac{b_{L1}(R_{dL}+sL_L)(1+sR_{cL}C_L)}{s^2L_LC_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+s\left(\frac{b_{L1}L_L}{R}+R_{dL}C_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+c_LR_{cL}C_L\right)+\frac{b_{L1}R_{dL}}{R}+c_L} \end{aligned} \tag{39}$$

Similarly, the KCL equation in (16) can be modified as follows:

$$\sum_{i=1}^{a_{M1}}\sum_{j=1}^{b_{M1}}\hat{i}_{LMij}+\hat{i}_{outM}=\hat{v}_{outM}\left(\frac{sRC_M+sb_{M1}R_{cM}C_M+b_{M1}}{R(1+sR_{cM}C_M)}\right) \tag{40}$$

The relationship between the output voltage and the output current for the M modules is derived by summing the M equations in (11), assuming $\hat{v}_{inM} = 0$, and $\hat{d}_{Mj} = 0$, $j = 1, 2, \ldots, M$, and substituting (7), (9), (19), (20) and (40).

$$\frac{D_{eff2}}{K_2}\boldsymbol{\gamma_M}\hat{v}_{inM} + \frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2} = \begin{pmatrix} -\frac{\boldsymbol{\beta_{M1}}K_2R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}}\left(\hat{v}_{outM}\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right) - \hat{\imath}_{outM}\right) + \\ \frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\boldsymbol{\gamma_M}\hat{v}_{inM} + \hat{d}_{M1} \end{pmatrix} \tag{41}$$

$$\begin{aligned} sL_M\left(\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM} - \hat{\imath}_{outM}\right) + \boldsymbol{c_M}\hat{v}_{outM} \\ - R_{dM}\left(\hat{v}_{outM}\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right) - \hat{\imath}_{outM}\right) \\ = sL_M\left(\left(\frac{sRC_M + s\boldsymbol{b_{M1}}R_{cM}C_M + \boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM} - \hat{\imath}_{outM}\right) + \boldsymbol{c_M}\hat{v}_{outM} \end{aligned} \tag{42}$$

Simplifying (42) would result in (43):

$$\begin{aligned} Z_{outM} &= \frac{\hat{v}_{outM}}{\hat{\imath}_{outM}} \\ &= \frac{b_{M1}(R_{dM} + sL_M)(1 + sR_{cM}C_M)}{s^2L_MC_M\left(1 + \frac{b_{M1}R_{cM}}{R}\right) + s\left(\frac{b_{M1}L_M}{R} + R_{dM}C_M\left(1 + \frac{b_{M1}R_{cM}}{R}\right) + c_MR_{cM}C_M\right) + \frac{b_{M1}R_{dM}}{R} + c_M} \end{aligned} \tag{43}$$

By adding Z_{outL} and Z_{outM}, the output impedance transfer function can be found.

2.2.4. Converter Gain

The generalized relationship between the output voltage and the input voltage of the hybrid ISIP-OSOP DC-DC converter can be found by performing two steps. The first step is adding the L number of KVL equations presented in (11) for the primary multimodule DC-DC converters, assuming $\hat{d}_{Lj} = 0$, $j = 1, 2, \ldots, L$, and substituting (2), (4), (14), (17) and (18) in the added equation. However, the second step is adding the M number of KVL equations presented in (11) for the secondary multimodule DC-DC converters, assuming $\hat{d}_{Mj}=0$, $j = 1, 2, \ldots, M$, and substituting (7), (9), (16), (19) and (20) in the added equation.

Adding the L number of KVL equations in (11), assuming $\hat{d}_{Lj} = 0$, $j = 1, 2, \ldots, L$, and substituting (2), (4) and (14) would result in:

$$\begin{aligned} \frac{D_{eff1}}{K_1}\sum_{j=1}^{L}\hat{v}_{cdLj} + \frac{\beta_{L2}V_{in}}{\beta_{L1}K_1}\begin{pmatrix} -\frac{\beta_{L1}K_1R_{dL}}{\beta_{L2}V_{in}}\hat{v}_{outL}\left(\frac{sRC_L + sb_{L1}R_{cL}C_L + b_{L1}}{R(1+sR_{cL}C_L)}\right) + \\ \sum_{j=1}^{L}\frac{a_{L2}b_{L1}\beta_{L1}R_{dL}D_{eff1}}{a_{L1}b_{L2}\beta_{L2}RV_{in}}\hat{v}_{cdLj} \end{pmatrix} \\ = sL_L\left(\frac{sRC_L + sb_{L1}R_{cL}C_L + b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL} + \sum_{j=1}^{L}\hat{v}_{outLj} \end{aligned} \tag{44}$$

Substituting (17) and (18) in (44) would give:

$$\begin{aligned}\frac{D_{eff1}}{K_1}\gamma_L\left(1+\frac{a_{L2}b_{L1}R_{dL}}{a_{L1}b_{L2}R}\right)\hat{v}_{inL} \\ =(sL_L+R_{dL})\left(\left(\frac{sRC_L+sb_{L1}R_{cL}C_L+b_{L1}}{R(1+sR_{cL}C_L)}\right)\hat{v}_{outL}\right)+c_L\hat{v}_{outL}\end{aligned} \tag{45}$$

Simplifying (45) would result in (46):

$$\begin{aligned}G_{vgL}&=\frac{\hat{v}_{outL}}{\hat{v}_{inL}} \\ &=\frac{\frac{D_{eff1}}{K_1}\gamma_L\left(1+\frac{a_{L2}b_{L1}R_{dL}}{a_{L1}b_{L2}R}\right)(1+sR_{cL}C_L)}{s^2L_LC_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+s\left(\frac{b_{L1}L_L}{R}+R_{dL}C_L\left(1+\frac{b_{L1}R_{cL}}{R}\right)+c_LC_L\right)+\frac{b_{L1}R_{dL}}{R}+c_L}\end{aligned} \tag{46}$$

Similarly, Adding the M number of KVL equations in (11), assuming $\hat{d}_{Mj}=0$, $j=1,2,\ldots,M$, and substituting (7), (9) and (16) would result in:

$$\begin{aligned}&\frac{D_{eff2}}{K_2}\sum_{j=1}^{M}\hat{v}_{cdMj}+\frac{\boldsymbol{\beta_{M2}}V_{in}}{\boldsymbol{\beta_{M1}}K_2}\left(\begin{array}{c}-\frac{\boldsymbol{\beta_{M1}}K_2R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}}\hat{v}_{outM}\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)+\\ \sum_{j=1}^{M}\frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\hat{v}_{cdMj}+\hat{d}_{M1}\end{array}\right)\\ &=sL_M\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM}+\sum_{j=1}^{M}\hat{v}_{outMj}\end{aligned} \tag{47}$$

Substituting (19) and (20) in (47) would give:

$$\begin{aligned}&\frac{D_{eff2}}{K_2}\boldsymbol{\gamma_M}\left(1+\frac{\boldsymbol{a_{M2}b_{M1}}R_{dM}}{\boldsymbol{a_{M1}b_{M2}}R}\right)\hat{v}_{inM}\\ &+\boldsymbol{c_M}\hat{v}_{outM}\left(\begin{array}{c}-\frac{\boldsymbol{\beta_{M1}}K_2R_{dM}}{\boldsymbol{\beta_{M2}}V_{in}}\hat{v}_{outM}\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)+\\ \sum_{j=1}^{M}\frac{\boldsymbol{a_{M2}b_{M1}\beta_{M1}}R_{dM}D_{eff2}}{\boldsymbol{a_{M1}b_{M2}\beta_{M2}}RV_{in}}\hat{v}_{cdMj}+\hat{d}_{M1}\end{array}\right)\\ &=sL_M\left(\frac{sRC_M+s\boldsymbol{b_{M1}}R_{cM}C_M+\boldsymbol{b_{M1}}}{R(1+sR_{cM}C_M)}\right)\hat{v}_{outM}+\sum_{j=1}^{M}\hat{v}_{outMj}\end{aligned} \tag{48}$$

Simplifying (48) would result in (49):

$$\begin{aligned}G_{vgM}&=\frac{\hat{v}_{outM}}{\hat{v}_{inM}}\\ &=\frac{\frac{D_{eff2}}{K_2}\gamma_M\left(1+\frac{a_{M2}b_{M1}R_{dM}}{a_{M1}b_{M2}R}\right)(1+sR_{cM}C_M)}{s^2L_MC_M\left(1+\frac{b_{M1}R_{dM}}{R}\right)+s\left(\frac{b_{M1}L_M}{R}+R_{dM}C_M\left(1+\frac{b_{M1}R_{cM}}{R}\right)+c_MC_M\right)+\frac{b_{M1}R_{dM}}{R}+c_M}\end{aligned} \tag{49}$$

By adding G_{vgL} and G_{vgM}, the output impedance transfer function can be found.

3. Hybrid Input-Series Output-Parallel (ISOP) Multimodule DC-DC Converter

In this section, the hybrid ISOP multimodule power converter circuit diagram, as well as the hybrid ISOP multimodule converter small-signal analysis, are discussed. The analysis carried out in this section is not limited to unidirectional power flow and can be applied for bidirectional power flow.

The generalized small-signal modeling presented in Section 2 is used to derive the small-signal model for the eight-module hybrid ISOP power converter.

3.1. ISOP Circuit Diagram

The conventional ISOP converter shown in Figure 5a consists of multiple DAB units that are connected in series and in parallel at the input and the output sides, respectively, where all the modules are assumed identical. However, the concept of the hybrid ISOP power converter shown in Figure 5b is dividing conventional ISOP multimodule DC-DC converters into two groups. The primary group consists of identical ISOP DC-DC converters and is responsible for delivering a large portion of the total required power with lower switching frequency. This is shown in Figure 5c. However, the secondary group consists of another identical ISOP multimodule DC-DC converters. It is responsible for delivering the remaining power with higher switching frequency. This is shown in Figure 5d. This would result in two groups of multimodule converters operating at a different switching frequency, and utilizing different leakage inductance, transformers, filter inductors, and capacitors.

In this paper, the EV UFC specifications are assumed to deliver a total power of 200 kW using a battery voltage of 400 V, and assuming a grid voltage of 10 kV. It is assumed that the primary group handles 80% of the total battery charging power, while the secondary group handles 20% of the total battery charging power. Therefore, the primary group is responsible for delivering 160 kW, which $\frac{4}{5}$ of the total required power. The primary group is assumed to operate at switching frequency f_{sL} of 10 kHz. However, the secondary group is responsible for delivering the remaining 40 kW, which is $\frac{1}{5}$ of the total required power. The secondary group is assumed to operate at switching frequency of f_{sM} 100 kHz. Accordingly, the input voltage of the primary group V_{inL} is 8 kV, which is $\frac{4}{5}$ of the total input voltage V_{in}, while the input voltage of the secondary group V_{inM} is 2 kV, which is $\frac{1}{5}$ of the total input voltage V_{in}. Similarly, the output current of the primary group I_{oL} is 400 A, which is $\frac{4}{5}$ of the total output current I_{out}, while the output current of the secondary group I_{oM} is 100 A, which is $\frac{1}{5}$ of the total output current I_{out}. It is essential to mention that the portions $\frac{4}{5}$ and $\frac{1}{5}$ are denoted as K_L and K_M, respectively.

By ensuring equal IVS for the primary group and secondary group, the input voltage per module in the primary group is reduced to $\frac{V_{inL}}{4}$, while the input voltage per module in the secondary group is $\frac{V_{inM}}{4}$. Besides, by ensuring equal OCS for the primary and secondary group, the output current of each module in the primary group is reduced to $\frac{I_{oL}}{4}$, while the output current of each module in the secondary group is reduced to $\frac{I_{oM}}{4}$. In which, V_{inL}, V_{inM}, I_{oL}, and I_{oM} are the input voltages and output currents of the primary group and secondary group, respectively.

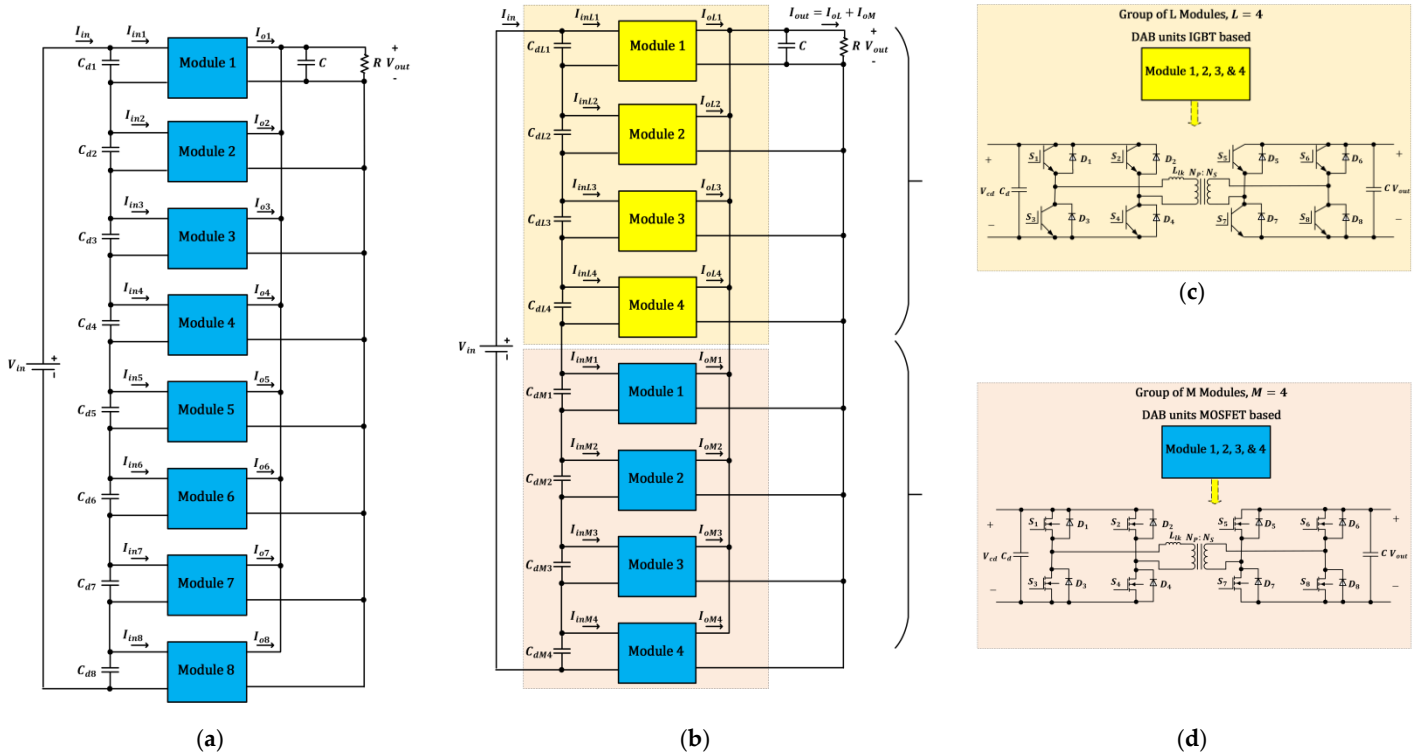

Figure 5. Eight-module ISOP multimodule DC-DC converter circuit diagram; (**a**) Conventional ISOP DC-DC Converter, (**b**) Hybrid ISOP DC-DC Converter, (**c**) DAB Converter based on IGBTs, (**d**) DAB Converter based on MOSFETs.

3.2. Hybrid ISOP Small Signal Analysis

The eight-module hybrid ISOP converter small-signal model shown in Figure 6 is derived using [36]. The generalized model derived in the previous section is used to derive the small-signal functions for the presented converter in Figure 6, as shown in Table 2. The presented transfer functions are used in the control strategy scheme presented in the power balancing section.

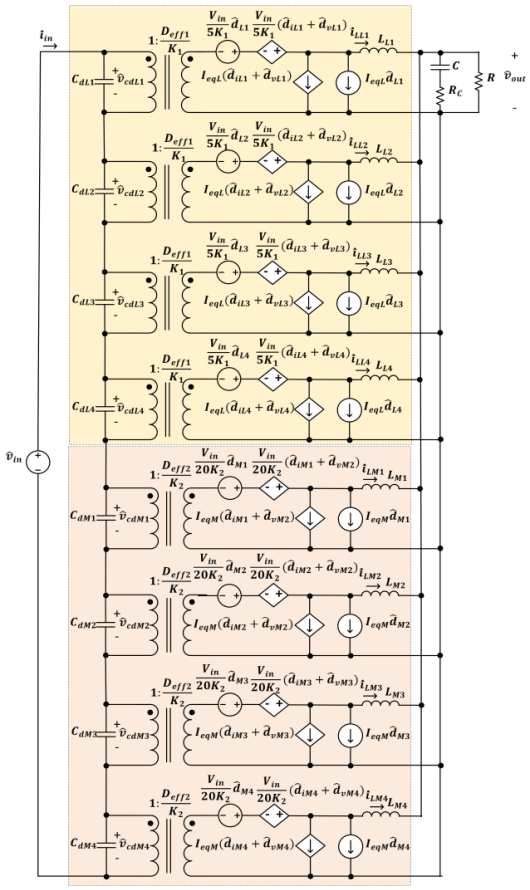

Figure 6. Hybrid ISOP DC-DC converter small-signal model for eight-modules.

Table 2. Generalized model verification with the eight-module hybrid ISOP DC-DC converter.

Transfer Functions for an Eight-Module Hybrid ISOP DC-DC Converter	
G_{vdL}	$\frac{\frac{V_{in}}{5K_1}}{s^2L_LC_L+s(\frac{L_L}{R}+R_{dL}C_L)+\frac{R_{dL}}{R}+4}$
G_{vdM}	$\frac{\frac{V_{in}}{20K_2}}{s^2L_MC_M+s(\frac{b_{M1}L_M}{R}+R_{dM}C_M)+\frac{R_{dM}}{R}+4}$
G_{idL}	$\frac{\frac{V_{in}}{5K_1}(sRC_L+1)}{R(s^2L_LC_L+s(\frac{L_L}{R}+R_{dL}C_L)+\frac{R_{dL}}{R}+4)}$
G_{idM}	$\frac{\frac{V_{in}}{20K_2}(sRC_M+b_{M1})}{R(s^2L_MC_M+s(\frac{L_M}{R}+R_{dM}C_M)+\frac{R_{dM}}{R}+4)}$
Z_{outL}	$\frac{(R_{dL}+sL_L)}{s^2L_LC_L+s(\frac{L_L}{R}+R_{dL}C_L)+\frac{R_{dL}}{R}+4}$
Z_{outM}	$\frac{(R_{dM}+sL_M)}{s^2L_MC_M+s(\frac{L_M}{R}+R_{dM}C_M)+\frac{R_{dM}}{R}+4}$
G_{vgL}	$\frac{\frac{D_{eff1}}{K_1}(1+\frac{R_{dL}}{R})}{s^2L_LC_L+s(\frac{L_L}{R}+R_{dL}C_L)+\frac{R_{dL}}{R}+4}$
G_{vgM}	$\frac{\frac{D_{eff2}}{K_2}(1+\frac{R_{dM}}{20R})}{s^2L_MC_M+s(\frac{L_M}{R}+R_{dM}C_M)+\frac{R_{dM}}{R}+4}$

4. Efficiency and Power Density Assessment of the Hybrid Multimodule DC-DC Converter

4.1. Efficiency Assessment

According to the presented ratings of the DAB units, the primary group utilizes power modules that are rated at 40 kW while the secondary group utilizes power modules that are rated at 10 kW. Accordingly, to realize the total desired power, relying only on the secondary group would result in a total number of 20 modules. However, relying on the primary group would result in a total number of five modules. Therefore, it can be said that the primary group results in a lower number of modules but has a limitation in terms of the switching frequency, while the secondary group results in a higher number of modules but with higher switching capability. On the other hand, applying the presented concept would result in a total number of eight modules. Table 3 presents a comparison between the three concepts in terms of the number of employed modules as well as power, voltage, and current ratings.

Table 3. System parameters for conventional and hybrid multimodule DC-DC converters.

Parameters	Multimodule Converter Relying on the Secondary Group	Multimodule Converter Relying on the Primary Group	Hybrid Multimodule Converter	
			Primary Group	Secondary Group
Total rated power	200 kW		160 kW	40 kW
Rated power per module	10 kW	40 kW	40 kW	10 kW
Overall input voltage	10 kV		8 kV	2 kV
Input voltage per module	500 V	2 kV	2 kV	500 V
Total input current	20 A			
Input current per module	20 A			
Overall output voltage	400 V			
Output voltage per module	400 V			
Total output current	500 A		400 A	100 A
Output current per module	25 A	100 A	100 A	25 A
Number of modules	20	5	Total of 8	
			4	4
Switching frequency	100 kHz	10 kHz	100 kHz	10 kHz

The converter efficiency can be presented as in (50):

$$\eta = \frac{P_{in} - P_t}{P_{in}} \tag{50}$$

where, P_t represents the total losses in the employed converter. The semiconductor devices' losses include two types; conduction and switching losses. It is worth mentioning that the following analysis is carried out considering MOSFETs for low power modules and IGBTs for high power modules. The semiconductor conduction losses of the primary and secondary sides can be obtained using the RMS switch currents $I_{S1,RMS}$ and $I_{S2,RMS}$, respectively with the primary and secondary drain-to-source resistances R_{DS1} and R_{DS2} in case of using MOSFETs. The RMS switch currents can be found from the RMS inductor current as follows [42]:

$$\begin{aligned} I_{S1,RMS} &= \frac{I_{L,RMS}}{\sqrt{2}} \\ I_{S2,RMS} &= n\frac{I_{L,RMS}}{\sqrt{2}} \end{aligned} \tag{51}$$

The conduction losses of the primary and secondary sides power switches can be represented as:

$$\begin{aligned} P_{S1,Cond.} &= 4(I_{S1,RMS})^2 R_{DS1} \\ P_{S2,Cond.} &= 4(I_{S2,RMS})^2 R_{DS2} \end{aligned} \tag{52}$$

In case of using IGBTs, the conduction losses can be obtained using the collector-to-emitter voltage $V_{CE(Sat)}$, average IGBT current I_{IGBT} and the duty cycle D. The conduction losses of the primary and secondary IGBTs can be represented as follows:

$$\begin{aligned} P_{S1,Cond.} &= 4V_{CE(Sat)}I_{IGBT1}D \\ P_{S2,Cond.} &= 4V_{CE(Sat)}I_{IGBT2}D \end{aligned} \tag{53}$$

The modulation schemes derived and presented in [29] allow the DAB power converter to operate under ZVS throughout the entire period. Hence the switching losses of the employed power devices can be neglected, assuming that the converter is operating under ZVS [42–45].

The aforementioned power losses are the conduction losses of only one DAB unit. However, the presented converter has a hybrid modular structure, meaning that Equations (52) and (53) are modified according to the configuration of the proposed multimodule converter to include the primary and secondary groups consisting of L and M isolated modules, respectively. Therefore, Equations (52) and (53) are modified to include the conduction losses in the IGBTs and MOSFETs for multiple numbers of DAB units, as shown in (54) and (55). The primary-side conduction losses of the hybrid multimodule converter include the conduction losses in the IGBTs and the conduction losses in the MOSFETs for L and M modules, respectively, and can be represented as follows:

$$P_{S1,Cond.} = 4LV_{CE(Sat)}I_{IGBT1}D + 4M(I_{S1,RMS})^2R_{DS1} \tag{54}$$

where, $I_{S1,RMS} = \frac{I_{LM,RMS}}{\sqrt{2}}$.

Similarly, the secondary-side conduction losses can be represented as follows:

$$P_{S2,Cond.} = 4LV_{CE(Sat)}I_{IGBT2}D + 4M(I_{S2,RMS})^2R_{DS2} \tag{55}$$

where, $I_{S2,RMS} = n\frac{I_{LM,RMS}}{\sqrt{2}}$.

To evaluate the losses associated with the hybrid ISOP DC-DC converter and compare it with conventional multimodule DC-DC converter relying on the secondary group and conventional multimodule relying on the primary group, Equations (52)–(55) are used to calculate the conduction losses associated with the semiconductor devices. It is assumed that the turns ratio of the employed transformers is 1 : 1 and that the duty cycle is 0.5 with an RMS inductor current of 25 A for each module, where each converter is rated at 200 kW. The number of L and M modules is specified in Table 3 for the three converters. In the provided assessment, the device parameters of a SiC MOSFET CMF20120D with a drain-to-source resistance of 80 mΩ and the device parameters of an IGBT IKW25N120T2 with a collector-to-emitter voltage of 1.7 V are considered. Considering only the conduction losses of the switching devices in the three multimodule converters, the following can be observed. Conventional multimodule DC-DC converter relying on the secondary group and conventional multimodule DC-DC converter relying on the primary group would results in losses of 5.1 kW (i.e., efficiency of 97.5%) and 680 W (i.e., efficiency of 99.6%), respectively. However, conduction losses in the hybrid multimodule DC-DC converter are found to be 1.6 kW ((i.e., efficiency of 99.2%). Figure 7 presents the efficiency loss curve with respect to power loading for the three converter systems.

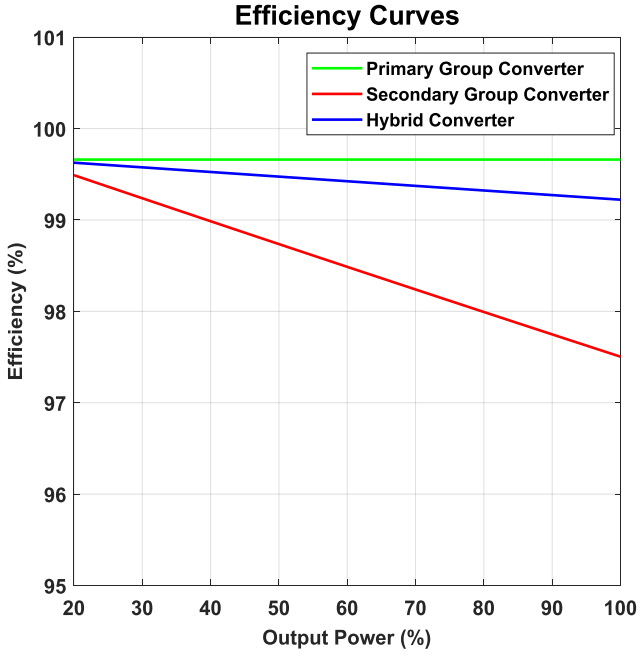

Figure 7. Hybrid Efficiency loss curve with respect to power loading.

4.2. Power Density Assessment

This subsection presents a rough estimation of the power density for the three converters presented in Table 3. The power density can be evaluated in terms of power losses and the volume of the converter components, as defined in (56). The total volume of the converter can be represented by summing up the volume of the utilized power switches, heat sinks, the transformer's winding, and the transformer's core as defined in (57) [46]:

$$\rho = \frac{P_{in} - P_t}{Volume} \tag{56}$$

$$Vol_t = Vol_{sw} + Vol_{HS} + Vol_{Core} + Vol_{Winding} \tag{57}$$

The volume of the overall converters is evaluated, considering the study provided in [47,48]. In which it is assumed that the converter components contribute with the same percentage as presented in [48]. Based on the study provided in [47,48], the volume contribution for the converter components is presented in Figures 8 and 9 considering hard switching and soft switching operation, respectively. It can be observed from Figure 8 that the volume of the heat sinks in the primary group multimodule DC-DC converter is almost the same as the volume of the heat sinks in the secondary group multimodule DC-DC converter. However, the volume of the transformer is higher in the primary group multimodule DC-DC converter due to the lower switching frequency. Accordingly, considering the losses for the three converters presented earlier, the power density of the conventional multimodule DC-DC converter relying on the secondary group is 12.2 kW/L, while the power density of the conventional multimodule DC-DC converter relying on the primary group is 9.9 kW/L. On the other hand, the power density in the hybrid multimodule DC-DC converter is found to be 10.3 kW/L.

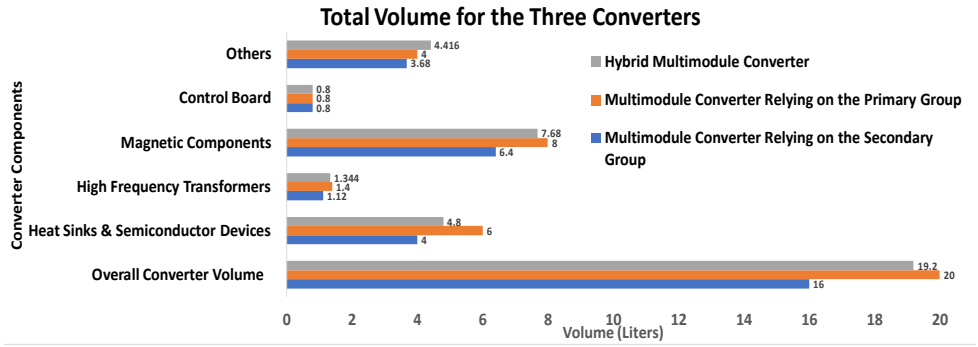

Figure 8. Converter components volume contribution in liters considering hard switching operation.

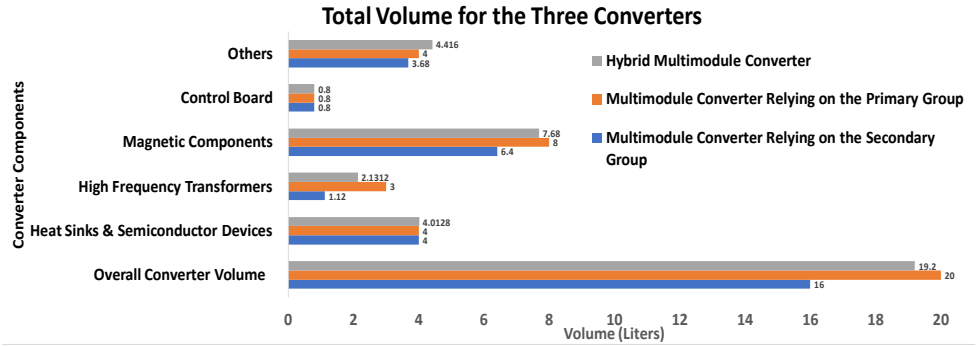

Figure 9. Converter components volume contribution in liters considering soft-switching operation.

5. Power-Sharing in the Eight-Module Hybrid ISOP Fast Charger DC-DC Converter

Since modules in practical applications are not identical, any mismatch in the parameter values can cause unequal power distribution among the modules. Consequently, the voltage of modules is unbalanced, which may cause heavy loading or thermal overstress [39]. Accordingly, a control scheme that ensures uniform power-sharing among the modules is required to achieve reliable operation for the hybrid ISIP-OSOP DC-DC converter.

Since the presented converter is connected in series and parallel at the input and output sides, respectively, a control scheme that ensures IVS and OCS is required. A control strategy for equal power-sharing among the modules is addressed for the eight-module hybrid ISOP DC-DC converter. In other words, a cross-feedback OCS (CFOCS) for ISOP has been presented in [49] to ensure both equal IVS and OCS. The OCS is achieved among the modules and automatically ensuring IVS without the need for an IVS control loop. The presented control strategy in [49] has a fault-tolerant feature even when introducing a mismatch in the module's parameters. In addition, the output voltage regulation for the converter is simplified. The concept of this control strategy is based on applying the feedback control to be the summation of all the other current control loops instead of applying its own current feedback control loop.

In this paper, the CFOCS is applied to the presented hybrid ISOP converter to ensure uniform power-sharing where the system parameters are shown in Table 4. The OCS control, shown in Figure 10, consists of one outer output current loop and eight inner current loops where four are dedicated to the primary multimodule group, and the other four inner loops are dedicated to the secondary multimodule group. The control scheme, shown in Figure 10, for the eight-module hybrid ISOP converter is current-controlled considering a reflex charging technique that is termed as burp charging or negative pulse charging. The control scheme, presented in Figure 10, is tested with reference current relying on the burp charging algorithm to the output current reference signal. The charging cycle starts with a positive sequence from 0.2 s to 0.6 s. After that, a rest period for 0.1 s is applied, then a short discharge sequence for 0.1 s.

Table 4. System parameters used in simulation.

Parameters	Primary Multimodule Group				Secondary Multimodule Group			
	Module 1	Module 2	Module 3	Module 4	Module 1	Module 2	Module 3	Module 4
Overall converter rated power	200 kW							
Rated power per module	160 kW				40 kW			
Total input voltage	40 kW				10 kW			
Input voltage per module	10 kV							
Overall output voltage	8 kV				2 kV			
Module output voltage	2 kV				500 V			
DAB units	400 V							
Turns ratio	400 V							
Leakage inductance	8							
Effective duty cycle	1 : 1	1 : 0.95	1 : 0.9	1 : 0.85	4 : 1	4 : 0.95	4 : 0.9	4 : 0.85
Input capacitance	80 µH	89 µH	99 µH	11 µH	500 nH	554 nH	617 nH	692 nH
Filter inductance	0.8	0.84	0.89	0.94	0.8	0.84	0.89	0.94
Filter capacitance	50 µF	80 µF	50 µF	80 µF	35 µF	57 µF	35 µF	57 µF
Resistance	50 mH	60 mH	60 mH	50 mH	35 mH	42 mH	42 mH	35 mH
Switching frequency	300 µF							
	0.8 Ω							
	10 kHz				100 kHz			

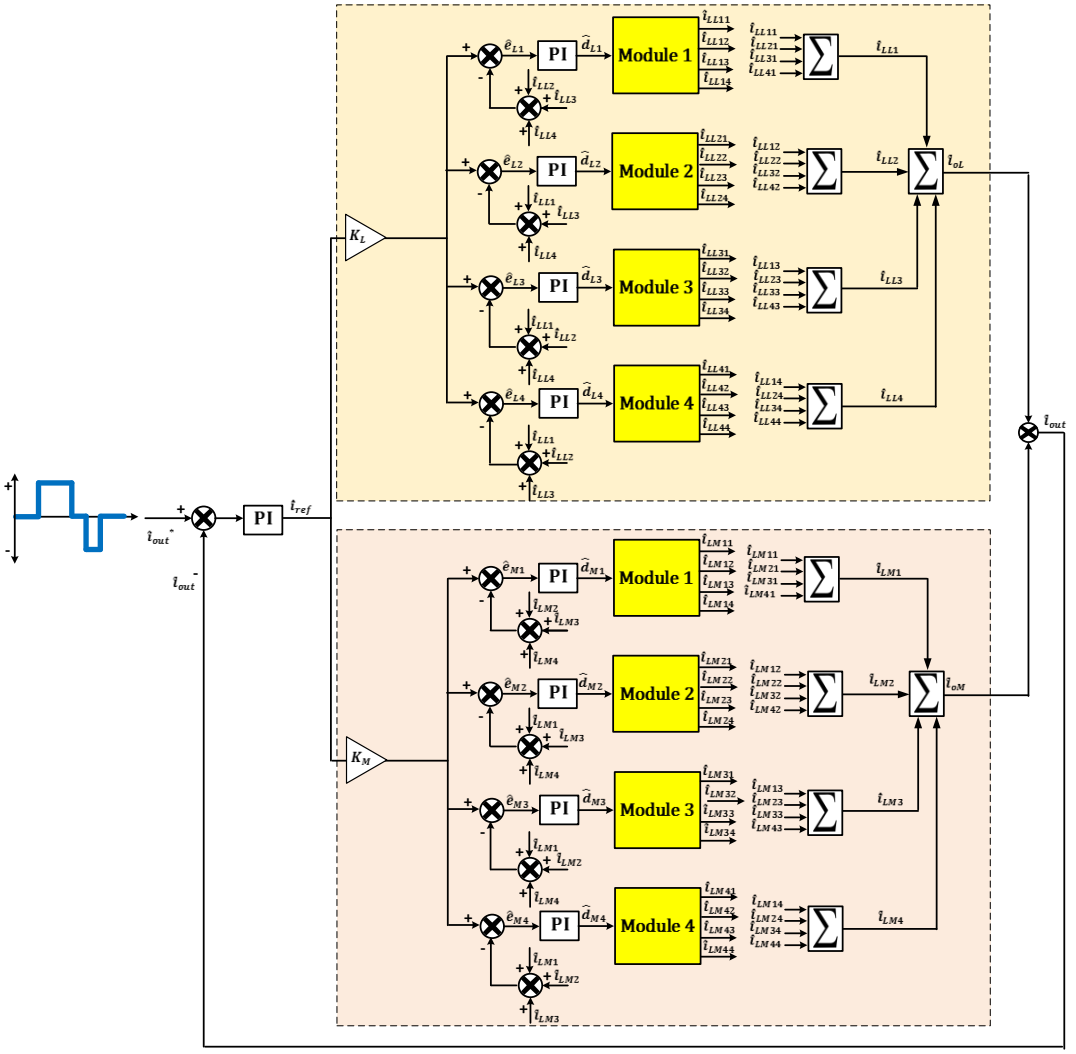

Figure 10. OCS control scheme for the proposed hybrid ISOP DC-DC converter.

6. Discussion

A MatLab/Simulink model is simulated using the small-signal model derived in Section 3 along with the control strategy presented in Figure 10, where the parameter mismatch presented in Table 4 is introduced to the employed modules.

As can be observed from Figure 11, the control strategy for the proposed eight-module hybrid converter can accomplish the requirements. Results, presented in Figure 11, demonstrate that the controller in Figure 10 compensates for the negative influences resulting from the system parameters mismatch. In which the modular input voltages and the modular output currents are equally shared between the four modules. It can be seen from the presented results in Figure 11 that the primary multimodule group is in charge of delivering $\frac{4}{5}$ of the total desired power while the secondary multimodule group is in charge of delivering $\frac{1}{5}$ of the total desired power. Besides, the output current of the proposed power converter tracks the reference current that relies on the burp charging algorithm. Accordingly, it can be concluded that the applied control strategy is reliable and that equal power-sharing is achieved between the employed modules.

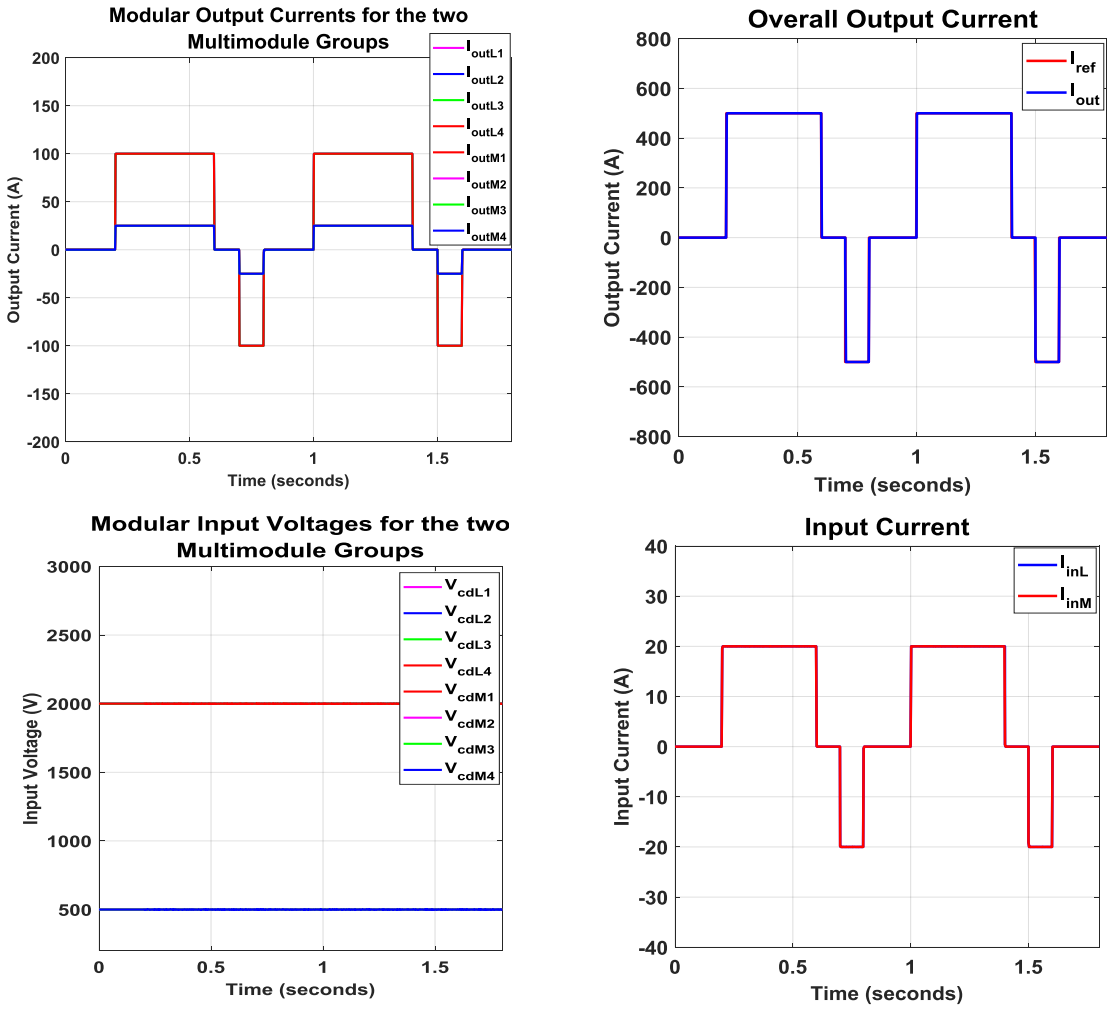

Figure 11. Simulation results for the eight-module hybrid ISOP system.

7. Conclusions

This paper introduces a hybrid multimodule DC-DC converter for EV UFC to achieve both high efficiency and high power density. The hybrid concept is achieved through employing two different groups of multimodule converters. The first is designed to be in charge of a high fraction of the total

required power, operating relatively at a low switching frequency. While the second is designed for a small fraction of the total power, operating relatively at a high switching frequency. To support the power converter controller design, a generalized small-signal model for the hybrid multimodule DC-DC converter is studied in detail. This in turn supports the analysis and control design. In addition, the efficiency and power density for the conventional multimodule DC-DC converter based on the primary group, conventional multimodule DC-DC converter based on the secondary group as well as the presented hybrid DC-DC converter are evaluated. In which it has been shown that the presented converter can achieve both high efficiency (99.6%) and high power density (10.3 kW/L), compromising between the two other conventional converters. Since the power switches are the key contributors to the losses and the volume of the overall converter. It is worth mentioning that the assessment provided in this paper takes into account the conduction losses and the volume of the semiconductor switches, assuming that the converters are operating under zero voltage switching (ZVS). Furthermore, cross feedback output current sharing (CFOCS) for the hybrid input-series output-parallel (ISOP) multimodule DC-DC converters to ensure uniform power-sharing among the employed modules and the desired fraction of power handled by each multimodule group is examined. The control scheme for a hybrid eight-module ISOP power converter of 200 kW is investigated. The controller is tested with a reference current that relies on reflex charging scheme. The power loss analysis of the hybrid multimodule converter is provided. Simulation results using the MatLab/Simulink platform are provided to elucidate the presented concept considering parameter mismatches. Simulation results show that the modular input voltage and the modular output current are equally shared among the four modules of each group with the required ratio between the two multimodule groups. Numerical calculation in terms of losses is carried out for the presented converter considering conduction losses of the power switches.

Author Contributions: M.E. and A.M. contributed to the whole research work and analysis tools; M.E. wrote the paper. This work was performed under the supervision with regular and continuous feedback of A.M. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

ICEs	Internal Combustion Engines
EVs	Electric Vehicles
UFC	Ultrafast Charging
DAB	Dual Active Bridge
DHB	Dual Half Bridge
ZVSZ	Zero Voltage Switching
CSC	Zero Current Switching
CFOCS	Cross Feedback Output Current Sharing
ISOP	Input-Series Output-Parallel
ISIP-OSOP	Input-Series Input-Parallel Output-Series Output-Parallel
ICS	Input Current Sharing
IVS	Input Voltage Sharing
OCS	Output Current Sharing
OVS	Output Voltage Sharing

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