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Reduced switch count-based *N*-level boost inverter topology for higher voltage gain

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*Marif Daula Siddique[1], Bhimireddy Prathap Reddy[1], Atif Iqbal[1] ✉, Saad Mekhilef[2]**

[1]*Department of Electrical Engineering, Qatar University, Doha, Qatar*
[2]*Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia*
**Current affiliation: School of Software and Electrical Engineering, Swinburne University of Technology, Melbourne, VIC 3122, Australia*
✉ *E-mail: atif.iqbal@qu.edu.qa*

Abstract: This study proposes a new boost inverter based on a switched-capacitor concept with reduced switch count. The basic unit is a five-level topology, which inherently generates the AC output voltage with the self-voltage balancing of the capacitors. A conventional carrier-based sinusoidal modulation technique has been designed to maintain the capacitor voltage up to the input source voltage. The *N*-level structure of the proposed basic unit is also presented, which has the additional advantage of higher voltage gain with a single input. A detailed comparison with other similar topologies has been carried out. A laboratory prototype has been used to test the workability of the proposed basic unit and its extension for seven-level through several results.

1 Introduction

Multilevel inverters (MLIs) have been preferred for DC–AC power conversion due to its numerous and unique features like better output voltage performance in terms of harmonics, lower voltage stresses across switches etc. for high- and medium-power/voltage applications. MLIs found their applications in almost every field like renewable energy systems, distributed generation system, high-voltage DC applications, uninterruptible power supplies, industrial drive applications etc. cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) have been three elementary and standard MLIs topologies used and commercialised from the last few decades. With a lot of research and development, these topologies have reached their maturity level [1, 2].

Recently, the topologies based on the switched-capacitor (SC) concept have gained a lot of attention from the researchers. Apart from the NPC which has the unbalancing of the capacitor voltages, and CHB which requires several isolated DC voltage sources, the SC-based MLI has several features like single source, self-voltage balancing, absence of magnetic components etc. The SC-based MLI can be categorised into two as boosting-type and non-boosting-type topologies. In non-boosting-type topologies, the boosting of the input voltage can be achieved with the help of DC/DC converter [3]. Wang *et al.* [4] presented a five-level (5L) active NPC inverter topology which uses seven switches, two diodes, and three capacitors. However, the limiting aspect of this structure has been the boosting factor of 0.5. A new 5L fault-tolerant inverter has been recommended in [5], which is a hybridisation of H-bridge and one leg of NPC. However, the peak of the output voltage has a lower magnitude than the magnitude of the input voltage.

Several switched-capacitor multilevel inverter (SCMLI)s have been proposed in the literature with a higher boosting factor. Generalised structure of SCMLI-based boost inverter topologies has been proposed in [6–9]; however, for higher voltage gain, these inverters suffer from the increased number of component count. Several SCMLI-based topologies have been proposed for higher boosting ability while reducing the switch count. A 5L boost topology has been presented in [10] which employs nine switches for a voltage gain of two. Similarly, another 5L inverter has been reported in [11]; however, two capacitors of voltage rating equal to the input voltage source have been used for obtaining twice voltage gain. A 5L FC-based topology has been introduced in [12] which uses four capacitors and ten switches. The higher number of components makes this topology obsolete for practical applications.

In this paper, an effort has been done to propose an improved structure of the boost inverter with higher voltage gains using a lower number of components. Some of the main aspects of the proposed inverter are:

- It uses a single input voltage and one capacitor for 5L with twofold voltage gain output voltage waveform.
- The general structure of the proposed topology allows for higher levels.
- Inherent reversing of polarity and self-balancing of the capacitor voltage.
- Two switches of the topology are operated at a fundamental frequency (50 Hz).

2 Proposed topology

2.1 Basic unit: 5L topology

The proposed 5L boost inverter topology is illustrated in Fig. 1. It consists of eight switches, one SC unit, and one input voltage source of magnitude V_{in} which can be a photovoltaic array, fuel cell or battery. The switches S_3 and S_4 are configured as reverse blocking switch, i.e. an insulated-gate bipolar transistor (IGBT) or metal oxide semiconductor field effect transistor (MOSFET) in series with a diode and the remaining switches are configured as an IGBT or MOSFET with an anti-parallel diode. Two cross-connected switches, i.e. S_1 and S_2 need to block a voltage of $2V_{in}$ with the other six switches of the voltage rating equal to the input voltage source. The proposed topology gives a boosting factor of two. In contrast to many other structures using the H-bridge for the generation of polarity, the proposed architecture has an inherent capability to generate both polarities of voltage. The voltage across the SC unit is equilibrated with a voltage magnitude of V_{in} without the need for any sensor and therefore renders the proposed topology cost.

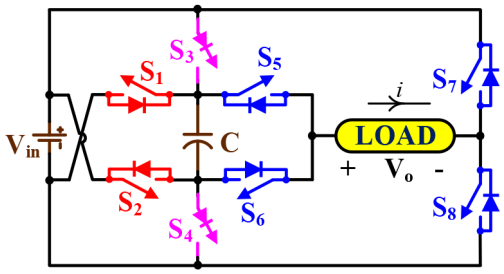


Fig. 1 *Proposed basic unit (5L) of boost inverter topology*

Table 1 Switching combinations of the proposed 5L MLI

S_1	S_2	S_3, S_4	S_5	S_6	S_7	S_8	V_o	V_C
0	1	0	1	0	0	1	$2V_{in}$	D
0	0	1	1	0	0	1	V_{in}	C
0	0	1	0	1	0	1	0	C
0	0	1	1	0	1	0	0	C
0	0	1	0	1	1	0	$-V_{in}$	C
1	0	0	0	1	1	0	$-2V_{in}$	D

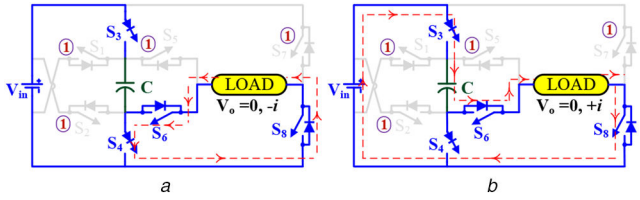


Fig. 2 *Switching states with*
(a) $V_o = 0, -i$, ***(b)*** $V_o = 0, +i$

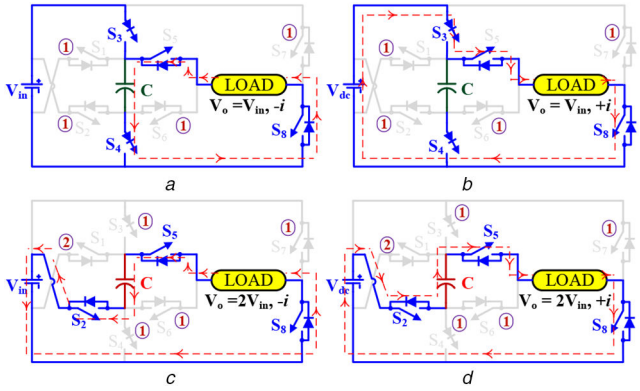


Fig. 3 *Switching combination of the 5L inverter in with*
(a) $V_o = +V_{in}, -i$, ***(b)*** $V_o = +V_{in}, +i$, ***(c)*** $V_o = +2V_{in}, -i$, ***(d)*** $V_o = +2V_{in}, +i$

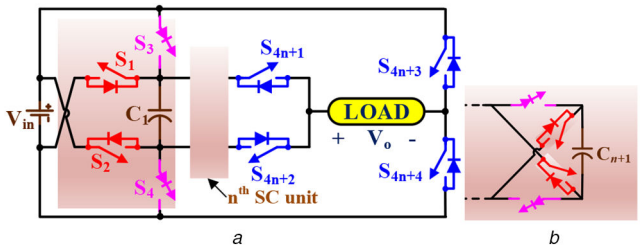


Fig. 4 *Extension of the Proposed Topology*
(a) Generalised structure, ***(b)*** Proposed SC unit

2.2 Voltage states of 5L topology

Table 1 lists the switching combination required to generate a 5L output voltage. The '1' and '0' entry indicates that the switch is ON and OFF state, respectively. The table also shows the effect on the SC voltage of each voltage level with 'D' and 'C' being referred to the discharging and charging of the SC unit, respectively. Different paths for the flow of current and corresponding active switches for each level with the positive polarity are depicted in Figs. 2 and 3. The zero output voltage across the load is depicted in Figs. 2*a* and *b*. From this figure it is observed that the current path for both directions of current is available. With the transition of the switching state of S_5 and S_6, the voltage V_{in} appears across the load. Figs. 3*a* and *b* show the connection diagrams of $+V_{in}$ level with both directions of currents. The capacitor C will be charged to the voltage of V_{in} by connecting in parallel to the input voltage source at the voltage levels of zero and V_{in}, as shown in Figs. 2 and 3. The connection of the output voltage of $2V_{in}$ with the discharging of the capacitor voltages is as shown in Figs. 3*c* and *d*.

2.3 Proposed N-level topology

The proposed 5L topology can also increase the number of voltage levels (N) by connecting several modules of the SC unit. The generalised structure of the proposed topology is shown in Fig. 4*a* with the proposed SC module illustrated in Fig. 4*b*. For the inverter topology illustrated in Fig. 3*a*, the equations with N number of levels are:

$$\left.\begin{aligned} N_{sw} &= 2(N-1) \\ N_C &= \frac{1}{2}(N-3) \\ G &= \frac{1}{2}(N-3) \end{aligned}\right\} \quad (1)$$

where N_{sw}, N_C, and G represent the switches count, capacitor count, and voltage gain of the proposed topology, respectively.

2.4 PWM strategy for the proposed 5L topology

For the control of the switches of the proposed inverter, the level-shifted pulse width modulation (LS-PWM) technique has been applied. With the 5L output voltage, four high-frequency carrier signals i.e. V_{cr1}–V_{cr4} are compared with a sinusoidal reference signal V_{sine}, having a frequency of the output voltage waveform. All the four carrier signals are shifted on the vertical axis with a magnitude of A_c, which is peak-to-peak magnitude of each carrier signal. Fig. 5 shows the LS-PWM technique for the proposed 5L topology. The gate pulses are generated using the logic given in Table 2. The modulation index (M) for the LS-PWM technique can be defined as

$$M = \frac{V_s}{2 \times A_c} \tag{2}$$

where V_s is the peak magnitude of the reference sinusoidal signal V_{sine}.

2.5 Capacitor sizing

The determination of the size of the capacitor has an important parameter to be considered for the SC-based topologies. The ripple voltage of the switched capacitor mainly depends on load current which is the discharging current for the SCs. Based on peak load current I_{peak}, the ripple voltage ΔV_C can be calculated as

$$\Delta V_C = \frac{I_{peak} \times \text{pf} \times \cos(90° - 0.5\theta)}{\pi \times f_o \times C} \tag{3}$$

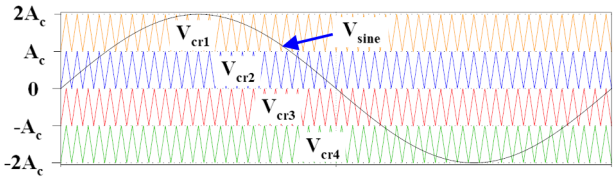


Fig. 5 *LS-PWM for the proposed 5L topology*

where θ is the maximum discharge angle, f_o is the fundamental frequency of the output voltage and C is the capacitance value of the SC unit. Fig. 6 relates the deviation of the capacitor voltage ΔV_C with the output voltage in the worse voltage condition with the carrier signals replaced by a DC line having an average magnitude of it. The capacitor voltage decreases during the voltage level of $2V_{in}$; however, it regains the magnitude of input voltage V_{in} during the charging of the capacitor with voltage levels of V_{in} and zero. Due to the symmetrical operation of charging and discharging of the capacitor C, the voltage across it remains balanced.

3 Comparison analysis

In order to distinguish the advantages of the proposed 5L inverter, Table 3 has been accomplished in terms of different parameters associated with a boost inverter topology as given in Table 3. For the comparison, the topologies with 5L output voltage waveforms have been considered. From the comparison table, the conventional topologies NPC and FC have one major disadvantage of lower voltage gain with a higher number of passive components and switches. The topology proposed in [6, 8, 9] requires six switches; however, the topology proposed in [9] requires an H-bridge with higher voltage switches and topology presented in [8] requires two capacitors. Similarly, the topologies proposed in [10–12] require a higher count of power semiconductor components and capacitors

Table 2 Conducting switches for 5L inverter

Relationship	ON state switches	V_o
$V_{sine} > V_{cr1}$	S_2, S_5, and S_8	$2V_{in}$
$V_{cr1} > V_{sine} > V_{cr2}$	S_3, S_4, S_5, and S_8	V_{in}
$V_{cr2} > V_{sine} > V_{cr3}$	S_3, S_4, S_6, and S_8	0
	S_3, S_4, S_5, and S_7	
$V_{cr3} > V_{sine} > V_{cr4}$	S_3, S_4, S_6, and S_7	$-V_{in}$
$V_{cr4} > V_{sine}$	S_1, S_6, and S_7	$-2V_{in}$

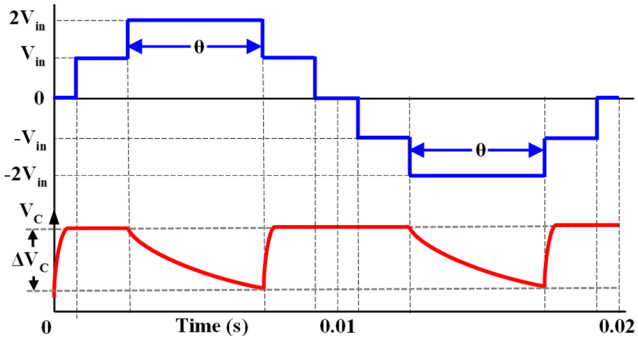


Fig. 6 *Capacitor ripple voltage variation*

Table 3 Comparison table for 5L topologies

Ref		NPC	FC	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[P]
N_{sw}		8	8	6	9	6	6	9	7	12	8
N_d		6	0	2	0	2	1	0	4	0	0
N_C		4	10	1	1	2	1	1	2	4	1
N_{gd}		8	8	6	9	6	6	9	7	12	8
N_{sc}		—	—	3	3	4	2	4	9	8	2
G		0.5	0.5	2	2	2	2	2	2	4	2
TSV		8	8	12	9	8	11	9	9	20	10
MBV		0.5	0.5	2	1	1	2	1	1	1	2
CF	0.5	26.5	26.5	15.5	15.5	16.3	13.3	16.5	24.5	26.6	14
	1.0	35	35	19	18	18.5	16.5	19	27	29.25	17
	1.5	43.5	43.5	22.5	20.5	20.8	19.8	21.5	29.5	31.9	20

N_d, number of diodes; N_{gd}, number of gate driver circuits; N_{sc}, number of devices in charging loop; TSV, total standing voltage ($\times V_{in}$); MBV, maximum blocking voltage ($\times V_{in}$); and [P], proposed.

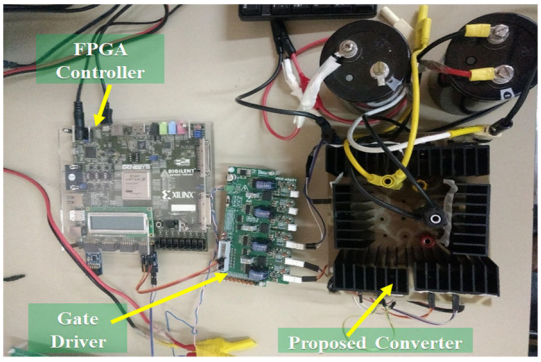
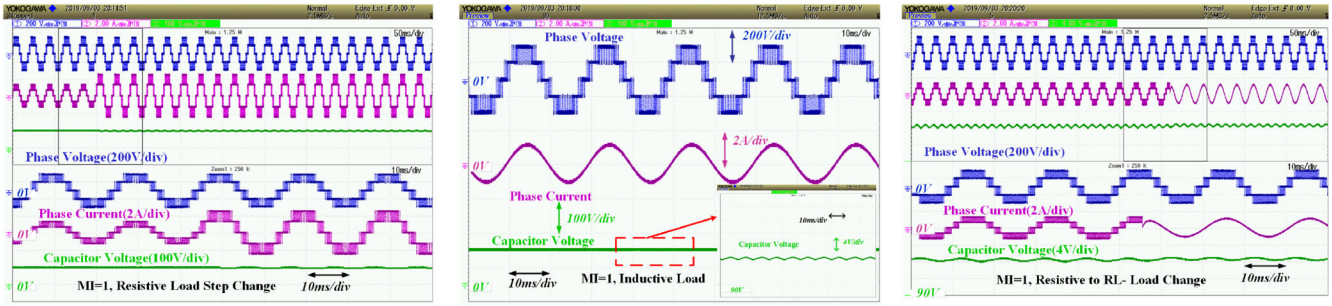
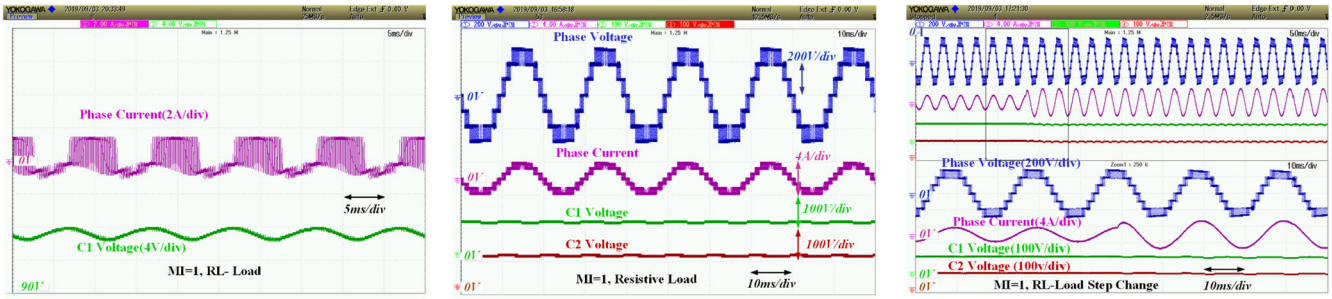


Fig. 7 *Hardware setup of the proposed inverter*



a *b* *c*

Fig. 8 *Hardware results of 5L waveform with*
(a) Change in R load, ***(b)*** RL load, ***(c)*** Load change from R load to RL load



a *b* *c*

Fig. 9 *Hardware results*
(a) Voltage and current of capacitor with a RL load, ***(b)*** 7L output waveform with R load, ***(c)*** 7L output waveform with step change in RL load

for the 5L. Similarly, the topology presented in [12] requires four capacitors for 5L output voltage. The proposed topology requires less power semi-conductive devices than the topologies proposed in [7, 10–12]. Similarly, the proposed topology requires only one switched capacitor unit for 5L output voltage; however, the topologies proposed in [8, 11, 12] require more than one capacitor for 5L. From these comparisons, the proposed basic unit with 5L is superior to the similar structures listed in Table 3.

One of the important parameters for the MLI topology is the cost. A cost function (CF) to explain this has been defined considering the effects of different constraints are as follows:

$$\mathrm{CF} = N_{\mathrm{sw}} + N_d + N_C + N_{\mathrm{SC}} + \alpha\frac{\mathrm{TSV}}{G} + \beta\frac{\mathrm{MBV}}{G} \tag{4}$$

where α and β are the factors associated with TSV and MBV factors against semiconductor count, respectively. Where TSV and MBV are more important than the device count, the value of $\alpha, \beta > 1$. If TSV and PIV are insignificant to the device count, α and $\beta < 1$. Table 3 gives the CF for different topologies and the proposed topology has the least CF compared to all other topologies. On the other side, the major short coming of the proposed MLI topology is the floating DC bus for getting multilevel voltage output.

4 Results and discussion

The validation of the proposed boost inverter is done with the laboratory prototype. This prototype is realised with G60N100 switches, 2200 µF electrolytic capacitor (PG6DI) and DC power supply with 100 V. The switching frequency has been set as 5 kHz. The gate pulses to drive the proposed boost inverter are generated from the Vertix-5 FPGA control board (XC5VLX50T). Fig. 7 illustrates the hardware prototype of the recommended inverter topology.

The proposed inverter topology has been tested for 5L and 7L. Fig. 8*a* presents the experimental results for change of resistive load from 150 to 75 Ω with a unity modulation index. As observed from this waveform, the output voltage is 200 V (peak) for an input voltage of 100 V since the proposed inverter amplified the voltage by two times. Further, it can be seen that the voltage of the capacitor is stable and matches the input voltage and step change in load does not affect the stability of the capacitor voltage.

The experimental results for RL load (150 Ω and 80 mH) with a unity modulation index of the proposed topology with 5L are shown in Fig. 8*b* with load parameters of 150 Ω and 80 mH. The experimental results during a step change in power factor (R load to RL load) are presented in Fig. 8*c*, where the load is changed from 150 Ω to 150 Ω + 80 mH. Fig. 9*a* illustrates the voltage and current of the capacitor for RL load with a unity modulation are presented. For clear visualisation the voltage ripple of the capacitor, in Figs. 8*a* and *b*, and the voltage of the capacitor are

shown with a base of 90 V and volt/division is 4 V, but the average capacitor voltage is 98.

The proposed inverter topology has also been tested with 7L output voltage using two switched capacitor units. Fig. 9*b* shows the experimental results with a resistive load of 150 Ω. Both capacitor voltages are stable at 100 V with the maximum voltage of the output waveform being 300 V. The results under step change in RL load (two RL loads are connected in parallel) of the proposed inverter are shown in Fig. 9*c*. All figures of Figs. 8 and 9 are evidence that the proposed inverter can work for a different step change in loads with boosting features and maintaining the self-balancing of the capacitor voltages.

5 Conclusion

This paper suggested an inverter topology with the characteristics of boosting of the input voltage, inherent voltage balance, and a reduced blocking voltage of the switch. The SC-based inverter proposed in this paper, with these attractive features, offers effective circuit and performance upgradation for DC–AC power conversion systems of high quality. The detailed comparative study has reinforced the superiority of the recommended inverter compared to related prior-art inverters for various conditions. The results obtained through laboratory prototype of the proposed inverter topology with 5L and 7L output voltage confirmed the validity with regard to an extensive range of real-time operational environments.

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