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Research paper

A high step-up DC–DC converter based on ASL and VMC for renewable energy applications

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ABSTRACT

In this paper, a new high step-up non-isolated DC–DC converter has been proposed and analyzed. The proposed topology provides a high DC output voltage, which is adjustable by two different duty cycles. Moreover, low voltage stress across the power switches can be marked as another advantage of this structure. The inequality of the switches' duty cycles helps obtain high output voltage with moderate duty cycles in this converter. Four inductors based on two magnetic cores, four capacitors, two diodes, and three switches make up the converter's components. Operational modes of the proposed topology are investigated under steady-state analysis in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary condition mode (BCM). In addition, mathematical calculations of voltage, current, and efficiency are provided in this paper. In addition, a comparison study of the proposed converter and other related structures is conducted to determine the advantages it offers. The proportion of losses and efficiency calculation are analyzed. Finally, a (500 W, 50 kHz) laboratory prototype is assembled and analyzed to validate the analytical findings in this paper.

1. Introduction

Nowadays, DC–DC converters' optimum design and modification are interesting research topics because of their vast applications in renewable energies. Renewable power generation sources produce low primary voltage levels. Therefore, high voltage gain and high power efficiency converters are required to connect grid and renewable energy sources (Sadaf et al., 2021; Talebian et al., 2021; Alavi et al., 2019). DC–DC converters are widely used in various applications, such as electric vehicles, wind turbines, fuel cells, and photovoltaic panels. These multiple applications of the high step-up DC–DC converters led to many high step-up topologies proposed in the prior years (Marzang et al., 2020b). Transformers in the isolated converters can provide high output voltage and decrease voltage stress on components. The voltage gain can be regulated by changing the transformer's turn ratio. In addition, the input side is isolated from the output side in these structures, which eliminates the common ground noises. Conversely, isolated converters have some disadvantages, such as the complexity of their analysis and design, high cost, high power loss, and the leakage inductances of transformers that cause voltage spikes across the implemented power switches (Nouri et al., 2019; Zhang et al., 2012).

Conversely, non-isolated DC–DC converters or transformerless converters have two different arrangements. First, non-isolated DC–DC converters with coupling inductors have more complexity in design and analysis. Conversely, two or more inductors are based on one magnetic core in these structures, which decreases the converters' size, power losses, and cost. In Liu et al. (2016), the non-isolated DC–DC converters with coupled inductors have been investigated. In addition, higher voltage gain is achievable easily in the coupled inductor-based structures (Hashemzadeh et al., 2022; Wong et al., 2017; Chen et al., 2020).

Second, this category lacks any coupling inductors; therefore, simple structure and analysis with low cost and high efficiency are the most significant features of the non-isolated DC–DC topologies without coupling inductors. However, in some topologies, high voltage gain is achievable only in a high-duty cycle. Refs. Li and He (2011) and Tofoli et al. (2015) present an overall view of non-isolated DC–DC converters.

There are numerous methods to increase the voltage gain. A new method presented in the previous years is energizing inductors. This method makes achievable high voltage gain in a low switches' duty cycle (Marzang et al., 2022; Lakshmi and Hemamalini, 2018; Sagar Bhaskar et al., 2019; Bhaskar et al., 2019; Maroti et al., 2019b,a). However, suffering from high voltage on the power switches and pulsating input current ripple are their drawbacks.

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Other common techniques for improving the output voltage are Active Switch Inductor (ASL) and Switched Capacitor (SC) cells. In Salvador et al. (2018, 2020), an ASL network and SC cell have been implemented to obtain high output voltage with lower voltage stress on the power switches. Topologies (Yang and Liang, 2012; Yang et al., 2009) have almost similar performances. An ASL network has been implemented to achieve both structures' desired output voltage with a low-duty cycle. In Yang and Liang (2012), a MOSFET is used instead of the output diode to make a bidirectional converter. In addition, the number of utilized magnetic cores has been reduced due to the utilization of coupled inductors, leading to lower cost and size. On the other side, the introduced structure in Yang et al. (2009) is a non-coupling converter with an extra magnetic core and more core losses.

Z-source topologies are other topologies to improve input voltage. In Haji-Esmaeili et al. (2018), a Quasi–Z Source converter has been presented to achieve desired output voltage by implementing the hybrid switched-capacitors switched-inductors method. Z-source structures limit the duty cycle's operating range, which is one of the drawbacks of these converters.

The topologies introduced in Babaei et al. (2018) and Marzang et al. (2019) are optimized for high power gain using the ASL network. The presented topology in Babaei et al. (2018) is a combination of the introduced structure in Yang et al. (2009) and an Active-Passive Inductor cell (APLC). In Axelrod et al. (2008), a new combination of the SC cells and ASL networks has been presented to achieve the desired high voltage gain without implementing transformers.

The analyzed structure in Marzang et al. (2020a) is a Multilevel Boost Converter (MBC). This structure has added the SC cells to the conventional boost converter. The series capacitors have been used to increase the output voltage. Another approach to increasing output voltage has been presented in Mashinchi Maheri et al. (2017); in this structure, high voltage gain can be achieved by increasing the number of ASL cells and the inductors' stored energy. In Nouri et al. (2014) and Freitas et al. (2021), a new topology with n stage of Diode–Capacitor–Inductor (DCL) cells and m units of voltage multiplier cells (VMC) has been implemented to obtain high voltage gain. In this structure, it is possible to reach the desired voltage gain by regulating the number of DCL stages and VMC units.

This study combined a VMC unit and an ASL network to increase voltage gain and decrease voltage stress on power semiconductors. These combinations make the proposed converter suitable for renewable energy applications by some significant advantages, which are detailed below:

- Three power switches operate with two different duty cycles. Therefore, inductors can be energized more than each switch's duty cycle.
- The desired high voltage gain can be achieved easily without high values of duty cycles.
- Voltage stress across the power switches is low. Consequently, it leads to cheaper power switches with lower $r_{DS(on)}$.
- The proposed structure utilizes a VMC unit to improve the output voltage and eliminate switches' voltage spikes.
- In the ASL unit, the inductors are assembled on one magnetic core. As a result, it decreases cost, core losses, and size and increases power density and efficiency.

The remaining sections of this paper are organized as follows: in Section 2, the topology of the proposed converter is introduced. In Section 3, the steady-state analysis of the proposed structure is presented. This section discussed Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), Boundary Condition Mode (BCM), voltage gain, voltage stress, current gain, and current stress. Furthermore, design considerations, efficiency analysis, and comparison results have been investigated in Sections 4, 5, and 6, respectively. Experimental waveforms and efficiency results have been analyzed in Section 7. Finally, a brief conclusion of the paper has been presented in Section 8.

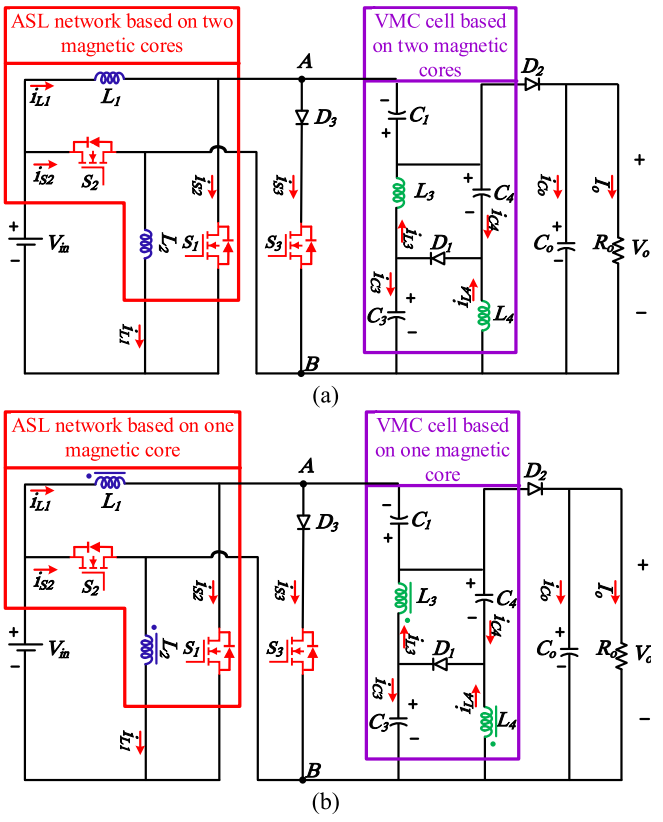


Fig. 1. Schematic of the proposed converter: (a) based on four magnetic cores, (b) based on two magnetic cores.

2. Proposed structure

The proposed topology can be implemented in two different ways. The first consists of three switches (S_1, S_2, and S_3), three diodes (D_1, D_2, and D_3), four capacitors (C_1, C_o, C_3, and C_4), and four inductors (L_1, L_2, L_3, and L_4) which is illustrated in Fig. 1(a). Section 3 will prove that the inductors L_1 and L_2 (or L_3 and L_4) have similar voltage and current relations. Therefore, all these inductors ($L_1 - L_2$ or $L_3 - L_4$) can be implemented based on two magnetic cores instead of four. The second schematic of the proposed converter is shown in Fig. 1(b). The proposed converter consists of an ASL network and a VMC unit as illustrated in Fig. 1. The ASL unit contains two switches (S_1 and S_2) and one magnetic core on which L_1 and L_2 are assembled. On the other side, the implemented VMC includes one magnetic core which winds L_3 and L_4 on it, three capacitors, and a power diode. The VMC unit increases the output voltage, clamps the switches' voltages, and decreases their voltage stress.

The input voltage, output voltage, and load resistance are represented by V_{in}, V_o, and R_o, respectively. T_s and f_s represent the switching period and switching frequency, respectively. The duty cycle of switches S_1 and S_2 is denoted by d_1, and the duty cycle of switch S_3 is indicated by d_2, in which the sum of d_1 and d_2 should be less than one.

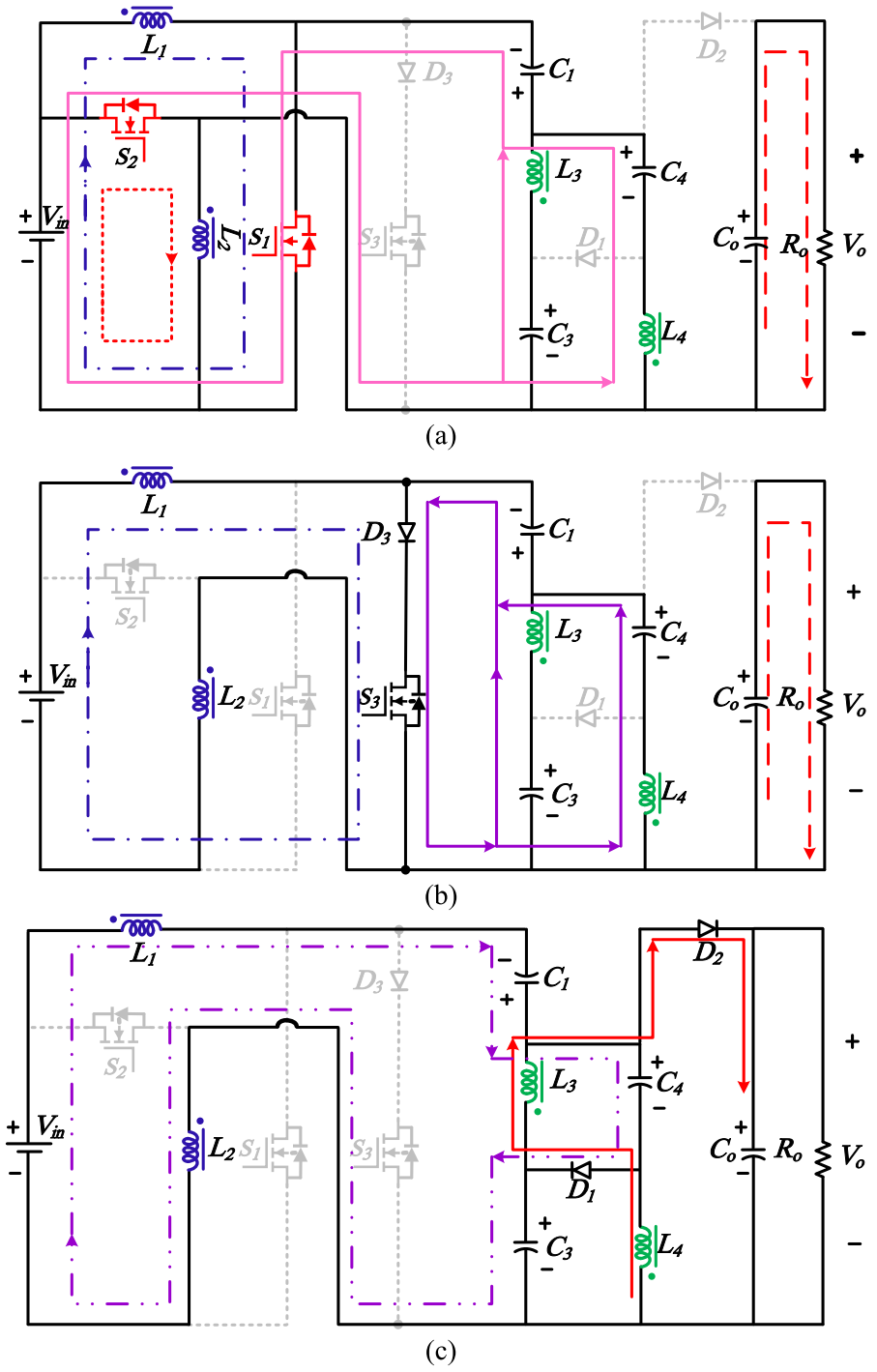


Fig. 2. The equivalent circuit of the presented topology: (a) Mode 1, (b) Mode 2, (c) Mode 3.

3. Steady-state analysis

This section examines the steady-state analysis, in which to simplify the proposed converter analysis, some assumptions have been considered as follows:

i Switches, diodes, and all energy storage elements are ideal. Therefore, the resistance and voltage drop of the power semiconductors, the ESR of inductors, and capacitors can be ignored.
ii The capacitors are assumed to be large enough. Hence, their voltages can be assumed to be constant.
iii The input voltage is constant.
iv The inductors are equal to $L_1 = L_2 = L_X$ and $L_3 = L_4 = L_Y$.
v Mutual inductances between the inductors on each core are denoted by M_X and M_Y. These inductances can be described based on the coupling coefficients (k_X and k_Y) as $M_X = k_X(L_1L_2)^{1/2} = k_XL_X$ and $M_Y = k_Y(L_3L_4)^{1/2} = k_YL_Y$, respectively.

By using the mentioned assumption, the inductors voltage can be expressed as (1) to (4):

$$V_{L1} = L_1\frac{di_{L1}}{dt} + M_X\frac{di_{L2}}{dt} = L_X\frac{di_{L1}}{dt} + k_XL_X\frac{di_{L2}}{dt} \quad (1)$$

$$V_{L2} = M_X \frac{di_{L1}}{dt} + L_2 \frac{di_{L2}}{dt} = k_X L_X \frac{di_{L1}}{dt} + L_X \frac{di_{L2}}{dt} \quad (2)$$

$$V_{L3} = L_3 \frac{di_{L3}}{dt} + M_Y \frac{di_{L4}}{dt} = L_Y \frac{di_{L3}}{dt} + k_Y L_Y \frac{di_{L4}}{dt} \quad (3)$$

$$V_{L4} = L_4 \frac{di_{L4}}{dt} + M_Y \frac{di_{L3}}{dt} = L_Y \frac{di_{L4}}{dt} + k_Y L_Y \frac{di_{L3}}{dt} \quad (4)$$

3.1. CCM analysis

The presented converter operates under three main operational modes. In this section, different operational modes and the related equations are investigated.

3.1.1. Operational mode

Mode 1: The first operational mode occurs when switches S_1 and S_2 are turned on. Hence, inductors L_1 and L_2 are paralleled with the input voltage source, and these inductors start to get magnetized during d_1. Also, the inductors L_3, L_4, and the capacitor C_1 get magnetized and charged by capacitors C_3, C_4, and the input voltage.

The proposed converter schematic in this operational mode is depicted in Fig. 2(a). The inductors' (L_1 and L_2) voltage relations during this mode can be expressed as:

$$V_{in} = V_{L1} = V_{L2} \quad (5)$$

Considering (iv), (v), (1), (2), and (5) can be written.

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{in}}{L_X(1+k_X)} \quad (6)$$

The inductors ($L_{3,4}$) relations can be expressed as follows:

$$\frac{di_{L3}}{dt} = \frac{V_{in} - V_{C1} + V_{C3}}{L_Y(1+k_Y)} \quad (7)$$

$$\frac{di_{L4}}{dt} = \frac{V_{in} - V_{C1} + V_{C4}}{L_Y(1+k_Y)} \quad (8)$$

By applying KCL, these relations can be written:

$$i_{C1,on} = i_{L3} + i_{L4} \quad (9)$$

$$i_{C3,on} = -i_{L3} \quad (10)$$

$$i_{C4,on} = -i_{L4} \quad (11)$$

$$i_{Co,on} = -I_o \quad (12)$$

$$i_{in} = i_{L1} + i_{L2} + i_{C1,1} \quad (13)$$

where $i_{C1,\ on}$, $i_{C3,\ on}$, $i_{C4,\ on}$, and $i_{Co,\ on}$ are the current during the on-state of the switches through the capacitors C_1, C_3, C_4, and C_o, respectively. Furthermore, the voltage and current equations are obtained as

$$i_{S1} = i_{S2} = i_{L1} + i_{Co,on} = i_{L2} + i_{Co,on} \quad (14)$$

$$V_{D1} = V_{D2} = -(V_o + V_{in} - V_{C1}) \quad (15)$$

$$V_{AB} = -V_{in} \quad (16)$$

Considering (16), the voltage across the AB point is negative. This negative voltage on the AB will turn on the intrinsic diode of S_3, making it bidirectional and not our favorite. Thus, a series diode with S_3 can be implemented to avoid bidirectional flow through AB, as shown in Fig. 1.

Mode 2: The second operational mode involves turning on the switch S_3 and turning off all the other switches and diodes. Still, inductors L_1 and L_2 get magnetized from the input voltage source and during d_2. Like the previous mode, the inductors L_3, L_4, and the capacitor C_1 get magnetized and charged by capacitors C_3, C_4, and the voltage source. During this process, the output capacitor C_o is discharged into the load. A diagram showing the equivalent circuit of this operational mode is illustrated in Fig. 2(b). L_1 and L_2 have the following voltage and current relationships:

$$i_{in} = i_{L1} = i_{L2} \quad (17)$$

$$V_{in} = V_{L1} + V_{L2} \quad (18)$$

Considering (1) and (2), the following relation is extracted from (17) and (18).

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{in}}{2L_X(1+k_X)} \quad (19)$$

Also, these relations can be obtained:

$$\frac{di_{L3}}{dt} = \frac{V_{C3} - V_{C1}}{L_Y(1+k_Y)} \quad (20)$$

$$\frac{di_{L4}}{dt} = \frac{V_{C4} - V_{C1}}{L_Y(1+k_Y)} \quad (21)$$

Furthermore, the voltage and current of other components can be obtained from (9)–(12) and the following relations:

$$i_{AB} = i_{L1} + i_{Co,on} \quad (22)$$

$$V_{S1} = V_{S2} = V_{in} - 0.5V_{L1} = V_{in} - 0.5V_{Lx} \quad (23)$$

$$V_{D1} = V_{D2} = -(V_o - V_{C1}) \quad (24)$$

Mode 3: In this mode, the switches are turned off, and the diodes (D_1 and D_2) are forward-biased. A schematic of the converter in this operational mode is shown in Fig. 2(c). Also, inductors magnetized until the beginning of this mode will start to get demagnetized in the capacitors. The output capacitors (C_o), C_3, and C_4 get charged, and capacitor C_1 gets discharged.

By applying KVL, the voltage relations are obtained as:

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{in} + V_{C1} - V_{C4} - V_{C3}}{2L_X(1+k_x)} \quad (25)$$

$$\frac{di_{L3}}{dt} = \frac{-V_{C4}}{L_Y(1+k_Y)} \quad (26)$$

$$\frac{di_{L4}}{dt} = \frac{-V_{C3}}{L_Y(1+k_Y)} \quad (27)$$

Current relations of the components can be obtained from (28) and (29). In these relations, $i_{C1,\ off}$, $i_{C3,\ off}$, $i_{C4,\ off}$, and $i_{Co,\ off}$ are the current of the capacitors C_1, C_3, C_4, and C_o during the off-state of the switches, respectively.

$$i_{L1} = i_{L2} = i_{C1,off} = i_{L3} - i_{C4,off} - i_{Co,off} - i_o \quad (28)$$

$$i_{C3,off} + i_{L3} = i_{C4,off} + i_{L4} \quad (29)$$

Power semiconductors can be characterized by voltages and currents by the following equations:

$$V_{S1} = V_{S2} = 0.5\,(V_{in} + V_{L1} - V_{C1}) \quad (30)$$

$$V_{AB} = V_o - V_{C1} \quad (31)$$

$$i_{D1} = i_{L3} - i_{C3,off} = i_{L4} - i_{C4,off} \quad (32)$$

$$i_{D2} = I_o - i_{Co,off} \quad (33)$$

In addition, the input current equation can be written as (17).

3.1.2. Voltage gain calculation

By applying the state-space averaging approach for the inductors L_1, L_2, L_3, and L_4, these relations can be written as (34)–(36).

$$\frac{V_{in}d_1}{L_X(1+k_X)} + \frac{V_{in}d_2}{2L_X(1+k_X)} + \frac{(V_{in} + V_{C1} - V_{C3} - V_{C4})\,(1-d_1-d_2)}{2L_X(1+k_X)} = 0 \quad (34)$$

$$\frac{(V_{in} - V_{C1} + V_{C3})\,d_1}{L_Y} + \frac{(V_{C3} - V_{C1})\,d_2}{L_Y}$$

$$+\frac{(-V_{C4})(1-d_1-d_2)}{L_Y}=0 \tag{35}$$

$$\frac{(V_{in}-V_{C1}+V_{C4})d_1}{L_Y}+\frac{(V_{C4}-V_{C1})d_2}{L_Y}+\frac{(-V_{C3})(1-d_1-d_2)}{L_Y}=0 \tag{36}$$

The capacitors' voltages can be obtained as follows:

$$V_{C3}=V_{C4}=(2d_1A+(1+d_1)(d_1+d_2))V_{in}/2A \tag{37}$$

$$V_{C1}=(-4d_1A+(1+d_1)(1-2d_1-2d_2))V_{in}/-2A \tag{38}$$

where A is equal to:

$$A=(1-d_1-d_2)/2 \tag{39}$$

Based on mode 3, the output voltage of the presented topology is equal to:

$$V_o=V_{C3}+V_{C4} \tag{40}$$

Using (37), (38), and (40), the voltage gain of the proposed structure (G_{CCM}) can be expressed as:

$$G_{CCM}=\frac{V_o}{V_{in}}=\frac{4d_1+2d_2}{1-d_1-d_2} \tag{41}$$

As can be seen, the voltage gain of the proposed topology is independent of the coupling coefficient. The reason is that the inductors are not coupling, and each inductor is magnetized by the input voltage and demagnetized into the other components. (Inductors are not magnetized or demagnetized by the primary side).

3.1.3. Switches and diodes voltage stress

By combining (23) and (30), the voltage stress range of the switches (S_1 and S_2) is obtained as (42).

$$0\le V_{S1,2}\le (V_{in}+V_o-V_{C1})/2 \tag{42}$$

The voltage stress range of the diodes can be obtained from (15) and (24) as follows:

$$-(V_o+V_{in}-V_{c1})\le V_{D1}\le 0 \tag{43}$$

$$-(V_o+V_{in}-V_{c1})\le V_{D2}\le 0 \tag{44}$$

3.1.4. Voltage stress across the AB point

As mentioned, to make a directional flow between points A and B, a diode is added to the AB path to prevent bidirectional current through the internal diode of the MOSFET (S_3). Based on the desired application, this branch can implement in two different ways. The first used in this paper is a combination of a series diode (D3) and a MOSFET (S3), which can be a good choice for high-frequency applications. The second option is implementing an IGBT (which *does not have an internal diode*) which can be a good choice for high-power applications with low switching frequency. Therefore, the first approaches have lower costs, but in the other way, the components' size decreases due to higher frequency. For each approach, the voltage stress on the components can be calculated as follows:

First approaches voltage stress (MOSFET +Series diode):

$$0\le V_{S3,MOSFET}\le V_o-V_{c1} \tag{45}$$

$$-(V_o+V_{in}-V_{c1})\le V_{D3}\le 0 \tag{46}$$

Second approaches voltage stress (an IGBT):

$$-V_{in}\le V_{AB,\,box}=V_{S3,IGBT}\le V_o-V_{c1} \tag{47}$$

3.1.5. Current gain calculation

In order to obtain the current relations and current gain of the proposed converter, the current-second balance principle is applied for capacitors as follows:

$$\frac{1}{T_s}\left(\int_0^{d_1T_s} i_{C,on}+\int_0^{d_2T_s} i_{C,on}+\int_0^{(1-d_1-d_2)T_s} i_{C,off}\right)=0 \tag{48}$$

By substituting current relations of the capacitors in (48), components currents can be obtained as:

$$i_{L3}=i_{L4}=-i_{C3,on}=-i_{C4,on}=I_o \tag{49}$$

$$i_{C3,off}=i_{C4,off}=(d_1+d_1)I_o/(1-d_1-d_2) \tag{50}$$

$$i_{Co,off}=I_o(d_1+d_2)/(1-d_1-d_2) \tag{51}$$

$$i_{C1,on}=2I_o \tag{52}$$

$$i_{L1}=i_{L2}=-i_{C1,off}=2I_o(d_1+d_2)/(1-d_1-d_2) \tag{53}$$

The input current can be calculated as:

$$I_{in}=\frac{1}{T_s}\left(\int_0^{d_1T_s}(i_{L1}+i_{L2}+i_{C1.on})+\int_0^{d_2T_s}(i_{L1})+\int_0^{(1-d_1-d_2)T_s}(i_{L1})\right) \tag{54}$$

By substituting (52) and (53) in (54), the input current can be achieved as follows:

$$I_{in}=I_o(4d_1+2d_2)/(1-d_1-d_2) \tag{55}$$

3.1.6. Components' current analysis

According to (14), switches currents (i_{S1} and i_{S2}) can be calculated as follows:

$$i_{S1,2,on}=2I_o/(1-d_1-d_2) \tag{56}$$

Using (22), the AB's current can be written as:

$$i_{AB}=i_{S3}=i_{D3}=2I_o/(1-d_1-d_2) \tag{57}$$

Considering (32) and (33), the diode current can be obtained as (58).

$$i_{D1}=i_{D2}=I_o/(1-d_1-d_2) \tag{58}$$

To calculate the RMS and average current through the switches and diodes, the following equations can be used:

$$I_{rms}=\sqrt{\frac{1}{T_s}\left(\int_0^{d_1T_s} i(t)^2dt+\int_0^{d_2T_s} i(t)^2dt+\int_0^{(1-d_1-d_2)T_s} i(t)^2dt\right)} \tag{59}$$

$$I_{avg}=\frac{1}{T_s}(i_{mode1}(t)d_1+i_{mode2}(t)d_2+i_{mode3}(t)(1-d_1-d_2)) \tag{60}$$

Based on these equations, the RMS and average currents of the power semiconductors can be achieved as follows:

$$I_{rms_{S1}}=I_{rms_{S2}}=2I_o\sqrt{d_1}/(1-d_1-d_2) \tag{61}$$

$$I_{rms_{S3}}=I_{rms_{D3}}=2I_o\sqrt{d_2}/(1-d_1-d_2) \tag{62}$$

In addition, the RMS and average currents of the diodes D_1 and D_2 are obtained as:

$$I_{rms_{D1}}=I_{rms_{D2}}=I_o/\sqrt{1-d_1-d_2} \tag{63}$$

$$i_{av_{D1}}=i_{av_{D2}}=I_o \tag{64}$$

Furthermore, Capacitors' and inductors' RMS currents can be calculated as below:

$$I_{rms_{C1}}=2I_o\sqrt{d_1+d_2}/\sqrt{1-d_1-d_2} \tag{65}$$

$$I_{rms_{C3}}=I_{rms_{C4}}=I_{rms_o}=I_o\sqrt{d_1+d_2}/\sqrt{1-d_1-d_2} \tag{66}$$

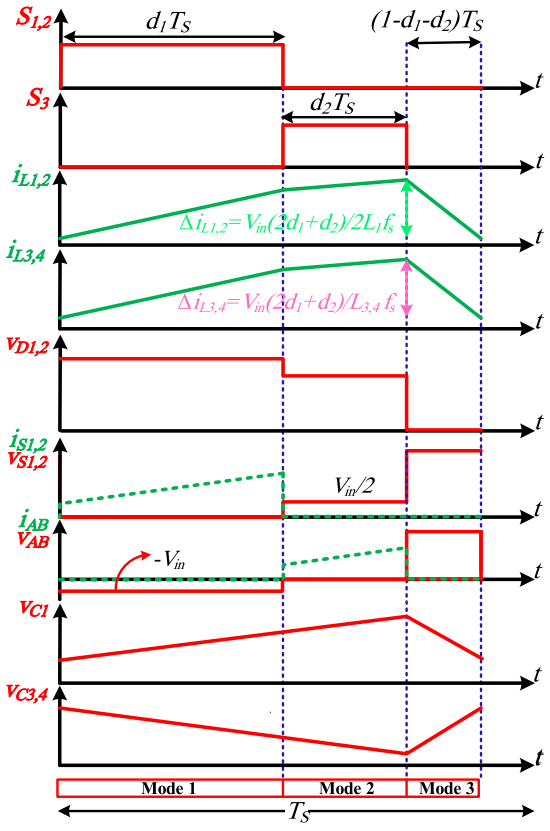


Fig. 3. Fundamental waveforms of the presented topology in the CCM operation.

$$I_{rms_{L1}} = I_{rms_{L2}} = 2I_o\,(d_1 + d_2) \,/\, (1 - d_1 - d_2) \tag{67}$$

$$I_{rms_{L3}} = I_{rms_{L4}} = I_o \tag{68}$$

The key theoretical waveforms of the proposed converter are illustrated based on the obtained relations in Fig. 3.

3.2. Discontinuous conduction mode (DCM) analysis

Fig. 4 shows the DCM switching pulses and inductors current ($i_{L1,2}$). In the DCM operation, modes 1, 2, and 3 are similar to CCM operation. As depicted, the inductors' current i_{L1} and i_{L2} reach zero at the end of the third operational mode (d_3T_s). In the fourth time intervale ((1-d_1 − d_2 − d_3)T_s), inductors current i_{L1} and i_{L2} equal zero, and all the switches and diodes are turned off and reversed biased.

The inductors L_1 and L_2 current ripple in the DCM operation equal the maximum current. Therefore, it can be written:

$$I_{L1,peak} = I_{L2,peak} = I_{Lx,peak} = \frac{V_{in}\,(2d_1 + d_2)}{2L_x f_s} = \frac{(V_o - V_{in} - V_{C1})\,(d_3)}{2L_x f_s} \tag{69}$$

The time intervale d_3 equals:

$$d_3 = \frac{V_{in}\,(2d_1 + d_2)}{(V_o - V_{in} - V_{C1})} \tag{70}$$

On the other hand, the current of the capacitor C_1 in each mode is obtained as follows:

$$\begin{aligned} i_{C1,mode1} &= i_{C1,mode2} = 2I_o \\ i_{C1,mode3} &= -I_{L1,2} = -I_{Lx} \\ i_{C1,mode4} &= 0 \end{aligned} \tag{71}$$

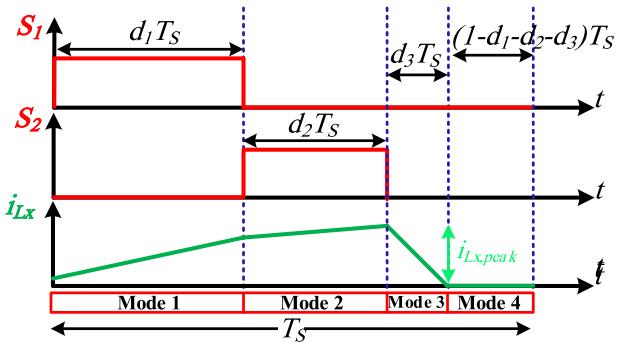


Fig. 4. Switching pulses and inductors' current ($i_{L1} = i_{L2} = i_{Lx}$) in the DCM operation.

By applying the current balance principle for C_1, the following relation is achieved for I_{Lx}.

$$2I_o(d_1 + d_2) - I_{Lx}d_3 = 0 \tag{72}$$

Therefore, I_{LX} is equal to:

$$I_{Lx} = \frac{2I_o(d_1 + d_2)}{d_3} = \frac{2V_o(d_1 + d_2)}{R_o d_3} \tag{73}$$

If assumed $I_{LX} = I_{L,peak}/2$, then $I_{L,peak}$ can be obtained as:

$$I_{Lx,peak} = 2I_{Lx} = \frac{4V_o(d_1 + d_2)}{2R_o d_3} \tag{74}$$

Another equation for the time intervale d_3 is achieved as follows:

$$d_3 = \frac{8V_o L_x f_s (d_1 + d_2)}{R_o V_{in}\,(2d_1 + d_2)} \tag{75}$$

Using equations obtained for d_3, the voltage gain in the DCM operation is calculated as follows:

$$G_{DCM} = \frac{V_o}{V_{in}} = \frac{(2d_1 + d_2)}{2}\sqrt{\frac{1}{\tau_{DCM}(d_1 + d_2)}} \tag{76}$$

where τ_{DCM} is equal to:

$$\tau_{DCM} = \frac{L_x f_s}{R_o} \tag{77}$$

3.3. Boundary condition mode (BCM) analysis

As voltage gain of the CCM and DCM are achieved, these voltages' regions can be separated by boundary condition mode (BCM). An area between CCM and DCM operation is called BCM. To specify this region and achieve τ_{BCM}, the CCM and DCM voltage gain equations should be equal. Therefore, τ_{BCM} can be calculated as:

$$G_{CCM} = G_{DCM} \Rightarrow \frac{4d_1 + 2d_2}{1 - d_1 - d_2} = \frac{(2d_1 + d_2)}{2} \times \sqrt{\frac{1}{\tau_{DCM}(d_1 + d_2)}} \Rightarrow \tau_{BCM} = \frac{(2d_1 + d_2)^2}{4\,(d_1 + d_2)\,G_{CCM}^2} \tag{78}$$

Fig. 5 shows variations of τ_{BCM} versus duty cycle d_1. The figure displays the CCM, DCM, and BCM regions for three values of duty cycle d_2. In this figure, the below area of the BCM curve is the DCM region, and the upper area of the BCM curve is related to the CCM operation.

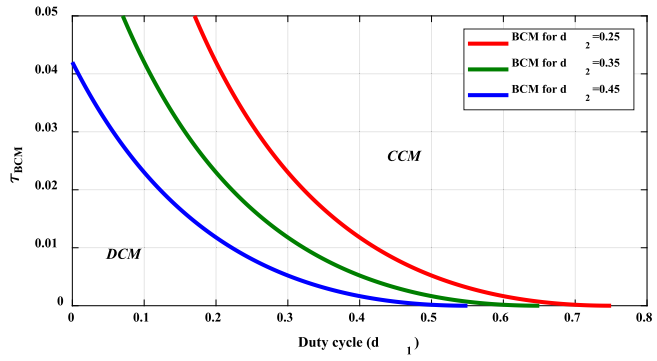


Fig. 5. The CCM, DCM, and BCM regions for the proposed topology.

4. Design considerations

In order to utilize the proposed converter with its best performance, its elements should be selected based on optimum design. Therefore, a comprehensive design of different components has been presented in this section. Parameters design is divided into two subsections: one section for inductors design and another section for capacitors design.

4.1. Inductor design

To find the optimum range of input inductors (L_1 and L_2), in time intervals d_1T_S and d_2T_S, these relations can be written:

$$V_{in} = V_{L1} = L_1 \Delta {i_{L1}}^{\mathrm{I}} / d_1 T_s \tag{79}$$

$$V_{in} = 2L_1 \Delta {i_{L1}}^{\mathrm{II}} / d_2 T_s \tag{80}$$

The upper indices I and II in Δi_{L1} represent the current ripple of L_1 in the first and second operational modes, respectively. By simplifying these relations, the inductors' current ripple can be obtained as:

$$\Delta i_{L1.2} = \Delta {i_{L1}}^{\mathrm{I}} + \Delta {i_{L1}}^{\mathrm{II}} = V_{in}\,(2d_1 + d_2) \,/ 2 f_s L_{1,2} \tag{81}$$

In the third operational mode (1-$d_1 - d_2$)T_S, the capacitors' C_3 and C_4 voltages have been clamped on the inductors L_4 and L_3, respectively. As a result, this relation can be obtained:

$$V_{C4} = -V_{L3} = -L_3 \Delta {i_{L3}}^{\mathrm{III}} / (1 - d_1 - d_2) T_s \tag{82}$$

where $\Delta {i_{L3}}^{\mathrm{III}}$ represents the current ripple of the inductor L_3. The current ripple of the inductors L_3 and L_4 in the time interval (1-$d_1 - d_2$)T_S can be calculated as:

$$\left|\Delta i_{L3,4}\right| = V_{C4,3}(1 - d_1 - d_2) / f_s L_{3,4} \tag{83}$$

where $\Delta i_{L3,4}$ represents current ripple of the inductors L_3 and L_4. To operate the proposed converter in the continuous conduction mode (CCM), condition $i_L \geq (\Delta i_L / 2)$ should be fulfilled. By applying this condition, the following relations are obtained:

$$L_{1,2} \geq (V_{in}(2d_1 + d_2)(1 - d_1 - d_2)) \,/\, (8 f_s I_o (d_1 + d_2)) \tag{84}$$

$$L_{3,4} \geq (V_{in}(2d_1 + d_2)) \,/ 2 f_s I_o \tag{85}$$

Furthermore, the relations above can be rewritten based on output power, switching frequency, duty cycles, and output voltage as follows:

$$L_{1,2} \geq \left(V_o^2 (1 - d_1 - d_2)^2\right) \,/\, (16 f_s P_o (d_1 + d_2)) \tag{86}$$

$$L_{3,4} \geq \left(V_o^2 (1 - d_1 - d_2)\right) / 4 f_s P_o \tag{87}$$

4.2. B. Capacitors design

Considering (49) and (51), the capacitors C_3, C_4, and C_o ranges can be obtained as:

$$C_{3,4} \geq I_o\,(d_1 + d_2) \,/ \Delta v_{C3,4} f_s \tag{88}$$

$$C_o \geq I_o\,(d_1 + d_2) \,/ \Delta v_{Co} f_s \tag{89}$$

According to (52), the capacitor C_1 range can be calculated based on the voltage ripple as follows:

$$i_{C1,on} = C_1 \Delta v_{C1} / (d_1 + d_2) T_s = 2 I_o \tag{90}$$

$$C_1 \geq 2 I_o\,(d_1 + d_2) \,/ \Delta v_{C1} f_s \tag{91}$$

5. Efficiency analysis

This section has calculated the power losses of different components, including power switches, diodes, capacitors, and inductors to analyze power efficiency. Then, the proposed converter's total losses and power efficiency are achieved.

5.1. Switches' power losses

The switches losses include two categories: switching losses and conduction losses. Consequently, the power switches losses can be described as follows:

$$P_S = P_{Sw} + P_{rS} = \sum_{i=1}^{3} P_{Sw_i} + \sum_{i=1}^{3} r_{Si} I_{rms_i}^2 \tag{92}$$

P_S, P_{rS}, and P_{SW} represent the total losses of the switches, switches conduction losses, and switching losses, respectively. Therefore, the switching losses (Marzang et al., 2020a) can be expressed as (73).

$$P_{Sw} = \frac{1}{2} f_s \sum_{i=1}^{3} \left[V_{Si} i_{av,Si} \left(t_r + t_f\right) + C_{oss_i} {V_{Si}}^2\right] \tag{93}$$

where t_r, t_f, and C_{oss} represent the switches' rise time, fall time, and parasitic output capacitance, respectively.

Consequently, the internal resistance losses can be determined as (77)–(79).

$$P_{r_{S1}} = r_{S1} I_{rms_{S1}}^2 \tag{94}$$

$$P_{r_{S2}} = r_{S2} I_{rms_{S2}}^2 \tag{95}$$

$$P_{r_{S3}} = r_{S3} I_{rms_{S1}}^2 \tag{96}$$

where r_{S1}, r_{S2}, and r_{S3} are the internal resistances of the power switches S_1, S_2, and S_3, respectively. Therefore, the total conduction losses of the switches can be obtained as (80).

$$P_{rS} = P_{rS1} + P_{rS2} + P_{rS3} \tag{97}$$

5.2. Diodes' power losses

The power losses related to power diodes can be divided into two categories.

First, conduction losses of the diodes are calculated from their internal resistances and their effective currents as follows:

$$P_{r_{D1}} = r_{D1} I_{rms_{D1}}^2 \tag{98}$$

$$P_{r_{D2}} = r_{D2} I_{rms_{D2}}^2 \tag{99}$$

In these relations, r_{D1} and r_{D2} are the internal resistances of the power diodes D_1 and D_2, respectively. Second, forward voltage drop losses of reverse biasing. These losses can be calculated from power diodes voltage drop and their average currents as:

$$P_{VF_{D1}} = V_{F_{D1}} I_{av} = V_{F_{D1}} I_o \tag{100}$$

Table 1
Comparison of the proposed topology and other similar structures.

Ref.	Voltage gain	Max. normalized voltage stress across the power		$V_{in}/Vout$	P_{out} [W]	Eff. [%]	Freq [Hz]	Number of $S.^*/D.^*/L.^*/C.I.^*/C.^*/T.^*$	Input current ripple
		Switches (Vs/Vo)	Diodes (V_D/Vo)						
Lakshmi and Hemamalini (2018)	$(1+d_1)/(1-d_1-d_2)$	1	$(M+1)/M$	20/200	120	93.7	50	3/2/2/–/1/8	Pulsating
Sagar Bhaskar et al. (2019)	$(2-d_2)/(1-d_1-d_2)$	$(M-1)./M$	$(M-1)/M$	38/400	500	95.4	50	3/3/2/–/2/10	Pulsating
Bhaskar et al. (2019)	$(3-d_1-2d_2)/(1-d_1-d_2)$	$(M-2)./M$	$(M-1)/M$	36/400	500	92.9	50	3/4/2/–/3/12	Pulsating
Maroti et al. (2019b)	$(2)/(1-d_1-d_2)$	0.5	1	30/400	500	94.7	50	3/3/2/–/2/10	Pulsating
Maroti et al. (2019a)	$(3-d_1-d_2)/(1-d_1-d_2)$	0.5	1	30/400	500	96.8	50	3/4/2/–/3/12	Pulsating
Salvador et al. (2018)	$(1+3d)/(1-d)$	$(M+3)/4M$	$(M+3)/2M$	20/260	200	94.3	50	2/2/3/–/3/10	Pulsating
Yang and Liang (2012)	$(1+d)/(1-d)$	$(M+1)/M$	–	14/42	200	92.7	50	3/0/0/1/1/5	Pulsating
Yang et al. (2009)	$(1+d)/(1-d)$	$(M-1)/2M$	$(M+1)/M$	12/100	40	90.8	100	2/1/2/–/1/6	Pulsating
Haji-Esmaeili et al. (2018)	$(2+d)/(1-2d)$	$(2M+1)/5M$	$(2M+1)/5M$	24/365	200	90.4	40	1/5/3/–/7/16	Pulsating
Babaei et al. (2018), n = 2	$(1+7d)/(1-d)$	$(3M+1)/4M$	$(M+1)/M$	30/160	200	95.6	20	4/16/8/–/1/29	Pulsating
Axelrod et al. (2008), n = 3	$3/(1-d)$	0.33	0.33	50/300	140	90	100	1/5/1/–/5/12	Non-Pulsating
Mashinchi Maheri et al. (2017), n = 2	$(1+3d)/(1-d)$	$(3M+1)/4M$	$(M+1)/M$	30/160	200	96	10	4/4/4/–/1/13	Pulsating
Nouri et al. (2014), n = m = 1	$(3+3d)/(1-d)$	$(M+4)/3M$	$(2M+8)/9M$	29/357	65.5	92	24	1/6/2/–/6/15	Discontinues
Chen et al. (2020), n = 1	$(5+d)/(1-d)$	$(M+1)/6M$	$(M+1)/3M$	25/400	200	93.5	100	1/6/–/1/6/14	Pulsating
Freitas et al. (2021), n = 2	$(3+d)/(1-d)$	$(M+1)/4M$	$(M+1)/2M$	26/380	200	94.35	50	1/4/1/1/5/12	Non-Pulsating
P^*	$2(2d_1+d_2)/(1-d_1-d_2)$	$(M+2)/2M$	$(M+4)/2M$	400/23.5	500	93	50	3/3/–/2/4/12	Pulsating

S^*: Switch, D^*: Diode, L^*: Inductor, C^*: Capacitor, $C.I^*$: Coupled Inductor, T^*: Total, P^*: Proposed

$$P_{VF_{D2}} = V_{F_{D2}} I_{av} = V_{F_{D2}} I_o \tag{101}$$

Therefore, the diodes' total losses can be described as:

$$P_D = P_{r_{D2}} + P_{r_{D2}} + P_{VF_{D1}} + P_{VF_{D2}} \tag{102}$$

5.3. Capacitors' power losses

Considering r_{C1}, r_{Co}, r_{C3}, and r_{C4} as internal resistance of C_1, C_o, C_3, and C_4, respectively. Thus, the total capacitors' power loss is achieved as follows:

$$P_C = r_{C1} I^2_{rms_{C1}} + r_{C3} I^2_{rms_{C3}} + r_{C4} I^2_{rms_{C4}} + r_{Co} I^2_{rms_{Co}} \tag{103}$$

Considering r_{L1}, r_{L2}, r_{L3}, and r_{L4} as the internal resistances of the inductors L_1, L_2, L_3, and L_4, respectively, the total conduction losses of the inductors can be described as follows:

$$P_L = r_{L1} I^2_{rms_{L1}} + r_{L2} I^2_{rms_{L2}} + r_{L3} I^2_{rms_{L3}} + r_{L4} I^2_{rms_{L4}} \tag{104}$$

In addition to the conduction losses, the inductor losses contain a loss that depends on magnetic cores. This type of loss is constant for a given condition and can be determined from the utilized magnetic cores datasheets (Marzang et al., 2020a; Alavi et al., 0000).

$$P_{Core1} = \left(P_{Core,\,L_{1,2}} \times f_s\right) / 100 \tag{105}$$

$$P_{Core2} = \left(P_{Core,\,L_{3,4}} \times f_s\right) / 100 \tag{106}$$

Thus, the total core losses are defined as:

$$P_{Core} = P_{Core1} + P_{Core2} \tag{107}$$

As a result, the total losses of the proposed converter can be obtained as follows:

$$P_{losses} = P_S + P_D + P_C + P_L + P_{Core} \tag{108}$$

Also, the proposed converter's efficiency is achieved as follows:

$$\eta = 100 / \left(1 - \left(P_{losses} / P_o\right)\right)\% \tag{109}$$

6. Comparison results

This section compares the proposed converter and other similar structures. This comparison is made regarding the voltage gain, maximum normalized voltage stress across the power switches/diodes, output/input voltage, output power, efficiency, frequency, number of components, and input current ripple. The results of this comparison are shown in Table 1.

Input current ripple is divided into two categories continuous and discontinuous. Also, continuous input current ripple has two types pulsating and non-pulsating. In Table 1, all topologies have pulsating input current ripple except (Axelrod et al., 2008; Freitas et al., 2021; Nouri et al., 2014), which have continuous (non-pulsating) and discontinuous input current ripple, respectively.

The voltage gain variation of the proposed converter versus the duty cycles is shown in Fig. 6(a). For most duty cycle values, the voltage gain of the proposed converter with $d_2 = 0.35$ is more remarkable than in other structures. Still, in some duty cycles, the voltage gain of the proposed converter is lower than (Haji-Esmaeili et al., 2018; Nouri et al., 2014; Chen et al., 2020). The total components number in Haji-Esmaeili et al. (2018), Nouri et al. (2014), and Chen et al. (2020) is significantly more than the proposed structure. Moreover, the presented topology in Haji-Esmaeili et al. (2018) suffers from duty cycle limitation ($d \leq 0.5$).

Fig. 6(b) demonstrates the voltage gain variations versus the continuous value of d_2 and discontinuous values of d_1. Also, the voltage gain of the proposed topology is compared with structures (Haji-Esmaeili et al., 2018; Chen et al., 2020). This figure indicates that the proposed converter's voltage gain can be increased by changing the ratio of duty cycles d_1 and d_2. Using this feature makes the voltage gain of the proposed topology higher than structures (Haji-Esmaeili et al., 2018; Chen et al., 2020). As a result, this figure reflects the flexibility of the presented topology's voltage gain in providing desired voltage gain with different combinations of duty cycles. Anyway, Fig. 6(a) and (b) prove the high voltage gain capability of the proposed topology.

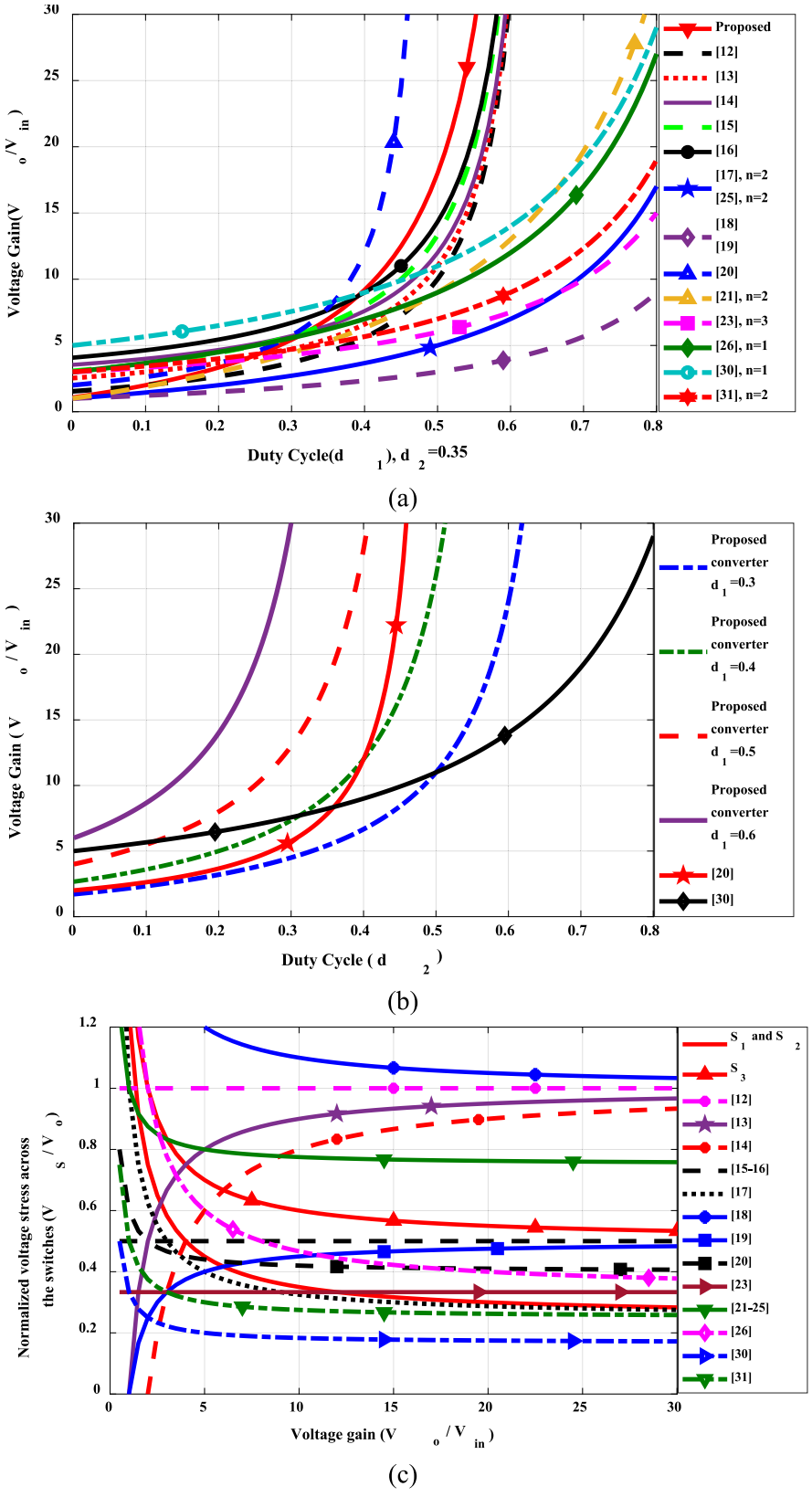


Fig. 6. Presented topology and other similar structures comparison in terms of: (a) voltage gain, (b) voltage gain with continuous variations of d_2 and discontinuous variations of d_1 with structures (Haji-Esmaeili et al., 2018; Chen et al., 2020), (c) maximum normalized voltage stress on the switches.

According to these figures, the proposed converter can provide even ultra-high step-up voltage gain without extreme values of duty cycles.

The power switch voltage stress in the conventional boost converter equals the output voltage. Also, this defect exists in structures (Lakshmi and Hemamalini, 2018; Yang and Liang, 2012), but

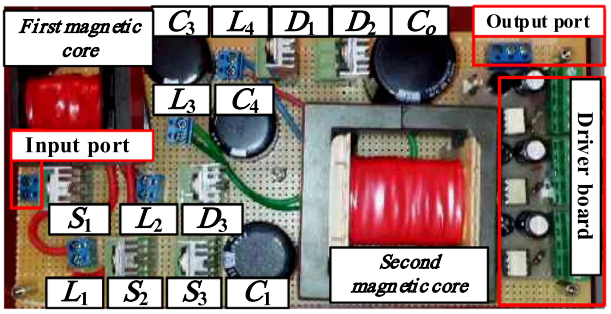


Fig. 7. Prototype of the proposed topology.

Table 2
Specifications of the proposed converter.

Parameter	Value
Input voltage/Output voltage	23.5 V/400 V
Output power	500 W
Frequency	50 kHz
Duty cycle	$d_1 = 0.5$ and $d_2 = 0.35$
$L_{1,2}$, (E32)	85 μH, $r_{L1,2} = 10$ mΩ, $\Delta i_{L1,2} = 3.2$ A
$L_{3,4}$ (E55)	1.5 mH, $r_{L3,4} = 0.17$ Ω, $\Delta i_{L3,4} = 0.4$ A
Capacitors	C_1:22 μF, $C_{3,4}$:10 μF, $r_C = 20$ mΩ
Output capacitor	C_o:220 μF (450 V), $\Delta v_{co} = 0.1$ V, $r_C = 40$ Ω
$S_{1,2}$ (IRFB4321Pbf)	$r_{DS(on)=}$12 mΩ, $t_r = 60$ nS, $t_f = 35$ nS, $C_{oss} = 390$ pF
S_3 (IRFB4229Pbf)	$r_{DS(on)=}$38 mΩ, $t_r = 21$ nS, $t_f = 31$ nS, $C_{oss} = 390$ pF
Diodes	$D_{1,2}$: SBR10U300CT, $r_D = 20$ mΩ, $V_F = 0.64$ V D_3: SBR30U300CT, $r_D = 30$ mΩ, $V_F = 0.76$ V

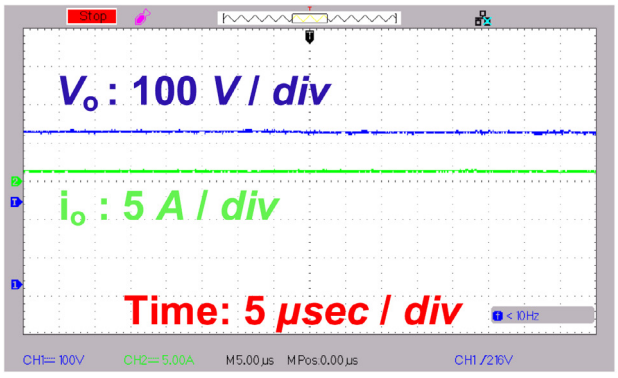
VMC and C1 decrease the voltage stress on the power switches in the proposed converter. Fig. 6(c) shows comparison results of the normalized

voltage stresses across the power switches. This figure illustrates that the voltage stresses across the switches (S_1 and S_2) are near the minimum voltage stress value on the other structures. In addition, the voltage stress on switch S_3 is lower than structures (Lakshmi and Hemamalini, 2018; Sagar Bhaskar et al., 2019; Bhaskar et al., 2019; Yang and Liang, 2012; Babaei et al., 2018; Mashinchi Maheri et al., 2017). As a result, it is possible to utilize the power switches with a low range of $r_{DS(on)}$ in this converter, which improves the presented topology's efficiency.

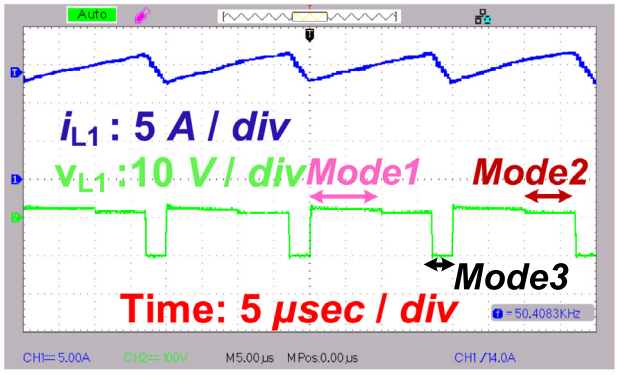
7. Experimental results

A laboratory prototype of the proposed converter is built to verify the mathematical analyses, as illustrated in Fig. 7. Also, details of the components are gathered in Table 2. The practical waveforms have been extracted, and the achieved experimental waveforms are shown in Fig. 8. The duty cycle of switches S_1 and S_2 is 50%, and the duty cycle of S_3 is 35%. Based on these duty cycles and Eq. (41), the theoretical voltage gain of the proposed converter is equal to 18.

Fig. 8(a) illustrates the proposed converter's output voltage and output current waveforms, which equal 400 V and 1.25 A, respectively. Fig. 8(b) shows the voltage and current waveforms of the inductor L_1. As can be seen, the inductor voltage is positive during the first and second modes. As a result, the inductor's current slope is positive during these operational modes (according to Eqs. (6) and (19)). The inductor voltage reaches negative values in the third operating mode, and its current decreases with a negative slope (25). The voltage and current waveforms of inductor L_3 are shown in Fig. 8(c). According to this figure, it is evident that the inductor is charged in modes one and two. Also, it gets discharged in the third operating mode. The duty cycle



(a)



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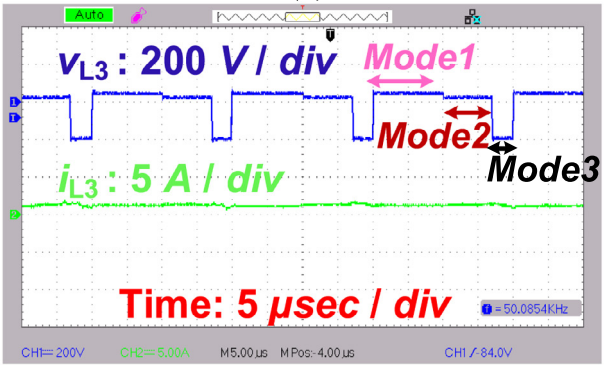
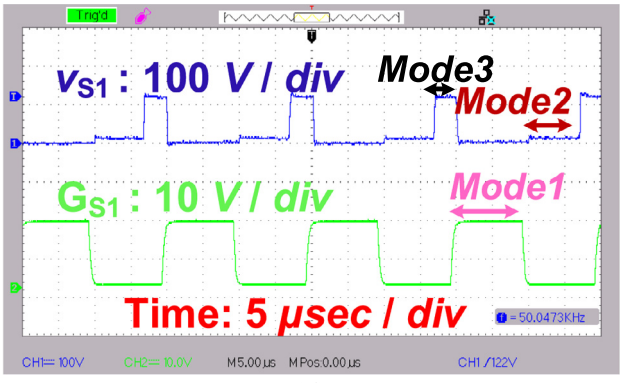
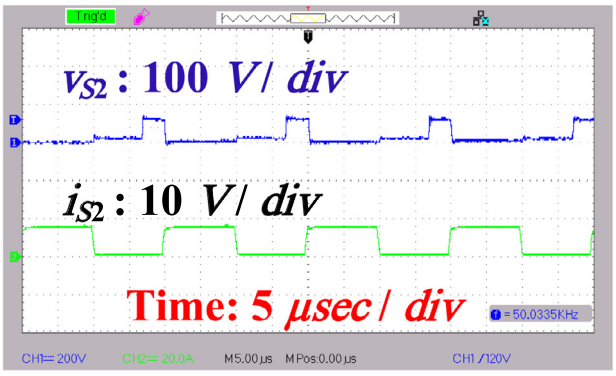


(c)

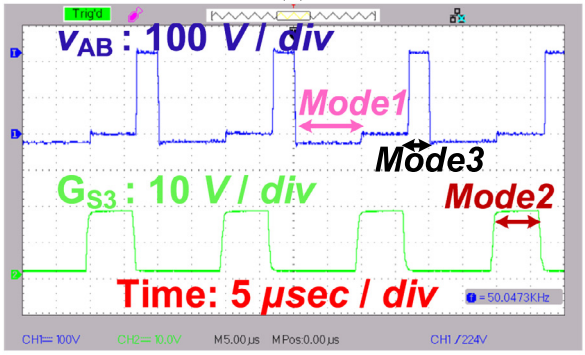


(d)

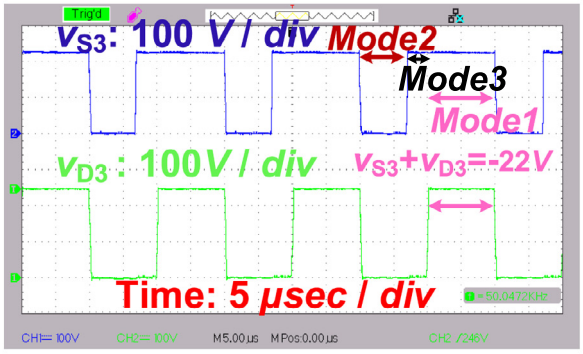
Fig. 8. Experimental waveforms of: (a) V_o and i_o, (b) i_{L1} and v_{L1}, (c) i_{L3} and v_{L3}, (d) v_{S1} and G_{S1}, (e) v_{S2} and i_{S2}, (f) v_{AB} and G_{S3}, (g) v_{S3} and v_{D3}, (h) v_{D2} and V_{C1}.



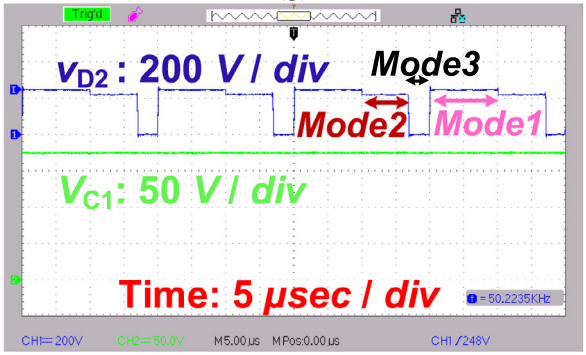
(e)



(f)



(g)



(h)

Fig. 8. (*continued*).

(d_1) and voltage waveforms of the power switch S_1 are shown in Fig. 8(d). As shown, the duty cycle is 50% ($d_1 = 0.5$), and the voltage stress equals 121 V, which verifies the theoretical relations ((23) and (30)). The voltage and current stress waveforms across the power switch S_2 are illustrated in Fig. 8(e). As depicted, voltage stress across switch S_2 is similar to V_{S1} (Fig. 8(d)) and equal to 121 V. Also, maximum current stress across S_2 equals 16 A. The voltage waveform across the AB point and the utilized switching pulses for its power switch is illustrated in Fig. 8(f). This figure proves that the duty cycle is 35% ($d_2 = 0.35$). Also, the voltage stress between the AB point is negative, and its maximum voltage stress is measured at 224 V, which proves the theoretical calculations ((16) and (31)). As mentioned in this paper, the AB branch is implemented by a power MOSFET (S_3) and a power diode (D_3). The experimental voltage waveforms of these elements have been illustrated in Fig. 8(g). In the first and second modes, the summation of power MOSFET and power diode voltages ($V_{S3} + V_{D3}$) equals $-V_{in}$ that verifies (16). Also, the power MOSFET voltage equals the AB box voltage in mode three. Finally, the voltage waveforms of the power diode D_2 and capacitor C_1 are depicted in Fig. 8(h).

Furthermore, a comparison of theoretical and experimental values is provided in Table 3. In this table, the comparison is done under similar condition ($V_{in} = 23.5$ V, $d_1 = 0.5$, $d_2 = 0.35$). Also, it compares the calculated, simulated, and measured values of output voltage, capacitors voltages, and voltage stress across the power semiconductors.

The next step to evaluate the quality of the proposed converter is comparing practical, simulation, and theoretical efficiencies. Table 4 shows the theoretical efficiency and distribution of power losses at 500 W output power. This table shows the RMS and average values of currents, internal resistances, core losses, forward voltage drop, switching losses of different components, and the percentage of losses in each element. As can be seen, almost 38% of the total losses depend on the switches' losses (switching losses and internal resistance losses). The inductors' total losses are nearly 39%, and the first coupled inductor losses are more than the second coupled inductor losses. In addition, the calculated efficiency and total power losses at 500 W output power are equal to 95.74% and 22.23 W, respectively.

Furthermore, the efficiency of the proposed converter is investigated in Fig. 9. In this figure, a comparison between the experimental and theoretical power efficiency with two different values of input voltage is illustrated. As depicted, the experimental efficiency at 500 W–23.5 V equals 94.5%. Here, it is evident that increasing the input voltage increases power efficiency. The maximum practical power efficiencies of the proposed structure are obtained at 300 W–23.5 V and 400 W–41.6 V and are equal to 95.02% and 96%, respectively.

8. Conclusion

This paper presents a new topology for high step-up non-isolated DC–DC converters. The ASL and VMC techniques in the proposed converter provide high voltage gain and low voltage stress across the power switches. Also, the implemented VMC unit decreases the switches' voltage stress in this converter. In addition, implementing two different duty cycles for the utilized power switches makes it possible to provide the desired high voltage gain with low values of duty cycles. Furthermore, operational modes, mathematical analysis, and efficiency calculations are analyzed in detail. From the comparison of the proposed converter with the state-of-the-art converters reported in the literature, it can be concluded that the voltage stresses across the power switches are low. Consequently, high power efficiency of the proposed converter can be realized by using including cheap and efficient switches. Finally, a laboratory prototype having power rating of 500 W and operating at switching frequency of 50 kH is assembled to validate the analytical findings reported in this paper.

Table 3
Experimental, simulation, and theoretical voltages values.

Parameter	Calculation	Simulation	Experimental
Output voltage (V_o)	423 V	412 V	400 V
Capacitors voltage (V_{C3} and V_{C4})	211.5 V	205.4 V	199.6 V
Capacitor voltage (V_{C1})	188 V	181.7 V	175 V
Voltage stress on the switches S_1 and S_2	129.25 V	128 V	121.7 V
Voltage stress on the *AB* Box	235 V	232 V	224 V
Voltage stress across the S_3	435 V	230 V	223 V
Voltage stress across the D_3	458.5 V	250 V	246 V
Voltage stress on the Diodes ($D_{1,2}$)	458.5 V	255 V	249.3 V

Table 4
Measured efficiency and distribution of power losses.

Type	i_{RMS}	I_{Avg}	Power losses due to				Losses [%]
			ESR	P_{Core}	V_F	Switching	
$S_{1,2}$	4.56	8.33	0.2500		–	2.5664	26.75%
S_3	3.82	5.83	0.5542		–	2.1676	11.02%
$D_{1,2}$	3.23	1.25	0.2083		0.8	–	9.04%
D_3	3.82	5.83	0.4375		0.95	–	6.22%
$L_{1,2}$	14.2	–	2.0069	1.1	–	–	22.93%
$L_{3,4}$	1.25	–	0.2656	3.4	–	–	17.63%
C_1	5.95	–	0.7083		–	–	
$C_{3,4,}$	2.98	–	0.1771		–	–	6.35%
C_o	2.98	–	0.3542		–	–	
$V_o = 400$ V, $P_o = 500$ W, $P_{losses} = 22.23$ W and $\eta = 95.74\%$							

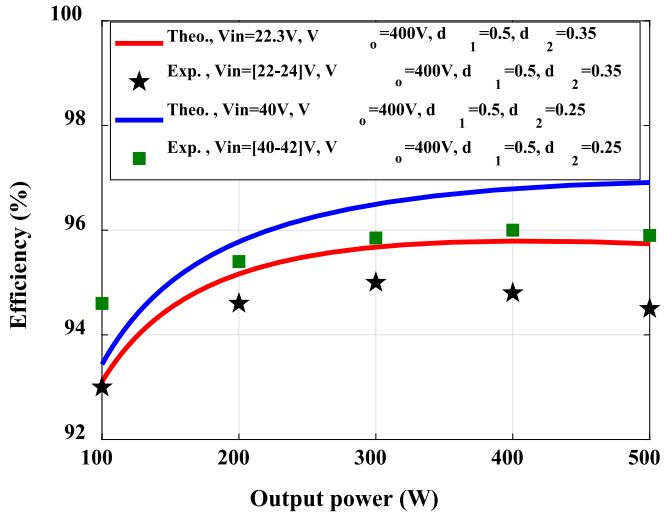


Fig. 9. Theoretical and experimental efficiency of the proposed converter versus output power.

CRediT authorship contribution statement

Vafa Marzang: Investigation, Conceptualization, Formal analysis, Resources, Software, Writing – original draft. **Ebrahim Babaei:** Project administration, Conceptualization, Validation, Supervision, Writing – review & editing. **Hasan Mehrjerdi:** Validation, Resources, Visualization, Data Curation, Formal analysis, Writing – review & editing. **Atif Iqbal:** Validation, Resources, Visualization, Data Curation, Formal analysis, Writing – review & editing. **Shirazul Islam:** Validation, Resources, Visualization, Data Curation, Formal analysis, Writing - review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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