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A New Non-Isolated High-Gain Single-Switch DC–DC Converter Topology with a Continuous Input Current

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Abstract: An ultra-high step-up, non-isolated DC–DC converter with a continuous input current was developed as a result of this research. This converter's architecture consists of a voltage multiplier cell (VMC), a positive output super lift Luo converter (POSLLC), and a quadratic boost converter (QBS) (also referred to as a cascaded boost topology (CBT)). Thus, the bold points of the topologies mentioned earlier enhance the voltage gain of the proposed topology. It is important to note that when the duty cycle is at 50%, the converter attains a voltage gain of ten. Additionally, the constant input current of the topology reduces the current stress on the input filter capacitor. This converter's topology was investigated and studied under various operating conditions: ideal and non-ideal modes, as well as continuous and discontinuous current modes (CCM/DCM). The converter's efficiency and voltage gain were also compared to those of newly proposed converters. PLECS and MATLAB software tools were used in the investigation of the proposed topology. A 200 V/200 W prototype was constructed. The experimental results validated the theoretical study and the simulation results. The extracted efficiency was 91%.

Keywords: DC–DC converters; high gain converters; non-isolated DC–DC converters

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1. Introduction

There are two basic topologies for DC–DC converters: isolated and non-isolated types [1–5]. The isolated types use a high-ratio high-frequency transformer to boost the voltage gain of the converter [6–9]. Furthermore, the transformer makes galvanic isolation between the source and the load and therefore better safety than the non-isolated converters [7]. However, using transformers increases the current stress on the switches and necessitates snubbers, which adds to the complexity, EMI noises, volume, and bulk [8]. As a result, non-isolated converters are a better alternative when the load does not need to be isolated from the source [9]. Theoretically and in an ideal case, the simple boost converter can increase its input voltage for all duty cycle values. However, in practical and non-ideal cases, high-duty cycle values dramatically reduce the efficiency and increase the voltage/current stresses on semiconductors. Furthermore, a substantial duty cycle percentage diminishes the diode's activation time. It is important to know that the diode's reverse recovery time prevents the diode from being quickly triggered. Consequently, the high-duty cycle is not appropriate for increasing the voltage gain in a simple boost converter. Therefore, other boost topologies are required for high step-up converters [10–17]. Other traditional structures that address some of the drawbacks of the boost converter are the Cuk, SEPIC, and Zeta converters. While the Cuk converter offers continuous input and output currents, the SEPIC converter only offers a continuous input current, and the Zeta topology offers a continuous output current. However, when employing a moderate duty cycle, these converters are unable to increase the voltage gain [1–9].

Given the aforementioned rationale, the optimal duty cycle should be around 50%. Thus, in this study, the various topologies will be examined and compared at a 50% duty cycle.

The CBT is a cascaded boost converter, also called a quadratic boost converter (QBC), and is one of these high-gain step-up converters [5,6]. The topology of QBC is illustrated in Figure 1a, it has an input block (IB-QBC) where the input inductor L_1 makes the current drawn from the source smooth. The output block (OB-QBc) is the voltage output filter. When the duty cycle is 50%, the converter provides a voltage gain of four. A ten-times voltage gain requires a higher duty cycle in this converter. The positive output super lift Luo converter (POSLLC), shown in Figure 1b, is another type of step-up converter topology with the continuous input current. Its output block (OB-POSLLC) is composed of two diodes and two capacitors. The ripples in the input current are an issue. We should mention that the voltage gain of the POSLLC is three at the 50% duty cycle. This converter cannot provide a high (i.e., ten) voltage ratio when using a lower duty cycle. The other high gain converter's topology is a voltage multiplier cell (VMC) boost converter; the topology is illustrated in Figure 1c. The input block (IB-VMC) and the output block (OB-VMC) are clearly shown. A voltage ratio of four is obtained for a 50% duty cycle, which is similar to the CBT. The input current continuity is notable, but its ripple is high [1–9].

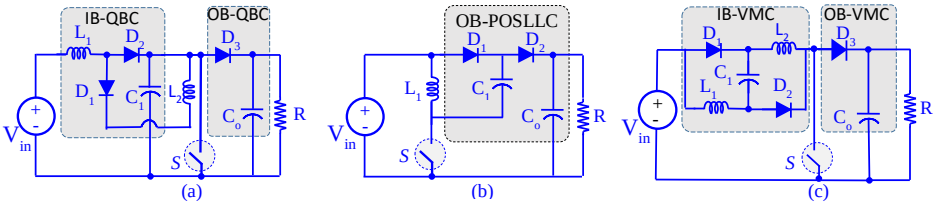

Figure 1. (**a**) Cascaded boost converter, (**b**) positive output super lift Luo converter, (**c**) modified form of the boost converter by a voltage multiplier cell.

The power electronics that researchers have recommended improve topologies due to the shortages of classic topologies. Reference [18] combined the modified boost and POSLLC. The input current continuity remained. However, the use of POSLLC led to an input current ripple increase. The number of semiconductors is another issue in this topology. In other words, two switches are used (besides the three diodes). However, using two switches and more diodes decreases the converter's reliability. We should note that the driving circuits of the MOSFETs are not the same. In other words, one switch is low-sided, and the other is high-sided. A seven-time voltage gain is the result of a 50% duty cycle. The proposed topology in [19] involves a two-switch and three-diode topology. The first inductor of this topology provides the input current continuity. This topology combined the modified boost and classic buck–boost topologies. Such a combination brings the reversed polarity of the output voltage. The voltage gain can provide higher voltage gains besides the duty cycle increasing from 50%. Additionally, the output voltage is four times more than the input voltage, while the duty cycle is 50%. Reference [20] proposed another two-switch–three-diode topology. It combines the modified forms of the boost and POSLL converters. The voltage gain for a 50% duty cycle is the same as [18]. The input current is continuous and appropriate for renewable energy applications. The lack of common ground between the input source and load is an issue in this topology. References [21–23] used quadratic boost structures. Reference [21] used two classic boost topologies. Both boost converters were stacked, and their stacked forms were combined. Such a topology lost the input current continuity. Consequently, the input filter capacitor suffers from dramatic high current stresses. Two MOSFETs and two diodes were the semiconductors used in this topology. A four-time voltage ratio was the result of a 50% duty cycle. Reference [22] proposed another quadratic boost topology. It increased its voltage by replacing the MOSFET of the conventional boost topology with an improved part. However, such an improved part led to a dramatically high diode voltage stress. The number of each component type was the same as in [21]. Reference [23] proposed another quadratic boost topology, combing boost, and Cuk topologies. The number of each component type was 2. Consequently, a low number of components were used. The same

with [22], i.e., the second diode withstood a higher voltage than the output voltage. Notably, higher duty cycle percentages provided higher voltage gains in [21–23]. Reference [24] proposed a high step-up voltage gain based on VMC and a voltage doubler cell (VDC). The base topologies of VMC and VDC (improved) are classic boost topologies. Consequently, the input current was continuous, and the common ground between the input source and load remained. This topology provides a six-time voltage gain by a 50% duty cycle. Reference [25] introduced a simple cascade connection of two boost converters and a VDC. Consequently, it could increase its input voltage to eight times more than itself, while the duty cycle is 50%. This converter uses the boost topologies in the CBT form. The authors of [26] suggested an improved topology of POSLLC. The provided voltage gain provides a five-time voltage gain, while the duty cycle is 50. The input current is continuous. However, the inrush currents of capacitors have increased the input current ripple. Reference [27] recommended another one-switch topology. The conventional buck–boost converter is the base of this topology. Notably, a VMC was replaced with the base topology inductor. Due to base topology shortages, the input current was not continuous. Additionally, the output voltage was reversed. The duty cycle was 50%, and the provided voltage gain was 3. Therefore, the duty cycle must approach unity to provide higher voltage gains. Reference [28] combined a VMC and VDC with a classic boost converter. Therefore, the resulting voltage gain with a 50% duty cycle was eight times. Using VMC instead of the boost converter's inductor increased the input current ripple. Reference [29] used two various VMCs with the conventional boost. The improved VMC was replaced with the converter's inductor. Notably, the input current ripple increased due to the mentioned replacement. Reference [30] combined two conventional boost topologies, VMC and POSLLC. The mentioned VMC was replaced with the inductor of the first boost topology. Consequently, the input current ripple increased. Moreover, the employed POSLLC at the second part led to another inrush current. Notably, the proposed converter in [30] provides a 10-times voltage ratio with a 50% duty cycle.

In this paper, a new topology is proposed to reach a voltage gain of 10 times at a 50% duty cycle. The composition of the proposed ultra-high step-up non-isolated DC–DC topology is depicted in Figure 2a. It is something of a cross between CBT, POSLLC, and VMC topologies, making it suitable as a high step-up converter. The complete circuit of the proposed topology is shown in Figure 2b. The proposed topology has the combined features of the three topologies. The CBT or QBC topology can increase its input voltage to four times when its duty cycle is 50%. Additionally, the POSLLC and VMC use the voltage lift technique to provide a higher voltage gain. The proposed topology is based on all three mentioned converters. CBT is the fundamental part of the proposed converter, and its various blocks have been improved by incorporating the POSLLC, which replaces the output block of the CBT (OB-QBC). In this case, there are two choices to use the VMC: (1) the VMC substitutes the inductor L_1 or L_2 of Figure 2a. Substituting L_1 will increase the input current ripples while substituting the inductor L_2 leads to an increase in the voltage gain and continuity of the input current. The proposed topology is therefore based on the latter approach (see Figure 2b), which employs a double voltage lift technique, allowing for a very high-voltage gain while ensuring input current continuity and small ripples.

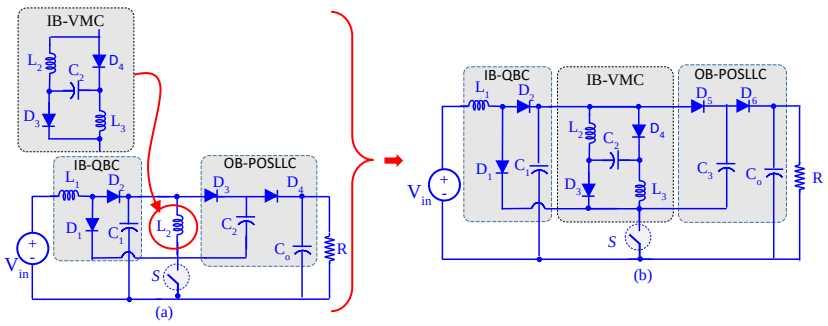

Figure 2. (**a**) The composition of the proposed converter, (**b**) the proposed converter.

2. Ideal and Continuous Current Mode of Converter

The proposed new topology of DC–DC converters is capable of providing a ten-times voltage ratio at a 50% duty ratio. As the front part is a CBT (see Figure 2a), the suggested converter draws a constant current from the source. As a result, the difficulties in the input filter design are overcome. Figure 2b illustrates the complete topology of the present converter, which is implemented by cascading a CBT, POSLLC, and VMC. In other words, this topology is a modified form of CBT. Note that the VMC has been placed instead of POSLLC's inductor. In the second step, the modified POSLLC is replaced with the second inductor of CBT (Figure 2a). Therefore, the voltage ratio of the topology increased, and the bold features of CBT remained. Notably, this converter was designed for a continuous current mode (CCM). Moreover, the extracted relations during this section are appropriate for the ideal mode.

The activation of the first switch starts the first operating mode. Due to the activation of the switch, the first, third, fourth, and fifth diodes are activated. All inductors are magnetized by their positive voltages during this operating mode. The second and third capacitors are charged as well. However, the rest of the capacitors become discharged. Notably, the first, second, and third capacitors are connected in parallel. Therefore, the first capacitor voltage is copied to the second and third capacitors. We should note that the expressing topology of the first mode is illustrated in Figure 3b. The inactivation of the switch starts the second operating mode. Consequently, the second and last diodes begin to 'conduct'. The applied voltage to the inductor becomes negative. Therefore, all of them are demagnetized. The first, second, and third capacitors are connected in series. Consequently, a higher voltage is applied to the second and third capacitors. Notably, the expressing circuit of the second mode is illustrated in Figure 3c. The voltage equations of the inductors and current relations of the capacitors are expressed as (1).

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - v_{C1}) \\ L_2 \dfrac{di_{L2}}{dt} = D(v_{C1}) + (1-D)(v_{C1} + v_{C2} - v') \\ L_3 \dfrac{di_{L3}}{dt} = D(v_{C1}) + (1-D)(v' + v_{C3} - v_{Co}) \\ C_1 \dfrac{dv_{C1}}{dt} = -D(i_{L2} + i_{L3} + i_{C2} + i_{C3}) + (1-D)(i_{L1} - i_{L2}) \\ C_2 \dfrac{dv_{C2}}{dt} = D(i_{C2}) + (1-D)(-i_{L2}) \\ C_3 \dfrac{dv_{C3}}{dt} = D(i_{C3}) + (1-D)(-i_{L2}) \\ C_O \dfrac{dv_{CO}}{dt} = D(-I_O) + (1-D)(i_{L2} - I_O) \end{cases} \quad (1)$$

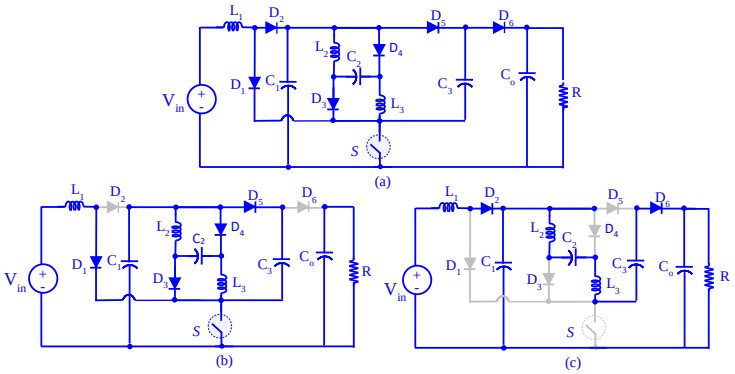

Figure 3. (**a**) The proposed converter, (**b**) the equivalent circuit of the first mode, (**c**) the equivalent circuit of the second mode.

The average voltage of the inductor and the average current of the capacitor is zero. In other words, all of the stated equations of (1) are equal to zero. Therefore, the average capacitor voltage and the average current of the inductor can be calculated as (2).

$$\begin{cases} V_{C1} = V_{C2} = V_{C3} = \dfrac{V_{in}}{1-D}, V_{Co} = \dfrac{3-D}{(1-D)^2} V_{in} \\ I_{L1} = \dfrac{3-D}{(1-D)^2} I_o, I_{L2} = I_{L3} = \dfrac{I_o}{1-D}, i_{C2} = i_{C3} = \dfrac{I_o}{D} \end{cases} \tag{2}$$

Hard-switching was selected for the proposed converter as shown in Figure 4. However, soft-switching has many advantages and its investigation will be in future research. The average crossing current of the semiconductors can be calculated by determining the average current of the inductor; the voltage stress can be determined by the average voltage capacitor as (3).

$$\begin{cases} I_S = \dfrac{1+2D-D^2}{(1-D)^2} I_o, I_{D1} = \dfrac{D(3-D)}{(1-D)^2} I_o \\ I_{D2} = \dfrac{3-D}{1-D} I_o, I_{D3} = I_{D4} = \dfrac{I_o}{1-D}, I_{D5} = I_{D6} = I_o \\ V_S = V_{D5} = V_{D6} = \dfrac{2V_{in}}{(1-D)^2}, V_{D1} = \dfrac{1+D}{(1-D)^2} V_{in} \\ V_{D2} = \dfrac{V_{in}}{1-D}, V_{D3} = V_{D4} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{3}$$

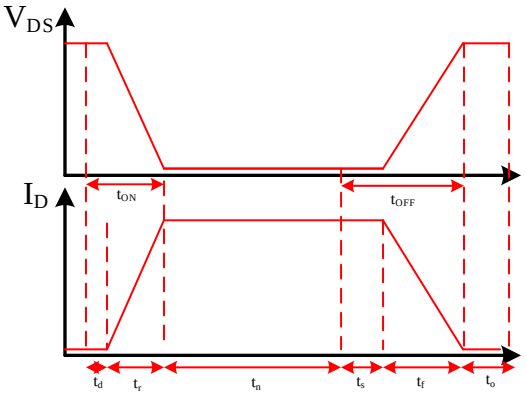

Figure 4. Drain current and drain-source voltage.

The current ripple of the inductor and the voltage ripple of the capacitor are as in (4).

$$\begin{cases} \Delta i_{L1} = \dfrac{DV_{in}}{L_1 f_s}, \Delta i_{L2} = \dfrac{DV_{in}}{L_2 f_s (1-D)} \\ \Delta i_{L3} = \dfrac{DV_{in}}{L_3 f_s (1-D)}, \Delta v_{C1} = \dfrac{2DI_o}{(1-D)^2 f_s C_1} \\ \Delta v_{C2} = \dfrac{I_o}{f_s C_2}, \Delta v_{C3} = \dfrac{I_o}{f_s C_3}, \Delta v_{Co} = \dfrac{DI_o}{f_s C_o} \end{cases} \tag{4}$$

3. Discontinuous Current Mode

The converters operating in the continuous/discontinuous conduction modes (CCM and DCM) depend on the average current of the inductor (besides the current ripple). In other words, the current ripple increases to more than twice the average current of the inductor, concluding DCM. Therefore, the boundary value of the inductor is written as (5).

$$L_1 > \frac{RD(1-D)^4}{2f_s(3-D)^2}, L_2 > \frac{RD(1-D)^2}{2f_s(3-D)}, L_3 > \frac{RD(1-D)^2}{2f_s(3-D)} \tag{5}$$

The average current of the inductor is related to the average output current. Consequently, the operating region of the converter in CCM or DCM was determined according to the duty cycle and output current, see Figure 5.

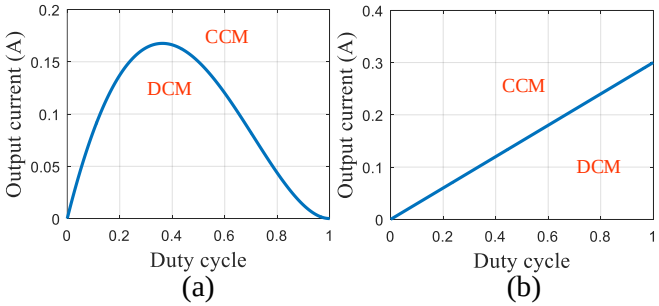

Figure 5. The operating region of the converter in continuous/discontinuous conduction mode; (**a**) the constant output voltage, (**b**) the constant input voltage.

CCM and DCM voltage gain relations are not the same. Considering D as the duty cycle and D1 as the ratio of the ON time of the last diode over the whole switching period, the expressing voltage gain of DCM can be expressed as (6).

$$\frac{V_o}{V_{in}} = \frac{(D + D_1)(3D_1 + 2D)}{D_1^2} \tag{6}$$

4. Converter Behavior in the Non-Ideal Mode

Considering the equivalent series resistance of the inductors, the switch and diodes determine the actual behavior of the converter. The mentioned relation is reported in (7).

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{3 - D}{(1 - D)^2}(1 - \frac{r_L}{R} f_1(D) - \frac{r_S}{R} f_2(D) - \frac{r_D}{R} f_3(D)) \\ f_1(D) = \frac{3D^2 - 10D + 11}{(1 - D)^4}, f_2(D) = \frac{3D^3 - 11D^2 + 7D + 5}{(1 - D)^4} \\ f_3(D) = \frac{D^2 - 8D + 12}{(1 - D)^3} \end{cases} \tag{7}$$

The written parts of the parasitic components are equivalent series resistances of the inductors (r_L), the dynamic resistance of the switch (r_S), and the dynamic resistances of the diodes. The written R in (7) presents the load value. According to the reported equations in (2) and (7), Figure 6 compares the voltage gains in both the ideal/non-ideal modes.

According to this figure, there are no differences in the behaviors of the ideal/non-ideal voltage ratios, while the duty cycle value is lower than 65%. However, the difference increases as the duty cycle approaches unity. Moreover, as the duty cycle approaches unity, the voltage ratio's 'decreasing behavior' appears. We should note that according to (7), the voltage ratio behavior in the non-ideal state depends on the load value. In addition, besides a constant output voltage, the decrease of the load resistance concludes and the output power increases. In Figure 7, the voltage gain of the non-ideal state is compared to the various output powers. It can be understood that the provided voltage gains in the various output powers are the same, while the duty cycle is lower than 60%. However, the difference between the mentioned plots increases as the duty cycle becomes closer to unity. Moreover, its maximum value and corresponding duty cycle decrease. Therefore, the output power increase decreases the corresponding interval of the voltage gain's rising behavior.

According to Figure 8, the provided voltage gains by the proposed converter and introduced topology in [30] are higher than the rest. In other words, the provided voltage gains by varying the duty cycle from 0 to 72% cover from 3 to 20-times. Notably, the

achieved voltage gains in the higher duty cycle percentages are useless. In other words, the provided voltage gain in the mentioned region has poor efficiency. Therefore, the voltage gains of the higher percentages are not recommended. Moreover, the proposed converter and [30] show their better functions in the lower duty cycle percentages than the rest.

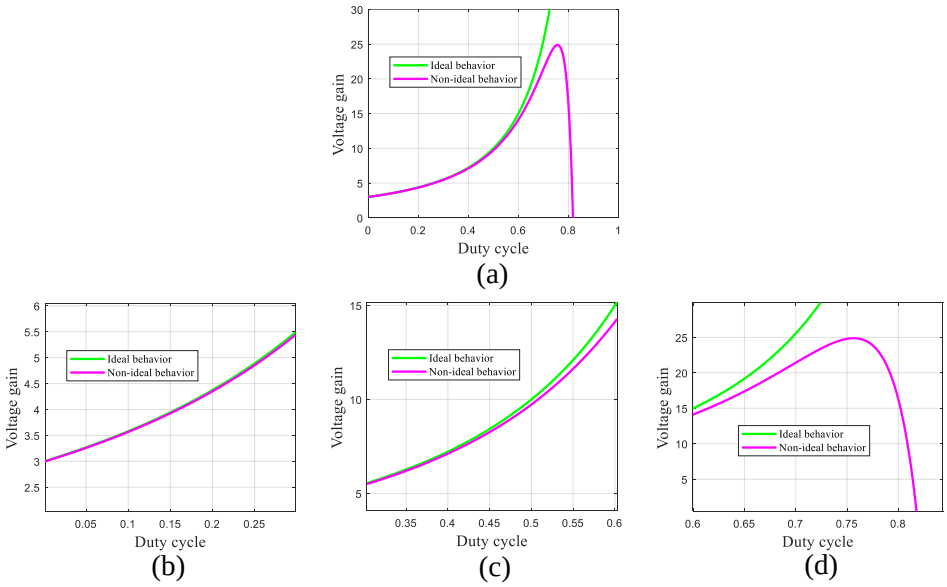

Figure 6. (**a**) Comparing the ideal and non-ideal voltage gains while the duty cycle varies: (**b**) from 0% to 30%, (**c**) from 30% to 60%, (**d**) from 60% to 85%.

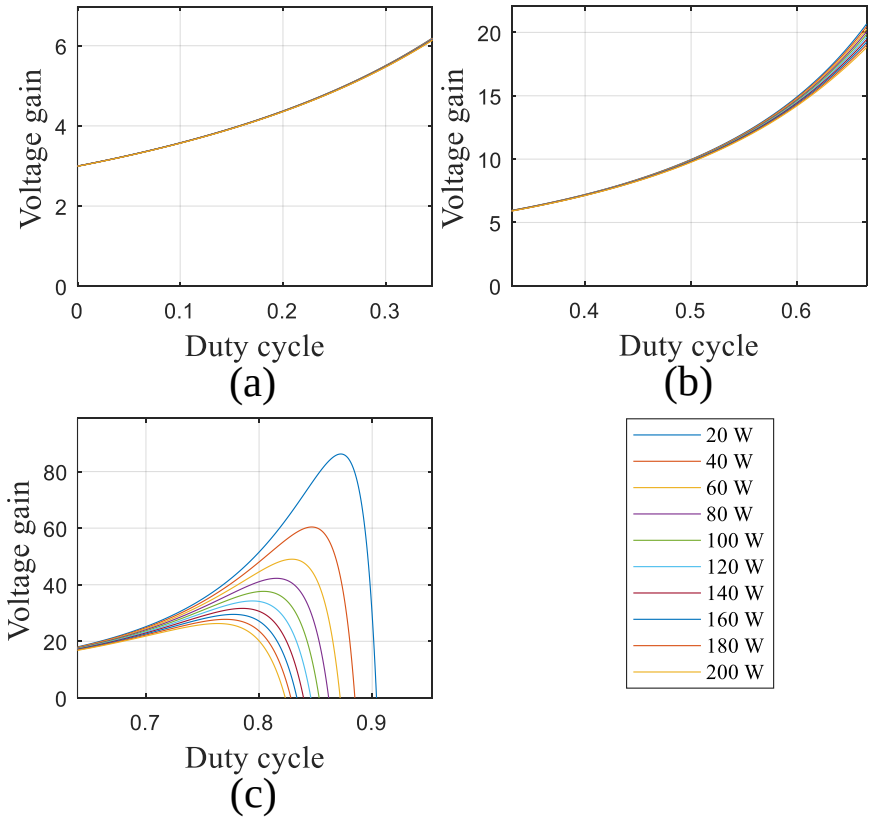

Figure 7. The voltage gain comparing the various output powers as the duty cycle varies from (**a**) 0 to 33%, (**b**) 33% to 66%, (**c**) and 66% to 100%.

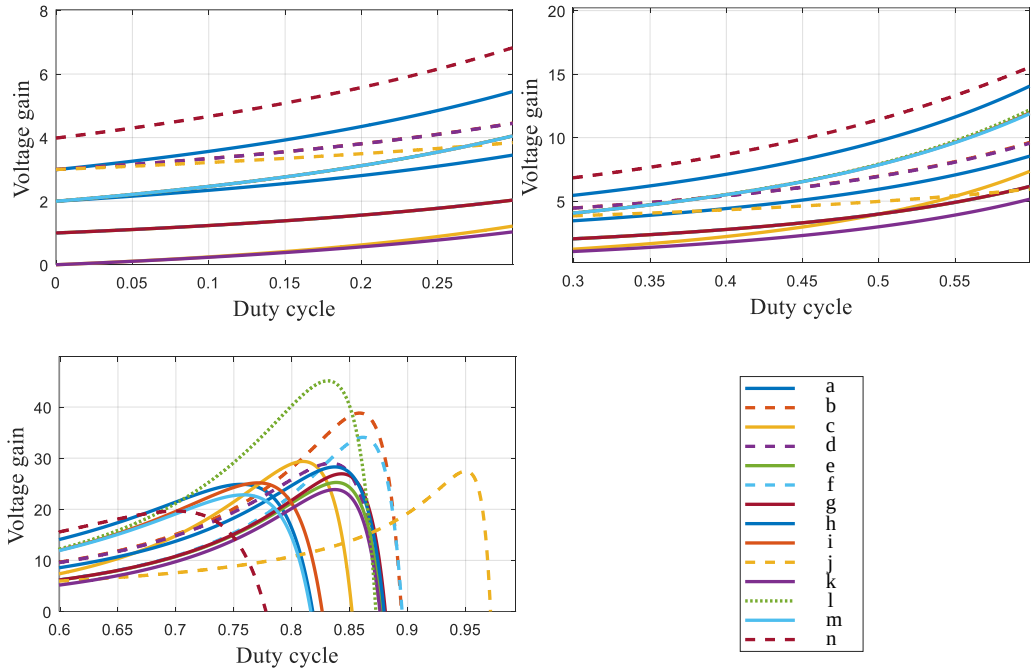

Figure 8. The comparison of the voltage gain: (a) proposed converter, (b) introduced topology in [18], (c) introduced topology in [19], (d) introduced topology in [20], (e) introduced topology in [21], (f) introduced topology in [22], (g) introduced topology in [23], (h) introduced topology in [24], (i) introduced topology in [25], (j) introduced topology in [26], (k) introduced topology in [27], (l) introduced topology in [28], (m) introduced topology in [29],(n) introduced topology in [30].

The efficiency of this converter was modeled considering the inductor conduction loss, MOSFET conduction and frequency loss, and diode conduction loss, besides neglecting the hysteresis and eddy current losses of the inductors and frequency losses of the diodes. The mentioned types of losses have been formulated (8).

$$\begin{cases} P_L = \left(r_{L1} \dfrac{(3-D)^2}{(1-D)^4} + (r_{L2} + r_{L3}) \dfrac{1}{(1-D)^2} \right) \dfrac{P_o}{R} \\ P_{SC} = \dfrac{(1+2D-D^2)^2}{D(1-D)^4}, P_{SS} = \dfrac{1+2D-D^2}{(1-D)^4} V_{in} I_o f_s t_{OFF} \\ P_D = \left(\dfrac{D(3-D)}{(1-D)^2} V_{DF1} + \dfrac{3-D}{1-D} V_{DF2} + \dfrac{V_{DF3} + V_{DF4}}{1-D} \right. \\ \left. ... + V_{DF5} + V_{DF6} \right) \\ \eta = \dfrac{P_o}{P_o + P_L + P_{SC} + P_{SS} + P_D} \end{cases} \tag{8}$$

Figure 9 presents the efficiency behavior and the varying output power. Notably, Figure 9a,b show the duty cycle percentages varying from 0% to 62%, concluding the converter's efficiency (higher than 90%). Moreover, as the duty cycle increases from 62% to 69%, the converter's efficiency becomes lower than 90% and higher than 80% for the output powers of 20 to 100 W. We should note that the increase in the duty cycle to more than 80% concludes the efficiency (lower than 80%) for all of the mentioned output powers.

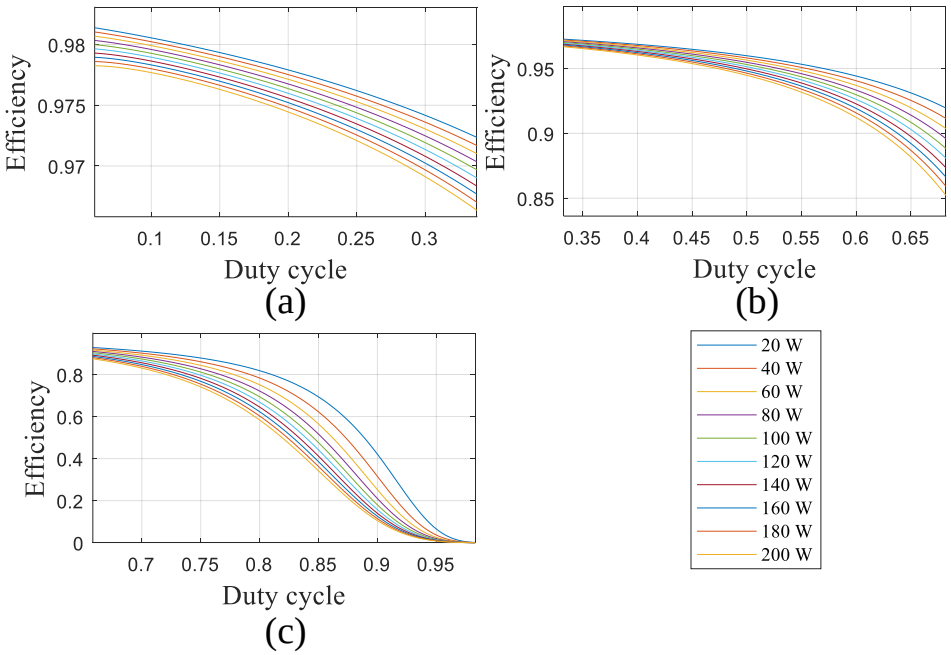

Figure 9. The efficiency comparing the various values of the output power while the duty cycle varies from: (**a**) 0 to 33%, (**b**) 33% to 66%, and (**c**) 66% from 100%.

Table 1 summarizes the comparisons between the topologies and features of the converters in [18–30] and the proposed converter. All topologies in [18–20] have two switches, three diodes, two inductors, and three capacitors. The proposed converters in [21–23] have two inductors, capacitors, switches, and diodes. The rest of the converters only have one switch. Topologies in [24,25,28,29] have five diodes, and the ones in [26,27] have four and three diodes, respectively. The converter in [30] and this paper have three inductors. Two inductors are used in [18–28] topologies and the rest have three inductors. The number of capacitors in [18–20,26,29] is three. In [24,25,28,30], four capacitors are used and the remaining topologies use just two capacitors. The topologies in [21,27] have discontinuous input currents. The input current ripples in [18,20,26,28–30] are not insignificant. Notably, the topologies of [19,22–25], and the proposed one eliminate the input current ripple via the presence of the inductor at the input of the converter. Finally, the topologies of [19,27] have no common ground between the input source and the load.

Table 1. Comparison of Voltage/current stresses

	No. Switch	No. Diode	No. Inductor	No. Capacitor	Continuity of Input Current	Input Current Ripple	Common Ground
[18]	2	3	2	3	yes	Not negligible	yes
[19]	2	3	2	3	yes	Negligible	No
[20]	2	3	2	3	yes	Not negligible	yes
[21]	2	2	2	2	No	Not negligible	yes
[22]	2	2	2	2	yes	Negligible	yes
[23]	2	2	2	2	yes	Negligible	yes
[24]	1	5	2	4	yes	Negligible	yes
[25]	1	5	2	4	yes	Negligible	yes
[26]	1	4	2	3	yes	Not negligible	yes
[27]	1	3	2	2	No	Not negligible	No
[28]	1	5	2	4	yes	Not negligible	yes
[29]	1	5	3	3	yes	Not negligible	yes
[30]	1	6	3	4	yes	Not negligible	yes
proposed	1	6	3	4	yes	Negligible	yes

Figure 10 compares the efficiency in the same output power among the proposed topology in this paper and [18–30]. While the duty cycle varies from 0 to 30%, all topologies provide efficiency higher than 94%. Increasing the duty cycle from 30% to 60% decreases the efficiency of [30] from 94% to 86%. However, the provided efficiency by the rest is higher than 90% in the mentioned duty cycle interval. The duty cycle varying from 60 to 70% concludes the efficiency value between 80 and 90%. However, the rest keep their higher values until there are higher duty cycle percentages. The proposed converter provides high-voltage gain and efficiency values through lower duty cycle percentages.

Figure 11 compares the inductor, switch, and diode losses beside the efficiency and duty cycle percentage. This comparison was conducted using a 200 W output power and a duty cycle that produced a 10-times voltage gain. The suggested topology inductor losses were less than the converters in [22,24,27]. Moreover, these losses were approximately the same as in [19,21,23,25,29]. Additionally, the suggested converter had a lower switch loss than the switches in [19,21,24–28,30]. In the diode losses, only the recommended topology of [30] had lower diode losses than the proposed converter. The higher losses were due to the six diodes in this converter. According to Figure 11d, the efficiency of the proposed converter is higher than in [24,30]. Note that the difference in the efficiency values is less than 4%. Figure 11e shows that the required voltage gain for the proposed converter is less than the gains in [18–29].

Figure 12 presents the normalized voltage stress of the proposed converter as well as [18–30]. According to this figure, all stresses are smaller than unity. However, some of the voltage stresses in [18,21–25,27,29] are equal to or greater than unity. Figure 13 shows the semiconductor's normalized current stress of 0.7. However, in [19,21,24–28], the stresses are more than 0.7. In the suggested converter, each diode current stress is less than 0.5. However, several of the diode stresses in [24,25,27–30] are more than 0.5.

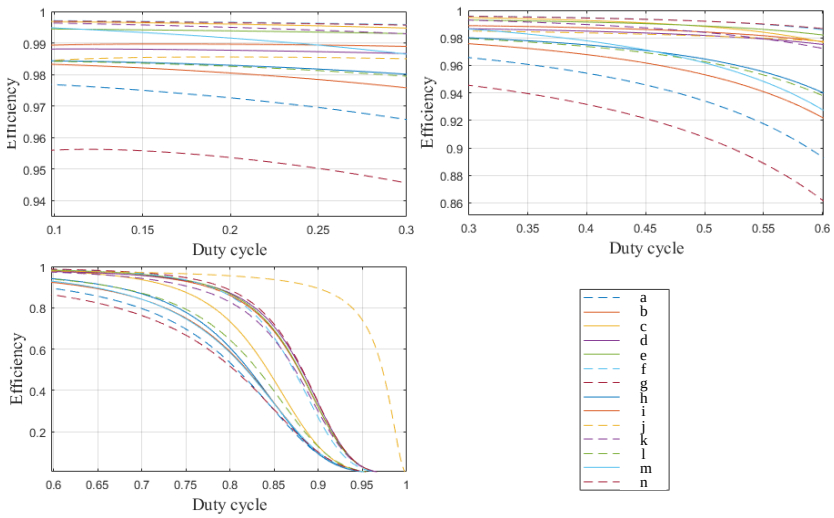

Figure 10. The efficiencies comparison: (a) proposed converter, (b) introduced topology in [18], (c) introduced topology in [19], (d) introduced topology in [20], (e) introduced topology in [21], (f) introduced topology in [22], (g) introduced topology in [23], (h) introduced topology in [24], (i) introduced topology in [25], (j) introduced topology in [26], (k) introduced topology in [27], (l) introduced topology in [28], (m) introduced topology in [29], (n) introduced topology in [30].

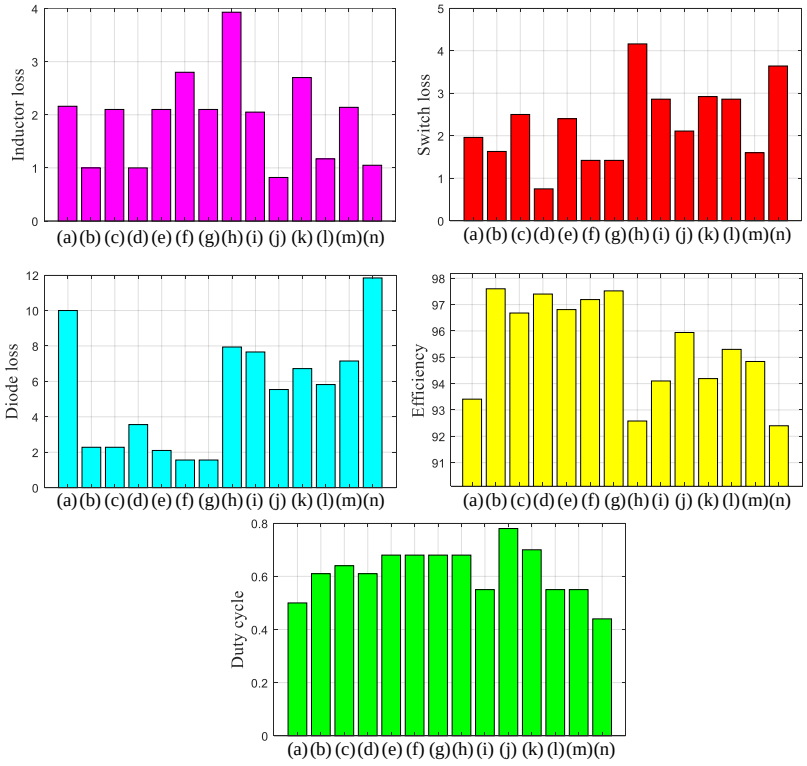

Figure 11. (a) proposed converter, (b) introduced topology in [18], (c) introduced topology in [19], (d) introduced topology in [20], (e) introduced topology in [21], (f) introduced topology in [22], (g) introduced topology in [23], (h) introduced topology in [24], (i) introduced topology in [25], (j) introduced topology in [26], (k) introduced topology in [27], (l) introduced topology in [28], (m) introduced topology in [29], (n) introduced topology in [30].

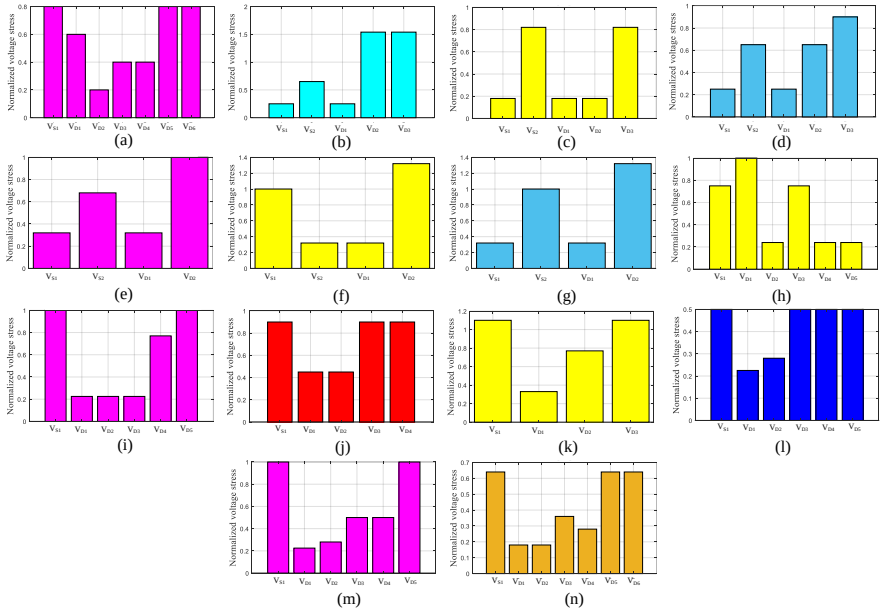

Figure 12. The comparison of the voltage stresses of the semiconductors and duty cycle among the proposed converter and recently suggested topologies for a duty cycle that provides a 10-times voltage gain: (**a**) proposed converter, (**b**) introduced topology in [18], (**c**) introduced topology in [19], (**d**) introduced topology in [20], (**e**) introduced topology in [21], (**f**) introduced topology in [22], (**g**) introduced topology in [23], (**h**) introduced topology in [24], (**i**) introduced topology in [25], (**j**) introduced topology in [26], (**k**) introduced topology in [27], (**l**) introduced topology in [28], (**m**) introduced topology in [29], (**n**) introduced topology in [30].

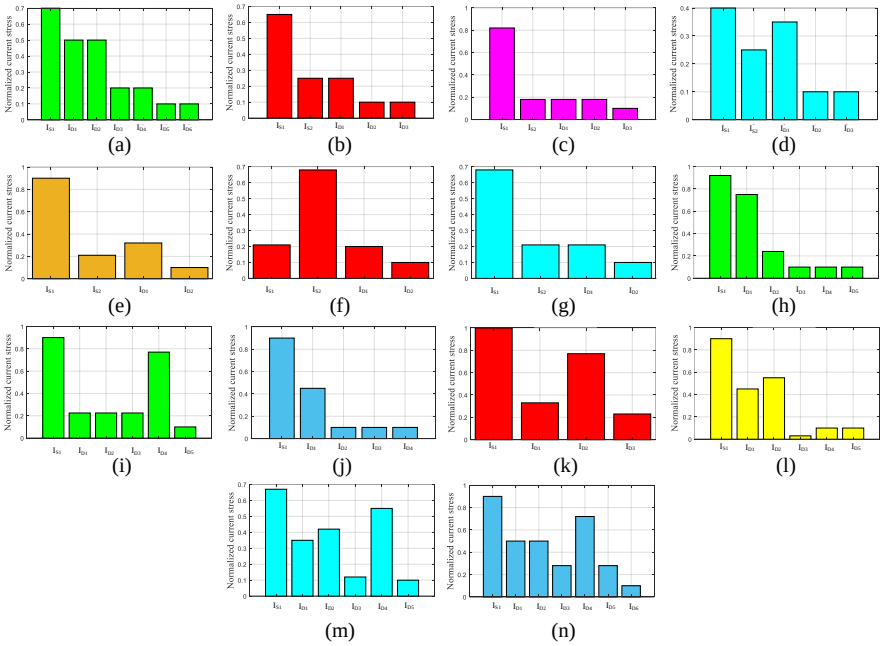

Figure 13. Comparison of the current stresses of the semiconductors and duty cycle, which provides a 10-times voltage gain: (**a**) proposed converter, (**b**) introduced topology in [18], (**c**) introduced topology in [19], (**d**) introduced topology in [20], (**e**) introduced topology in [21], (**f**) introduced topology in [22], (**g**) introduced topology in [23], (**h**) introduced topology in [24], (**i**) introduced topology in [25], (**j**) introduced topology in [26], (**k**) introduced topology in [27], (**l**) introduced topology in [28], (**m**) introduced topology in [29], (**n**) introduced topology in [30].

5. Simulation and Experimental Results

This section presents the simulation and experimental results to validate the theoretical analysis. PLECS software tools were used to simulate the proposed converter. Such software is suitable for power electronics and control projects. Simulation results were obtained using realistic assumptions. Moreover, the energy-storing components had to be determined using functional constraints, such as input voltage, the duty cycle, the output current, the current ripple of inductors, and the voltage ripple of capacitors. The input voltage was 20 V, which was defined by the equipment limits. In addition, the switching frequency of MOSFET was 50 kHz due to the frequency limits of employing the wires of the inductors. Moreover, the power quality considerations defined 30% and 5% as the current ripple of the inductor and the voltage ripple of the capacitor, respectively. As mentioned before, the duty cycle was 50%, with an equal energy-storing/releasing time and provided suitable operating conditions; moreover, (9) expresses the average current of the inductor and average voltage of the capacitor.

$$\begin{cases} V_{C1} = V_{C2} = V_{C3} = 40 \text{ V}, V_{Co} = 200 \text{ V} \\ I_{L1} = 10 \text{ A}, I_{L2} = I_{L3} = 2 \text{ A} \end{cases} \tag{9}$$

Using the calculated average voltages/currents (besides the specified current/voltage ripples) gives the following inductors and capacitors in (10).

$$\begin{cases} L_1 = 66.6 \text{ µH}, L_2 = L_3 = 666.6 \text{ µH} \\ C_1 = 40 \text{ µF}, C_2 = C_3 = 10 \text{ µF}, C_o = 1 \text{ µF} \end{cases} \tag{10}$$

Using the parameters in (10) gave the simulation results in Figures 14 and 15. Figure 14 depicts the inductor current, the capacitor voltage, and the semiconductor current waveforms. Additionally, Figure 15 shows the inductor voltage, the capacitor current, and the semiconductor voltage. According to the inductor current and capacitor voltage waveforms, their average values are as in (11).

$$\begin{cases} V_{C1} = 40 \text{ V}, V_{C2} = 38.5 \text{ V}, V_{C3} = 39 \text{ V}, V_{Co} = 196 \text{ V} \\ I_{L1} = 10 \text{ A}, I_{L2} = I_{L3} = 2 \text{ A} \end{cases} \quad (11)$$

The comparisons of the corresponding values of (11) and (9) defined their compatibilities and validated the correctness of the extracted relations. The differences in the average voltage of the capacitors refer to the voltage drops of the diodes.

A 200 W prototype of the proposed converter was built and it is illustrated in Figure 16. The components' voltage/currents are shown in Figures 17 and 18, which present the experimental results. Figure 16 shows the current waveforms of the inductors and semiconductors, besides the capacitor's voltage waveforms. Figure 17 shows the inductor voltage, the capacitor current, and the semiconductor voltage waveform. From Figures 17 and 18, the average current and voltage of inductors are given by (12).

$$\begin{cases} V_{C1} = 38 \text{ V}, V_{C2} = 37 \text{ V}, V_{C3} = 36 \text{ V}, V_{Co} = 190 \text{ V} \\ I_{L1} = 9.4 \text{ A}, I_{L2} = I_{L3} = 1.9 \text{ A} \end{cases} \quad (12)$$

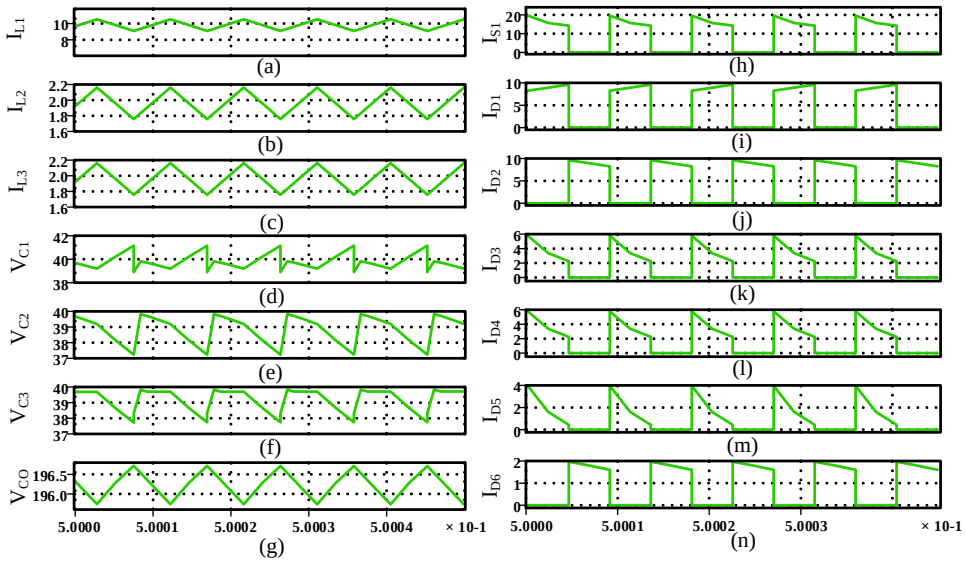

Figure 14. Simulation results: (**a**) first inductor current, (**b**) second inductor current, (**c**) third inductor current, (**d**) first capacitor voltage, (**e**) second capacitor voltage, (**f**) third capacitor voltage, (**g**) output capacitor voltage, (**h**) switch current, (**i**) first diode current, (**j**) second diode current, (**k**) third diode current, (**l**) fourth diode current, (**m**) fifth diode current, (**n**) sixth diode current.

Comparing the experimental results with the simulation results and primary design considerations, we can see the expected difference. This discrepancy relates to the voltage drop in the prototype's diodes. Therefore, the voltage values are lower than the simulation results and design considerations. According to Figure 17, the average voltage of the inductors and the average current of the capacitors are zero, as assumed. Moreover, (13) gives the semiconductor current/voltage stresses according to Figures 17 and 18, respectively.

$$\begin{cases} I_{S1} = 6.3 \text{ A}, I_{D1} = 4.5 \text{ A}, I_{D2} = 4.5 \text{ A}, I_{D3} = 1.8 \text{ A} \\ I_{D4} = 1.8 \text{ A}, I_{D5} = 0.9 \text{ A}, I_{D6} = 0.9 \text{ A} \\ V_{S1} = 154 \text{ V}, V_{D1} = 116 \text{ V}, V_{D2} = 38 \text{ V}, V_{D3} = 80 \text{ V} \\ V_{D4} = 80 \text{ V}, V_{D5} = 154 \text{ V}, V_{D6} = 154 \text{ V} \end{cases} \quad (13)$$

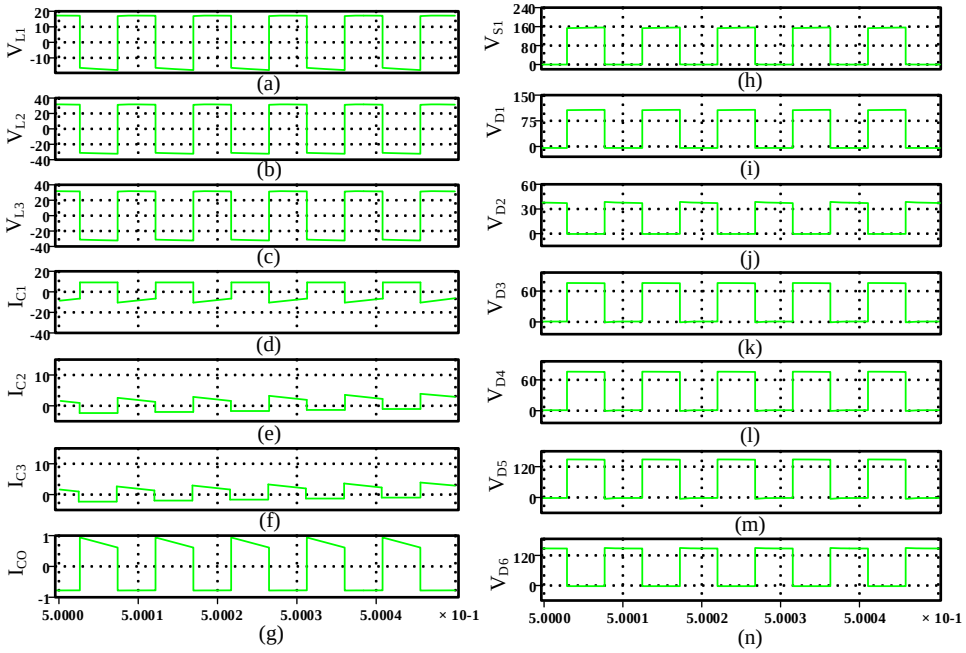

Figure 15. Simulation results: (**a**) first inductor voltage, (**b**) second inductor voltage, (**c**) third inductor voltage, (**d**) first capacitor current, (**e**) second capacitor current, (**f**) third capacitor current, (**g**) output capacitor current, (**h**) switch voltage, (**i**) first diode voltage, (**j**) second diode voltage, (**k**) third diode voltage, (**l**) fourth diode voltage, (**m**) fifth diode voltage, (**n**) sixth diode voltage.

According to the theoretical relations of the voltage/current stresses, the mentioned values are as in (14).

$$\begin{cases} I_{S1} = 6.65 \text{ A}, I_{D1} = 4.75 \text{ A}, I_{D2} = 4.75 \text{ A}, I_{D3} = 1.9 \text{ A} \\ I_{D4} = 1.9 \text{ A}, I_{D5} = 0.95 \text{ A}, I_{D6} = 0.95 \text{ A} \\ V_{S1} = 160 \text{ V}, V_{D1} = 120 \text{ V}, V_{D2} = 40 \text{ V}, V_{D3} = 80 \text{ V} \\ V_{D4} = 80 \text{ V}, V_{D5} = 160 \text{ V}, V_{D6} = 160 \text{ V} \end{cases} \tag{14}$$

Based on the simulation results, the voltage/current stresses of the semiconductors are as in (15).

$$\begin{cases} I_{S1} = 7 \text{ A}, I_{D1} = 5 \text{ A}, I_{D2} = 5 \text{ A}, I_{D3} = 2 \text{ A} \\ I_{D4} = 2 \text{ A}, I_{D5} = 1 \text{ A}, I_{D6} = 1 \text{ A} \\ V_{S1} = 157 \text{ V}, V_{D1} = 117 \text{ V}, V_{D2} = 40 \text{ V}, V_{D3} = 78 \text{ V} \\ V_{D4} = 78 \text{ V}, V_{D5} = 157 \text{ V}, V_{D6} = 157 \text{ V} \end{cases} \tag{15}$$

The differences in the reported values stand from the average voltage in the capacitor prototype. Therefore, there is a difference in the semiconductor voltage compared to the theoretical values and simulation results. Moreover, the output voltage difference causes the contrast of the average output current. Therefore, the average currents of the inductors and semiconductors are different from the simulation/theoretical outcomes. In other words, there is a negligible difference.

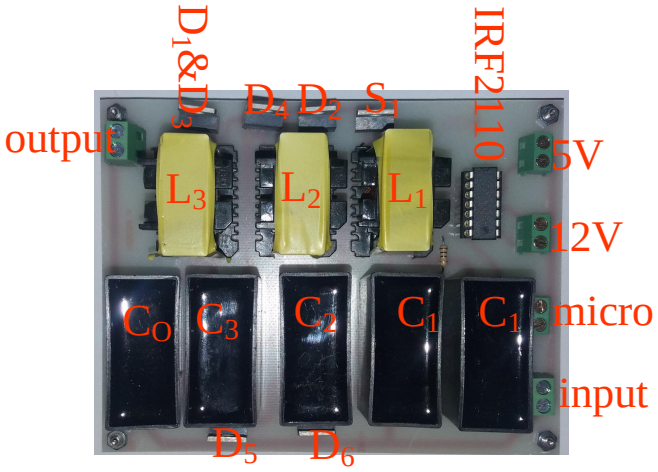

Figure 16. The prototype.

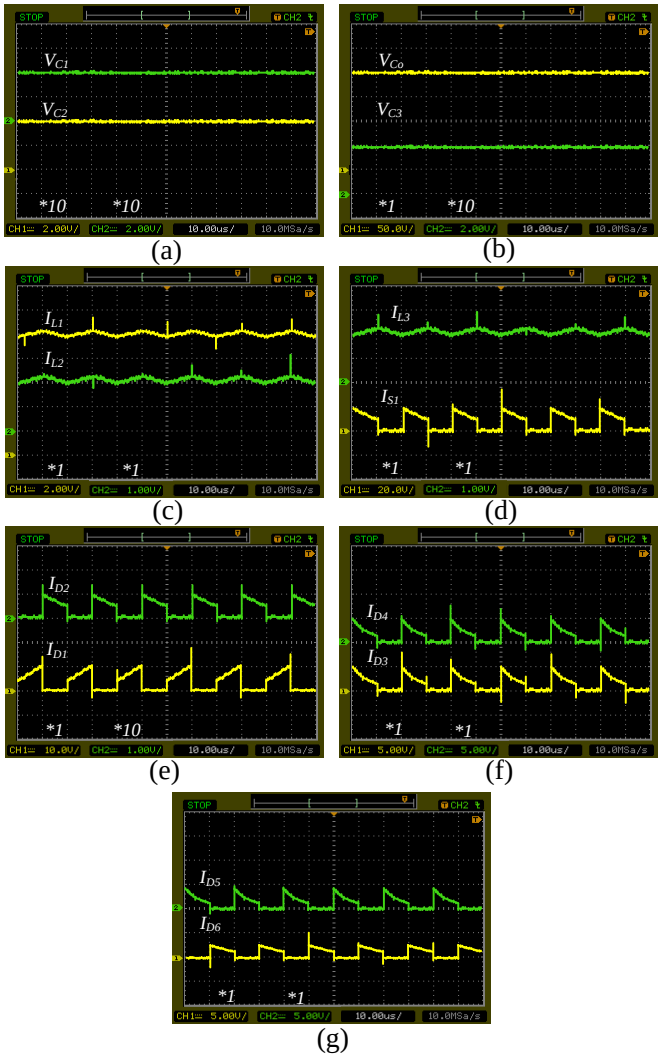

Figure 17. The experimental outcomes: (**a**) first and second capacitors' voltage, (**b**) third and last capacitors' voltage, (**c**) first and second inductors' current, (**d**) third inductor and switch current, (**e**) first and second diodes' current, (**f**) third and fourth diodes' current, (**g**) fifth and sixth diodes' current.

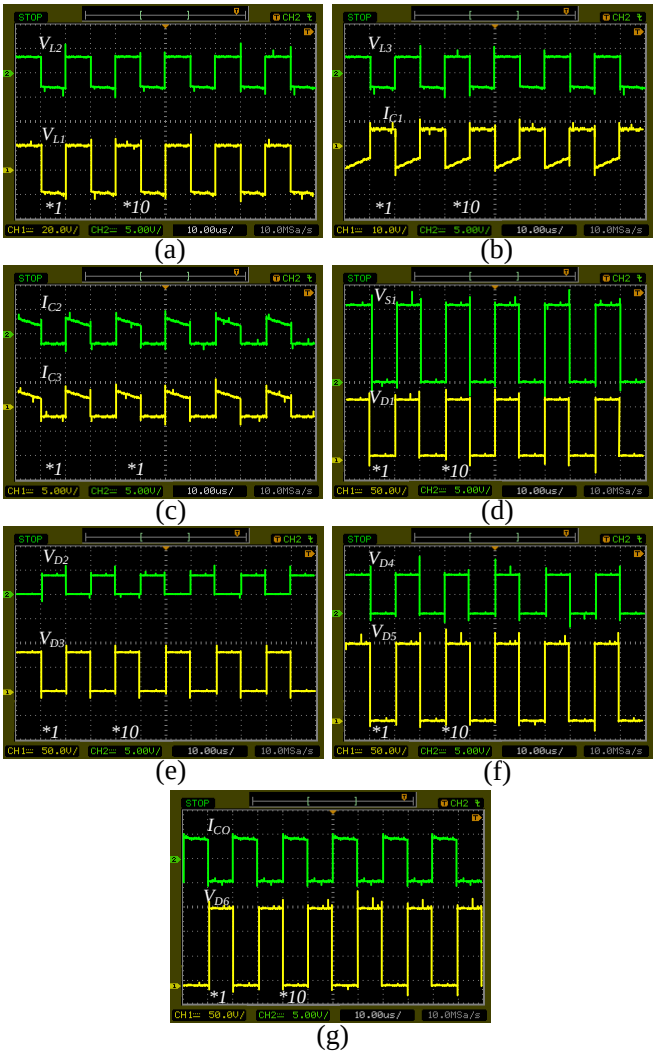

Figure 18. The experimental outcomes: (**a**) the first and second inductors' voltage, (**b**) the third inductor's voltage and first capacitor current, (**c**) second and third capacitors' current, (**d**) switch and first diode's voltage, (**e**) second and third diodes' voltage, (**f**) fourth and fifth diodes' voltage, (**g**) last capacitor's current and sixth diode's voltage. .

Notably, the proposed converter's voltage gain was extracted based on the theoretical relation and experimental results for three different types of inductors. As can be understood from Figure 19, the E–E type, E–I type, and toroid type of the inductor were used. According to Figure 18, the E–E type of the inductor has better behavior regarding the voltage gain. In other words, due to the use of a low wire in the E–E type, the ESR of the inductor is low. Consequently, the corresponding figures of the E–E type have rising behaviors of wider spans. The differences in the corresponding figures regard the theoretical relations and the experimental results considering approximations. Therefore, the higher duty cycle makes the mentioned differences appear. In Figure 20, the converter's efficiency based on the theoretical equations and the experimental outcomes were extracted for the E–E, E–I, and toroid types. We should note that the E–E type of inductor requires a lower wire value to achieve inductance than the rest. Therefore, the corresponding efficiency of the E–E type provides the highest value in the theoretical/experimental outcomes. The toroid type needs the highest value of the wire to achieve the same inductance. Therefore, the lowest value of the efficiency belongs to the toroid type. It is worth noting that the differences in the corresponding figures of the theoretical and experimental results were caused by neglecting some type of loss in the theoretical relation. Such an analysis was done for switches, and the results are illustrated in Figure 21. IRF540, IRF630, and VMK16N70OC2

are considered the first, second, and third types of switches. In Figure 21, the highest value of the efficiency (in both theory and experiment) belongs to IRF540. The dynamic resistance of the mentioned switch is lower than the rest. In addition, the VMK16N70C2, due to its high capabilities, has the highest dynamic resistance. According to the mentioned figure, IRF540 has a better function than the others. Finally, in Figure 22, the converter's efficiency was extracted for three different types of diodes. The first, second, and third diodes belong to MBRB1045G, 2015OCT, and FES8GT, respectively. In the mentioned figure, the corresponding figure of the first type obtained the highest value compared to the rest in both theory and experimental results. The last three figures explain the efficiency sensitivities according to the circuit element changes; it can be deduced that the diodes have significant effects due to their highest numbers in the proposed topology.

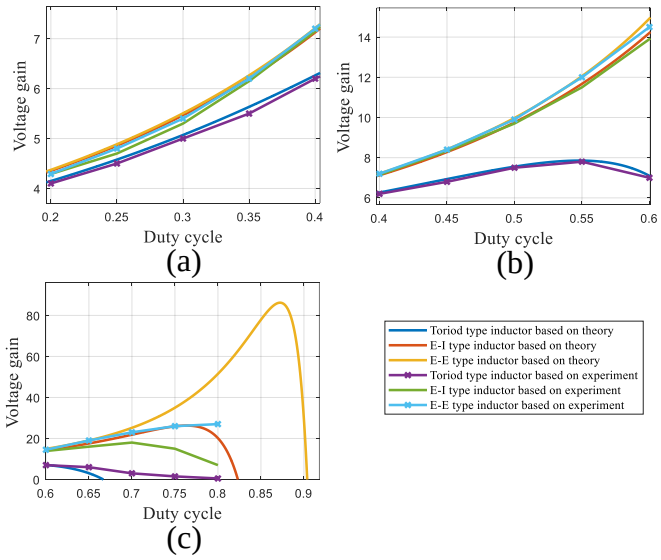

Figure 19. The voltage gain comparison based on the theory and experimental results of the toroid type, E–E type, and E–I type of the inductor cores while the duty cycle varies from (**a**) 0 to 33%, (**b**) 33% to 66%, and (**c**) 66% to 100%.

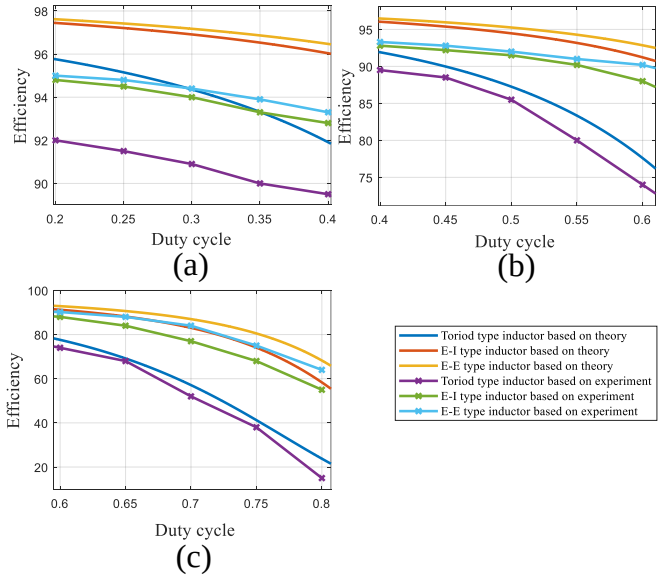

Figure 20. The efficiency comparison based on the theory and experimental results of the toroid type, E–E type, and E–I type of the inductor cores as the duty cycle changes from (**a**) 0 to 33%, (**b**) 33% to 66%, and (**c**) 66% to 100%.

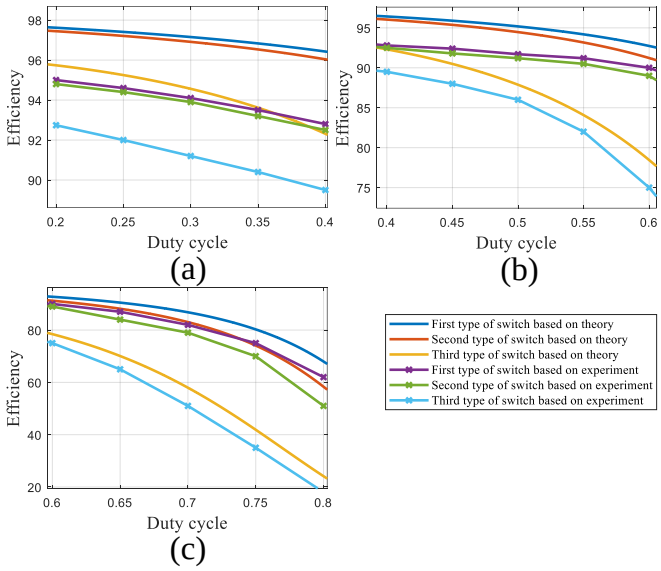

Figure 21. The efficiency comparison based on the theory and experimental results of the three various switch types while the duty cycle changes from (**a**) 0 to 33%, (**b**) 33% to 66%, and (**c**) 66% to 100%.

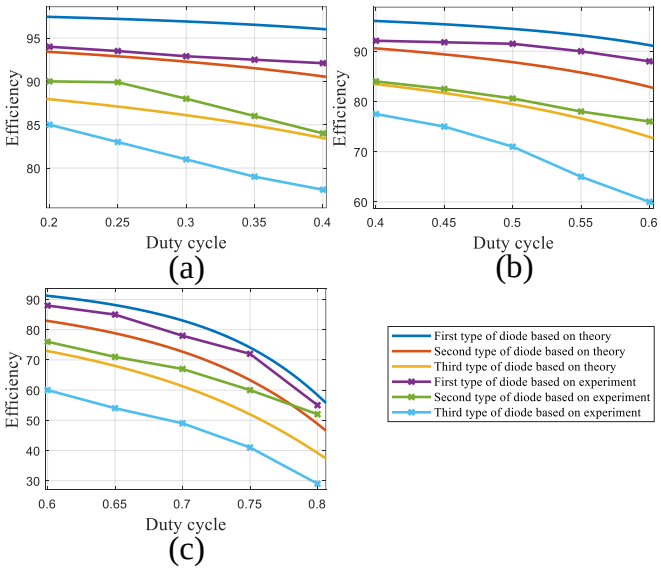

Figure 22. The efficiency comparison based on the theory and experimental results of the three various diode types while the duty cycle varies from (**a**) 0 to 33%, (**b**) 33% to 66%, and (**c**) 66% to 100%.

6. Conclusions

This paper introduced an ultra-high step-up DC–DC converter with a continuous input current. This converter's architecture consists of a novel combination of VMC, POSLLC, and QBC topologies. When the duty cycle is at 50%, the converter attains a voltage gain of ten. The constant input current of the topology reduces the current stress on the input filter capacitor. This converter's topology was investigated and studied under various operating conditions: ideal and non-ideal modes, as well as continuous and discontinuous current modes (CCM/DCM). The theoretical study of the proposed topology was studied for both CCM and DCM. The converter's behavior was discussed for both the ideal and the non-ideal states of the circuit components. The proper functionality of the non-ideal case was discussed and compared with the recently suggested converter topologies. The mathematical derivation was further substantiated by a comparison of the theoretical non-ideal voltage gain relation with the experimental findings. Additionally, the efficiency of the

converter was theoretically and experimentally compared to that of previously suggested converter topologies. Finally, a 200 W prototype was constructed using 20 V input voltage, 50 kHz switching frequency, 1 A output current, and operating at a 50% duty cycle. The inductors' average current, capacitor average voltage, semiconductor average current, and semiconductor voltage were measured and compared with the theoretical results. Additionally, sensitivity analyses for the voltages were performed; it was determined that they were consistent with the derived relations. The extracted efficiency of the prototype was around 92%, which could be improved with better circuit components.

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