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Review article

A structural overview on transformer and transformer-less multi level inverters for renewable energy applications

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ABSTRACT

In general, multilevel inverters (MLIs) are regarded as advanced power conversion systems required for medium-voltage and high-power applications. The purpose of this article is to provide an overview of recently investigated MLI topologies classified into various categories based on the transformer requirement such as the transformer less (TL-MLI) and transformer-based (T-MLI) with single and multi-source topologies of symmetric, asymmetric, hybrid and single DC sources for renewable energy applications. For the previous few decades, multiple new variants of each group have been developed. The design and functioning of each topology, as well as each group, are examined in this study. T-MLI topologies of H-bridge, three-leg inverter-based, and other T-MLI configurations are discussed from a configuration standpoint. Each topology's state-of-the-art of both MLI configurations and problems are treated separately. Furthermore, the disadvantages and benefits of each topology have been thoroughly addressed. Finally, a comparison of existing topologies is conducted to determine the optimal topology based on several performance characteristics and the cost evaluation has been presented. This article provides a comprehensive overview of recently developed multilevel inverters and provides a solution for developing the MLIs for future research on renewable energy applications.

Contents

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1. Introduction

The world's fossil resources have been depleted due to the rise in electricity consumption. As a result, several measures are to be taken to make fossil fuels last longer. Two basic strategies distinguish the literature. It is necessary to make the most efficient use of existing power resources, as well as to increase the usage of renewable energy sources including photovoltaics, wind, geothermal, and nuclear power. Electrical power converters can technically perform the tasks with a high level of efficiency. i.e., all harmonics are present in a square wave created by DC to AC converter (inverter). As a result, low pass filters are removed to increase the waveform quality. Higher voltage is not supported with more than one switch in high-power applications, a typical two-level inverter is used. MLIs are indicated as a suitable option for high-power and medium-voltage applications under certain scenarios. The basic classification of MLI based on several parameters is represented in Fig. 1. For easy understandability, a summary of the concept is represented in Fig. 2. The typical two-level inverter and basic MLI designs, such as Diode Clamped MLI, Flying Capacitor MLI, and Cascaded MLI, are shown in Fig. 3 presented progressively by Nabae et al. in Nabae et al. (1981), Meynard et al. in Meynard and Foch (1992), and Hammond in Hammond (1997) are the main MLI configurations.

Each basic MLI may have its own set of characteristics and challenges. Indeed, in any MLI, increased levels enrich the output waveform's quality, and appropriate switching strategies increase their potential when it comes to load balancing, reducing losses, a good power factor, a much smaller filter, lower power switching device voltage stress and increased efficiency. Several approaches are introduced to modulate the overall performance of MLI are introduced in José et al. (2009). Most of the industries now operate on a variety of MLIs, including power quality appliances (José et al., 2009), traction (Akagi and Hatada, 2009), renewable energy uses (Liu et al., 2009), automobiles, transmission of energy (Liu et al., 2014), uninterruptable electricity supply (Etxeberria-Otadui et al., 2008), industrial drives (Islam et al., 2014). Multi-level inverters have been designed as one of the most appealing alternative methods for the use of medium/high voltage converters for more than five decades (Islam et al., 2014). Individual or diversified DC sources such as batteries or rectifiers, flying condensers, pumping lines, and photovoltaic (PV) panels utilize MLIs to provide a sinusoidal voltage with little distortion in Vijeh et al. (2019).

High voltage waveforms can be efficiently generated at the converter output using a mix of low voltage DC sources and semiconductor switches (Ghasemi et al., 2012). The voltage stress on the switches is substantially lower than the output stress since the switch rating is controlled by the DC source rating. Boker and Bannister in Ng et al. (2008) designed the first topology converter with multiple DC sources in the 1970s, which is generally referred to as cascading H-bridge (CHB) MLI. Each source has been linked to a single-phase inverter, resulting in a single cell. As shown in Fig. 3(a), it is possible to create a multi-level output using many cells in a cascade. Baker developed a single source MLI topology called diode clamping (NPC) a few years later, in the 1980s in Nabae et al. (1981). Despite only having one DC source, it necessitates a large number of diodes connected to a neutral point, as illustrated in Fig. 3(b). By employing Pulse Width Modulation (PWM) schemes, Nabae et al. (Kouro et al., 2010) published the NPC implementation in 1981. Fig. 3(c) illustrates flying condensers or flying condensers MLI, by Meynard and coll and Lavieville et al. respectively introduced in the 1990s in Meynard and Foch (1992), Chivite-Zabalza et al. (2013). While only one DC source is needed, the size of flying condensers is increased in FC-MLI, which creates control complexity. The three topologies have been viewed in literature as the fundamental MLI topologies (Vijeh et al., 2019; Gupta et al., 2016; Bana et al., 2019; Rodríguez et al., 2002). MLIs are extensively utilized for DC-to-AC conversions in power and transportation systems, as well as renewable energy systems in flexible AC transmission systems (FACTS) (Chivite-Zabalza et al., 2013; Soto and Green, 2002), High voltage DC transmission systems (HVDC) (Jung et al., 2017), High power frequency systems (HPF) (Shu et al., 2017; Hoon et al.,

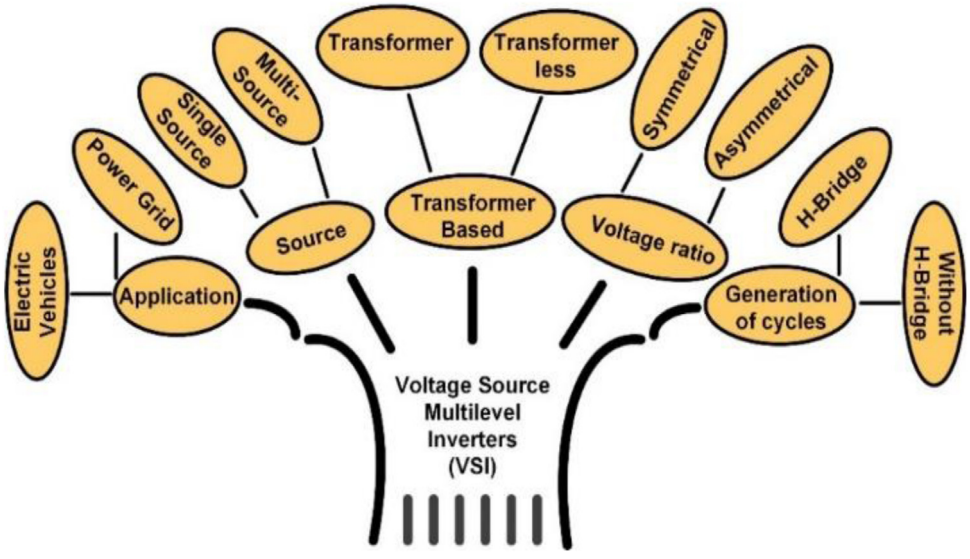

Fig. 1. Classification of multilevel inverters.

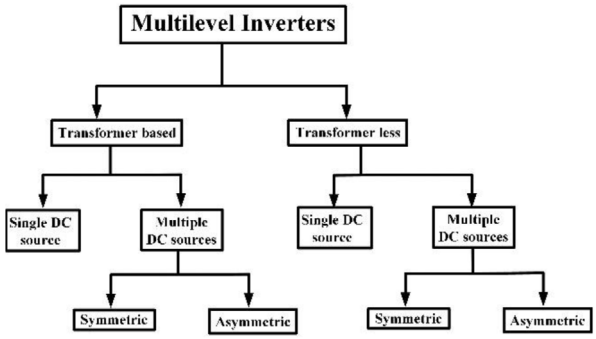

Fig. 2. Summary of the concept of MLI.

2018), varying frequency drives (VFD) (Diab et al., 2018; Dixon et al., 2010), pumped storage plants (PSP) (Joseph and Chelliah, 2018; Bocquel and Janning, 2005; Pronin et al., 2012), hydrogen fuel cell (Dhanamjayulu et al., 2020b) and grid-connected or standalone PV systems (Zhang et al., 2018b).

The MLIs offer various advantages described in Raju et al. (2019), Priya et al. (2019):

- The creation of high-quality waveforms with low harmonics and low-stress dv/dt, results in significant reductions in electromagnetic interference (EMI) and total harmonic distortion (THD).
- Working in low and fundamental switching systems, particularly for high-power applications, can result in lower switching losses, which is beneficial in improving efficiency and cooling requirements.
- The integration of low-rate standard semi-conductors in high-voltage production without being coupled in series, as in medium-sized two-level inverters.
- In many situations, a low/zero common voltage (CMV) can reduce CMV drawbacks, such as stress in power systems in carriages of driven motors fed by MLIs.

Various MLIs also have other strategic advantages, such as decreased operation, modularity, transformer voltage and current scalability, high redundancy, and fault tolerance in the switching states. These benefits are also covered by the expenses of a large variety of passive and active components such as DC sources, flying condensers, inductors, diodes, and switches (Kaarthik et al., 2015). As a result, the inverter's size, cost, and complexity have increased (Xiao et al., 2015). As a result, one of the most important research developments in this field is the current proposal for unique mixes to enhance the level number while using a small number of components (Gupta and Jain, 2014a). Every year, various articles were published on the topics of increased efficiency, energy density, control simplicity, reliability, cost, and MLI application extension. As a result, it is critical to evaluate state-of-the-art information in this field regularly to keep the baselines or current considerations up to date, and there are numerous reviews available in this field. (Hasan et al., 2014). The majority of these studies provide a detailed assessment of MLIs based on specific applications or converter families, such as transportation (Ronanki and Williamson, 2018), medium voltage (Rodriguez et al., 2007) modular MLIs (Ronanki and Williamson, 2018), HVDC

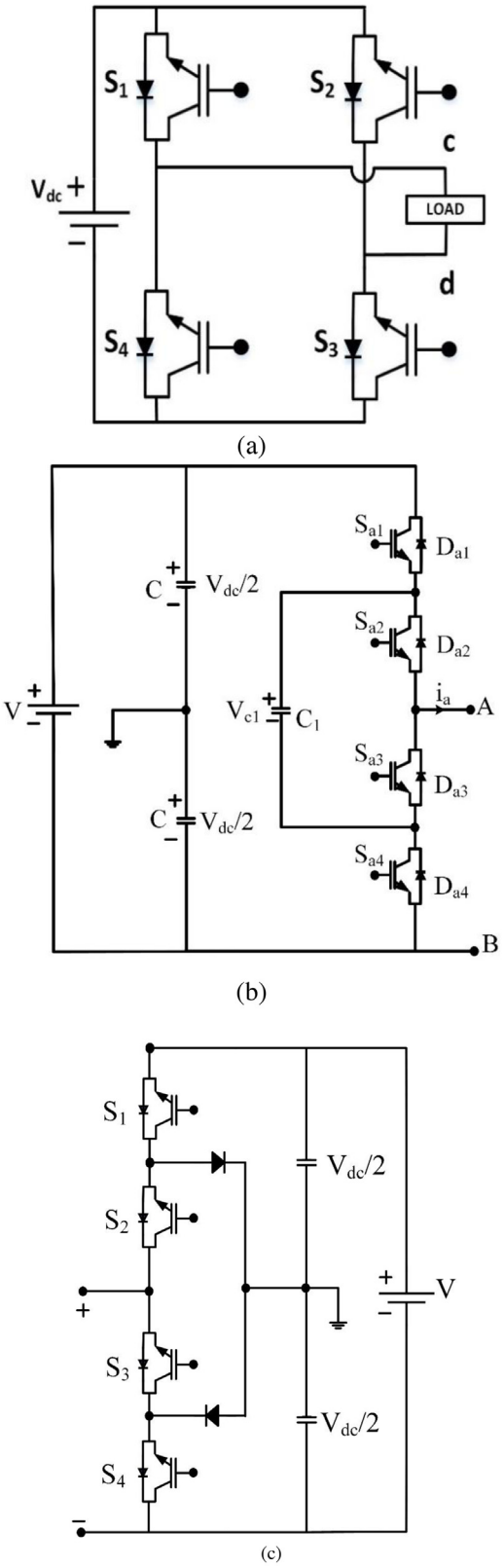

Fig. 3. Classical topologies (a) CHB-MLI (b) NPC-MLI (c) FC-MLI (Venkataramanaiah et al., 2017).

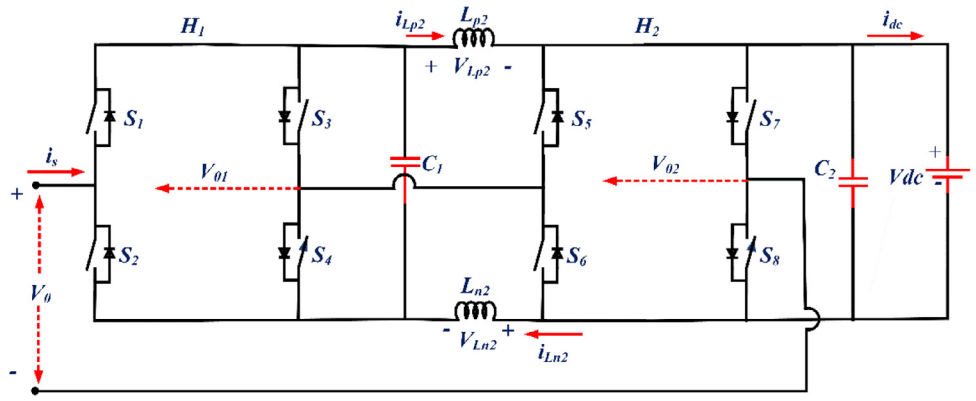

Fig. 4. A new cascaded MLI with a non-isolated dc-link (Soto et al., 2003).

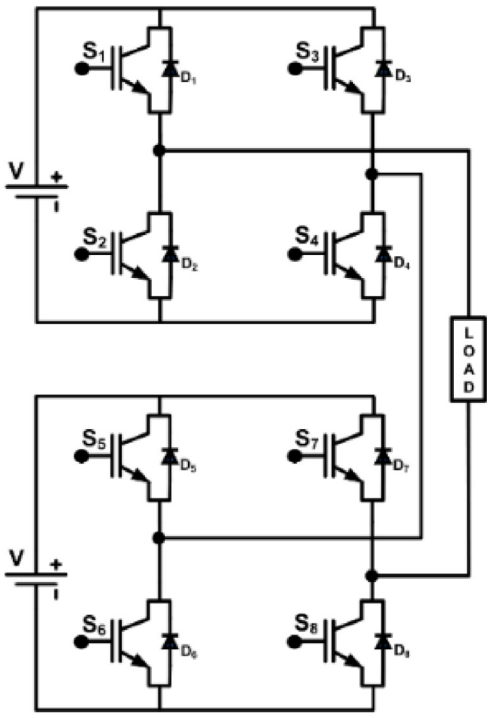

Fig. 5. CHB-MLI configuration (Saeedifard et al., 2012).

applications (Nami et al., 2015) and renewable energy integration (Bana et al., 2019). The switch to the level ratio (SLR) or component by a level factor (CLF) is also employed as a standard count among topologies in previous analyses (Salem et al., 2015), it does not take into account component rates, costs and stress (Rabinovici et al., 2013).

Transformer-less MLI (TL-MLI) topologies, on the other hand, reduce DC voltage sources. However, it suffers from the same drawbacks as symmetrical and asymmetrical MIs, which can be addressed by employing the transformer-based MLIs (T-MLI) (Muneshima et al., 2011). As a result, MLI topologies based on a single DC source became widespread. Transformer-less single DC source MIs (TL-SDCMI) and transformer-based single DC source MLIs are the two varieties (T-SDCMI) (Gateau et al., 2001) as shown in Fig. 2.

Renewable energies account for 25% of worldwide power generation capacity in the current environment (Najjar et al., 2016). The rise in clean energy plants is primarily due to the high levels of pollution produced by burning fossil fuels to meet rising electricity demand. As a result, PV systems need multiple inverters to convert direct current to alternating current. However, the use of multilayer inverters in renewable energy applications poses unique issues, such as the need for a transformer in grid-connected systems to avoid leakage currents. The work's state-of-the-art is a result of the growing demand for more renewable energy and the usage of transformer-based and transformer-less inverters as a grid interface for these technologies. A comparison of the primary multilevel inverter voltage-source topologies utilized in transformerless and transformer-based PV systems is also presented in the article.

The single DC source (T-SDCMLI) can be used without any additional passive components with the help of a transformer. Other advantages of using a transformer in a single DC source MLI include (Bircenas et al., 2002; Singh et al., 2018):

- ➢ Between the AC load and the DC source, the T-SDCMLI provides galvanic isolation.
- ➢ The voltage transformation can be accomplished by adjusting the turns-ratio of the various transformers.
- ➢ The transformer aids in the production of a large number of levels with low THD.
- ➢ Interfacing with utility applications is simple.
- ➢ The cascaded transformer leakage reactance reduces high-order harmonics in the output voltage.

Regardless of the merits mentioned above, as the number of levels in the output voltage increases, using a lot of transformers in a topology increases the cost, weight, and size (Surendra Babu and Fernandes, 2014). The TSDCMLI topologies. The main problem is to reduce the number of transformers and semiconductor switches to obtain a large number of levels and, as a result, increase the output voltage (Khasim et al., 2021). In light of the

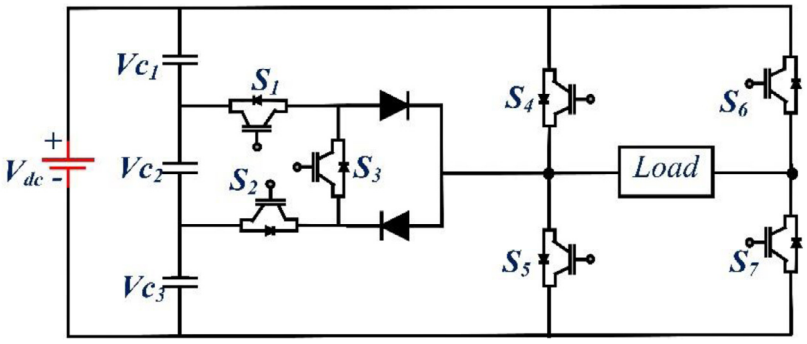

Fig. 6. 7-level MLI with series capacitors (Choi and Kang, 2015).

foregoing, this work gives an outline of the issues, as well as the benefits and limitations of TSDCMI topologies. Furthermore, by comparing several topologies, the ideal topology for a certain application may be quickly identified and deployed based on the requirements. The TSDCMI based topologies are well suited for the applications in which utilization of more than one DC source is required such a electric vehicles (Reddi Khasim and Dhanamjayulu, 2021).

Using various performance measures, several topologies were examined in terms of the number of transformers, semiconductor devices, and output voltage levels (Lu et al., 2013). Furthermore, the equipment required for all T-MLI implementations is described in great detail. Existing topologies include multiple circuit components with multiple sources, increasing circuit complexity and MLI cost (Stynski et al., 2009). In addition, procuring the numerous sorts of sources is problematic in real-time implementation. Existing MLIs have stronger harmonics, a higher TSV, and more power losses, which raises their cost. As a result, these are the limitations identified in the literature, which can be addressed by developing a solution for future single DC source MLIs with optimal components for renewable energy applications (Moeini et al., 2014). A brief of this study also assists researchers in identifying a suitable topology based on application-oriented needs that can be used in future publications.

The remainder of the article is as follows. The various architectures of transformer-less MLIs and a detailed classification and comparisons are presented in Section 2. Section 3 represents the transformer-based architectures with detailed comparisons and classifications. The cost evaluation of the MLIs is presented in Section 4. Finally, Section 5 provides a conclusion and future scope.

2. Transformer less MLI

Fig. 3 (Hammond, 1997; Kang et al., 2005) represents the traditional topologies developed in the 1980s and a patent was obtained to decrease the number of sources. In the 1990s, the CHBMLI-based inverter became popular in the case of the cascaded H-bridges (Hammond, 1997). Later launched was the MLI flying capacitor (FCMLI) (Meynard and Foch, 1992). These extra components were used by only one source (Rodríguez et al., 2002). On the other hand, CHBMLI resolves these problems, but it drives the H-bridge more than with its source. The respective parametric classifications are given in Table 1.

2.1. Single source transformer less MLI

As more input, DC sources have been used to operate symmetric and asymmetrical MLIs, as mentioned above. As a result, a massive input setup with separate input transformers and restructuring of circuits is performed (Babaei et al., 2013). These systems' total cost, installation area, and inverter efficiency play a major role. To overcome these economic and technological challenges, researchers are creating a new MLI configuration based on a single DC source, which is explained in this section in detail. The characteristics of symmetric type MLIs are given in Table 2 and the component comparison is represented in Table 3.

When a single input DC source is used in Soto et al. (2003), authors Soto et al. showed a novel MLI. It is a five-leg structure, as shown in Fig. 4, consisting of two H-bridge cells connected in a cascade and two inductors at the center of the H-bridges (Ghat and Shukla, 2018). In this case, the positive poles of the two H-bridges are linked to one inductor, while the negative poles of the H-bridge cell are connected to the other (Pimentel et al., 2009). In addition, higher levels can include more H-bridge cells and interface inductors. The energy transfer from rear to front is a crucial feature of this edition. High-current switches are required at rates greater than those of a normal CHB inverter.

The availability of substituting the dc sources with H-bridge cells is implemented by the authors in Sepahv et al. (2013). In reality, condensers are placed in h-bridge cells where dc sources are provided, and only one authentic dc source is sent to a complete H-bridge cell. Fig. 1 depicts this system. 15. (b). This method enables the production of low-cost converters. However, the proposed design has one significant flaw: the condenser's voltage balance. To overcome the voltage balancing problem, a new algorithm PWM modulation of the phase shift approach is given. The suggested control technique provides extraordinarily flexible regulation when the inverter feeds contaminated load (highly inductive load).

The authors of Saeedifard et al. (2012) discussed the idea of the ability to balance loads by employing an Active Neutral Closed Point (ANPC), which examines and assesses its achievement shown in Fig. 5. The authors investigate the load balancing potential further using a new Space Vector Modulation (SVM) control method (Gao, 2016). Authors in the proposed SVM-based balancing technique, in particular, seven-tier converters are proposed and assessed different operating situations. In comparison with its seven-level hybrid arrangement (Manjrekar et al.,

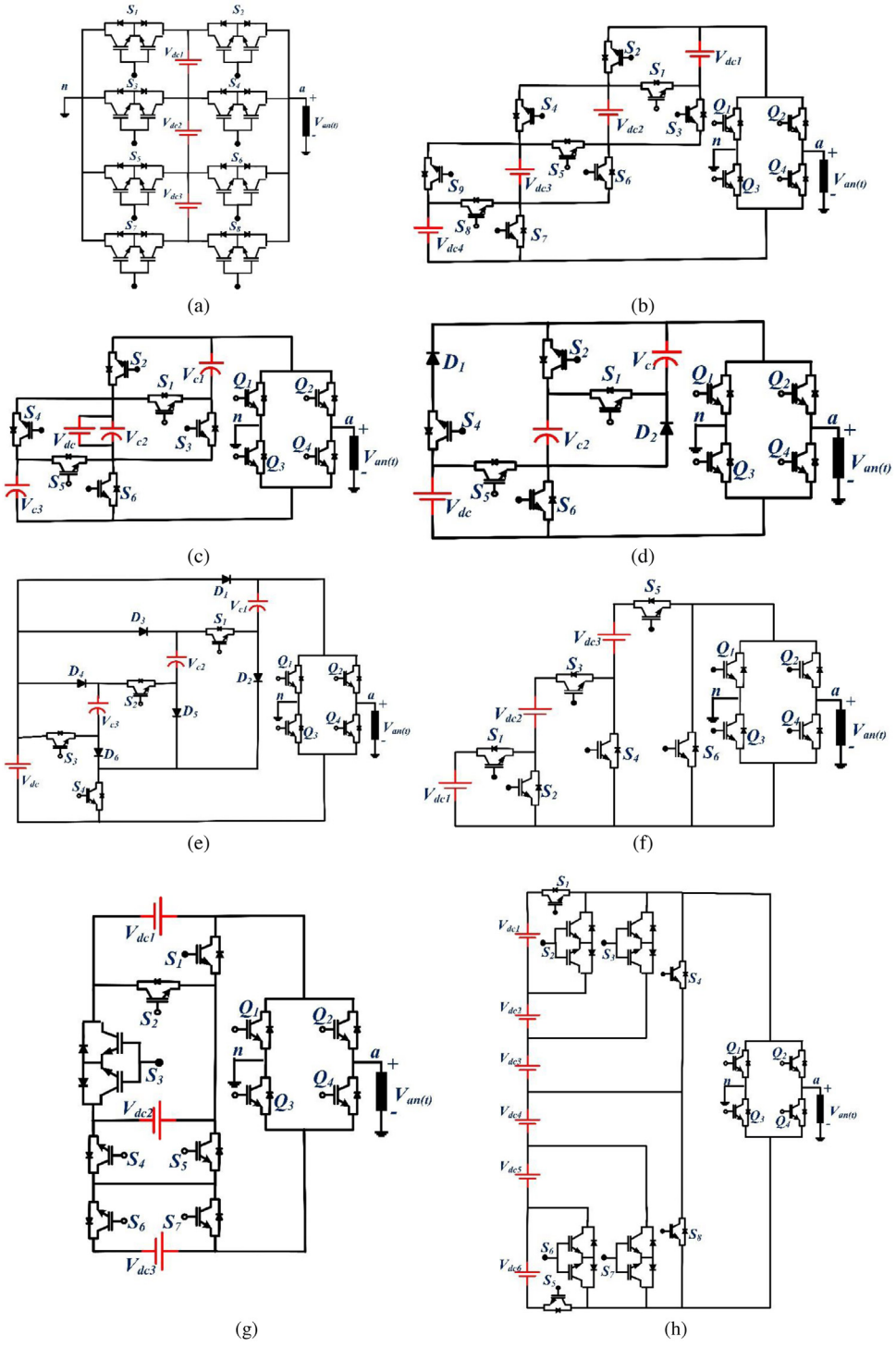

Fig. 7. Symmetrical MLI structures (a) Babaei (2008) (b) Hinago and Koizumi (2009) (c) Hinago and Koizumi (2012) (d) Liu et al. (2017) (e) Ye et al. (2014) (f) Choi and Kang (2009) (g) Sarbanzadeh et al. (2019) (h) Kangarlu and Babaei (2013).

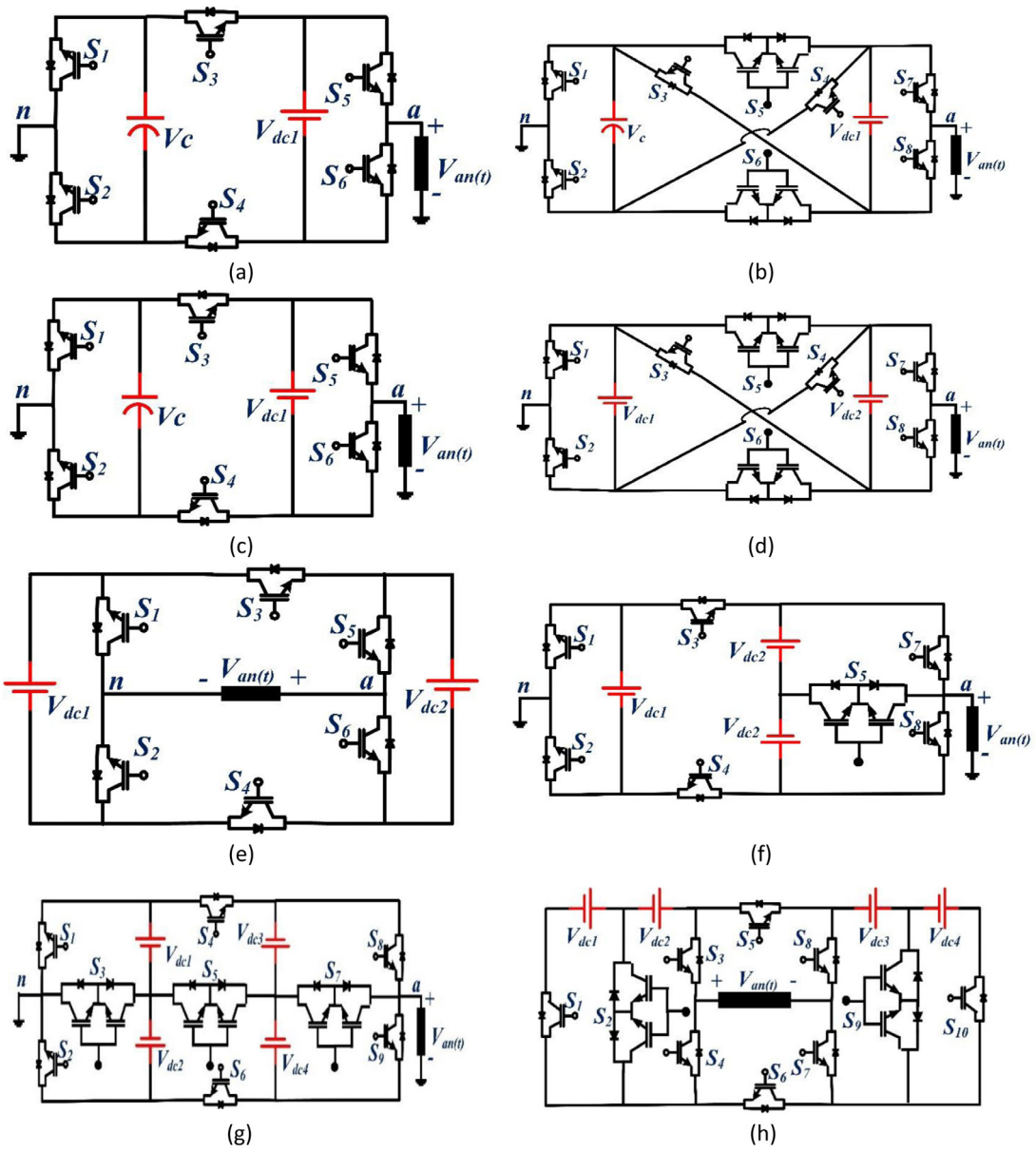

Fig. 8. Asymmetrical MLI structures: (a) Vahedi and Al-Haddad (2016b) (b) Vahedi et al. (2013) (c) Gupta and Jain (2013) (d) Gupta and Jain (2012b) (e) Babaei and Laali (2015) (f) Vijeh et al. (2016) (g) Samadaei et al. (2018) (h) Alishah et al. (2016).

2000) which uses eight semi-conductor devices per phase, the suggested architecture for seven levels requires more switching devices, and consists of 14 devices per phase. As more voltage condensers are present in the topology, which is a significant disadvantage.

In Choi and Kang (2015), the author developed a seven-level PWM inverter with a single DC supply represented in Fig. 6. The proposed design can significantly increase output voltage by using fewer switching components (Malinowski et al., 2010). In this design, the author used cascade H-bridges, diodes, active switches, and series capacitors. When energy storage devices such as capacitors are employed in a circuit, the circuit becomes more efficient., it is well known that voltage balance issues may arise (Sahoo and Bhattacharya, 2018). The author, on the other hand, discusses this issue thoroughly and presents a novel control mechanism that is suitable for the application. The Maximum Voltage Ratio (MVR) is a recommended approach parameter according to the author and is MVR = 1 hence the design is not suited for use in a high-voltage environment.

Summary

Only single-phase (Banaei et al., 2012; Soto et al., 2003; Sanjeevan et al., 2016) MLI topologies have been presented in this section, and they are all based on single DC source MLI topologies. Because configuration operates on huge devices like condensers,

Table 1
Classification & features of conventional MLI.

Parameters	Diode clamped (Dargahi et al., 2014)	Flying capacitor (Khazraei et al., 2012)	Cascaded H-Bridge MLI (Franquelo et al., 2008; Qi et al., 2016)
Switch count in terms of number of level (N_L)	$2(N_L - 1)$	$2(N_L - 1)$	$2(N_L - 1)$
Number of dc sources	1	1	$(N_L - 1)/2$
Number of diodes	$(N_L - 1)\times(N_L\text{-}2)$	0	0
Number of capacitors	$(N_L - 1)$	$N_L\times(N_L - 1)/2$	0
Zero level generation	Clamping diodes and switches	Clamping capacitors and switches	Only semiconductor switches/diode
Key features	• Only one dc source is required as an input • Structure with a more dependable and efficient basic frequency	• There is only one isolated source. • More flexibility in active and reactive power control	• Fewer devices count • The circuit structure is scalable, easy and very modular
Shortcomings	• Many condensers and clamping diodes are necessary for greater level generation. • Voltage balance is hard	• Includes more condensers to achieve higher levels • For high-power applications, the structure is large and costly.	• More devices count • More isolated dc sources are required
Suggested applications	• For Medium and low voltage • PV application and AC motor driving applications	• For Medium and low voltage • Drives application	• Medium-high voltage • Drives, electric vehicles and applications for renewable energy

inductors, and transformers is indeed troublesome for medium power applications. These topologies could be widely used in the electrical market once bulky gadgets are removed. Due to the uneven architectures, the comparison of components becomes complex.

2.2. Multi-source transformer less MLI

In general, multi-source MLIs are classified based on the magnitude of sources, such as symmetric based on equal sources (Gupta and Jain, 2014a; Farhadi Kangarlu and Babaei, 2013; Jacobson et al., 2010) shown in Fig. 7, asymmetric based on unequal sources (binary, trinary and etc.) (Alishah et al., 2016; Lai and Shyu, 2002; Gupta and Jain, 2012b) shown in Fig. 8, with inherent negative level (Vahedi and Al-Haddad, 2016a,b) or without inherent negative level (Thamizharasan et al., 2014; Babaei and Laali, 2015) single sources by capacitor links (Ilves et al., 2013; Hagiwara et al., 2010) regenerative architecture that can be used as a rectifier or inverter (Mudadla et al., 2015; Odeh et al., 2016) and NPC, FC, and CHB combine to form a hybrid (Hagiwara et al., 2010; Odeh et al., 2016). It is worth noting that the majority of these topologies share comparable structures, which will be addressed in more detail in the next sections. A generalized comparison of symmetrical and asymmetrical MLIs are represented in Tables 4 and 5 respectively.

The literature on hybrid MLIs is discussed in this section (HMLI). The major goal of studying HMLI topologies is to combine a variety of semi-conductive switches, topologies, and/or modulation algorithms to maximize the overall system's power processing capability. Zhou et al. on the other hand, published a study on HMLI-Topology hybrid modulation schemes in Jinghua and Zhengxi (2008). However, the author made no mention of semiconductor switches or hybrid systems based on topologies. This section about discusses the current hybrid architectures and control methods. Manjrekar et al. (2000), Manjrekar and Lipo (1998) developed a new seven-level HMLI that used two separate cascade-connected H-bridges based on equipment changes. As a result, the converter output has a lower THD and a greater output voltage. All bridges, on the other hand, are powered by an isolated dc source with varying switching frequencies to represent the increased complexity of the switching and the necessity for the input transformer (Lund et al., 1999), topology's effectiveness is drastically reduced due to circulating currents in the H-bridges resulting in modularity loss and increased manufacturing costs, hence there exists limited commercial uses (Abu-Rub et al., 2010).

The authors presented a symmetrical MLI design on 5, 7, and 15 levels. The suggested 5-level MLI is designed utilizing the basic unit developed without the addition of circuit components. The circuit comprises fewer switches than the previous topologies. This architecture includes nine switches and three condenser-less DC springs represented in Fig. 9(a). Problems with power quality, such as THD, a smaller number of switches, and dv/dt stress, are eliminated with the proposed multi-level inverter. Three V_1, V_2, V_3 switches as well as nine S_1, S_2, S_3, S_4, S_5, S_{H1}, S_{H2}, S_{H3}, and S_{H4} switches, are included in the H-Bridge modules (Sé et al., 2008). The solution reduces the number of switches required and reduces the requirement for additional DC sources. Fig. 8 depicts the five-level MLI operation modes. The suggested 7-level MLI is built with an enhanced basic unit that contains an additional S_6 switch that is connected to the S_1 and V_1 series. There are fewer switches in this circuit than in earlier topologies. Fig. 9(b) shows a topology with ten switches and three DC sources without capacitors. Problems with power quality such as THD, less number of switches, and dv/dt stress, are eliminated with the proposed multi-level inverter. With two built fundamental units, the proposed 15-level MLI is formed in a cascade without the addition of circuit components. This architecture is developed using seven DC sources and seven switching diodes, as shown in Fig. 9(c). Power quality issues such as THD, fewer switches, and dv/dt stress are reduced with this newly designed multilevel inverter. To create a negative voltage level, the S_{H1}, S_{H2}, and S_{H4} switches are connected with an H-Bridge. The characteristics of asymmetrical MLI are shown in Table 6.

The proposed 15-level MLI is built around two fundamental basic units cascaded and does not require any circuit components. The architecture includes seventeen capacitor-free switches and

Table 2
Features of symmetrical type MLI architectures.

Ref.	Merits	Limitations
Lai and Peng (1996)	• You can modify the voltage level by adding or removing the H-bridge units. • Easy to design and upgrade to	• There are extra losses and a large installation area, and safety circuits are to contend with. • All levels are not possible to generate • More circuits are required for Gate drives
Babaei et al. (2007)	• It has reduced the number of gate drive circuits. • It is possible to take it to a greater level. • There is no need for a second H-bridge.	• More switches than SCHB-MLI topology are required • Not appropriate for applications with fault tolerance
Babaei (2008)	• It produces all levels at its output • There are fewer gate driver circuits required.	• An extra H-bridge is required to generate a complete AC waveform.
Babaei and Hosseini (2009)	• It can produce all levels at full capacity. • The device count is lower than in the previous three topologies.	• A voltage balancing issue can occur. • Switches of various ratings are required. • A second H-bridge is required.
Choi and Kang (2009)	• The number of IGBT switches required is significantly less than in the previous symmetrical systems mentioned.	• Asymmetrical DC input values cannot be used with this structure.
Hinago and Koizumi (2010)	• It is possible to share the load equally. • If it reaches a higher level, it has fewer semiconductor switches than symmetrical CHB.	• The load was shared unequally across the input DC sources. • The higher-rated switches are not switched at the same pace as the lower-rated switches.
Waltrich and Barbi (2010)	• Valid for all uses where a multilayer symmetric CHB inverter is employed.	• A large number of DC input sources is required.
Farhadi Kangarlu et al. (2012)	• The construction can be extended to the second level. When compared to the symmetrical designs previously stated, the necessity for gate drive circuits is considerably reduced.	• To generate a complete AC waveform, an additional H-bridge is necessary.
Babaei et al. (2012)	• The SPWM technique is used to implement it. • Lesser conduction losses	• Switches made of semiconductors with greater voltage ratings are required. • A second H-bridge inverter is required.
Patra et al. (2018)	• Switching losses are minimized. • It is capable of fundamental switching.	• It is not possible to share the weight equally. • A second H-bridge inverter is needed.
Farhadi Kangarlu and Babaei (2013)	• The less important the device is as symmetrical as CHB • It is not necessary to use an external H-bridge.	• Multi-tension strains on semiconductor switches
Gupta and Jain (2012a)	• The device count is significantly lower than in a symmetrical CHB design.	• It is impossible to share the load equally. • Basic switching modulation is no longer valid.
Alishah et al. (2014)	• It is simple to take it to the next level. • The most cost-effective converter • It provides the smallest number of gadgets to gain additional levels.	• To generate the full AC waveform, H-bridge must be included
Mokhberdoran and Ajami (2014)	• The number of duplicate states is increasing. • Equal load sharing is possible	• Not all output voltage levels (only a few unusual voltages can reach 5, 9, 13, 17... etc.) are possible.
Babaei et al. (2015)	• It can extend to any level • The less important the device is as symmetrical as CHB	• To generate all output levels of the proposed architecture, the inverter requires additional DC. • A second H-bridge is also necessary.

seven DC sources, as shown in Fig. 9(c). This multilevel inverter solves power quality issues such as THD, fewer switches, and dv/dt stress. The negative voltage is created by connecting the H-Bridge Switches S_{H1}, S_{H2}, S_{H3}, and S_{H4} (see Fig. 10).

Fig. 11 represents the suggested architecture for each phase, which includes two bidirectional and nine unidirectional power semi-conductive switches for each phase (Vodyakho et al., 2008). Short circuits are prevented by using bi-directional switches, which block the DC supply in either direction. This architecture usually achieves the desired stress from numerous DC voltage connections or sources. The suggested 3-phase 19-level MLI is represented in Fig. 11. Based on the DC sources, cascaded MLIs are classified as symmetrical or asymmetrical. In the symmetrical kind, the voltage of the DC connections is maintained at the same level. The disadvantage of the symmetric architecture is that the output voltage rises with the number of switches.

The challenge of designing an HMLI is significantly increased as a result of this. Rech and Pinheiro addressed this issue in Rech and Pinheiro (2007). The proposals were made for the development of innovative HMLI configurations with several topologies in each cell (two, three and five-level blocks). The circulation energy in the cells was reduced in this way, but it did not affect the output voltage level because the third cell is lower than the

Table 3
Generalized components data for MLI.

	N_{DC}	N_L	N_{IGBT}	N_G	N_{MCPS}	$V_{L,max}$	$V_{dc,(j)}(j = 1, 2, \ldots n)$
Manjrekar et al. (2000)	p	2(p+1)-1	4p	4p	2p	$(2p-1)V_{dc}$	$2^{j-1}\times V_{dc}$
Lai and Shyu (2002)	p	3^p	p	4p	2p	$(3p-1)V_{dc}/2$	$3^{j-1}\times V_{dc}$
Mueller and Park (1994)	p	$2 \times 3^{(p-1)} + 1$	4p	4p	2p	$3(p-1)V_{dc}$	$V_1 = V_{dc} V_j = (2 \times 3)^{j-2}\times V_{dc}(j = 2, 3, \ldots p)$
Du et al. (2006)	p	4p-1	2p+4	2p+4	p	$(2p-1)V_{dc}$	$V_1 = V_{dc}$; $V_j = 2V_{dc}(j = 2, 3, \ldots p)$
Babaei et al. (2007)	p	p^2+p+1	4(p+1)	2(p+1)	4	$(2p-1)V_{dc}$	$2^{j-1}\times V_{dc}$
Gupta and Jain (2012b)	p	6p-3	4p	4p	p+1		$V_1 = 3V_{dc}$; $V_n = V_{dc}(j = 2, 3, \ldots p)$
Babaei et al. (2012)	p	2(p+1)-1	2p+4	2p+4	p+2	$(2p-1)V_{dc}$	$2^{j-1}\times$Vdc
Gupta and Jain (2014a)	p	p^2+p+1	2(p+1)	2(p+1)	p+1	$p(p+1)V_{dc}/2$	–
Babaei et al. (2014b)	p	$2 \times 3^{(p)} + 1$	4(p+1)	4(p+1)	2p+2	$(3p-1)V_{dc}$	$3^{j-1}\times V_{dc}$
Alishah et al. (2014)	p	2(p+1)-1	p+4	p+4	p+2	$(2p-1)V_{dc}$	$2^{j-1}\times V_{dc}$
Babaei et al. (2014a)	2p	2(p+1)-1	2p+2	2p+2	2p+1	$3 \times 5^{p-1} V_{dc}$	–
Mokhberdoran and Ajami (2014)	2p	5p/2	3p	3p	2p	$\{(5^{p-1})/2\}V_{dc}$	$5^{j-1}\times V_{dc}(j = 1, 2, \ldots .p)$
Samadaei et al. (2016)	4p	3p+1	2.5p	2p	5p	20p	$V_1 = V2 = 2\times V_{dc} V_3 = V4 = V_{dc}$
Ounejjar et al. (2011)	p	2(p+1)-1	2(p+1)	2(p+1)	p+1		$V_1 = V_{dc} V_j = NL\times V_{dc}(j = 2, 3, \ldots p)$

load voltage (highest cell). However, only a few relevant variables are considered in this analysis, Efficiency, weight/volume, and other harmonic aberrations are examples. Also, only single-phase topologies have been described by Rech and Pinheiro. The characteristics of hybrid MLIs are provided in Table 7.

The MLI proposed MLI in Prasad et al. (2021) of 31 levels expands the architecture of thirteen output levels as shown in Fig. 12. The proposed 31-level MLI comprises 14 one-way switches from S_1 to S_{14} and 4 voltage sources V_1, V_2, V_3, and V_4. As each of the four sources consists of a different voltage magnitude, the proposed topology layout becomes unbalanced. The input voltages are chosen sequentially for the 31-level DC source with a ratio of 1:2:4:8.

Fig. 13 represents a new 15-level inverter topology. The DC-link voltage of the solar PV boost converter is delivered to the proposed inverter as a source. The inverter includes eight unidirectional switches and three DC sources. The switches are selected in the specific direction of the current crossing based on a way to avoid short circuits in the proposed asymmetric MLI of 15 levels. The S_2, S_3, S_5, and S_7 switches, which create a locked channel with accurate short circuits, provide the starting level. The total standing voltage is calculated by taking into consideration the blocking voltage of switches in this mode of operation. In the second mode of operation, the S_2, S_3, S_5, and S_8 switches are used. These are chosen to avoid a short circuit, and there is a lower value for adding the maximum blocking voltages of each semiconductor switch, resulting in reduced TSV and costs. The switches are chosen based on the above criteria, with the full switch control loop delivering an efficient inverter with a reduced voltage across the switches.

Fig. 14 in Hinago and Koizumi (2009) Hinago and Koizumi represent a novel HMLI. It is made up of two distinct, series-connected topologies that are driven by hybrid switches (Liu et al., 2008; Zhang et al., 2001). The above-mentioned parts are explored individually from these two series of topologies. In comparison to symmetric CHB inverters, these are modulated at a basic frequency and converted to H-bridge at high frequencies, the serial-parallel converter features a lesser number of switching components. As a result, in high-power applications, the introduced version is employed. It can also be expanded to satisfy more stringent requirements. However, there are some disadvantages, including a modularity loss, high control complexity, and higher production costs. The single-phase design is in such a way that it covers exclusively in the author's report. Nami et al. presented a new hybrid converter in Nami et al. (2011) that consists of two independent conventional MLI (diode clamped MLI and cascaded H-bridge MLI) configurations coupled in series to achieve higher output levels with minimal losses. In this scenario, a clamped diode inverter receives its input from a multi-output boost (MOB) converter. This design worked asymmetrically instead of symmetrically to get a few more output volts. With the same number of components as before and the same filter size, THD is greatly improved. In order to maintain the supply input, however, advanced modulation techniques and extra circuits are required.

Rajeevan et al. in Rajeevan et al. (2011) For industrial driving applications, a new hybrid nine-level inverter structure was designed. Two conventional three-phase (two levels) inverters are supplied by separated input in this configuration. Six H-bridges are fed by capacitors and are connected to DC sources. It has a few unique characteristics, such as eliminating three-phase harmonic winding current and lowering switching losses by using a high-voltage inverter with low switching frequencies. It may also be utilized in three-level mode if a switch fails in H- Bridges. When the level rises, however, the design is complicated to control.

Applications of all aforesaid configurations

Table 4
Generalized components data of symmetrical type MLIs.

	N_S	N_G	N_D	N_{DC}	N_C	(TSV)×V_{DC}	Negative level
CHB	$4\left[\frac{N_L}{2}\right]$	$4\left[\frac{N_L}{2}\right]$	$4\left[\frac{N_L}{2}\right]$	$4\left[\frac{N_L}{2}\right]$	–	$4\left[\frac{N_L}{2}\right]$	
Sun et al. (2016)	$14\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	
Vizheh et al. (2016)	$11\left[\frac{N_L-3}{10}+1\right]$	$10\left[\frac{N_L-3}{10}+1\right]$	$11\left[\frac{N_L-3}{10}+1\right]$	$6\left[\frac{N_L-3}{10}+1\right]$	–	$22\left[\frac{N_L-3}{10}+1\right]$	inherent
Gupta and Jain (2013)	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	–	$8\left[\frac{N_L-2}{4}+1\right]$	
Gupta and Jain (2012b)	$10\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$10\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	–	$8\left[\frac{N_L-2}{4}+1\right]$	
Babaei et al. (2014c)	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L}{2}\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	
Alishah et al. (2016)	$8\left[\frac{N_L-2}{6}+1\right]$	$7\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$13\left[\frac{N_L-2}{6}+1\right]$	
Babaei (2008)	$2(N_L+1)$	N_L+1	$2(N_L+1)$	$\left[\frac{N_L}{2}\right]$	–	$\left[\frac{(N_L+1)(3N_L-1)}{8}\right]$ for odd sources $\left[\frac{(N_L+1)(3N_L+5)}{8}\right]$ for even sources	
Su (2004)	N_L+3	N_L+3	N_L+3	$\left[\frac{N_L}{2}\right]$	–	$3(N_L-1)$	
Babaei et al. (2014b)	$8\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	$12\left[\frac{N_L-2}{4}+1\right]$	
Hinago and Koizumi (2009)	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\left[\frac{N_L}{2}\right]$	–	$\frac{7N_L-13}{2}$	
Hinago and Koizumi (2012)	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	1	$\left[\frac{N_L}{2}\right]$	$\frac{7N_L-13}{2}$	With H-bridge
Zamiri et al. (2016)	$22\left[\frac{N_L-3}{16}+1\right]$	$22\left[\frac{N_L-3}{16}+1\right]$	$28\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-3}{16}+1\right]$	$6\left[\frac{N_L-3}{16}+1\right]$	$88\left[\frac{N_L-3}{16}+1\right]$	
Liu et al. (2017)	$9\left[\frac{N_L-2}{6}+1\right]$	$9\left[\frac{N_L-2}{6}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	$17\left[\frac{N_L-2}{6}+1\right]$	
Ye et al. (2014)	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$14\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$3\left[\frac{N_L-2}{8}+1\right]$	$17\left[\frac{N_L-2}{8}+1\right]$	
Choi and Kang (2009)	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$21\left[\frac{N_L-2}{6}+1\right]$	
Najafi and Yatim (2012)	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$19\left[\frac{N_L-2}{6}+1\right]$	
Sarbanzadeh et al. (2019)	$12\left[\frac{N_L-2}{6}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$19\left[\frac{N_L-2}{6}+1\right]$	
Moham-madalibeigy and Azli (2014)	$10\left[\frac{N_L-2}{8}+1\right]$	$7\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{8}+1\right]$	$4\left[\frac{N_L-2}{8}+1\right]$	–	$8\left[\frac{N_L-2}{8}+1\right]$	
Farhadi Kangarlu et al. (2012)	$16\left[\frac{N_L-3}{14}+1\right]$	$12\left[\frac{N_L-3}{14}+1\right]$	$16\left[\frac{N_L-3}{14}+1\right]$	$7\left[\frac{N_L-3}{14}+1\right]$	–	$72\left[\frac{N_L-3}{14}+1\right]$	
Kangarlu and Babaei (2013)	$16\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$16\left[\frac{N_L-2}{12}+1\right]$	$6\left[\frac{N_L-2}{12}+1\right]$	–	$44\left[\frac{N_L-3}{14}+1\right]$	

There exists various applications for the MLIs, out of these some of them are as follows: the authors described in Babaei et al. (2014b), Rech and Pinheiro (2007) and Khomfoi and Aimsaard (2009) use a combination of all MLI variations in active filters in power system operation. For hybrid electric vehicle applications, the authors proposed in Ruiz-Caballero et al. (2010), Rajeevan et al. (2011) and Pereda and Dixon (2011), In the interfacing of renewable energy sources, the authors proposed in Nami et al. (2011) and Saeedifard et al. (2012). For HVDC transmission systems, the authors in Babaei et al. (2014b) and Samadaei et al.

Table 5
Generalized components data of asymmetrical type MLIs.

	N_S	N_G	N_D	N_{DC}	N_C	(TSV)×V_{DC}	Negative level
CHB (binary)	$8\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	
CHB (trinary)	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$2\left[\frac{N_L-2}{8}+1\right]$	–	$16\left[\frac{N_L-2}{8}+1\right]$	
Vahedi and Al-Haddad (2016a)	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	
Vahedi and Al-Haddad (2016b)	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	inherent
Vahedi et al. (2013)	$10\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$20\left[\frac{N_L-2}{8}+1\right]$	
Gupta and Jain (2013)	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	
Gupta and Jain (2012b)	$10\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$14\left[\frac{N_L-2}{6}+1\right]$	
Babaei and Laali (2015)	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	
Vijeh et al. (2016)	$8\left[\frac{N_L-3}{10}+1\right]$	$7\left[\frac{N_L-3}{10}+1\right]$	$8\left[\frac{N_L-3}{10}+1\right]$	$3\left[\frac{N_L-3}{10}+1\right]$	–	$22\left[\frac{N_L-3}{10}+1\right]$	
Sarbanzadeh et al. (2016)	$10\left[\frac{N_L-2}{12}+1\right]$	$8\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$25\left[\frac{N_L-2}{12}+1\right]$	
Samadaei et al. (2016)	$10\left[\frac{N_L-2}{12}+1\right]$	$8\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$28\left[\frac{N_L-2}{12}+1\right]$	
Samadaei et al. (2018) (binary)	$12\left[\frac{N_L-2}{12}+1\right]$	$9\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$29\left[\frac{N_L-2}{12}+1\right]$	
Samadaei et al. (2018) (trinary)	$12\left[\frac{N_L-3}{16}+1\right]$	$9\left[\frac{N_L-3}{16}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$4\left[\frac{N_L-3}{16}+1\right]$	–	$39\left[\frac{N_L-3}{16}+1\right]$	
Alishah et al. (2016)	$12\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$30\left[\frac{N_L-2}{16}+1\right]$	

(2016) are employed. Manjrekar and Lipo (1998) and Kiran Kumar and Sivakumar (2015) are widely in motor driven applications and Pereda and Dixon (2012) and Araujo-Vargas et al. (2014) are proposed MLIs for aviation and marine propeller transportation and the representation is shown in Fig. 15. The control scheme and power electronic switches design and various quantitative details are tabulated in Table 8.

3. Transformer based MLI

As the single-sourced T-MLI technology is becoming more widely used in a variety of applications, several difficulties need to be addressed in detail. Due to the number of output voltage levels requiring fewer components, new topologies are replaced with the traditional topologies with the reduction of driver circuits, transformers and power switches. As a result, reducing switches has a direct impact on conduction losses, resulting in efficiency levels. Furthermore, due to the modulation, each unit having the same construction may be used separately. Because of the modulation nature, the fault can be replaced quickly and maintenance expenses are reduced. To resolve these issues, the current work investigates each T-MLI architecture discussion. The switching techniques and applications are tabulated in Table 9. The state-of-art of the MLI with its generalized features are represented in Table 10.

The MLI is now employed in a variety of applications, even with semiconductor devices rated at a moderate power level This is due to substantial developments in power electronics in recent years (Reddy et al., 2015). These are discussed in a variety of contexts, including, industrial applications (Kawabata et al., 1996) usage, power quality applications (Varschavsky et al., 2010; Acuna et al., 2014), traction motor applications and also renewable energy supply in Carpita et al. (2008), power stations and systems whose services in Mohamed et al. (2013), and heavy machinery in Kouro et al. (2010) and Gupta et al. (2016). MLIs have several advantages, including lower switching losses, less voltage stress between devices, and fewer harmonics (Colak et al., 2011). Fig. 16 represents a graphical representation of the types and utilization of various transformer-based topologies. There exists a variation in several characteristics with the increase of voltage (Belkamel et al., 2013; Bayat and Babaei, 2012).

In general, there exist two types of MLIs based on their energy conversion processes such as direct conversion and indirect conversion (Abu-Rub et al., 2010). Load is directly connected to the supply in the direct conversion process whereas, in indirect conversion, there exists an energy storage element like the capacitor is connected in between the load and source. High-power applications have a limitation on direct conversion systems, whereas low-power applications on indirect conversion systems (Prabaharan and Palanisamy, 2017). Single and multiple DC sources (Venkataramanaiah et al., 2017) are incorporated into modern topologies. For symmetric and asymmetric topologies,

Table 6
Features of asymmetrical MLI.

Ref.	Merits	Limitations
Manjrekar et al. (2000)	• The first asymmetrical topology in CHB (binary mode) • The unit cell has a lower voltage of connections with a high DC connection voltage • Switching losses are less	• Switches of various ratings are required. • The charge balance is not achievable due to higher design costs. • Modularity is lost.
Mueller and Park (1994)	• Compared with As-1 topology the level for this topology is much raised • It has consistent MVR which results in better production. • This is called an almost linear setup	• Switches with different ratings are needed. • The charge balance is not achievable due to design costs. • Modularity declines
Lai and Shyu (2002)	• One of the most common asymmetric topologies is this one. • This is called Trinary configuration • It has the highest level of the above two topologies for a given number of input DC sources	• It is required to have a large number of DC voltage sources. • Different switch ratings are required. • The charge balance is not achievable due to higher design costs. • Modularity is lost.
Babaei et al. (2007)	• There are the fewest driving path devices accessible. • Voltage decreases and driving losses are decreased • Negative levels do not necessitate the use of a high-voltage H-bridge.	• Some levels are skipped • Various switch ratings are necessary. • Not applicable for applications tolerated by fault • It is not possible to maintain a charge balance. • Modularity is lost.
Du et al. (2006)	• It is possible to share the load equally • Conduction losses are minimized • The structure is very simple	• For negative levels, another H-bridge is necessary. • Rounding state switching is lower • Various switch ratings are necessary
Ounejjar et al. (2011)	• It has a few capacitors and power • Devices for increased phase output levels • The production costs are quite low • Negative levels do not necessitate the use of a high-voltage H-bridge.	• Various voltage rating switches are necessary • Loss of modularity • Design cost is more
Gupta and Jain (2012b)	• It is feasible to achieve a charge balance. • Because more redundant states are available, they can be used in fault-tolerant applications. • Without the use of additional H-bridges, it can potentially yield negative levels during the output phase.	• Loss of Modularity • Various voltage rating switches are necessary.
Babaei et al. (2012)	• Equal load sharing is possible • Simple structure • Fewer power Semiconductors switch frequently enough to produce greater output voltages.	• There are several different types of input DC voltage sources. • To generate negative levels, a Loss of Modularity. • H-bridge is needed.
Gupta and Jain (2014a)	• When compared to cascaded H-bridge topologies, there are fewer active switches. • Switching losses are kept to a minimum.	• Switches of various ratings are required. • Inverter costs are substantial. • For higher levels, it is impossible to distribute the load evenly across all input sources.
Babaei et al. (2014b)	• The number of DC sources that are independent is decreasing.	• The problem of voltage balance is increasingly serious.
Alishah et al. (2014)	• It has a lower number of power switching devices and gate drivers than other topologies. • The overall cost of an inverter is minimal.	• An additional high-voltage H-bridge is required. Maintaining a charge balance is impossible. • Modularity is lost.
Babaei et al. (2014a)	• It has switches with a reduced blocking voltage. • Less complexity • The inverter's entire cost must be kept to a minimum.	• Higher voltage source variations are necessary • MVR is high
Mokhberdoran and Ajami (2014)	• Negative levels do not necessitate the use of a high-voltage H-bridge. • For the same amount of DC sources, it has the highest NL than other topologies	• More diodes with varying ratings are necessary • Switches with various voltage ratings are required.
Samadaei et al. (2016)	• It is simple to do. Modularized • Negative levels do not necessitate a high-voltage H-bridge. • Can be employed in defect-tolerant applications. • It is feasible to achieve a charge balance. • Only two voltage sources are available. • It is not possible to have a short circuit. • The expense of design is modest.	• More DC inputs than other topologies are required • It features the maximum number of current path devices that lead to further driving losses

Table 7
Features of hybrid MLI.

Ref.	Merits	Limitations
Manjrekar et al. (2000)	• It increases the power quality by creating additional steps with specific H-bridge modules. • Using particular H-bridge modules enhances power quality by creating additional steps.	• Switching pressures are higher. • Isolated asymmetric DC sources are required.
Rech and Pinheiro (2007)	• A Hybrid MLI model that has been generalized. • The flow of energy between standard cells can be minimized	• The design of the circuit was challenging as topology needed more
Khomfoi and Aimsaard (2009)	• It has fewer switches to achieve optimal voltage than normal cascaded MLI	• Charge balance and energy concerns severely affect the system as a whole when problems arise in choosing DC sources
Ruiz-Caballero et al. (2010)	• It improves low distortion and smaller output filter shape • The DC source in the waterfalls of the H-bridge is less isolated than	• CHB MLI requires more than semiconductive devices
Hinago and Koizumi (2009)	• The number of switching components is reduced when compared to the Multi-Level Inverter. • Compact in size and easy to extend to higher	• Loss of modularity • It requires many isolated DC sources
Nami et al. (2011)	• Its control complexity is simpler, and it can attain higher voltage resolution.	• Since clamping diodes and rectifiers were added, the total cost of the system has increased.
Rajeevan et al. (2011)	• It has lower switching losses	• When the level rises, the charge balancing becomes more complicated.
Babaei et al. (2012)	• The voltage ratings for power switches decreasing make them more compatible with higher voltage networks.	• The use of voltage balance control techniques does not appear to be promising. • MLI's rated output voltage limits higher voltage levels, but some switches should be able to handle it.
Alishah et al. (2014)	• By reducing the number of switching devices, it may acquire the maximum number of voltage levels.	• Voltage stresses the switches, which act as a limiter for greater voltage levels. • It is only employed in unidirectional power flow situations.

there is also an asymmetrical (different sources picked occasionally in binary or trinary form) topology classification (Barzegarkhoo et al., 2016; Elias et al., 2014). The higher levels of voltage are discussed in Morales et al. (2015). When determining the inverter topology, DC sources are an important factor to consider (Babaei et al., 2014c). If higher inverter levels are employed in Agrawal and Jain (2017), complexity and prices will rise. The necessity of lowering circuit size and DC source parameters is increasingly emphasized by researchers (Araujo-Vargas et al., 2014).

3.1. Single source transformer-based MLI

Kang et al. (2005) Employs a multilevel PWM inverter cascaded transformers represented in Fig. 17. The suggested MLI differs from traditional multilevel arrangements in such a way that it is powered by a single source that is split into two pieces depending on its functionality. PWM controls one portion, while the other is employed to create a waveform staircase. Water-based transformers provide galvanic separation between the input DC source and the load, resulting in less semiconductor switching and increased reliability. As a result, these topologies are better suited to photovoltaic applications. However, a huge transformer has been used, which harms the performance of the inverter.

The DC sources count has been limited and (Kouro et al., 2010) utilized as a three-phase cascaded transformer network represented in Fig. 18. The output voltage from $+V_{dc}$ to $-V_{dc}$ is the primary winding of the single-phase cascaded transformers that have been integrated into the proposed architecture unlike in traditional topologies. However, the secondary windings of each bridge are connected in a cascade per phase. As stated, the primary complexity in this topology is to create stairwell forms with lower THD while reducing the number of transformers utilized. However, the problem of cascading transformer implementation is huge and expensive.

There will be a reduction in the number of transformers. When the current transformers' instantaneous voltages are added or subtracted, the turn ratio changes. The output voltage will be enhanced in addition to a reduction in the number of transformers used (Sabate et al., 2004). The architectural layout of the proposed method based on the reduction in the transformers count is presented in Carpita et al. (2008). The turns required to construct a waveform staircase and the output voltage possibilities are given in Eq. (1).

$$N_L = 3^n,\ n = 1, 2, 3, \ldots. \tag{1}$$

Choi and Kang (2009) Describes a new MLI structure that generates nineteen output voltage levels. However, like all other topologies have many drawbacks such as the controlling algorithms are quite complex in this design implementation. For a 3-phase operation, the total operation and layout are quite sophisticated. In addition to all of this, there creates an additional burden of expensive costs (see Fig. 19).

Franquelo et al. (2008) Describes a complex method of decreasing the use of transformers and SDC by dividing the output into two sections. The inverter creates voltages between $+V_{dc}$ and $-V_{dc}$ with topology linkages shown in Fig. 20. The number of levels is given in Eq. (2).

$$N_L = 3^{n-1} + 2,\ n = 1, 2, 3, \ldots. \tag{2}$$

Before implementing designs, the three-phase operation faced a hurdle. The use of a cascaded transformer in low-frequency three-phase is the goal of this method. In addition, $+V_{dc}$, 0 and

Table 8
Challenges and current scenario of MLI system.

MLI type & suggested literature	MLI control scheme	Controller used to control MLI	Power electronic switches used in MLI design	Quantitative details		
				N_l	f_{SW} (Hz)	f_0 (Hz)
Mokhberdoran and Ajami (2014)	Fundamental frequency switching PWM	dsPIC30f4011	BUP403 IGBT	9/25/31/49	–	50
Gupta and Jain (2014b)	Multi-carrier PWM	dSpace DS1103	IRF460 MOSFET	5	1k	50
Odeh et al. (2016)	Single carrier fundamental frequency switching PWM	–	IXYS FII40-06D IGBT	9/17	–	50
Samadaei et al. (2016)	SHE-PWM	ATMEGA16	12N60A4D IGBT	13	–	50
Aly et al. (2017)	Thermal stress relief PWM	DSP TMS320F28335	IGBTs	5	5k	50
Samadaei et al. (2018)	NLC	ATMEGA16	12N60A4D IGBT	33/289	–	50
Lee et al. (2018)	SHE & SPWM	Real time software & NI data acquisition	SiC MOSFETs	7/13	–	50
Mohamed Ali and Krishnasamy (2019)	Parabolic SPWM	dSpace DS1104	SKM75GB063D IGBT	9	2.5k	50
Vahedi et al. (2015)	Self-voltage balancing PWM	dSpace DS1103	SCT2080KE MOSFET	5	2k	50
Vahedi et al. (2018)	Self-voltage balancing PWM	dSpace DS1103	FGH30N60LSD IGBT	7	2k	50
Khazraei et al. (2012)	PS-PWM	DSP TMS320F28335	–	7	4k	50
Wang et al. (2014)	Modified PS-PWM	–	–	5	2k	50
Amini et al. (2017)	Knapsack PWM	dsPIC30F4011	IRF740 MOSFET	13	3k	50
Farivar et al. (2016)	SPWM	dSpace DS1006	PP75B060 IGBT	7	800	50
Viju Nair et al. (2017)	SVPWM	DSP TMS320F28335 & fpga	IGBTs	9	2k	50
Rahman et al. (2019)	PS-PWM	FPGA Virtex 5	–	7	1k	50
Zhang et al. (2018a)	SPWM	–	IGBTs	5	20k	50
Sun et al. (2015)	SPWM	DSP TMS320F28335	–	7	10k	50
Selvamuthukumaran et al. (2015)	Hybrid multicarrier PWM	Xilinx FPGA	PM50RSD120 IGBT	5	3k	50
Panda et al. (2018)	Logical switching state selection PWM	Arduino Mega 2560	12N60A4D IGBT	7	5k	50
Kartick et al. (2016)	PS-PWM	dSpace DS1104	K75T60 IGBT	9	3k	50
Farivar et al. (2016)	SPWM	dSpace DS1006	PP75B060 IGBT	7	800	50
Fuentes et al. (2017)	PS-PWM	dSpace DS1103	FSBB30CH60 IGBT	7	4.1k	50
Manoharan et al. (2017)	Hybrid PWM	DSP TMS320F28335	IRFP4868, IRFP4568 MOSFET	27	10k	60
Hammami and Grandi (2017)	SPWM	DSP TMS320F28377	IPMPS22A76 IGBT module	5	25k	50
Kumar and Verma (2018)	PS-PWM	dSpace DS1104	SKM50GB063D IGBT	7	2k	50
Vahedi et al. (2018)	Self-voltage balancing PWM	dSpace DS1103	FGH30N60LSD IGBT	7	2k	50
Ma et al. (2013)	POD-PWM	–	5SDF10H4503 IGCT	5	800	50
Carnielutti et al. (2017)	Modified PS-PWM	DSP TMS320F28335 & FPGA	IGBTs	7	2k	50

(*continued on next page*)

Table 8 (*continued*).

MLI type & suggested literature	MLI control scheme	Controller used to control MLI	Power electronic switches used in MLI design	Quantitative details		
				N_l	f_{SW} (Hz)	f_0 (Hz)
Sharma and Das (2019)	PS-PWM	DSP TMS320F28335	IGBT modules	7	5k	50
Young et al. (2013)	Harmonic reducing algorithm	HT463R24	MOSFETs	7	–	50
Kandasamy et al. (2015)	Multi-dimensional PWM	dSpace DS1104	IGBTs	5	1k	50
Wang et al. (2016)	PS-PWM	–	–	11	1k	50
Gholizad and Farsadi (2016)	Staircase PWM	Arduino	IRFP540N MOSFET	11	–	50
Ge et al. (2018)	PS-PWM	DSP TMS320F28335	–	7	10k	50
Busquets-Monge et al. (2020)	Virtual vector PWM	dSpace DS1006	FDPF3860T MOSFET	7	10k	50
Selvamuthukumaran et al. (2015)	Hybrid multicarrier PWM	Xilinx FPGA	PM50RSD120 IGBT	5	3k	50
Van et al. (2014)	Zero CMV PWM	DSP TMS320F28335	FGL-60N100-BNTD	5	2.1k	50
Nguyen et al. (2016)	Zero CMV PWM	DSP TMS320F28335	FGL-60N100-BNTD IGBT	5	2k	50
Sonti et al. (2017)	Modified reference PWM	DSP TMS320F28335	–	5	10k	50

Table 9
Switching methods and application requirements of T-MLI.

Topology	THD <5%	Switching frequency methods		Load			Applications					
		High	Fundamental	R	RL	Motor	Motor	PV	STATCOM	Active filters	Electric vehicle	Metro locations
CT	✓	✓	✓	✓	–	✓	✓	–	–	–	–	–
TCT	✓	✓	✓	✓	✓	–	✓	✓	–	–	–	–
PWMCT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–
HFL	✓	✓	–	–	✓	✓	✓	✓	–	–	✓	–
SICT	–	✓	–	–	✓	–	–	–	–	–	–	–
ZCT	–	✓	–	–	✓	–	–	–	–	–	–	–
ZZTT	–	–	✓	–	–	–	–	–	–	–	–	–
DST	–	✓	✓	–	✓	–	–	–	–	–	–	–
TCAC	–	–	✓	–	–	–	–	–	–	–	–	–
RC	–	✓	–	–	✓	–	–	–	–	–	–	–
CTRS	–	–	–	–	✓	–	–	–	–	–	–	–
BSCT	–	–	✓	–		–	–	–	–	–	–	–
ERSCT	–	–	–	–	✓	–	–	✓	–	–	–	–
SAM	✓	✓	–	–	✓	–	–	–	–	–	–	–
COHB	✓	✓	–	–	✓	–	–	–	–	–	–	–
FCCT	–	–	✓	–	–	–	–	✓	–	–	–	–

$-V_{dc}$ output voltages will be given. Using k transformers, Fig. 21 represents the architecture with H-bridges (Venkataramanaiah et al., 2017; Suresh and Panda, 2010, 2016). By connecting the secondary windings of transformers in series, third harmonics are produced. The voltage is changed as needed for the application by modifying the turn ratio. The characteristics of the single source transformer-based MLI topologies are given in Table 11.

This method is based on the usage of a buck converter to generate several voltage sources. The diagram of this approach is shown in Fig. 22 (Sajith and Sunitha, 2014). The main winding, tertiary winding, and secondary winding are all part of the buck converter seen above. The buck converter is a transformer that is isolated from the rest of the system. It solves the problem of magnet saturation by connecting the tertiary and main windings. The circuits for rectifying and filtering are linked in Fig. 22 to provide an isolating DC output, which is delivered to the H-bridge to create a 15-level staircase. The disadvantages of this architecture include the fact that it is incompatible with high-power applications. Furthermore, because a separate circuit is required to stabilize the output, the entire system is extremely complex and expensive.

This method was first utilized with FCMLI in McGrath and Holmes (2009). The system's architecture is complicated, yet it lowers the condenser voltage. To solve this problem, a new topology featuring FCMLI, CHBMLI, and bidirectional switches was created. Fig. 23 (Suresh and Panda, 2016) represents the

Table 10
Brief particulars of various state-of-the-art MLI topologies and the proposed topology.

	Banaei et al. (2012)	Farakhor et al. (2015)	Khounjahan et al. (2015)	Gandomi et al. (2015)	TBCHBT	Behara et al. (2016)	Behara et al. (2018b)	Behara et al. (2018a)
N_{SW}	N_L+1	$6\frac{\ln(N_L)}{\ln(5)}$	N_L+1	$2\frac{\ln(N_L+1)}{\ln(2)}$	$4\frac{\ln(N_L)}{\ln(3)}$	N_L+1	$4\frac{\ln(N_L)}{\ln(3)}$	$4\frac{\ln(N_L)}{\ln(3)}$
N_{gd}	N_L+1	$4\frac{\ln(N_L)}{\ln(5)}$	$\frac{N_L+1}{3}$	$2\frac{\ln(N_L+1)}{\ln(2)}$	$4\frac{\ln(N_L)}{\ln(3)}$	N_L+1	$3\frac{\ln(N_L)}{\ln(3)}$	$4\frac{\ln(N_L)}{\ln(3)}$
N_{tr}	$\frac{N_L+1}{2}$	$2\frac{\ln(N_L)}{\ln(5)}$	$\frac{N_L-1}{2}$	$2\frac{\ln(N_L+1)}{\ln(2)}-2$	$\frac{\ln(N_L)}{\ln(3)}$	$\frac{N_L-1}{2}$	$\frac{\ln(N_L)}{\ln(3)}-1$	$\frac{\ln(N_L)}{\ln(3)}-1$
N_{dc}	1	1	1	1	1	1	2	1
N_{cap}	0	2	2	0	0	0	0	0
$V_{in,dc}$	V_{dc}	$2V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}, V_{dc}	V_{dc}
V_{cap}	–	V_{dc}	V_{dc}	–	–	–	–	–
TBV	$(N_L+1)\ V_{dc}$	$6\frac{\ln(N_L)}{\ln(5)}V_{dc}$	$\left(\frac{N_L}{2}+3\right)V_{dc}$	$2\frac{\ln(N_L+1)}{\ln(2)}V_{dc}$	$4\frac{\ln(N_L)}{\ln(3)}V_{dc}$	$(N_L+1)\ V_{dc}$	$6\frac{\ln(N_L)}{\ln(3)}$	$4\frac{\ln(N_L)}{\ln(3)}$
V_{0p}	$\frac{(N_L-1)V_{dc}}{2}$	$\frac{(N_L-1)V_{dc}}{2}$	$\frac{N_L-1}{2}$ $\frac{(N_L-1)V_{dc}}{2}$	$\frac{(N_L-1)V_{dc}}{2}$	$\frac{(N_L-1)V_{dc}}{2}$	$\frac{(N_L-1)V_{dc}}{4}$	$\frac{(N_L-1)V_{dc}}{2}$	$\frac{(N_L-1)V_{dc}}{2}$
Type	Symmetric	Finary	Symmetric	Binary	Ternary	Symmetric	Ternary	Ternary
Turns ratio	(1,1….)	(1, 1.5, 5, 25, 25…)	(1, 1,…)	(2, 4, 8…)	(1,3,9,27..)	(1,1…)	(3,9,27..)	(3,9,27..)

architecture of this strategy. The architecture exhibited works in an asymmetrical style. One of the advantages of this method is that it can be implemented in one or three steps. Another concern is that as levels get increased, the number of cascaded transformers gets increases.

As previously stated, the shoot-through (Shen et al., 2007) looks to be a source of the problematic condition. But it all comes down to how it can convert it into an advantage and use it. To increase the input voltage, the Shoot through Condition is used. The modulation index must traditionally be changed to raise voltage (Banaei et al., 2013). The model index and turns ratio, however, remain unchanged as a result of this method. As a result, the output's THD will remain constant. The H-bridge cascading input receives the Z-impedance network output voltage. The combined secondary voltages of the cascaded transformers depicted in Fig. 24 are equal to the staircase output voltage, Vo. The advantages and disadvantages of the various other hybrid topologies are given in Table 12.

The authors of Pereda and Dixon (2012), suggested that the EV application should have a single, high frequency (HFL) connection and this work pioneered the use of a low power transformer with modulation adjustment. The recommended switching method reduces the HFL's size from 20% to less than 2% of the machine's total power. Although some H-bridges do not transfer any power to the load in their current state, the remaining inverters still have operational filters. The architecture employs a high-frequency H-bridge, toroidal transformer, and a variable DC, MOSFET, or IGBT-based correcting device (Pereda and Dixon, 2011). The isolated DC sources are generated by HFL using the single DC source as a source. As previously stated, MLI necessitates the use of several DC sources to increase the quality of the electricity. This is a problem that must be solved as a challenge. Different modulation approaches are used to overcome this challenge in Shen et al. (2007).

The high-frequency H-bridge generates a square wave voltage of 10–20 kHz, which is transmitted to a toroidal transformer with various turnings. A rectifier and DC connection condenser are used to rectify and filter an isolated winding output. The cascaded HB is coupled with the DC link condenser to synthesize a multilayer waveform. As shown in Rotella et al. (2009), Fig. 25 represents a 27-level MLI with H-bridge. Because of some of the current limitations, such as considerable shift losses, poor efficiency, and expensive overall hardware, this concept is in the works and will require significant improvements.

A novel architecture (Banaei et al., 2012) described the cascaded reduced inverter switch (CTRSI). For single DC sources with single-phase transformers, this typology worked well. Every transformer generates two three-level semiconductor switches. In this regard. For all transformers, two switches can be utilized to change the direction of the separate DC source. In Kang et al. (2005), Four switches, on the other hand, are used. The findings show that with the proposed inverter design, high-quality output voltages can be attained with a small number of semiconductor switches. The main disadvantage of this method is that it uses switches with higher current levels than the PWM multilevel converters previously discussed (Kang et al., 2005).

A novel three-phase multilevel inverter with a single DC supply was proposed in Tsang and Chan (2014). This incorporates a cascaded H-bridges with a standard two-level inverter. With a small number of switching components, the suggested arrangement generates multilayer output voltage. A 19-level three-phase inverter was used to test the proposed version. The author used four H-bridges and one normal inverter to test the 19-level inverter. The author only used genuine sources in this example, while the rest were replaced with capacitors. This technique is similar to that of Sepahv et al. (2013), but the design is significantly different from that of Banaei et al. (2012). It is recommended that the design supplied be verified in a novel approach. The author observed that just 22 power switches were used to generate 19 three-phase waveform levels after comparing the proposed design to earlier topologies.

The authors presented a three-phase multi-level inverter with a single DC supply in Araujo-Vargas et al. (2014). The architecture offered is, in fact, rather new. The proposed variant is well suited to medium-power applications. With single insulated Dc sources, the author employed a 3-phase cascade H-bridge transformer. According to the author, the proposed design can also be run if the H-bridge cascade is replaced with a neutral point clamped circuit. As a result, we can choose a three-phase inverter that suits our requirements. Later, like an inverter, a single 16-bit microcontroller switching mechanism was introduced. The seven-level inverter's design was validated by the author. Furthermore, when

Table 11
Features of various topologies of T-MLI.

Topology	Advantages	Disadvantages
CT (Bircenas et al., 2002; Salem et al., 2015)	• When compared to typical topologies, it reduces DC sources. • Modular structure.	• There are fewer output voltage levels to choose from. • Several transformers were required to enhance the number of levels in the output voltage.
PWMCT (Kang et al., 2004, 2005; Soon, 2009)	• The setup does not necessitate the use of passive components. • Because a cascaded transformer improves low voltage, it is simple to incorporate with AC power. • Because the cascaded transformer's leakage reactance creates filter operation, the output voltage's harmonic content is minimized. • Switches in semiconductors have less dv/dt stress. • The power exerted on the transformer can able to lower by changing the PWM, which reduces the transformer's size.	• To maximize the number of levels, several cascaded transformers are required, which increases the cost, losses, installation area, and reliability. • When functioning in three steps, the system becomes cumbersome. • Unlike traditional switching systems, the switching and control algorithm is sophisticated. • Due to the variable power distribution, this design does not fully utilize the transformers. • Because it uses high-frequency PWM, the efficiency of a PWM inverter is lowered. • There will be a need for a range of transformers with different turn ratios.
TCT (Song et al., 2009; Suresh et al., 2010; Panda and Suresh, 2012)	• Because of the high-quality output voltage and input current, low switching losses are accomplished. • It has a low-frequency transformer and is modular in design. • The output voltage is devoid of third harmonics. • Without the usage of additional components, galvanic isolation is present.	• A three-phase transformer has a larger size than a single-phase transformer. • Series coupled H-bridges and transformers are used to generate high-quality voltage, which increases the cost and installation area.
FCCT (Sajith and Sunitha, 2014)	• It is used to cut down on the amount of DC sources. • This design was tested at a low power of around 200 W.	• To improve the power quality, a greater number of components are necessary. • Many passive components make up the forward converter. • Multilevel operation necessitates the use of a specific transformer. • Only used in low-power applications
SICT (Suresh and Panda, 2016)	• For high-voltage applications, SMC is used (above 5 kV). • For output voltage levels and apparent frequency, SMI provides significantly better dynamic performance. • It minimizes semiconductor losses while also lowering the amount of energy retained. • It has a modular design that makes use of fewer semiconductor chips. • The switching frequency is extremely low, which results in increased efficiency.	• The SMC's general structure is complicated, and it includes capacitors, resulting in a voltage imbalance problem. • Due to the enormous number of single-phase cascaded transformers, the system becomes too bulky to produce high-quality output voltage in a three-phase operation.
HFL (Pereda and Dixon, 2012, 2011)	• The HB-based AMI employs just one DC source instead of many. • The operation of the transformer allows for automatic voltage balance throughout HB. • The total harmonic distortion (THD) is exceedingly low and practically constant over the whole working range. • It is possible to think of topology as a regenerating process. • A toroidal transformer makes up the HFL. This topology can be employed for high-power applications because its weight and power rating are lower than those of other types of power transformers.	• Due to additional DC-link diodes, rectifiers, and variable DC supply, the circuit complexity grows as the number of levels in the output voltage increases. • The capacitor's quick dynamic activity is limited due to its participation.
ZCT (Banaei and Dehghanzadeh, 2012; Banaei et al., 2013)	• It operates on a shoot-through basis, making it more dependable.	• Capacitors and inductors were employed as extra components. • To reduce THD, additional transformers are necessary.

compared to other procedures, verifications indicate that efficiency is slightly lower. The construction pattern, on the other hand, is rather straightforward, which makes the design the ideal option when additional control loops are avoided.

3.2. 3-L inverter-based topologies

Their modular construction makes the system simple to operate and are frequently employed. The respective merits and demerits of the 3 level topologies are given in Table 13. Inverters are divided into four categories, each of which is detailed below:

3.2.1. Delta-star connected transformer (DST) based inverter

This method necessitates converters with a $\sqrt{3}$:1 turnover ratio linked to the star (Mueller and Park, 1994). On contemporary topologies, DST-based inverters have greatly improved. The top 3L is directed to the positive source terminals, while the bottom 3L is directed to the negative source terminals represented in Fig. 26. For voltage balancing, no capacitors are necessary. With just one delta star coupled transformer, inverters based on the DST topology can create seven levels of output, which is its greatness. However, even though this has downsides, the

Table 12
Features of miscellaneous topologies.

Topology	Advantages	Disadvantages
CTRS (Babaei et al., 2012) BSCT (Patra et al., 2018)	• A cascaded H-bridge multilevel inverter uses more switching components than the published scheme. • In comparison to the topologies presented. • This topology requires fewer components.	• Transformer saturation can occur if proper switching is not given. • Bidirectional switches and two more capacitors are used in the suggested topology.
ERSCT (Gupta and Jain, 2012a)	• In comparison to the topologies presented in Babaei et al. (2012), • There are fewer transformers and switches.	• It is not built in a modular fashion. • Except for a few topologies, additional components were used. • The system becomes cumbersome when generating a large number of levels.
SAM (Alishah et al., 2014)	• The PIV of semiconductor switches has been reduced. • Power losses and on-state drop across switches are decreased since there are fewer devices in the current route. • Both symmetric and asymmetric operating modes are efficient. • It has a modular design to it. • THD is lower in an asymmetric mode.	• In total, two capacitors are required. • Each module necessitates bidirectional switches. • Because each module requires two single-phase cascaded transformers, the system is complicated.
COHB (Mokhberdoran and Ajami, 2014)	• The number of levels is enhanced using turns-ratio algorithms, resulting in less THD as compared to the binary strategy method. • Modular structure.	• On two switches per module, the peak inverse voltage (PIV) is increased. • To obtain a staircase waveform with lower THD, two cascaded transformers are required.

Table 13
3-Leg based topologies.

Topology	Merits	Limitations
ZZTT (Manjrekar et al., 2000)	• The output voltage is free of 24 1 harmonic components thanks to space vector modulation (SVM) and a unique transformer connection. The harmonic order is denoted by the letter h.	• This layout involves the use of a custom-built transformer with two secondary windings, resulting in a complicated, expensive, and heavy overall system. • Only 13 levels are produced in the output voltage, compared to the earlier MLI, which used more components. • Due to a different type of transformer, the topology does not have a modular structure and is limited to four 3-L and transformers.
DST (Mueller and Park, 1994)	• Extra circuitry for the capacitor's voltage balancing approach is not required.	• To achieve a 7-level topology, high-capacity semiconductor devices and a transformer are required. • To reduce harmonics, the design only provides a 7-level load voltage. The system becomes more sophisticated as more L-C filters are added.
TCAC (Mueller and Gran, 1998)	• The arm-based architecture of the three-phase T-common SDCMI uses fewer switching elements, resulting in a smaller gate driver and total system size. • The number of pieces needed to defend against the current is cut in half. For a shared arm, only one current protection circuit is necessary.	• Because the common arm's current rating is five times that of the other arms, a different IPM and transformer rating is necessary. • The system is substantial due to the utilization of six three-phase transformers.
RS (Lai and Shyu, 2002)	• 3-L replaced an HB by incorporating a single-phase cascaded transformer. • The phase shift has been extended. With PWM, a single module may provide a 7-level staircase voltage, effectively removing low-frequency harmonics in the DC link current.	• Each module will require two cascaded single-phase transformers. • Its framework is not modular.

filter circuits can be removed and the SVM algorithm must be improved. Because of the high-frequency operation, efficiency suffers and variable losses increase resulting in higher output levels.

This strategy aims to decrease the component count while simultaneously increasing output (Mueller and Gran, 1998). This arrangement includes six 3-L modules with 36 switches and 18 IGBTs as well as five three-phase transformers. The 3-L can also be made with 18 H-bridge modules. This is not a flexible topology, and it is also quite expensive.

3.2.2. Reduced switch type (RS) MLI

The proposed architecture is shown in Fig. 27 (Lai and Shyu, 2002), which uses a cascaded transformer instead of H-bridges to construct 3L. This necessitates complex control strategies. The 5th level will be treated equally, whereas the 7th level will be treated

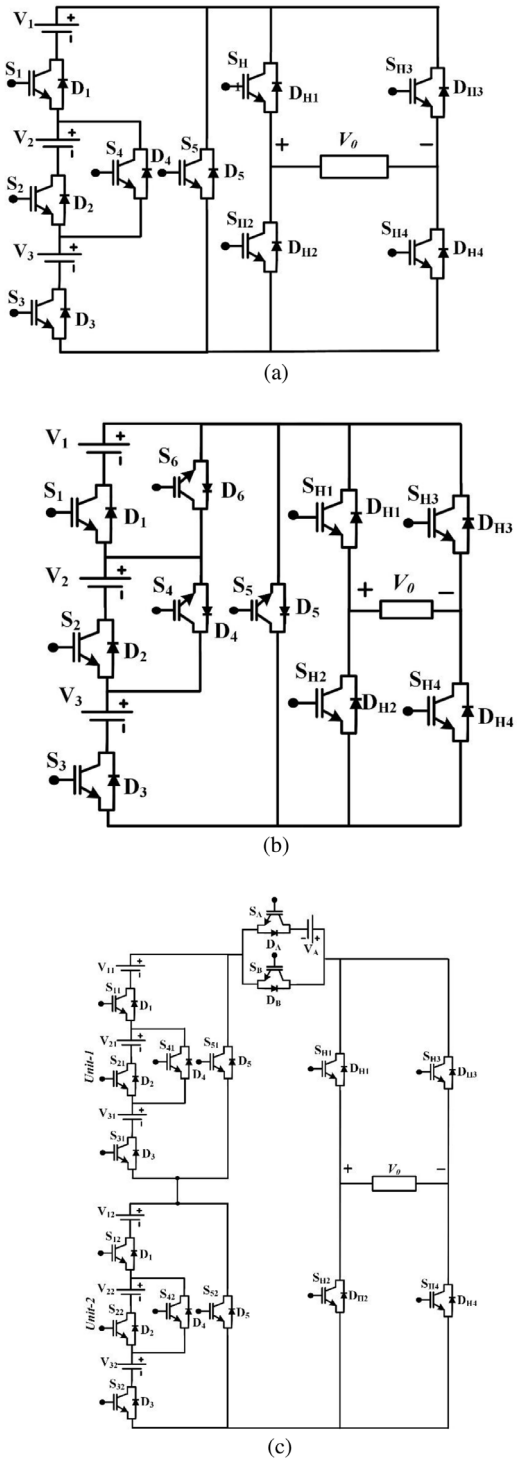

Fig. 9. MLI structures: (a) 5-level MLI (b) 7-level MLI (c) 15-level MLI (Dhanamjayulu et al., 2020b).

unequally. To generate extra levels, changes must be made to the inverter.

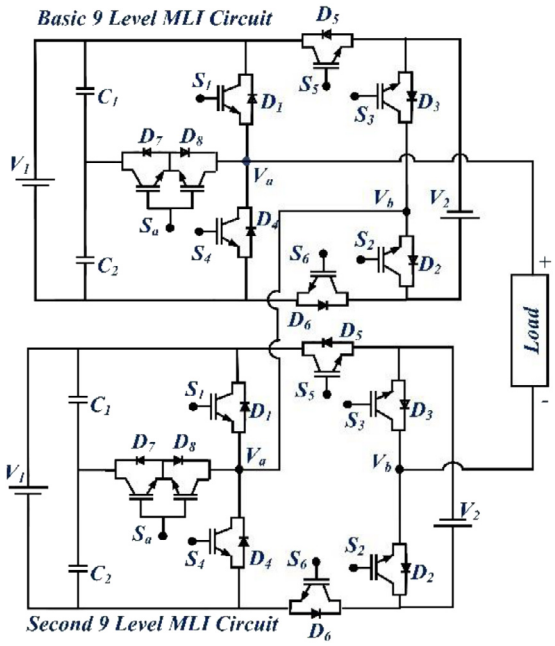

Fig. 10. 17-level cascaded H-bridge MLI (Dhanamjayulu et al., 2021b).

3.3. Hybrid topologies

3.3.1. Cascaded transformer-based reduced device count (CTRS) inverter

A series of transformers that transform and isolate voltage, switches, and a single DC voltage source is connected in series (Babaei and Hosseini, 2007) is used to achieve this technique shown in Fig. 28. While this architecture uses fewer switches than prior architectures and the rated power of the switches employed is higher than usual, a power loss occurs. Voltages between $+V_{dc}$ and $-V_{dc}$ could be used to generate it. The number of switches must be increased to increase the levels. Another drawback is a lack of suitable switching mechanisms.

3.3.2. MLI based on bi-directional switches with cascaded type transformer (BSCT)

Transformers, unipolar switches, and two-way switches, and two capacitors are used in this construction, as illustrated in Fig. 29 (Laali et al., 2010). This decreases the risk of loss, as well as the cost and size of the relocation. However, as in the past, the losses increase with the increase of layers count.

3.3.3. MLI based on reduced switch type cascaded transformer (RSCT)

The technique represented in Fig. 30 (Ounejjar et al., 2011) has the benefit of using fewer switches, condensers, and drivers which produces a 9-level output. As a result, there will be fewer losses to replace. Each of the four components contains four diodes and a switch.

To give a 5-stage output, 6 switches with 2 CTs are required (Zeng et al., 2010), which is a better solution than earlier (Lai and Peng, 1996). This architecture is a combined H-bridge (COHB) based T-SDCMI, necessitates the use of semi-director

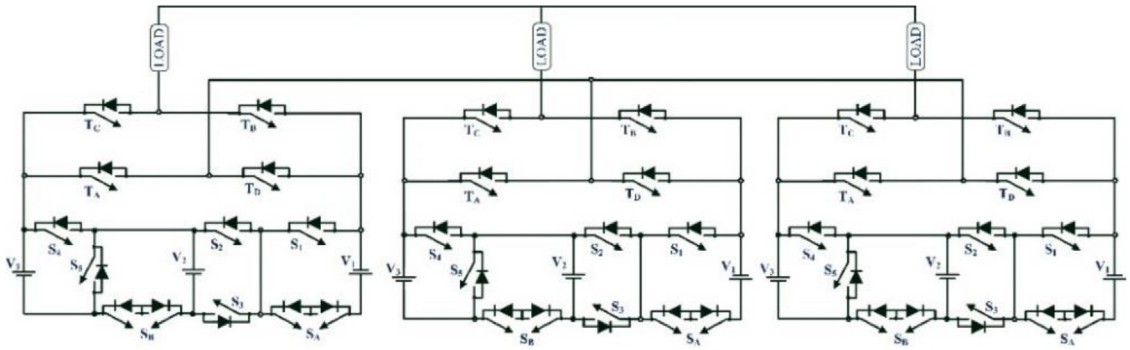

Fig. 11. Three-phase 19-level MLI (Dhanamjayulu et al., 2020a).

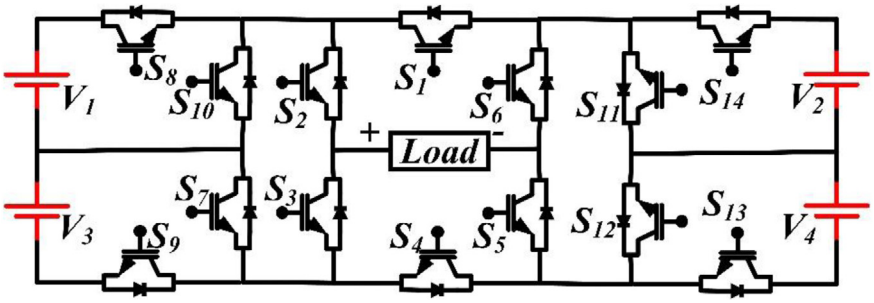

Fig. 12. 31-level MLI structure (Prasad et al., 2021).

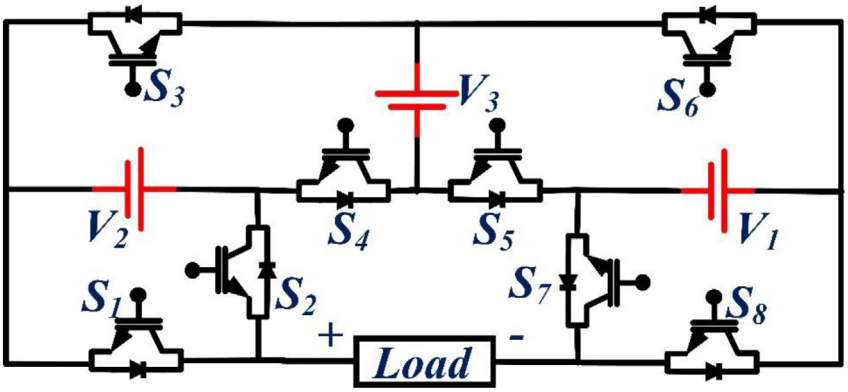

Fig. 13. 15-level MLI topology (Dhanamjayulu et al., 2021a).

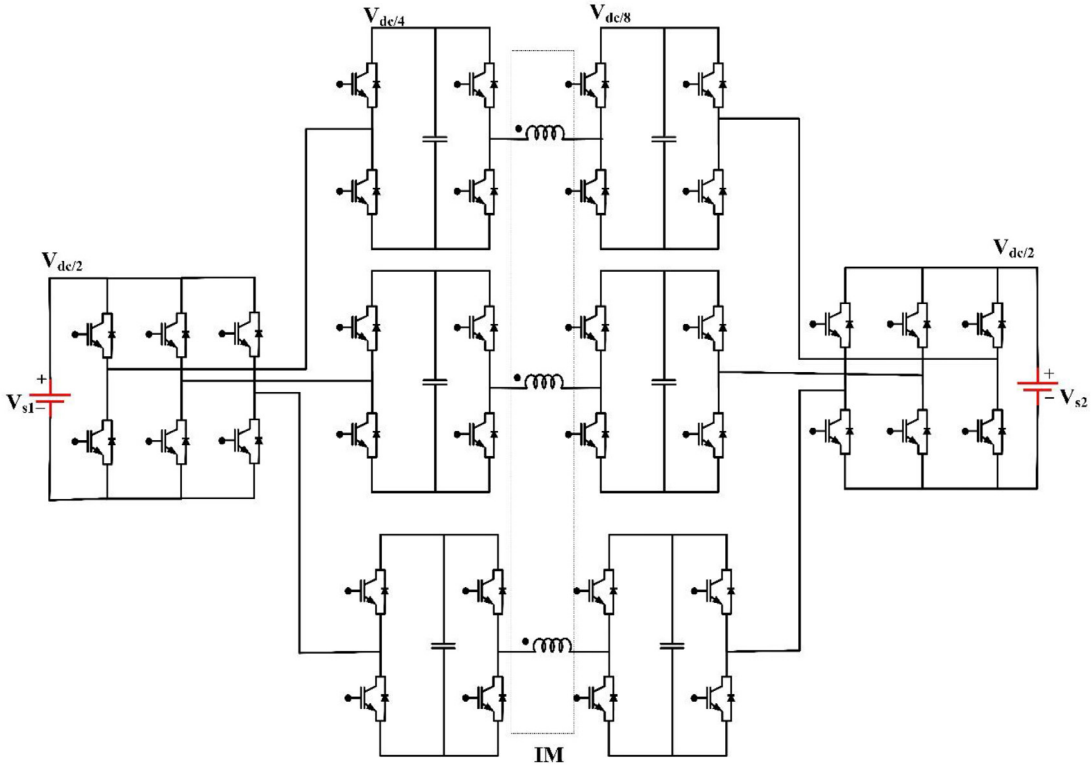

Fig. 14. Double side CHB connected hybrid 9-level MLI (Hinago and Koizumi, 2009).

switches with varying evaluations, which boosts costs, and raises the voltage stages by one module. The rotation ratio is chosen in a binary manner. Each switch has a different reverse peak tension. This is one of the most important issues in this type of architecture.

3.3.4. Transformer type MLI cascaded multi-source RES

As described, the multiple transformer topology is used in PV systems (Kouro et al., 2007), and the PV-based standalone micro inverter is presented in Babaei and Hosseini (2007). This is comparable to the classic cascaded H-bridge multilevel converter illustrated in Fig. 31 in terms of construction. When compared to the traditional cascading architecture, however, it is clear that it requires fewer DC sources. In practice, only one DC supply is required for a single-phase multiple transformer system. It is also essential to treble the number of DC sources and transformers for a three-phase grid-connected PV system (Kouro et al., 2010). Two further properties that have been confirmed are robustness and reliability. Some commercial inverters were based on this architecture because of these unique properties (Hannan et al., 2014). Three DC sources, on the other hand, are required for three-phase applications. The fluctuation of the electricity generated by each PV source is another cause of concern. The injected AC currents will be uneven if the PV sources produce unequal power.

To improve existing power conditioning systems, this study proposes a novel topology. The proposed topology for a grid-connected three-phase system is shown in Fig. 31. It just requires two PV sources and comprises two four-leg two-level VSIs, as can be seen. The inverters' AC terminals will be connected to two Scott transformers, which will have their secondary windings coupled in a series configuration. In contrast to the traditional multiple-transformer topology (Hannan et al., 2014). This technique reduces the number of switches from 24 to 16, as well as the number of PV sources from three to two. Furthermore, the unbalance of the injected three-phase currents into the grid (produced by unbalanced PV power output) will be reduced due to the usage of Scott transformers.

4. MLI: Cost assessment

It is worth noting that the overall cost of the MLI rises as the number of components increases. In many applications, the primary rationale for avoiding the use of a typical MLI architecture is its higher cost. As a result, it is necessary to compute the total cost while developing the unique RS MLI topologies. The number of semiconductor switches, drivers, diodes, and capacitors required determines the cost of an MLI. Furthermore, TSV and PIV should be given equal weight when determining the rating of these components, which contributes to the final cost. Table 14 shows the costs of a few insulated-gate bipolar transistors (IGBT) switches, diodes with a fixed current rating of 75 A for a wide range of voltage, isolated driver circuits, isolated dc sources with a 50 A rating, and capacitors with a fixed capacitance of 3.3 mF that can be used to design various RS MLI topologies. The component ratings given here are only examples of a sample cost analysis for

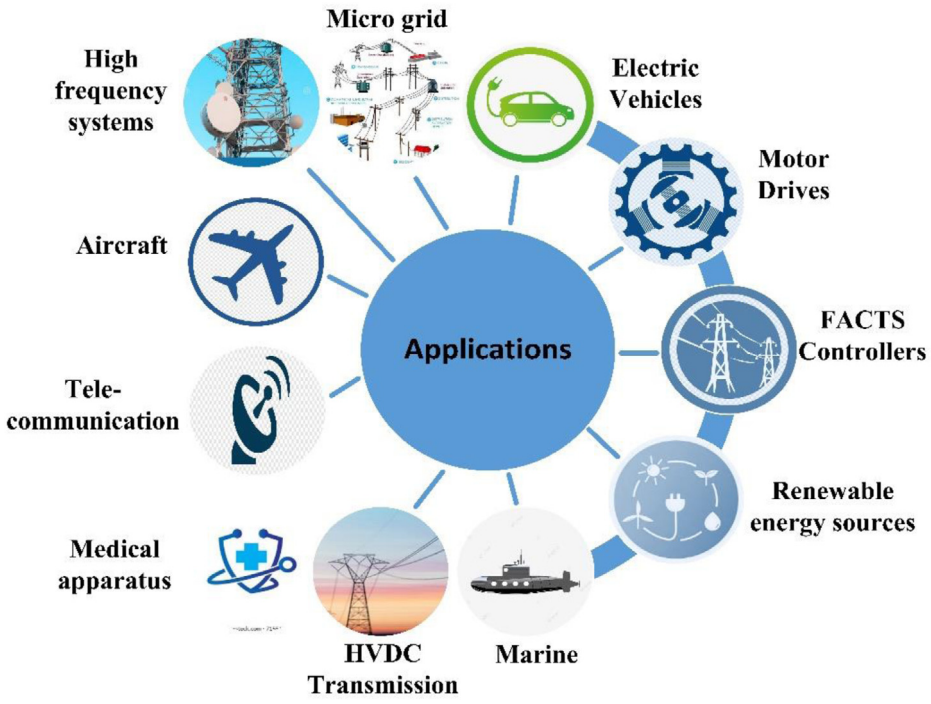

Fig. 15. Overview of the application of MICs based on the classification.

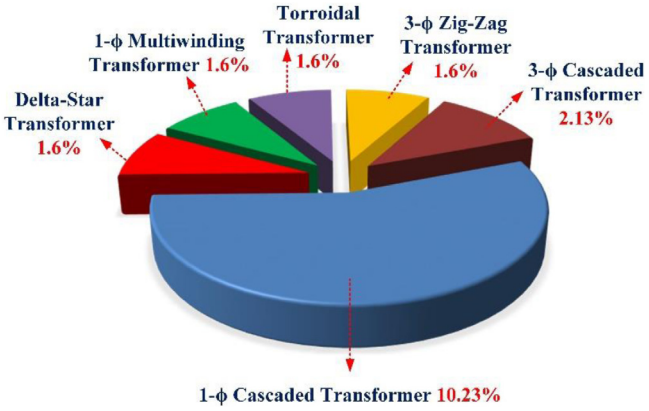

Fig. 16. Different types of transformers used in various topologies.

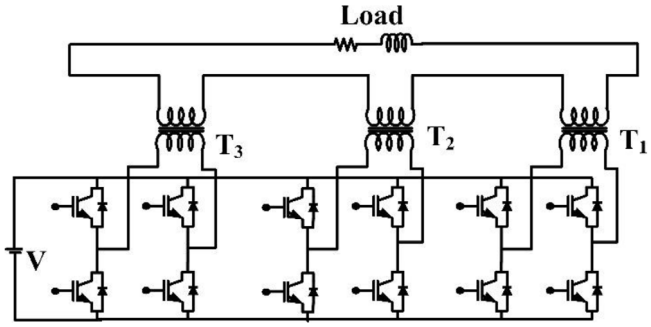

Fig. 17. Cascaded single phase transformer MLI configuration (Kang et al., 2005).

an MLI; the parameter/cost will vary depending on supply and market growth.

The performance of the various MLIs along with the cost function is discussed in Mueller and Gran (1998). Table 15 lists the specific tools and apparatus required for T-MLI implementation. The MLIs with single and multi-sources are discussed in Hannan et al. (2014) which has more device count implemented for PV applications.

Finally, the various parameters of the existing MLIs are presented and made a comprehensive structural review with a detailed comparison. This research helps young researchers to propose optimized structural and cost-effective MLIs for renewable energy applications. This can be also applicable to the grid-connected and FACTS devices for the improvement of power quality.

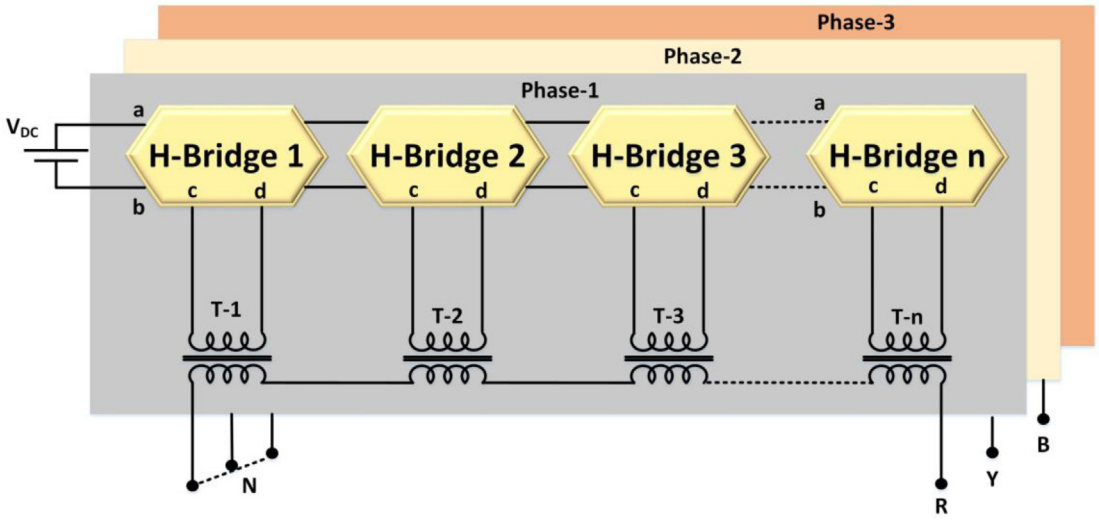

Fig. 18. CT based MLI (Kouro et al., 2010).

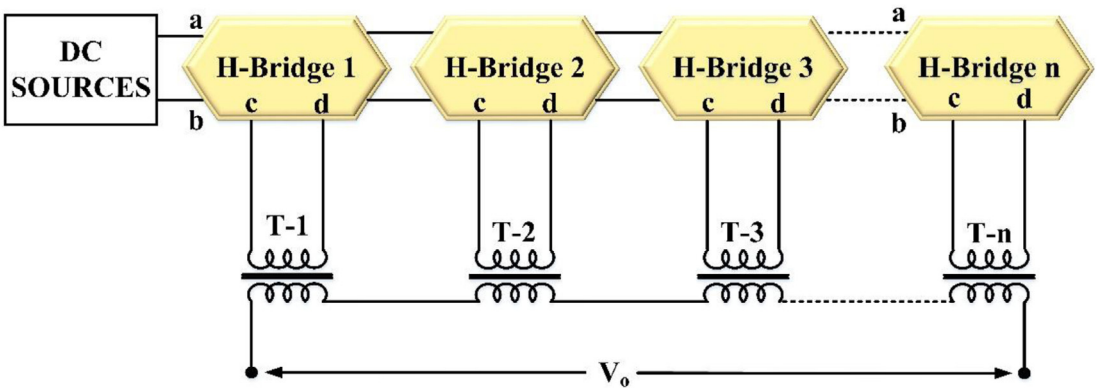

Fig. 19. Single-phase PWMCT based MLI (Carpita et al., 2008).

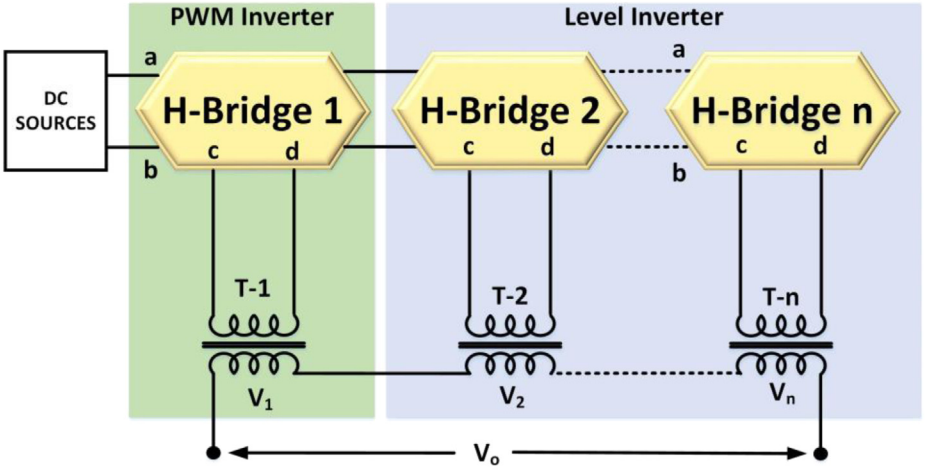

Fig. 20. M-PWMCT based MLI (Franquelo et al., 2008).

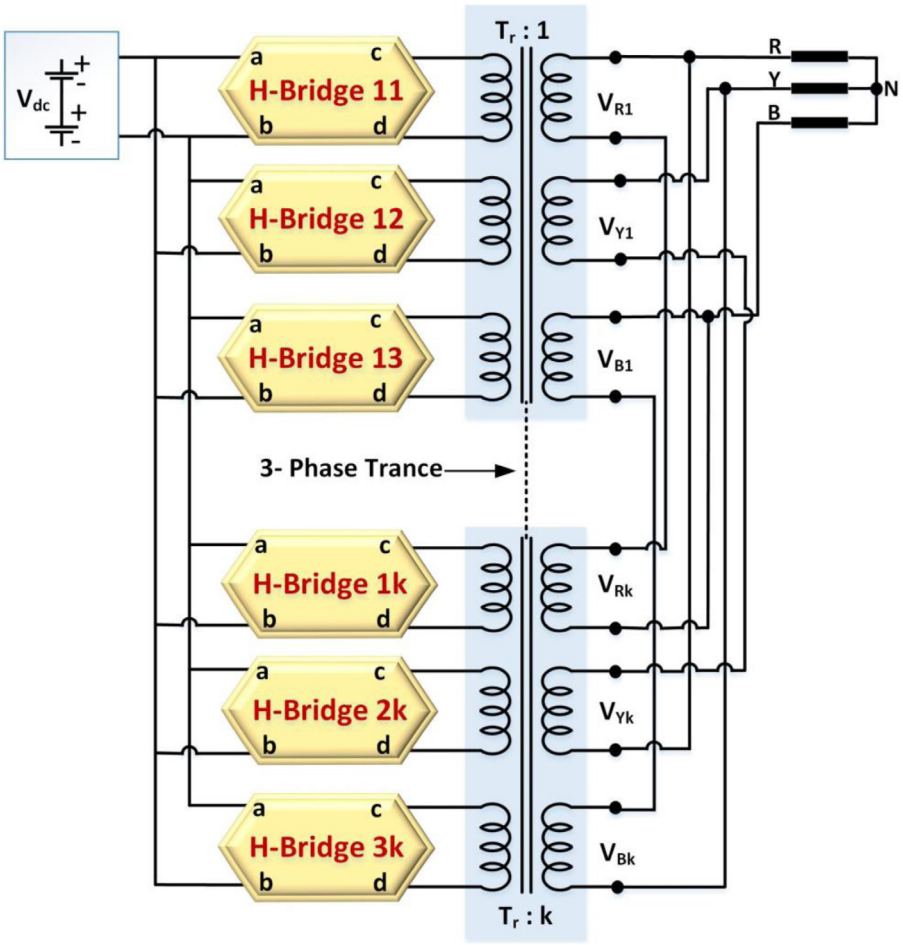

Fig. 21. TCT based MLI (Suresh et al., 2010).

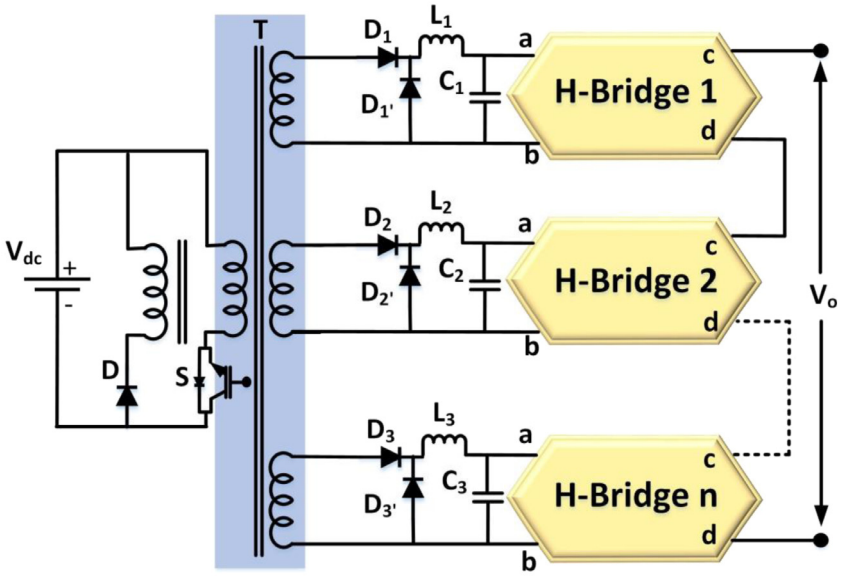

Fig. 22. FCCT based MLI (Sajith and Sunitha, 2014).

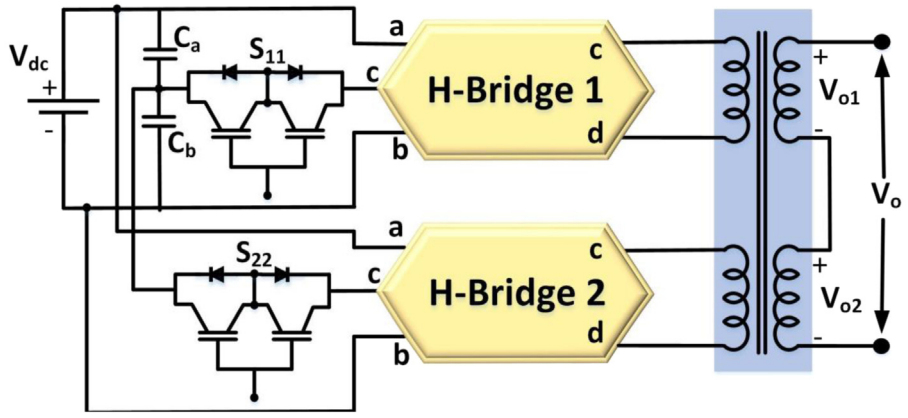

Fig. 23. SICT configuration (Suresh and Panda, 2016).

Table 14
Cost evaluation of MLI.

Component name	Component number	Voltage rating (V)	Unit price (USD)
IGBTs (75A)	IXGH60N30C3	300	3.89
	IXGH72N30B3	600	5.70
	IXGH50N90B2	900	5.96
	IXGH32N100A3	1000	6.87
	IXGH32N120A2	1200	8.12
	IXGH25N160	1600	10.418
	IXGH32N170	1700	16.78
	IXGH20N360	3600	35.49
Discrete diodes (75A)	APT60S20	200	5.91
	APT75DQ60	600	4.74
	APT75DQ100	1000	4.90
	APT75DQ120	1200	7.02
Driver circuits	TLP250	–	2.04
	TLP350	–	2.83
	HCPL-316J	–	6.17
	HCPL-3120	–	3.25
	HCNW-3120	–	5.06
	HCPL-3180	–	3.85
	IR2110	–	1.84
	MCT2E	–	0.37
	MOC3021	–	0.43
Isolated dc power supplies (50A)	TL250048 (2.5 kW)	48	1504.5
	N8759A(5 kW)	100	6821
	N6702C(1.2 kW)	150	4199
Capacitors (3.3 mF)	LLS2A332MELA	100	4.96
	LLG2D332MELC50	200	9.87
	LQR2V332MSEG	350	54.51
	LQR2G332MSEG	400	65.73
	LNX2H332MSEH	500	111.08
	LNX2J332MSEJ	630	216.07

5. Conclusion

This article focuses on the existing transformer-less and transformer-based MLI structures that fall into the categories of Symmetric, Asymmetric, Hybrid, and Single DC source-based structures, as well as their interesting features like power quality, cost, modularity, and other characteristics that result in a high-quality output waveform for medium to high-power applications with less THD. The merits, limitations and applications of conventional MLI topologies have been thoroughly investigated, as well as the applications of contemporary topologies. In this way, each topology and category of transformer and transformer-less

Table 15
Component details of the various topologies of T-MLI.

MLI Topology	Power electronic switches used in MLI design	Gate driver	Input DC/AC output voltage rating	Maximum power	Frequency (Hz)	Transformer		Processor
						Specification	Turns ratio	
CT PWMCT	FS100UMJ03 Power MOSFET	TLP250	57/12/110 PV array, 51/110	3 kVA 1 kW	60 60	1.3 kVA EI lamination	1:a, 1:3a, 1:9a a = 1.625	DSP Controller
TCT	FGH20N60UFD IGBT	–	60/220	–	50	EI lamination (3EA)	1:1	DSP Controller-F2812 and Xilink
STCT	FGH20N60UFD IGBT	HCPI-316J	120/230	–	50	2 kVA, EI lamination	1:1	
HFL	–	–	150	2 kW, 3 kW, 18 kW	50		9N:3N:N	ABB AC800PEC
ZCT	IRFP640 and MUR820G	TLP250	60/150	–	50		1:1	PCI-1716DAQ
ZZTT	–	–	300/326.5	6 kW		$N_p = 500$, $N_1 = 102$, $N_2 = 37$, $N_3 = 124$, $N_4 = 72$	481:278	16-bit dsPIC33FJ256MC710A DSP-2812
CTRS	IRF460 MOSFET	TLP521–1	12 V	–	50	–	1:1	ATMEGA 32-8PT
BSCT	IRFP250 MOSFET	TLP250/HC573	20 V	–	50	–	–	DSP TMS320F28335
SAM	H25R1202 IGBT	–	100/200 and 60/360	–	–	PC 40 ferrite core	100:100 100:500	–

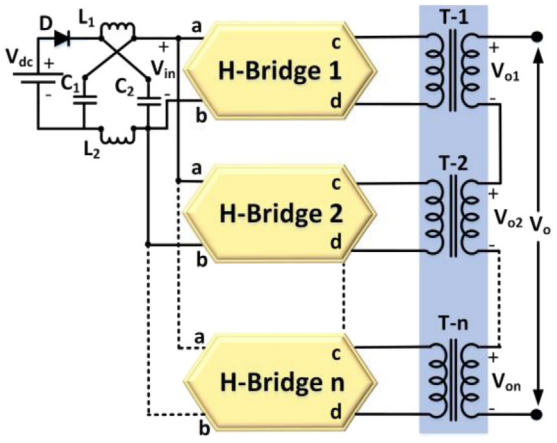

Fig. 24. ZCT based MLI (Shen et al., 2007).

MLI structures are thoroughly investigated along with the general advancements and issues in the field.

Several topologies have been evaluated in terms of the number of transformers, semiconductor devices, and output voltage levels using various performance metrics. In addition, the equipment required for all T-MLI implementations is explained in detail and in-depth. The existing topologies have several circuit components with multi-sources which increases the circuit complexity and the cost of the MLIs. In addition, procuring the different types of sources is difficult in real-time implementation. The existing MLIs have higher harmonics, high TSV, and power losses which increases the cost of the MLIs. Hence these are the drawbacks available in the literature and can be overcome by providing a solution in the future implementation of single DC source MLIs with optimal components for renewable energy applications. Furthermore, a summary of this paper aids researchers in determining a well-suited topology based on application-oriented requirements that can be incorporated in future works.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability statement

The findings of this review work no data associated with this article.

Acknowledgment

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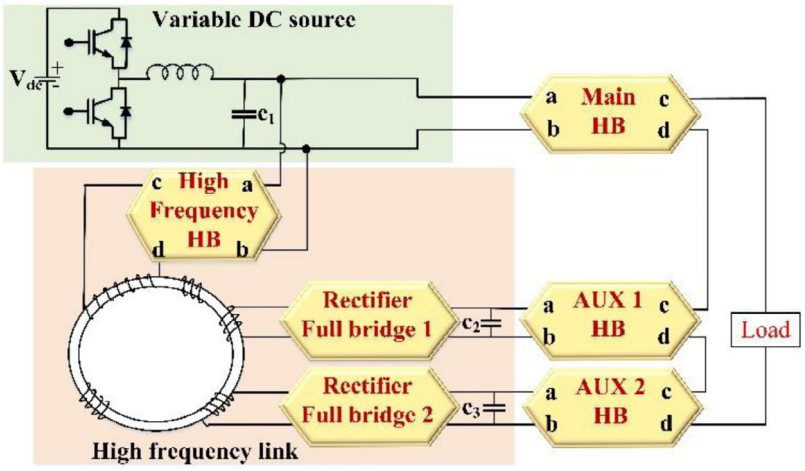

Fig. 25. HFL based MLI (Rotella et al., 2009).

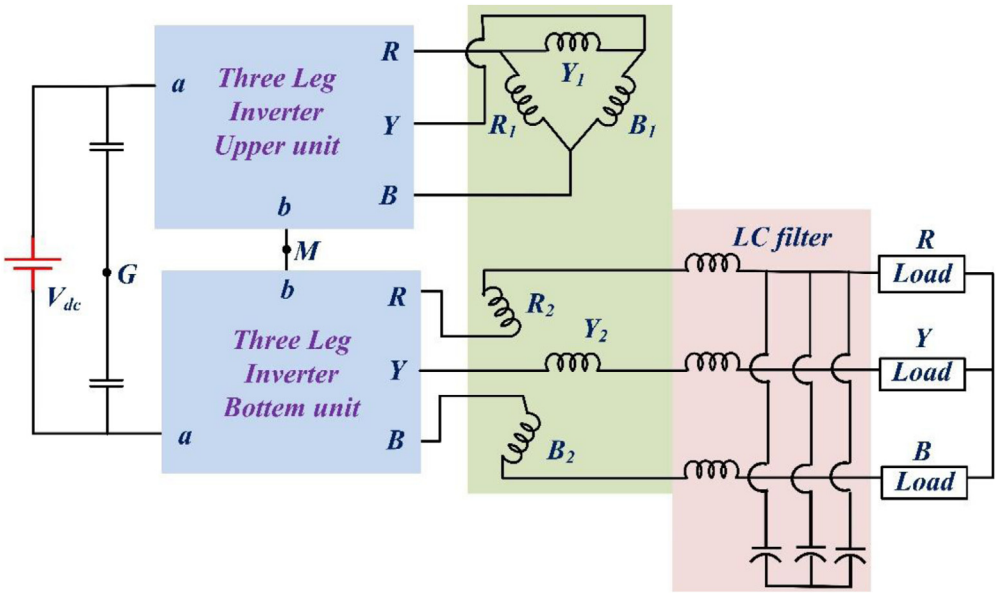

Fig. 26. DST based MLI (Mueller and Park, 1994).

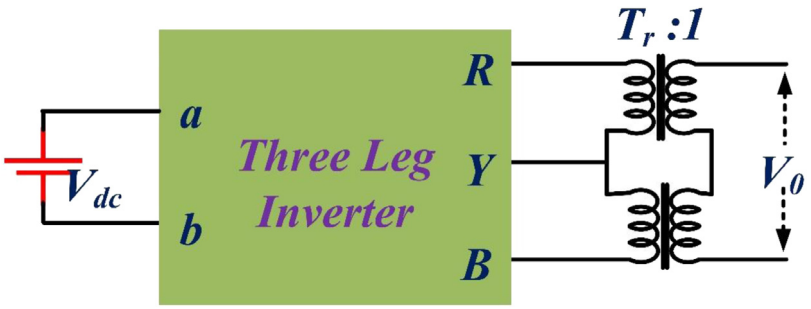

Fig. 27. RS based MLI (Lai and Shyu, 2002).

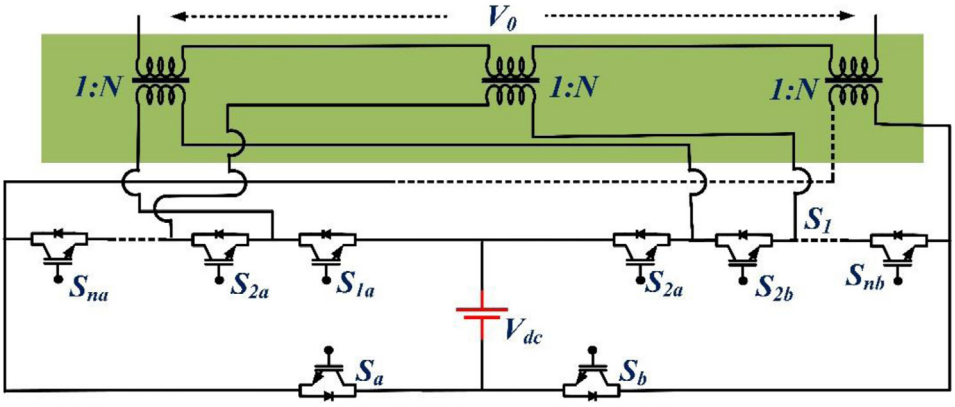

Fig. 28. CTRS based MLI (Babaei and Hosseini, 2007).

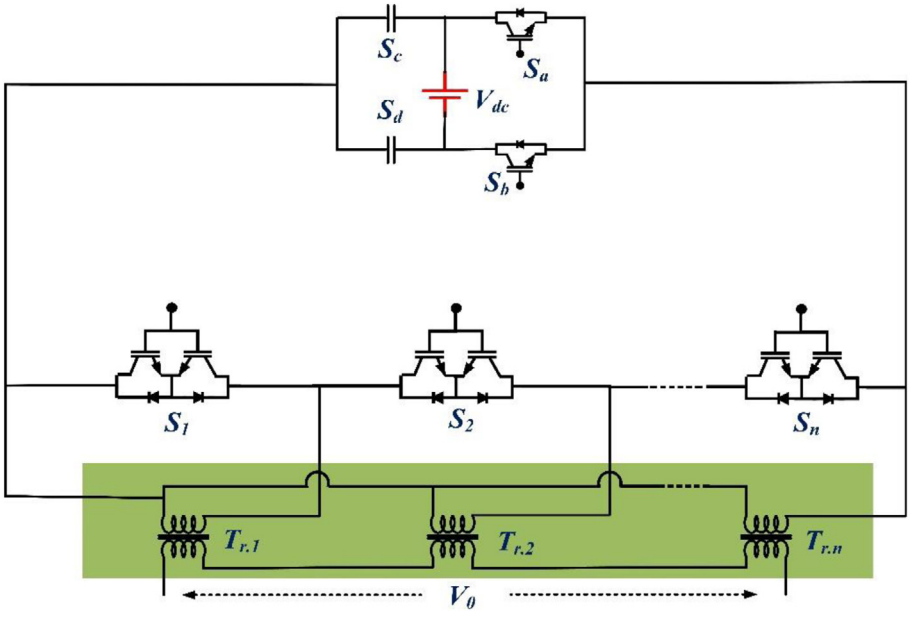

Fig. 29. Single-phase BSCT based MLI (Laali et al., 2010).

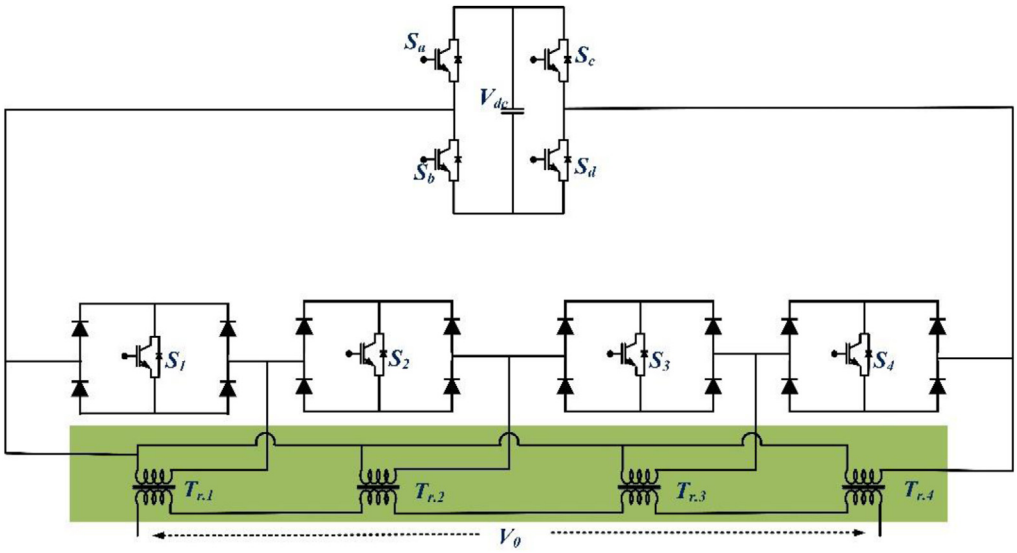

Fig. 30. ERSCT based MLI (Ounejjar et al., 2011).

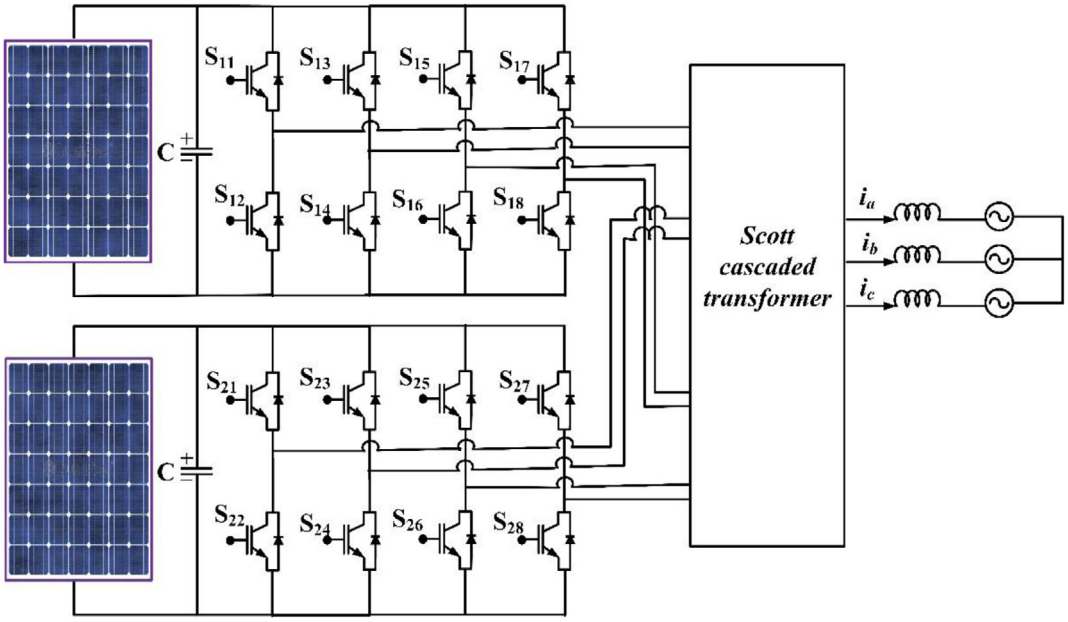

Fig. 31. Solar PV fed MLI configuration (Hannan et al., 2014).

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