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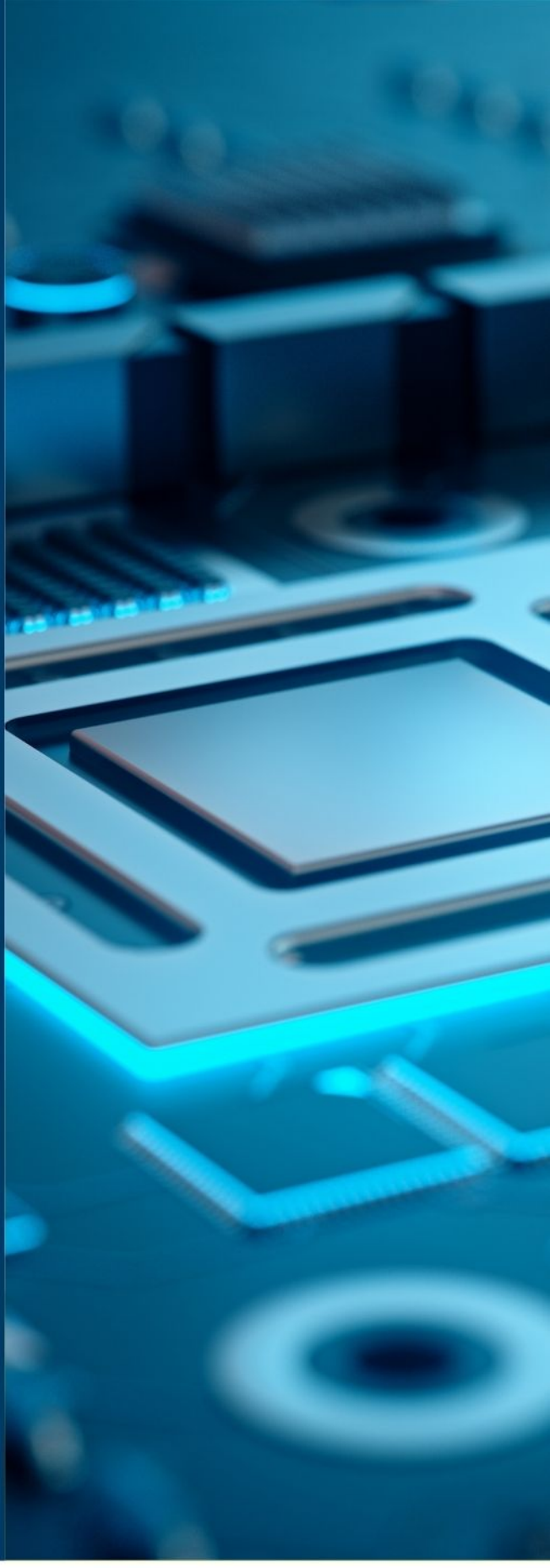

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RAPID COMMUNICATION

A non-isolated symmetrical design of voltage lift switched-inductor boost converter with higher gain and low voltage stress across switches

Md Samiullah[1] | **Marif Daula Siddique**[1] | **Atif Iqbal**[1] | **Pandav Kiran Maroti**[1] | **Subrata Banerjee**[2]

[1]Department of Electrical Engineering, Qatar University, Doha, Qatar

[2]Department of Electrical Engineering, NIT Durgapur, Durgapur, India

Correspondence
Atif Iqbal, Department of Electrical Engineering, Qatar University, Doha, Qatar.
Email: atif.iqbal@qu.edu.qa

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Abstract

The DC–DC converters have to be characterized by high gain, low voltage stress, small size, and high efficiency for most of the applications including fuel cell and photovoltaic integration to microgrid. However, conventional, quadratic, interleaved, three-level and cascaded boost converters are not able to satisfy the requirements. This letter proposes a new, non-isolated DC–DC converter with switched-capacitor and switched-inductors that can achieve high-gain, wide-ranging input-voltage, and low-voltage stress across the switches. This paper analyses the operating principle, the design of component parameters and comparisons with other high-gain converters. Experimental results for 22 V/400 V, 50 kHz prototype finally verifies the proposed converter with a voltage gain of 19.

1 | INTRODUCTION

High gain DC/DC converters are required for a variety of different applications, including the integration of distributed generation into microgrids, UPS battery backup, high intensity discharge lighting, electric traction, and some medical devices [1–5]. A high gain DC–DC converter is eventually required for grid interaction of renewable-based generating stations to high voltage DC buses as can be seen in Figure 1. However, using a high duty ratio to produce high voltage gain has a number of drawbacks, including higher switching and conduction losses, poor transient responsiveness, voltage spikes, and EMI [5–7]. Furthermore, it generates significant diode reverse recovery problems [8, 9]. Therefore, the potential problem is to create an efficient converter capable of producing higher output voltage while maintaining a low duty ratio. Improvements are also sought in terms of power supply rejection ratio, input voltage and current fluctuations, electromagnetic interference (EMI), and converter cost in various applications.

High-voltage gains may be accomplished in isolated transformer-based DC–DC converters such as phase shifted full-bridge (PSFB) converters, fly-back, and forward type converters by properly setting the turn ratio of the associated high-frequency transformer [2, 4, 9–11]. However, the presence of the transformer increases the size, weight, and volume of the converter. Non-isolated dc–dc converters have gained a lot of attention due to their reduced size, low losses, and lower cost [6, 12, 13]. The cascaded boost converter may deliver significant voltage gain at low duty ratios. However, as the number of stages rises, the control becomes complicated. To address the concern, quadratic boost converter is proposed which is easy to control but have higher voltage stress that is equal to output voltage which limits its application at certain voltage level only [11]. Coupled inductor based converters are also discussed to alleviate the voltage gain but they suffer with EMI issue, circulating current and sometimes resonance with the diodes parasitic elements which requires snubber circuits to damp down [7, 14, 15]. Moreover leakage current in these converters occurs like an isolated converters which requires clamping or recycling. With switched networks that include inductors and capacitors, increasing the voltage gain is quite easy. These devices may be effectively coupled in larger numbers to provide a noticeably

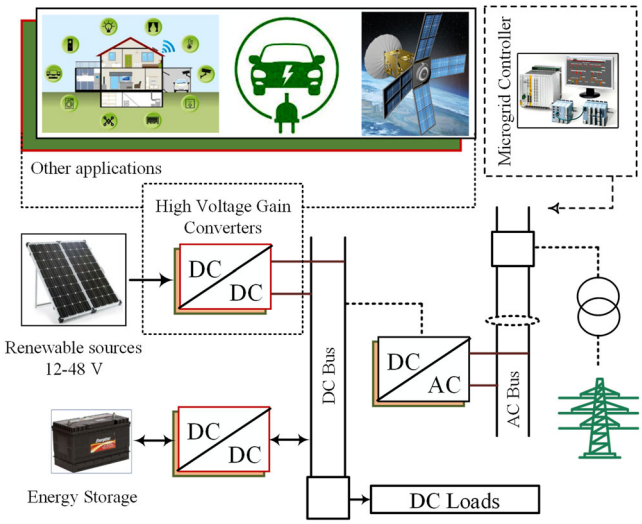


FIGURE 1 The DC microgrid: Brief layout

higher voltage [16–19]. Compared to switched inductor circuits, switched capacitor circuits are lighter and more resistant to EMI. However, the circuits adopting SC are more vulnerable to voltage imbalance and instability under varying loads. Higher voltages can also be obtained by combining multiplier cells at the cost of increased complexity size and control. A serious issue with these converters is the increased voltage stress across the switches, which limits their usage for very high voltage applications. The converters proposed in [20–22] use double duty ratios to control and regulate the output voltage for a wider range of operation but again their auxiliary switch and the output diode suffer with higher voltage stresses. This paper introduces a symmetrical voltage lift switched inductor converter (SVLSI) with the following key features:

- Capable of providing higher gains at low duty ratios with the switches having low voltage stress across them.
- Having continuous input current and output current.
- Lower PIV at the output diode.
- Suitable for various applications, such as PV and fuel cell integration to a DC microgrid.
- Transformer/coupled inductor free design and simple control.

2 | THE PROPOSED CONVERTER

2.1 | Description

The circuit assembly of the proposed high gain converter is shown in Figure 2. It consists of two switches, four inductors, five capacitors and seven diodes. The components L_1, L_2, C_1, D_1 and D_2 forms a voltage lift switched inductor (VLSI) section. A similar structure has been formed by L_3, L_4, C_2, D_3 and D_4. The two switches S_1 and S_2 are turned ON at same time and is termed as Mode I as shown in Figure 3. In Mode I, all four inductors and two capacitors

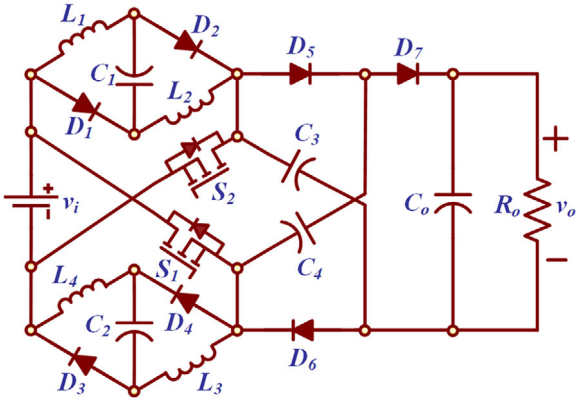


FIGURE 2 The proposed converter

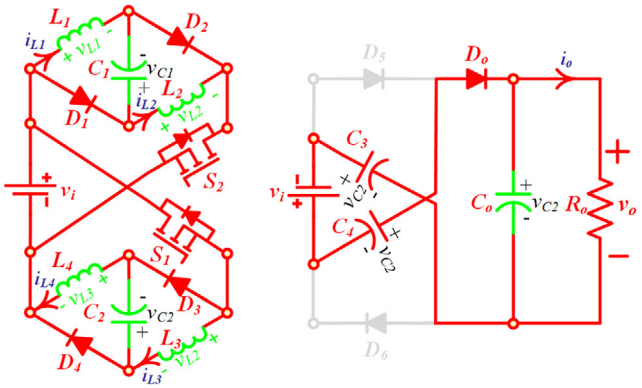


FIGURE 3 Mode I of the proposed converter

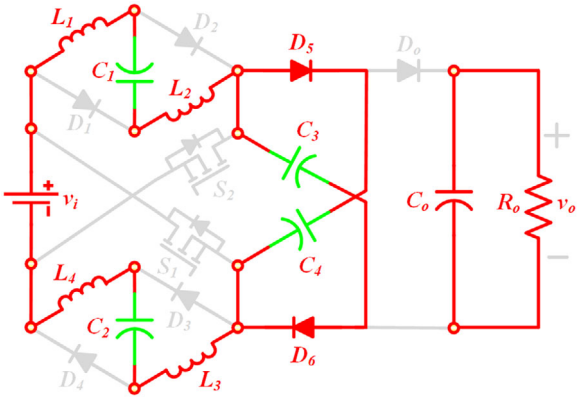


FIGURE 4 Mode II of the proposed converter

of VLSI section gets charged up to the voltage level equal to the source voltage v_i. The output capacitor C_o gets charged by the series connection of capacitors C_3 and C_4 along with the input voltage. Therefore, capacitors C_3 and C_4 gets discharged in Mode I. In Mode II, both switches are turned OFF and capacitors C_3 and C_4 gets charged by the series connection of $L_1, L_2, C_1, L_3, L_4, C_2$ and v_i (Figure 4). During Mode II, the diode D_o is turned OFF and the output capacitor C_o supplies

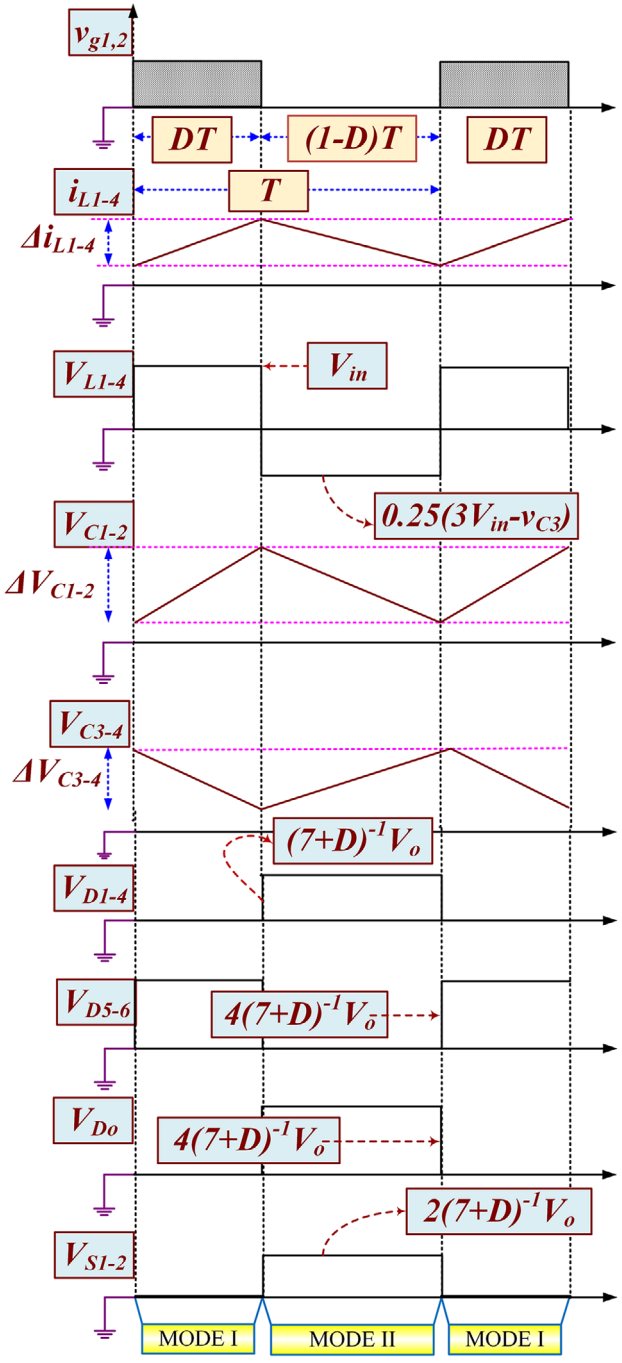


FIGURE 5 Characteristics plots

power to the load. The key waveforms associated with Modes I and II are illustrated in Figure 5.

2.2 | Voltage gain analysis

Equivalent inductor voltage equations in Mode-I are:

$$v_{L1} = v_{L2} = v_{L1} = v_{L2} = V_{in} \tag{1}$$

$$V_{C1} = V_{C2} = V_{in} \tag{2}$$

$$V_{in} + V_{C4} + V_{C3} = V_o \tag{3}$$

Equivalent inductor voltage equations in Mode-II are:

$$4v_L = V_{in} + V_{C1} + V_{C2} - V_{C3} \tag{4}$$

$$v_L = \frac{3V_{\text{in}} - V_{C3}}{4} \tag{5}$$

$$v_L = \frac{3V_{\text{in}} - V_{C4}}{4} \tag{6}$$

Where $v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_L$; V_o is the output voltage, and it is equal to the voltage across the output capacitor C_o. Now using Volt-Sec balance principle on the inductors,

$$V_{in}D + \left(\frac{3V_{in} - V_{C3}}{4}\right)(1 - D) = 0, \tag{7}$$

$$\frac{V_{C3}}{V_{in}} = \frac{V_{C4}}{V_{in}} = \frac{3 + D}{1 - D}. \tag{8}$$

Where D is the duty ratio. Now after solving Equations (3) and (8), the following voltage gain relation is obtained.

$$\frac{V_0}{V_{in}} = \frac{7 + D}{1 - D} \tag{9}$$

3 | DESIGNING OF THE CONVERTER

When it comes to certain applications, the design of the converter as well as the choice of components that are appropriate are of the utmost significance. This converter has been designed to work in continuous conduction mode. The components selection is done as per the following relations:

3.1 | Inductor design

The selection of inductor value depends on the average value of the charging current, its ripples, duty ratio, and switching frequency. The ripple current through each inductor in the charging condition is obtained as follows,

$$\frac{V_{in}DT_S}{L} = \Delta i_L \tag{10}$$

Where, Δi_L is ripple current values of each inductor (L_1, L_2, L_3 and L_4). Therefore, the critical value of each inductor required to operate the proposed converter in CCM can be calculated as,

$$L_{Cri} > \frac{V_{in}DT_S}{\Delta i_L} = \frac{V_{in}D}{\Delta i_L f_S} \tag{11}$$

Thus, the value of each inductor can be chosen based on Equation (12), where Δi_L is 20–40% of the average inductor current value and f_s is the switching frequency to control the switch.

3.2 | Capacitor design

The capacitor value depends on its charging current, the ripple in voltage across it, duty ratio, and switching frequency. Capacitors C_1, C_2 and C_o are charged in Mode-I. whereas, capacitor C_3 and C_4 charged in Mode-II. Thus, the critical values of capacitors C_1, C_2, C_3 and C_o can be obtained as follows,

$$C_1 = C_2 \geq \frac{i_{in}(1-D)}{\Delta V_{C1,2} f_S} \tag{12}$$

$$C_0 \geq \frac{i_0(1-D)}{\Delta V_{C0} f_S} \tag{13}$$

$$C_3 = C_4 \geq \frac{i_{in}(1-D)}{\Delta D V_{C3,4} f_S} \tag{14}$$

Where,$\Delta V_{C1}, \Delta V_{C2}, \Delta V_{C3}, \Delta V_{C4}$, and DV_{Co} are the voltage ripple contents of the capacitors C_1, C_2, C_3, C_4, and C_o respectively; i_o is the output current.

3.3 | Selection of diodes

The maximum value of voltage stress across all the diodes are expressed as follows,

$$DiodeD_{1/2/3/4} : \begin{cases} 0, & 0 < t < DT_S \\ -\dfrac{V_0}{(7+D)}, & DT_S < t < T_S \end{cases} \tag{15}$$

$$DiodeD_0 : \begin{cases} 0, & 0 < t < DT_S \\ -\dfrac{4V_0}{(7+D)}, & DT_S < t < T_S \end{cases} \tag{16}$$

$$DiodeD_{5/6} : \begin{cases} -\dfrac{4V_0}{(7+D)}, & 0 < t < DT_S \\ 0, & DT_S < t < T_S \end{cases} \tag{17}$$

Therefore, the diodes are selected to sustain the voltage stress as mentioned in the above equations:

$$V_{D_{1,2,3,4}} \geq \frac{V_0}{(7+D)}, V_{D_{5,6}} \geq \frac{4V_0}{(7+D)} \tag{18}$$

3.4 | Selection of switches

Both the switches S_1 and S_2 are selected based on their respective voltage stress in the circuit. It is observed that the voltage across both the switches S_1 and S_2 is zero in Mode I. The maximum value of voltage stress across the switches S_1 and S_2 is expressed as follows,

$$SwitchS_{1/2} : \begin{cases} 0, & 0 < t < DT_S \\ \dfrac{2V_0}{(7+D)}, & DT_S < t < T_S \end{cases} \tag{19}$$

Therefore, both the switches S_1 and S_2 are selected to sustain the voltage stress mentioned in the Equation (20).

$$S_{1/2} \geq \frac{2V_o}{7+D} = \frac{V_{in}+V_o}{4} \tag{20}$$

3.5 | Efficiency analysis

3.5.1 | Switches loss

The total loss by the switches is calculated as:

$$P_S = P_{SW} + P_{con} \tag{21}$$

Where, P_{SW} is switching loss and P_{con} is conduction loss which are calculated as follow,

$$\left.\begin{aligned} P_{SW} &= P_{SW1} + P_{SW2} \\ &= \frac{V_0^2}{6R(1-D)}(t_R + t_F) f_S \end{aligned}\right\} \tag{22}$$

$$\left.\begin{aligned} P_{\text{con}} &= I_{S1(RMS)}^2 r_{DS1} + I_{S2(RMS)}^2 r_{DS2} \\ &= \frac{(7+D)^2 V_0^2 D r_{DS}}{2(1-D)^2 R^2} \end{aligned}\right\} \tag{23}$$

3.5.2 | Diodes loss

The power loss contributed by the diode is the addition of loss by internal forward voltage drop (V_f) and loss by internal forward resistance (r_D) which is calculated as:

$$P_{D,loss} = P_{D(VF)} + P_{D(rD)} \tag{24}$$

The power loss by the diode due to the forward voltage drop of VF is calculated as,

$$P_{D(VF)} = I_{in} V_F \tag{25}$$

The power loss by the diode due to the internal forward resistance r_L is calculated as,

$$P_{D(rD)} = \frac{V_o^2}{R^2}\left(\frac{(7+D)^2 + 2D(1-D) - 2D(7+D)(1-D)}{(1-D)^2}\right) r_D \tag{26}$$

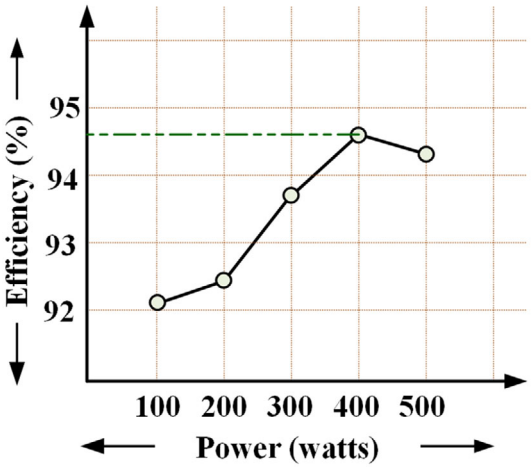


FIGURE 6 Efficiency plot of the converter

3.5.3 | Inductor loss

Total inductor power loss is calculated as;

$$P_L = \left(\sum_{n=1}^{4} i^2_{Ln-(rms)} r_{Ln} \right) \tag{27}$$

Therefore, the efficiency of the proposed converter is calculated with the help of Equations (18)–(24) as (Figure 6);

$$\eta = \frac{P_o}{P_o + P_L + P_{con} + P_{D(VF)} + P_{D(rD)}} \tag{28}$$

$$= \frac{(1-D)^4 I_{in} R V_o^2}{(1-D)^4 V_{in} R^2 + 16 V_{in}^2 I_{in} [64M_1 + 4M_2 + M_3]} \tag{29}$$

$$M_1 = (r_L + D^2 r_{DS}), M_2 = (1-D)^2 V_F, M_3 = (4-3D)^2 r_D \tag{30}$$

4 | COMPARATIVE STUDY

Comparison of the converters having similar boosting networks involving switched inductors and capacitors are discussed in this section and they are briefly summarized in the Table 1. Most of the compared converters are multiple switch type which involves more than one switch in their designs. A switched inductor (SL) based converter is presented in [23] which is developed by three diodes and two inductors such that inductors magnetize in parallel and demagnetize in series. However, the voltage stress across the only active switch is same as the output voltage. To counter the issue [24], presented three designs of active switched inductor (ASL) which involves capacitors in them and have lower voltage stress on the switches. However, switches are floating such that they need separate drivers and control. Also the gain of these converters is not that sufficient to be used for high voltage applications. Multi-cell based configurations are presented in [25] where SL and SC networks are extended with their different modules to obtain higher voltage gain but doing this increases the size, complexity, and cost of the converter. A new idea is presented in [20, 26] in which inclusion of third switch in ASL based boost converter is introduced. This modification has made the converter to be operated and controlled with double duty cycles. Now a wider range of control is possible by varying one or all the duty ratios. An extension to this converter is presented in [21] in which a pair of diode capacitor is included to the converter. The voltage gain is enhanced, but so are the ripples in the input current. The converter in [22] involves two switched inductors (SL) connected in series with the respective branch switches. By using the auxiliary switch, this converter is also set to run in extended duty mode. One of the key advantages of these converters is that they can control multiple entities at the same time. However, they suffer from high voltage stress across the third switch and the output diode which then is not allowed to operate the converter for very high voltage gain. All the discussed voltage gain and switch voltage stress are plotted in the Figure 7a,b, respectively.

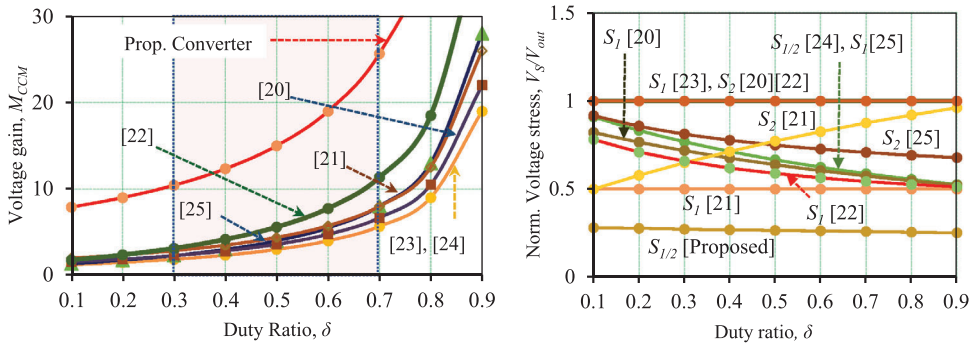
TABLE 1 Comparison among relevant converters topology

Ref.	Voltage gain	N_S	Switches Voltage stress	Norm. Voltage Stress of switches
[23]	$\frac{1+D}{(1-D)}$	1	$S_1 = V_o$	$S_1 = 1$
[24]	$\frac{1+D}{(1-D)}$	2	$S_{1/2} = \frac{V_{in}+V_o}{2}$	$S_{1/2} = \frac{1+G}{2G}$
[25]	$\frac{1+2D}{(1-D)}$	2	$S_1 = \frac{2V_{in}+V_o}{3}$ $S_2 = \frac{V_{in}+2V_o}{3}$	$S_1 = \frac{2+G}{3G}$ $S_2 = \frac{1+2G}{3G}$
[20]	$\frac{1+D_1}{1-D_1-D_2}$	3	$S_1 = \frac{V_{in}+V_o}{2}$ $S_2 = V_o$	$S_1 = \frac{1+G}{2G}$ $S_2 = 1$
[21]	$\frac{(2-D_2)}{1-D_1-D_2}$	3	$S_1 = \frac{V_o}{2}$ $S_2 = V_o - V_{in}$	$S_1 = 0.5$ $S_2 = \frac{G-1}{G}$
[22]	$\frac{(1+3D_1+D_2)}{1-D_1-D_2}$	3	$S_1 = \frac{V_{in}+V_o}{2}$ $S_2 = V_o$	$S_1 = \frac{1+G}{2G}$ $S_2 = 1$
[26]	$\frac{(4-D_2)}{1-D_1-D_2}$	3	$S_1 = \frac{V_o}{2}$ $S_2 = \frac{V_o}{2}$	$S_1 = 0.5$ $S_2 = 0.5$
[24]	$\frac{(3-D)}{1-D}$	2	$S_1 = \frac{V_o - V_{in}}{2}$ $S_2 = \frac{V_o - V_{in}}{2}$	$S_1 = \frac{G-1}{2G}$ $S_2 = \frac{G-1}{2G}$
Pro	$\frac{(7+D)}{(1-D)}$	2	$S_1 = \frac{V_{in}+V_o}{4}$ $S_2 = \frac{V_{in}+V_o}{4}$	$S_1 = \frac{1+G}{4G}$ $S_2 = \frac{1+G}{4G}$

Abbreviations: D, Duty ratio; N_S , switch count; G= voltage gain.

5 | RESULTS AND DISCUSSIONS

The proposed converter is experimentally validated at a duty ratio of 0.6 (Figure 9). For the input voltage of 22 V, magnitude of the output voltage is 400 V, which confirms the voltage gain of 19. The schematic of the control circuitry used regulate the



(a) Voltage gain comparison

(b) Comparison of Switch voltage stress

FIGURE 7 Comparison plots among different discussed SL, SLC models

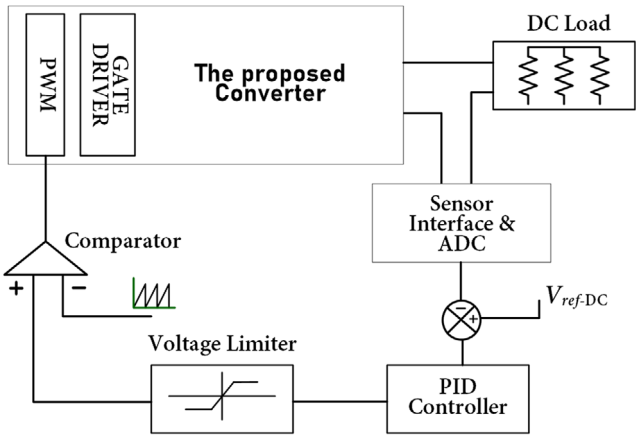


FIGURE 8 Schematic of the converter control

converter voltage is depicted in the Figure 8. The waveforms of input and output voltages are shown in Figure 10a. In addition to the voltage and current waveforms of the input and output, the voltage of different components has also been examined. Figure 10b illustrates the voltage stress of the switches S_1 and S_2. An important feature of the proposed converter is to have low voltage stress across the components and it can be observed that the peak voltage across switches S_1 and S_2 is about 100 V while the magnitude of the output voltage is 400 V. This confirms the low voltage stress of switches S_1 and S_2. Further, Figure 11a voltage across capacitor C_1 and voltage stress of diode D_1. The voltage of capacitor C_1 is equal to the input voltage and has a magnitude of 22 V, while the peak voltage stress of the diode D_1 is equal to the sum of capacitor voltage C_1 and voltage of inductor L_1. The inductor current L_1 and L_3 are also shown in Figure 11a,b illustrates the voltage of capacitors C_3, C_4, and output capacitor C_o. The voltage of the capacitor C_3 and C_4 has a magnitude which is half of the output voltage, that is, 200 V whereas the voltage of the output capacitor is equal to the output voltage, that is, 400 V. Similarly, the voltage stress of diodes D_5, D_6 and D_o are shown in Figure 12. All these three diodes have a peak voltage of 200 V, that is, half of the

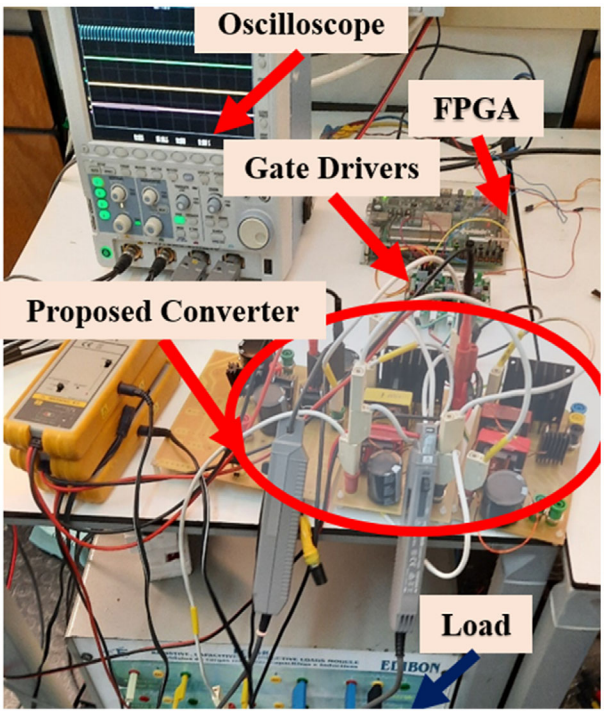


FIGURE 9 Experimental setup for the converter testing

output voltage. All these waveforms confirm the high gain of the proposed converter using the lower voltage rating devices (Table 2).

6 | CONCLUSION

The article discusses the novel topology with high gain and low voltage stress DC–DC converter based on switched-capacitor and switched-inductors for fuel cell and PV applications. The converter performance is analysed and verified with the hardware prototype (22/400 V, 50 kHz). At a duty ratio of 0.6, the converter is able to maintain 200 V for an input

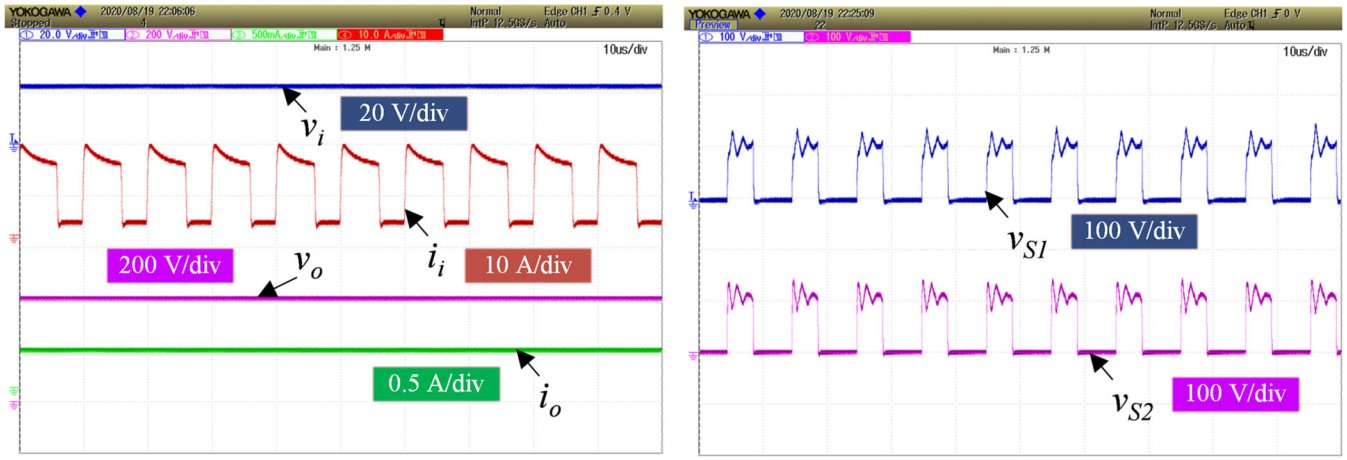


FIGURE 10 Experimental results: V_o, V_{in}, i_o, i_{in}, V_{S1}, V_{S2}

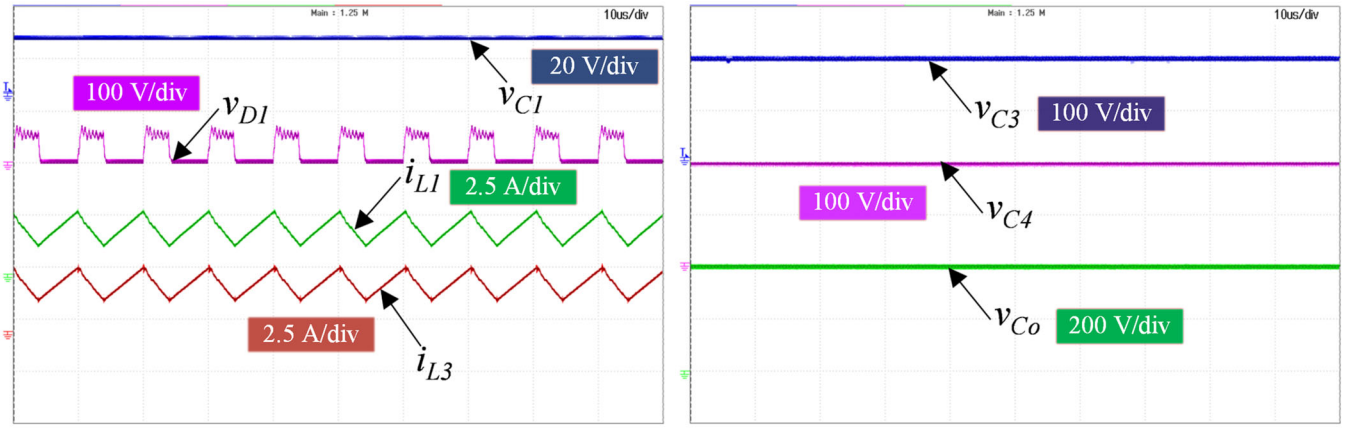


FIGURE 11 Experimental results: V_{C1}, V_{D1}, i_{L1}, i_{L2}, V_{C3}, V_{Co} and V_{C4}

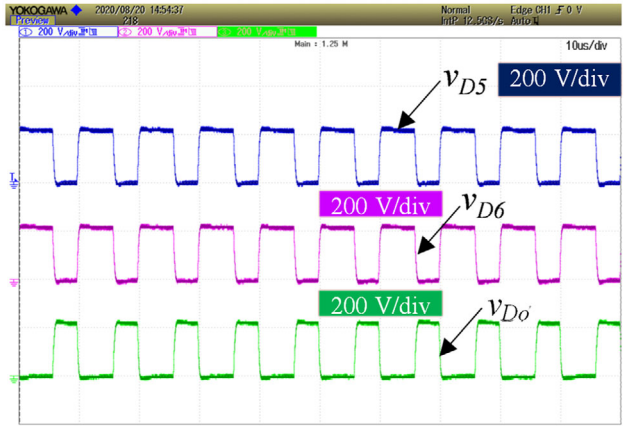


FIGURE 12 Experimental results: V_{D5}, V_{D6} and V_{D7}

voltage of only 22 V. The switches experience a voltage of 50 V across them which is only 0.25 times the output voltage. The reported maximum efficiency is 94.7% at a load of 250 Ω.

TABLE 2 Parameters for experimental validation

Parameters	Values
Power	500 W,
Switching frequency	50 kHz
Load	Resistive 150–450 Ω
Inductance L_1 and L_2	1.5 mH
Capacitance	C_o =220 μF, $C_{1,2,3,4}$ =100 μF
Switches S_1 and S_2	SiC MOSFET-C3M0065090
Diodes D_o and $D_{1,2,3,4}$	STTH30R0/6 and SDUR3020W

AUTHOR CONTRIBUTIONS

MD Samiullah: Conceptualization, formal analysis, investigation, methodology, resources, writing - original draft, writing - review and editing. Marif Siddique: Conceptualization, formal analysis, methodology, validation, writing – original draft, writing – review and editing. Atif Iqbal: Funding acquisition, resources, supervision, validation, visualization, writing - review and editing. Kiran Maroti: Methodology, validation,

writing - original draft, writing - review and editing. Subrata Banerjee: writing - review and editing.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable – no new data generated, or the article describes entirely theoretical research.

ORCID

Atif Iqbal https://orcid.org/0000-0002-6932-4367

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