QATAR UNIVERSITY

COLLEGE OF ENGINEERING

TRANSFORMERLESS MICROINVERTER WITH LOW LEAKAGE CURRENT CIRCULATION AND LOW INPUT CAPACITANCE REQUIREMENT FOR PV APPLICATIONS

BY

Ahmad Mirdad Khan

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COMMITTEE PAGE

The members of the Committee approve the thesis of **Ahmad Mirdad Khan** defended on

8/1/2017

_____

Prof.
Lazhar Ben-Brahim
Thesis/Dissertation Supervisor

_____

Prof.
Adel Gastli
Thesis/Dissertation Co-Supervisor

_____

Dr.
Mounir Bouzguenda
Committee Member

_____

Dr.
Ahmed Massoud
Committee Member

_____

Dr.
Hasan Mehrjerdi
Committee Member

Approved:

_____

Dr. Khalifa Al-Khalifa, Dean, College of Engineering

ABSTRACT

The inevitable depletion of limited fossil fuels combined with their harmful footprint on the environment led to a global pursuit for alternative energy sources that are clean and inexhaustible. Renewable energies such as wind, biomass and solar are the best alternative energy candidates, with the latter being more suitable for GCC countries. Besides, the energy generated from photovoltaic (PV) modules is one of the elegant examples of harnessing solar energy, as it is clean, pollutant-free and modular. Furthermore, recent advances in PV technology, especially grid-connected PV systems revealed the preeminence of using multiple small inverters called (Microinverters) over using the conventional single inverter configuration. Specifically, the break-even cost point can be reached faster and the system modularity increases with microinverters usage. Nonetheless, due to microinverter's small ratings designers prefer transformerless designs because transformer removal achieves higher efficiency and power density. However, the transformer removal results in loss of galvanic isolation that leads to dangerous leakage current circulation that affects system safety. Another issue with microinverters is that since they are installed outside their bulky DC-Link electrolytic capacitor lifetime deteriorates the system reliability because electrolytic capacitor failure rate increases as temperature increases. Moreover, the DC-Link capacitor is used to decouple the 2^{nd} order power harmonic ripples that appear in single-phase systems. Thus, the objective of this thesis is to design an efficient transformerless microinverter that has low leakage current circulation and low input capacitance requirement with a minimum number of active switches. In other words, the objective is to increase the safety and the

reliability of the system while maintaining the high efficiency. Eventually, the configuration selected is the transformerless differential buck microinverter with LCL filter and it is modeled with passive resonance damping and active resonance damping control.

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Chapter 1 : Introduction

1.1. Background

The rapid increase in the energy demand is coupled with the rapid exhaustion of the limited fossil fuel sources. This fact increased the global requirement for clean energy sources and efficient and reliable harnessing technologies [1]-[5]. Unlike fossil fuel based systems, technologies involved in the utilization of renewable energy resources such as solar energy, wind energy and biomass energy are environmentally clean and this is the reason why these sources are more significant in this century. For instance, sun's energy is inexhaustible, effective and environmentally friendly [6]-[10]. Also, the energy generated from photovoltaic (PV) modules is one of the elegant examples of harnessing solar energy, as it is clean, pollutant-free and modular [11]. Beside, PV modules are noiseless, require low maintenance and have simple operation [12]. Since most power systems and loads are AC, PV module's DC output power is unsuitable for them and many power conversion stages must be added. Traditionally, PV DC output power is converted to an AC-side power through a single central inverter (Figure 1.1 (a)) or by the other different conventional configurations as in Figure 1.1 (b) and (c). Also, to assure that the system is extracting the maximum power from the PV panel, a DC/DC converter is used with maximum power point tracking (MPPT) algorithm and it is connected prior to the inverter.

However, the traditional methodology used in grid-connected PV systems is challenged by a new methodology. Specifically, multiple small inverters are deployed

with each PV module and their output is connected in parallel with the utility grid (Figure 1.1 (d)). These small inverters are called Microinverters. According to [13]-[15], microinverter-based PV systems improve energy harvest and system efficiency. In addition, microinverter-based PV system reduces installation cost, boosts flexible future expandability option and increases system modularity [13]-[15]. Microinverter configuration is crucial to Gulf Cooperation Council (GCC) region countries because microinverter provide a flexible future expandability option instead of derating or overrating the central or the string inverter in case of PV system expansion or expected expansion. Figure 1.1 shows a structural comparison between the microinverter configuration and the conventional configurations in PV systems. Note that, ratings of

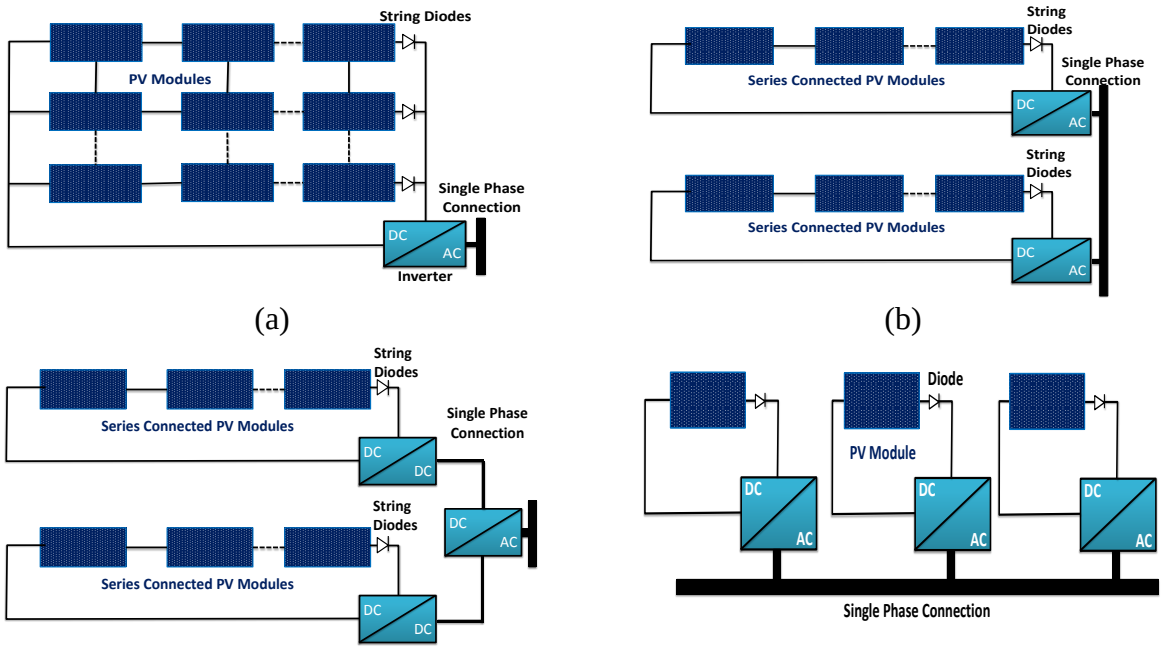


Figure 1.1: Structural comparison between conventional inverter configuration and microinverter configuration in grid-connected PV systems: (a) centralized configuration, (b) string configuration, (c) multi-string configuration and (d) microinverter configuration

microinverters are related to the commercially available PV modules which are between 200W and 700W [16].

Grid-connected microinverters are classified as transformer or transformerless type based on the existence of galvanic isolation. The galvanic isolation is realized practically with a transformer. In addition to isolation, these transformers can be utilized as voltage boosters. Moreover, the transformer in the microinverter is either placed in the AC side with line frequency operation or in the DC side with high frequency operation. Unfortunately, line frequency transformers are impractical because line frequency transformers are bulky. Similarly, the high frequency transformers also introduce extra losses. According to [17], removing the transformer from the inverter or microinverter achieves 1% to 2% higher efficiency, improves the power density and reduces the cost [18]-[20]. Thus, microinverter developers are recently concentrating on transformerless designs.

However, this global movement toward transformerless designs raised a safety flag regarding the loss of galvanic isolation and the amount of the circulating leakage current [21]. This leakage current is caused by the existence of the parasitic capacitance between the PV terminals and the ground. In addition, leakage current circulation causes power losses, current harmonics and electromagnetic interference [21], [22]. Therefore, the suppression of this leakage current improves the reliability of the system [23]. Recently, new requirements were added to the German PV system grid connection standard -Verband Der Elektrotechnik (VDE) - about the maximum leakage current magnitude and its sudden variation [24]; if the leakage current is over 300mA RMS or

the sudden variation reaches 30mA RMS the inverter is automatically disconnected from the grid irrespective of the power conversion level [25].

One of the other important issues with single phase systems is that the instantaneous power consists of an average term and double line frequency pulsating term. However, with single phase generators such as synchronous generators the double grid frequency power is filtered by the inertia of the rotor and the prime mover combined. Unfortunately, due to the zero inertia of PV systems, this double frequency power is not filtered and it is transferred to the DC-side. The classical solution to minimize the power pulsating is to use a large electrolytic capacitor in the DC-side. However, the electrolytic capacitor deteriorates the reliability of the system since it is responsible for most system failures [15], [26]. Besides, since microinverters are installed outdoor without any auxiliary cooling systems there is a concern about the performance of the electrolytic capacitor; because of its reliability sensitivity to the temperature change. Additionally, the usage of polypropylene film capacitor is not possible due to the high capacitance requirement –in mF for a system with a 600W rating only - that increases the cost of the film capacitor [27]. In other words, reducing the input capacitance requirement would allow the usage of smaller reliable capacitor –film type not electrolytic type- at the DC-link; therefore, boosting the overall system reliability.

1.2. Thesis Objective

The objective of this thesis is to 1) study and review techniques of mitigating leakage current and power ripples in transformerless single phase microinverters, 2) design a highly efficient transformerless microinverter with low leakage current circulation using

a minimum number of switches and 3) design a suitable controller to lower input capacitance requirement. This will improve the safety and reliability of the designed microinverter as reducing the leakage current improves the safety aspects, and lowering the input capacitance allows the usage of film capacitors that boosts the system reliability.

1.3. Thesis Scope

The scope of this thesis focuses on the study and design of DC/AC converter side and the grid connection of the transformerless microinverters. In other words, the high gain DC/DC boost converter that is equipped with MPPT algorithms prior to the DC-link capacitor; is out of the scope of this thesis. These topics (high gain requirement issue with microinverters) are well discussed in previous literature [28]-[31]. Note that, in this thesis there is no quantitative measurement of the reliability improvement. Nevertheless, according to the suggestions of [32], [33], decreasing the input capacitance and avoiding the usage of electrolytic type DC-Link capacitor would enhance the overall system reliability (longer lifetime).

1.4. Thesis Outline

The thesis report starts with an introductory overview in Chapter 1 (this chapter) describing the background, statement of the problem, objectives and outline of the thesis. Chapter 2 extensively surveys the existing methods to tackle the leakage current and the power ripples issues. In Chapter 3 a thorough study is conducted to compare various leakage current reduction topologies and the possibility of transistorless power

decoupling. Chapter 4 discusses the design methodology adopted in this study. Chapter 5 explores extensively the microinverter design adopted (LCL Differential Buck Microinverter) to simultaneously decouple the power ripples and reduce the leakage current. Chapter 6 describes the simulation results of the proposed techniques. Chapter 7 concludes and outlines future works.

Chapter 2 : Literature Review

The literature review chapter is divided into two sections: 1) analysis and review of leakage current reduction techniques and 2) double grid frequency power ripples issue. Specifically, in each section a detailed investigation of the generation mechanism of each phenomena is presented and techniques to mitigate them are surveyed.

2.1. Leakage Current Review

This section surveys the leakage current generated by different full-bridge microinverter topologies. Specifically, elaboration on how the leakage current is linked to the common mode voltage and how Pulse Width Modulation (PWM) scheme affects the leakage current. In addition, the existing methodologies that are used to reduce the leakage current in microinverter topologies are discussed. The survey excludes the family of half-bridge topologies because they need twice the grid peak voltage at the DC-link which stresses further the high gain boost DC-DC converter connected with the PV module [28]- [31].

2.1.1 Common Mode Voltage and Leakage Current

The general transformerless microinverter configuration circuit with the parasitic elements is shown in Figure 2.1. This configuration is used to analyze and explain the generation of the leakage current.

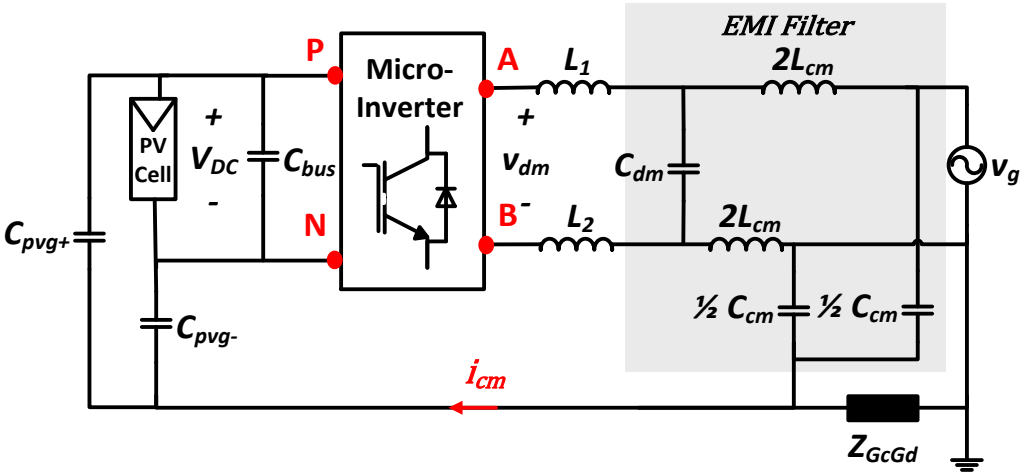
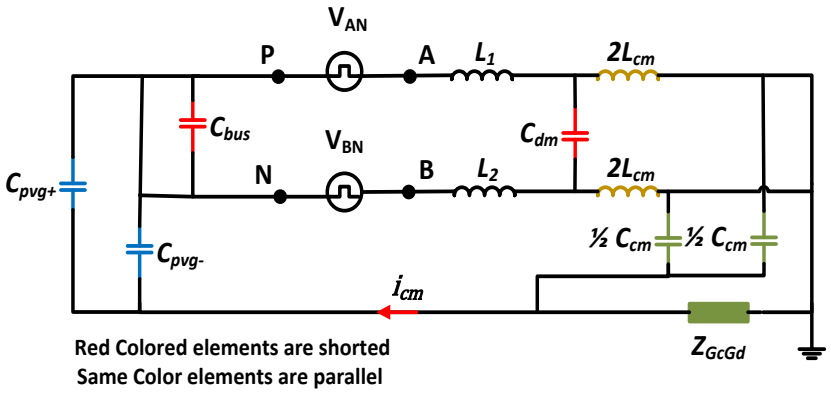


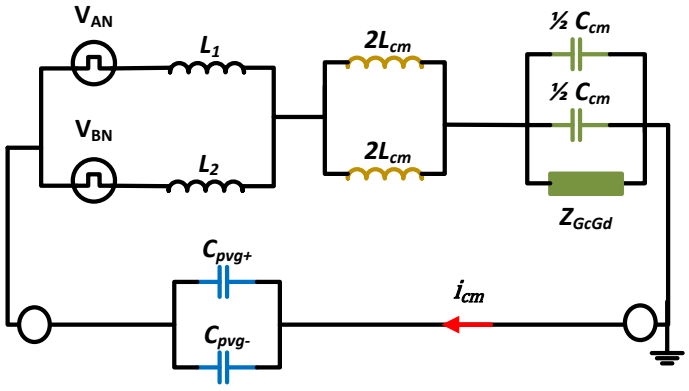
Figure 2.1: Transformerless PV microinverter general circuit configuration with parasitic elements representation

Without the galvanic isolation between the grid and the PV system, a Common Mode (CM) resonant circuit is formed. This CM circuit consists of the stray capacitances between the PV panel terminals and the ground C_{pvg+} and C_{pvg-}, the impedance of the negative terminal of the grid and the ground of PV panel Z_{GcGd}, and the EMI filter components. Analyzing the high frequency CM noise in Figure 2.1, it is clear that the equivalent CM model can be represented as four different voltage sources, V_{DC}, v_g , v_{AN} and v_{BN}. The four distinct sources have different frequencies, hence superposition analysis must be considered. Nevertheless, the grid voltage and PV source can be ignored

because of its low frequency content compared to the two CM noise sources v_{AN} and v_{BN} [34]. Also, because the CM current is of capacitive nature, high frequency signals are the major concern. Evidently any impedance connected in parallel with the neglected sources (e.g. C_{bus} in Figure 2.1) is shorted. According to [34], C_{dm} does not affect the CM current and it is also shorted in the analysis. Consequently, the high frequency CM equivalent circuit can be represented as in Figure 2.2 (b) [35].



(a)



(b)

Figure 2.2: Microinverter high frequency CM model: (a) steps to obtain the high frequency CM circuit and (b) the high frequency CM equivalent circuit

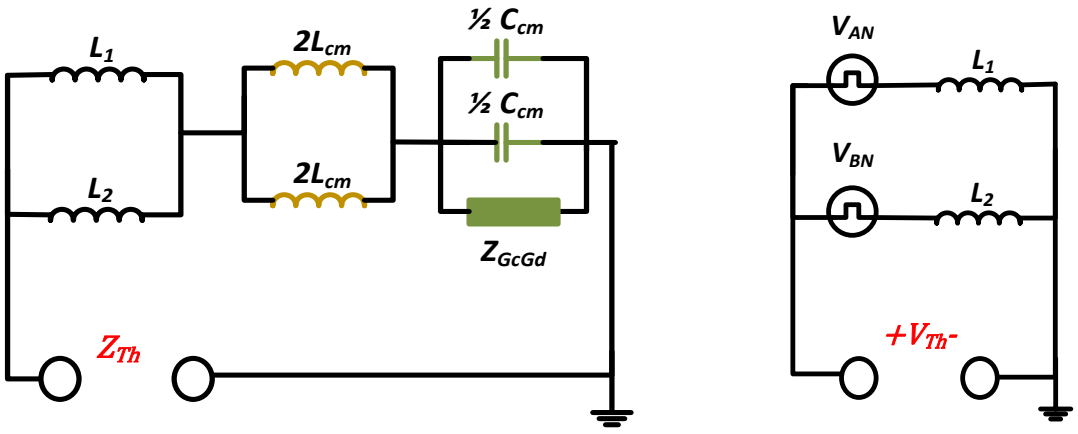
Using Thevenin's theorem, it is possible to find a general term for the total CM noise. Explicitly, according to Figure 2.3 (a), Z_{Th} is expressed as in (2.1)

$$Z_{Th} = L_1//L_2 + 2L_{cm}//2L_{cm} + \frac{C_{cm}}{2}//\frac{C_{cm}}{2}//Z_{GcGd} \tag{2.1}$$

and according to Figure 2.3 (b), V_{Th} is the open circuit voltage at the C_{pvg+} and C_{pvg-} terminals.

$$V_{Th} = v_{total\_CM} = \frac{v_{AN}L_2 + v_{BN}L_1}{L_2 + L_1} \tag{2.2}$$

Notice that $(2L_{cm}//2L_{cm})$ and $\left(\frac{C_{cm}}{2}//\frac{C_{cm}}{2}//Z_{GcGd}\right)$ are in series with the stray capacitances C_{pvg+} and C_{pvg-}, so they have zero current during V_{Th} analysis (open circuit). As a result, V_{Th} is equivalent to the total high frequency CM voltage as in (2.2).



(a) (b)

Figure 2.3: Microinverter modified CM equivalent circuit: (a) analysis to obtain Z_{Th} and (b) analysis to obtain V_{Th}

Considering the conventional CM voltage as

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} \tag{2.3}$$

and the differential mode voltage as

$$v_{dm} = v_{AN} - v_{BN} \tag{2.4}$$

It is possible to obtain

$$v_{AN} = \frac{v_{dm}}{2} + v_{cm} \tag{2.5}$$

$$v_{BN} = -\frac{v_{dm}}{2} + v_{cm} \tag{2.6}$$

Therefore, combining (2.2), (2.5) and (2.6) the total high frequency CM voltage can be expressed as

$$v_{total\_CM} = v_{cm} + v_{dm} \frac{L_2 - L_1}{2(L_2 + L_1)} \tag{2.7}$$

Thus, the CM noise circuit model can be further simplified as in Figure 2.4 without considering the Z_{GcGd}, EMI filter components and shorting the Thevenin impedance as suggested by [35].

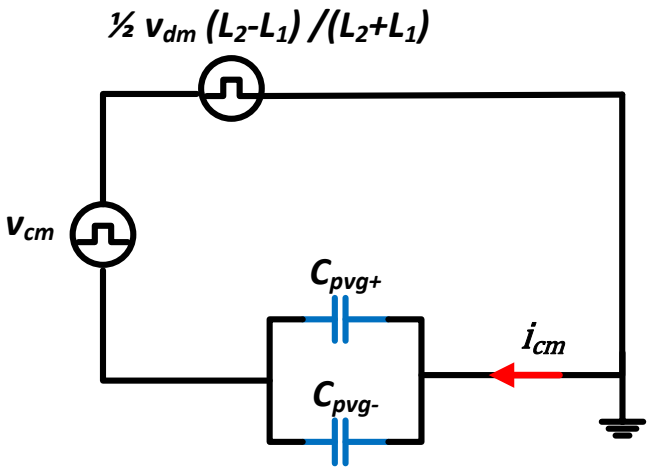


Figure 2.4: CM noise simplified circuit model suggested by [35]

As indicated in [34]-[37], the total CM noise has contribution from the differential voltage and is related to the two filter inductors L_1 and L_2. By selecting identical values of the two filter inductances L_1 and L_2, it is possible to eliminate the contribution of the differential voltage in (2.7) to the total CM voltage which becomes

$$v_{total\_CM} = v_{cm} = \frac{v_{AN} + v_{BN}}{2} \tag{2.8}$$

Hence, after the simplification done in Figure 2.4 and considering (2.8), the leakage current is the current that flows in the equivalent capacitance C_{pvg} of the two stray capacitances C_{pvg+} and C_{pvg-} and can be expressed as

$$i_{cm} = C_{pvg} \frac{dv_{total\_CM}}{dt} \tag{2.9}$$

According to (2.9), it is clear that the sufficient condition to eliminate the leakage current is to maintain the total CM voltage at a constant value [35], [36], [38]. Practically, the low frequency component of the CM voltage is not the major concern, since the values of the stray capacitances are small. While the high frequency components are the major contributor to the leakage current [25].

2.1.2. Leakage Current Relation with the PWM Scheme

Based on the findings of the previous section that the non-constant CM voltage results in large leakage current circulation as in (2.9). Therefore, exploring how the leakage current is related to the PWM scheme can be done observing the CM voltage on the existing 4-swtich symmetrical inductor microinverter configuration with the basic PWM techniques as in Figure 2.5. The basic PWM techniques are: Bipolar modulation [39], Standard

Unipolar modulation, Unipolar II modulation and Unipolar III modulation [39], [40]. Note that the most commonly used PWM technique is the bipolar one (Figure 2.5 (b)) [39].

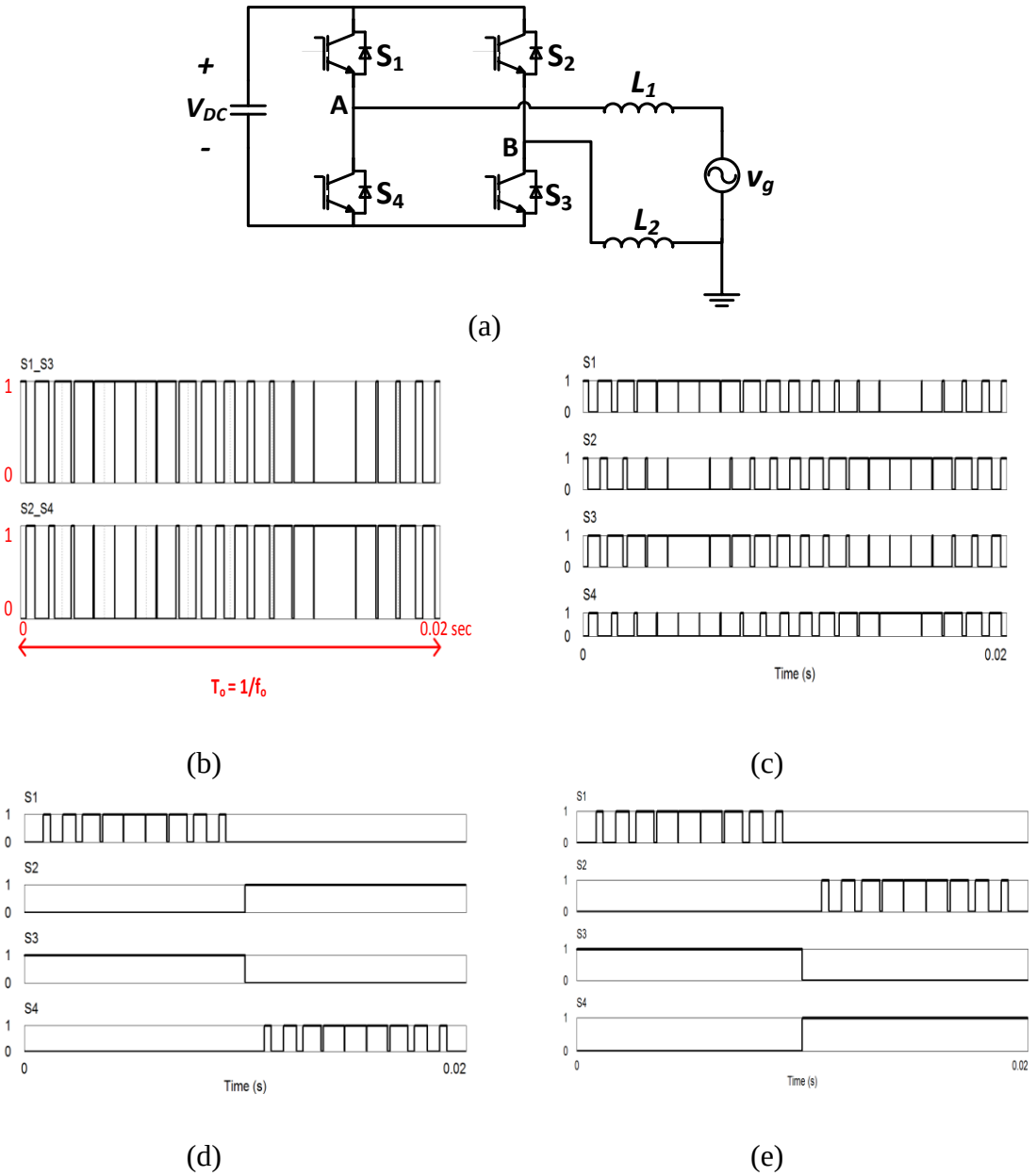


Figure 2.5: Existing PWMs of 4-Switched microinverter: (a) Full Bridge microinverter, (b) Bipolar modulation [39], (c) Standard Unipolar modulation, (d) Unipolar II modulation and (e) Unipolar III modulation [40]

Note that for more clarity of the waveforms, all PWM scheme graphs are illustrated for one period of the grid cycle (f_o=50Hz*)* and at the lower switching frequency (f_s=1kHz). Also, in all microinverter figures, MOSFET parallel diode is the intrinsic body diode but the IGBT diode is the normal Si diode.

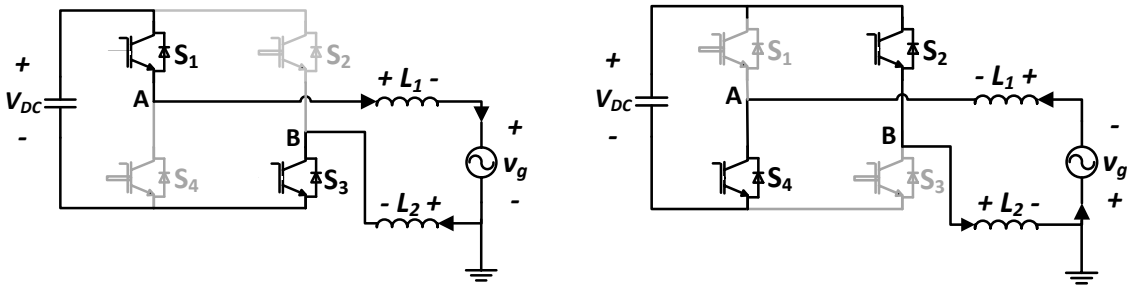


Figure 2.6: Bipolar PWM operation modes [39]: (a) During the positive output, (b) during the negative output

Analyzing the CM noise generated by the bipolar scheme shows that there are two operation modes and at each mode, the CM voltage is ½V_{DC} as shown in Figure 2.6. Therefore, the CM current is very low since the derivative of a constant CM voltage is zero. However, at the transition stage between the two operation modes shown in Figure 2.6, small leakage current spikes occur during the transition from mode (a) to mode (b) or vice-versa. The benefit of the bipolar modulation is the simplicity and the low CM noise. Unfortunately, there are some major drawbacks with the usage of bipolar modulation. One of the greatest issues is that the switching ripples in the output current occur at the switching frequency. Furthermore, the bipolar swing in the output voltage

between V_{DC} and $-V_{DC}$ causes great amount of core losses in the output inductors filter and increases its size [35].

The Unipolar PWMs is achieved using two sinusoidal references that are shifted by 180 degrees and each microinverter leg has its own reference [39]. Unlike the bipolar scheme, the unipolar scheme has four different operating modes during one grid cycle. Also, different unipolar PWMs gates signals are shown in Figure 2.5 (c), (d), and (e). Taking the standard unipolar modulation as an example of illustration as in Figure 2.7, it is clear that the CM voltage pulsates between $\frac{1}{2}V_{DC}$ and zero at the repeated transition between mode (a) and mode (b). Also, the same voltage pulsation occurs at the terminals A and B during the negative half cycle ((c) and (d) of Figure 2.7) resulting in large CM noise. Hence, the leakage current generated by this modulation is relatively large because the CM voltage is non-constant. According to [41], [42], unipolar modulation deteriorates the CM performance of the system and causes a large amount of leakage current circulation. On the other hand, unipolar modulation reduces the filtering requirements because the frequency of the switching ripples is twice the switching frequency [43], [44]. Additionally, during the positive half cycle, the filter inductors are exposed to voltage variations between V_{DC} and zero and during the negative half cycle between $-V_{DC}$ and zero. This enables the usage of smaller filter inductors and hence, reduces core losses [43].

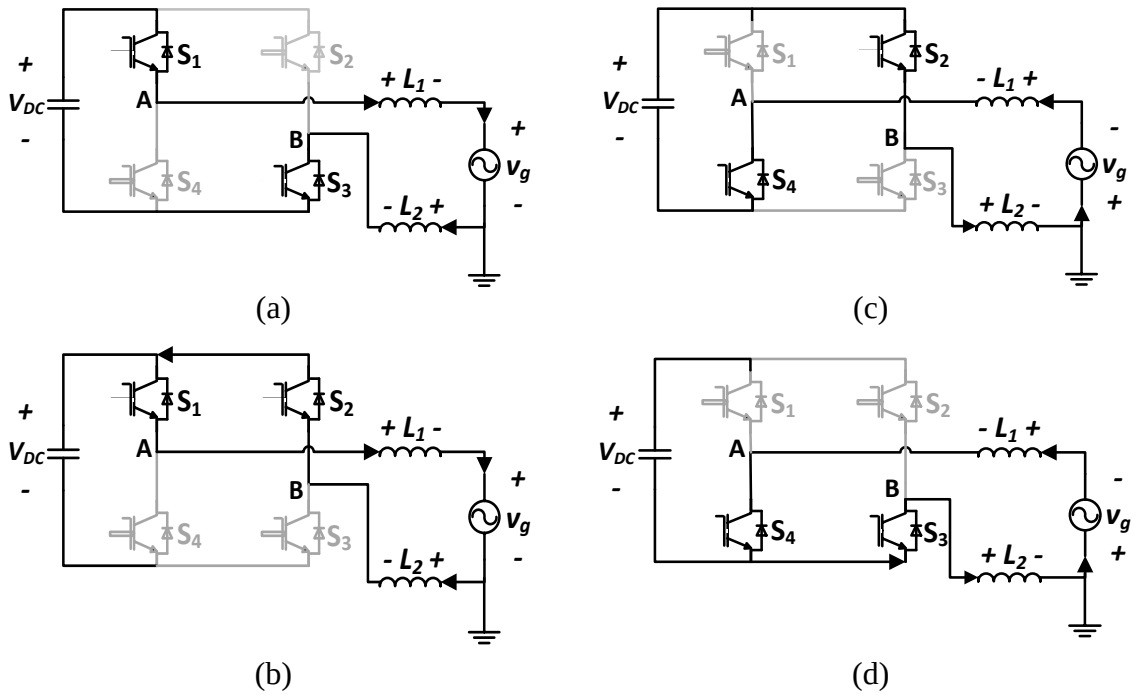


Figure 2.7: Standard Unipolar modulation operation modes [39]: (a) and (b) equivalent circuits in the positive half cycle, (c) and (d) in the negative half cycles

2.1.3. Mitigation Methods

The effective methods to reduce the leakage current can be classified into two categories: first one is to reduce the high frequency components of the CM voltage by disconnecting the microinverter from the PV terminals during the zero level voltage generation in the microinverter output (active switches modification); the second one is to bypass the CM current and deviate it from the ground leaking loop with passive elements such as capacitors (without active switches modification).

2.1.3.1. Elimination of Leakage Current with Active Switches Modification

The elimination of the leakage current with active switches modification is divided to:

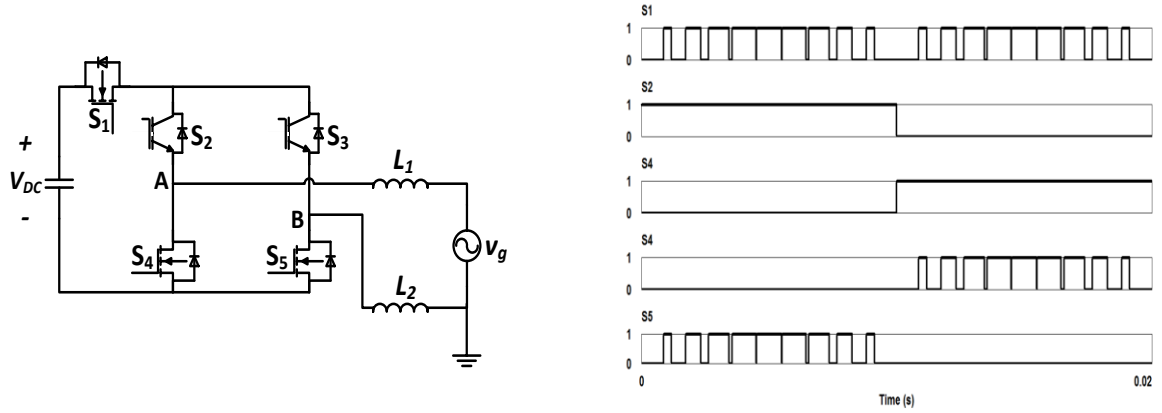
- ✓ DC Decoupling Networks and
- ✓ AC Decoupling Networks

A. DC Decoupling Networks

a. H5 and H6 topologies

The H5 microinverter in Figure 2.8 (a) is a small variation of the 4-switch microinverter topology which results in reducing the leakage current significantly. According to [45], [46], an extra high frequency semiconductor switch located at the positive terminal of the PV panel would reduce the leakage current. In addition, the extra switch guaranties the disconnection of the terminals A and B during the freewheeling stages from the PV parasitic capacitance (Figure 2.8 (a)). Note that, the freewheeling stages are the operation modes where the microinverter output (V_{AB}) is zero. Besides, the PWM used with the H5 topology is similar to unipolar III except that the extra switch has a gate signal that is equal to the summation of both high frequency switches gate signals (Figure 2.8 (b)). Unfortunately, due to the fact that three switches are operating simultaneously, conduction losses are high. In addition to higher conduction losses, the losses are unbalanced; which results in less power density and burdened heat-sinks [25]. Also, due to the control strategy, reactive power flow is not possible [47]. Another problem with the H5 microinverter is that harnessing MOSFETs intrinsic diodes is not possible in the place of S_2 and S_3 (Figure 2.8 (a)) because of MOSFET's body diode slow reverse recovery issue [48]. On the other hand, a parallel diode must be connected with

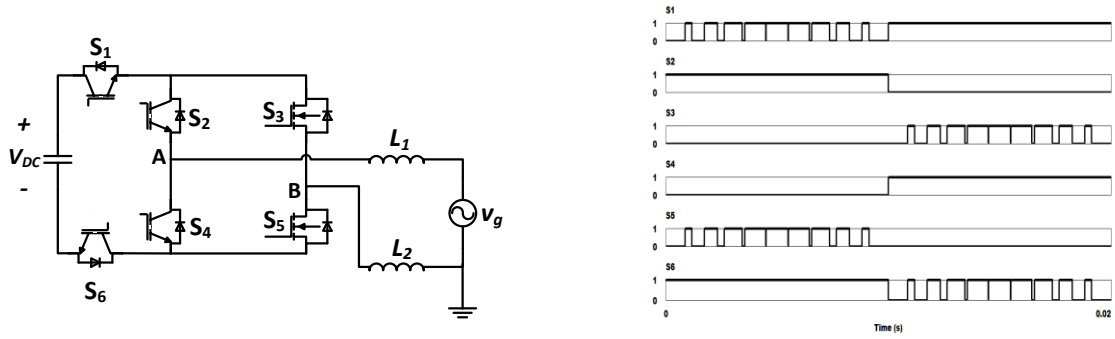
all MOSFETs in the case of SiC switch usage because the reverse current of SiC semiconductor MOSFETs never flows in the body diode [49]. Note that H5 is patented by SMA company [50].



(a) (b)

Figure 2.8: H5 microinverter: (a) configuration and (b) PWM scheme [36], [45], [46], [47]

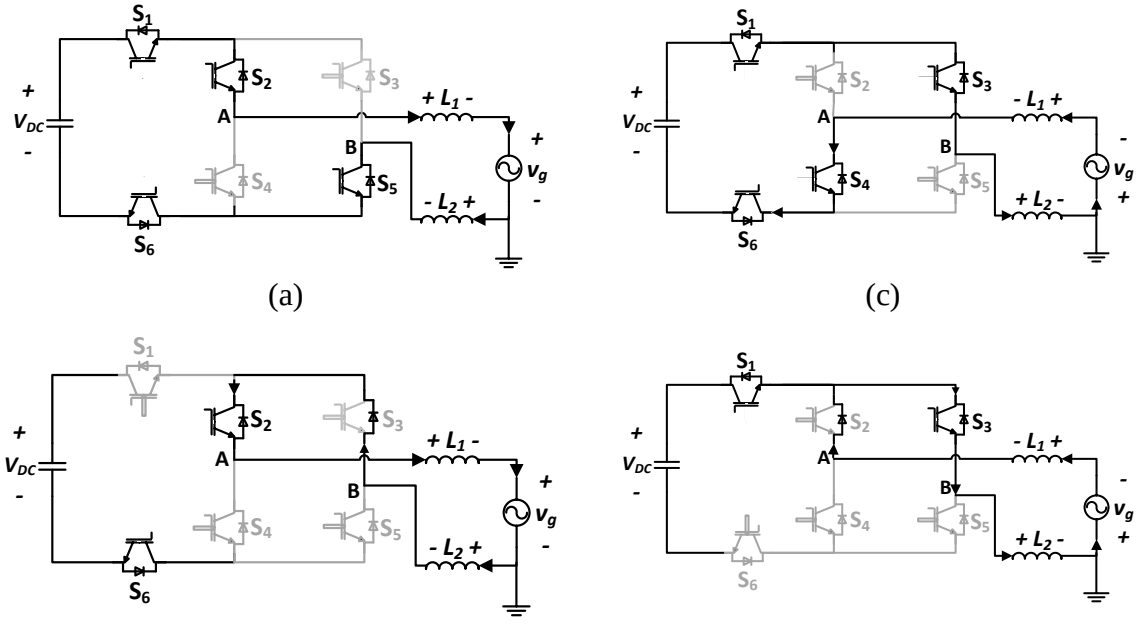
There are many adaptations that can be applied to H5 microinverter to further balance the switching losses. For example, placing an extra switch at the negative terminal of the PV would balance the switching losses with modified PWM [51]. The extra switches S_1 and S_6 have a combination of the low frequency gate signal and the high frequency gate signal (Figure 2.9 (b)). Nevertheless, the biggest drawback of this type of H6 microinverter is that four of its semiconductor switches are in conduction mode most of the time; hence, higher conduction losses [25].



(a) (b)

Figure 2.9: H6 microinverter (balanced losses): (a) configuration and (b) the PWM scheme [51]

The principle of reducing the CM current with DC decoupling network microinverters can be demonstrated by analyzing the operation modes of H6 as an example (Figure 2.10). The significant reduction in the leakage current is because of



(a) (c)

(b) (d)

Figure 2.10: H6 microinverter operation modes [51]: (a) and (b) equivalent circuits in the positive half cycle, (c) and (d) in the negative half cycles

disconnecting the terminals A and B from the parasitic capacitance that are causing the circulation of the leakage current in the freewheeling stages (stage (b) and (d) in Figure 2.10).

Authors in [52] suggested a method to reduce the conduction losses. Their suggested method states that shifting S_6 of Figure 2.9 (a) to the bypass branch as in Figure 2.11 would reduce the conduction losses because two switches are in conduction during the negative half line frequency cycle. The leakage current performance of H6 or the improved H6 is similar to H5 microinverter Nevertheless, the weakness of these previous designs appears when the effect of the semiconductors junction capacitance is taken into account.

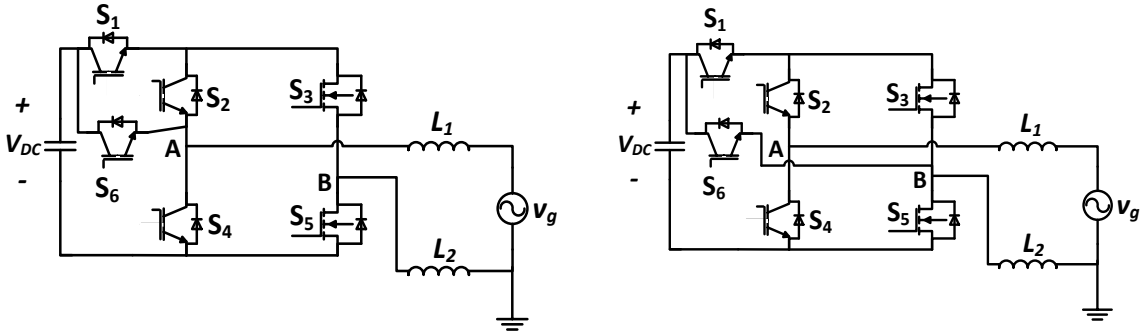


Figure 2.11: Two possible topologies of H6 microinverter with reduced conduction losses [52]

Precisely, the junction capacitance is in the range of several hundred picofarads to several nanofarads [53]. According to [53]-[55], this junction capacitance contributes to the leakage current due to parasitic resonance. As a result, new types of microinverters were

introduced. These new types have the ability to reduce this parasitic resonance leakage current and they are called Neutral Point Clamped (NPC) topologies. NPC DC network decoupling microinverters types will be discussed further in the next subsection.

b. DC-Based Neutral Point Clamped

As mentioned earlier, the H6 microinverter or their modified versions lack the ability to eliminate the leakage current produced by the resonance of the transistors junction capacitance. However, [25] showed that splitting the DC-link capacitor into two

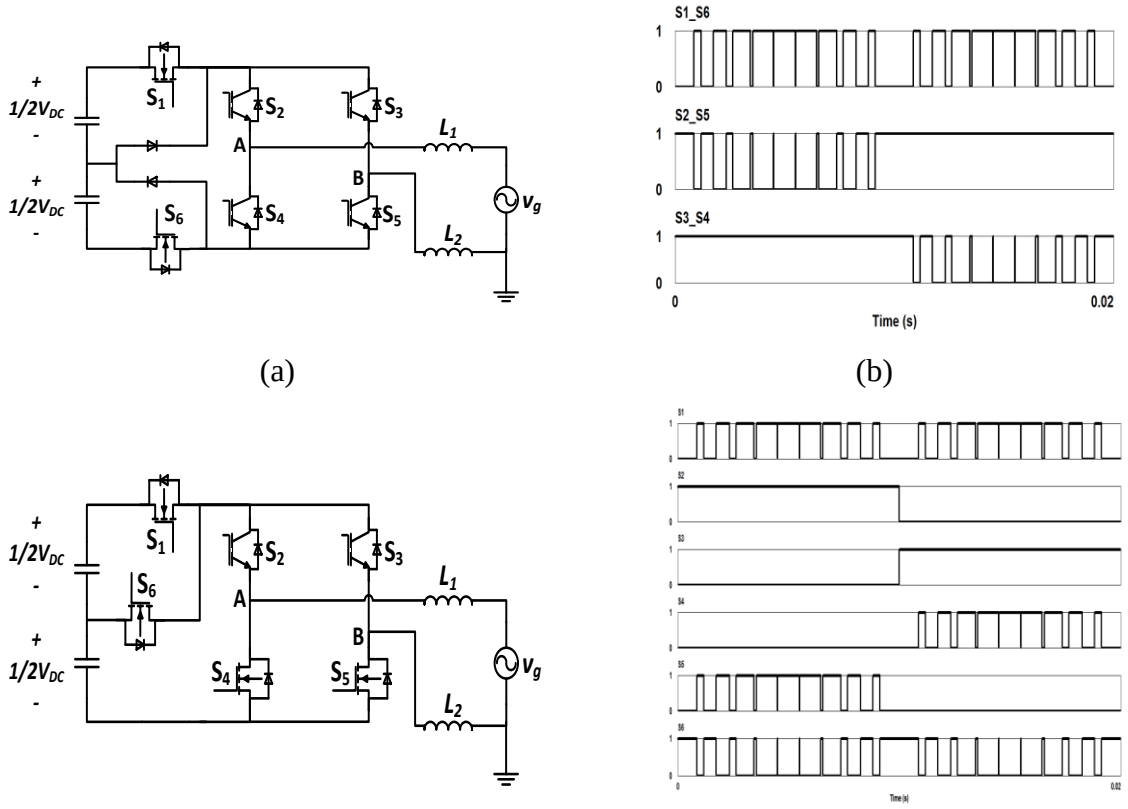


Figure 2.12: Existing DC-based Neutral Point Clamped (NPC) Microinverters: (a) Passive Neutral Point Clamp (PNPC) Microinverter [57], [58] and (b) its PWM, (c) Active Neutral Point Clamp (ANPC) Microinverter and (d) its PWM [55], [58]

capacitors and inserting a clamping cell at the DC side would enhance the CM operation of the H6 microinverter. After the clamping function is added to the H6 microinverter leakage current would be very small. Additionally, as shown in Figure 2.12, the clamping function can be done in two ways: active or passive. Paper [56], gives a generalized approach for designing such NPC circuits. The Passive NPC DC-based decoupling network microinverter uses the PWM shown in Figure 2.12 (b). The CM voltage is constant at $½V_{DC}$. Hence, the leakage current RMS value would be very small. On the other hand, the Active NPC DC-based decoupling network microinverter (Figure 2.12 (c)) CM voltage is almost constant except at the zero crossing of the grid voltage where large voltage spike occurs and contributes to the generation of leakage current. Besides, both NPC-based designs suffer from switching losses since two semiconductor switches are operating at high frequency all the time. However, regarding the conduction losses the Active NPC possesses less conduction losses compared to Passive NPC because only one switch is operating at the grid frequency, whereas, in the Passive NPC two switches are operating simultaneously at high frequency.

As an example of illustration, let us analyze the operation modes of the H6 Passive NPC DC decoupling network microinverter (Figure 2.12 (a)). In this case, the CM noise is constant at $½V_{DC}$ during all the operation stages because of the clamping diodes (see Figure 2.13).

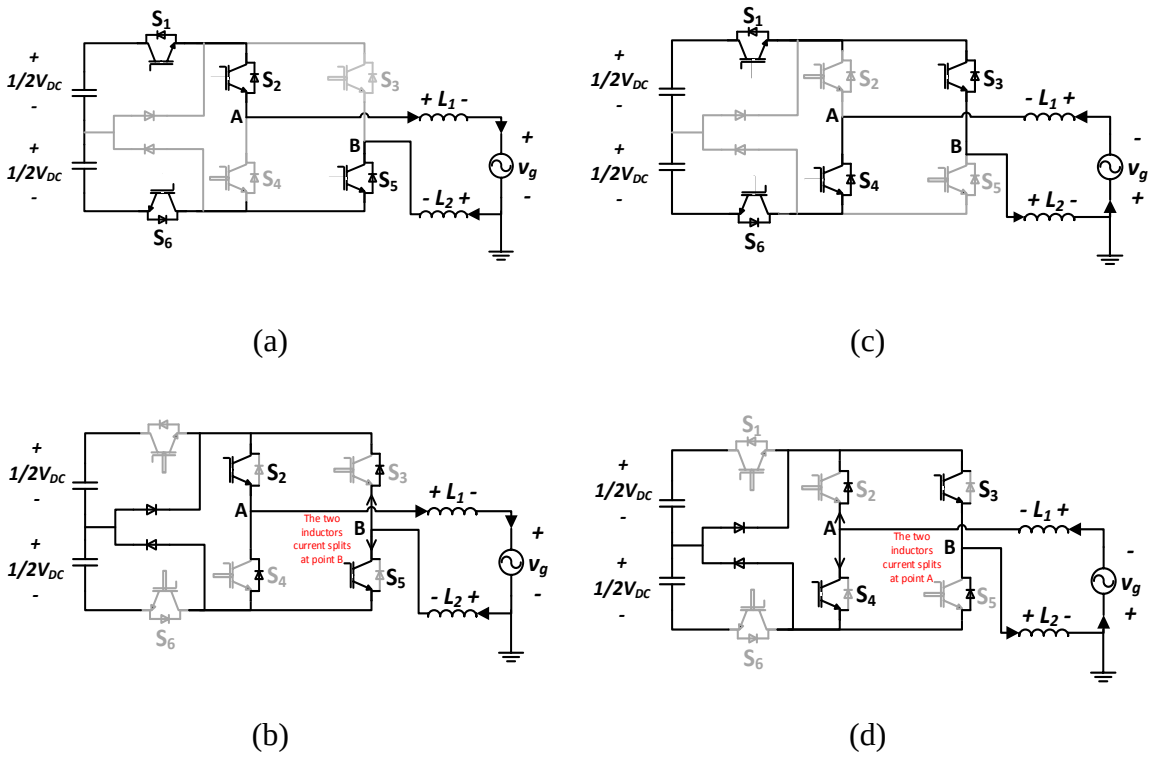


Figure 2.13: H6 Passive NPC (PNPC) operation modes [57], [58]: (a) and (b) equivalent circuits in the positive half cycle, (c) and (d) in the negative half cycles

B. AC Decoupling Networks

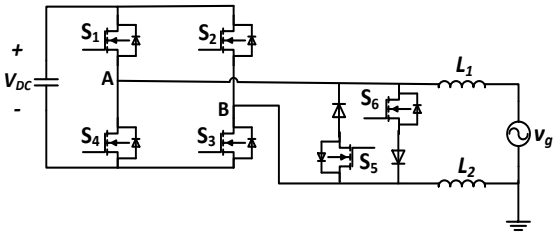
a. HERIC topologies

The Highly Efficient Reliable Inverters Concept (HERIC) is a well-known family of transformerless inverters. In these topologies, reduction of the leakage current can be also achieved by adding extra circuitry at the AC side of the microinverter. For instance, inserting a bidirectional switch between the output terminals A and B would enhance the CM performance of the microinverter [53]. According to [59], one IGBT in series with a diode and their counterparts can be combined to implement a bidirectional switch. The same configuration is realized with two anti-parallel IGBTs or full-bridge diodes with

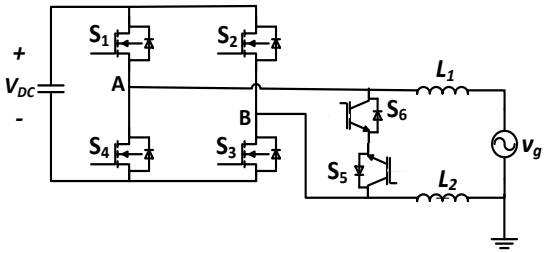
single IGBT. Unlike, the DC-based decoupling H6 microinverters two switches maximally are in the conduction state at any operation mode of these AC-based decoupling microinverters [25] (except HERIC-III three switches are in conduction in the negative non-freewheeling stage [52] and HERIC-V three switches are in conduction in all non-freewheeling stages [60]). Thus, the conduction losses are anticipated to decrease compared to DC-based decoupling types.

Five configurations of HERIC microinverter topologies are shown in Figure 2.14. The first three microinverters, HERIC-I (Figure 2.14 (a)), HERIC-II (Figure 2.14 (b)), and HERIC-III (Figure 2.14 (a)) are similar in operation and the CM noise is therefore similar. HERIC-I design was introduced to use all MOSFET switches so the utilization of the MOSFET body diode is possible. Also, avoiding series connection of bidirectional switches in HERIC-II eliminates the need for PWM dead time. Additionally, HERIC-III bidirectional switches (S_5 and S_6) location are modified to derive the active neutral point clamped configuration which will be illustrated in the next subsection.

HERIC-IV bidirectional switch is designed by one MOSFET and four diodes and has a switch operating at high frequency all the time. Thus, HERIC-IV has the highest switching losses. Moreover, [61] used the same arrangement but with six switches. The extra switch was placed in parallel to the fifth switch (Figure 2.14 (d)) in order to distribute the switching losses and use a smaller heatsink. Finally, HERIC-V (Figure 2.14 (e)) is a combination of two half bridge microinverters [60].



(a)



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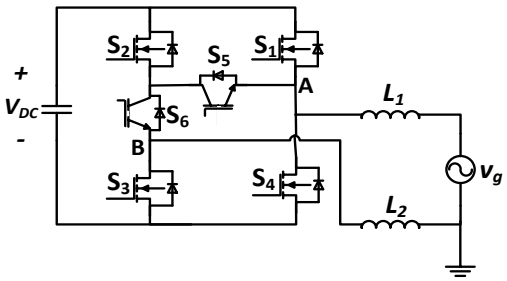
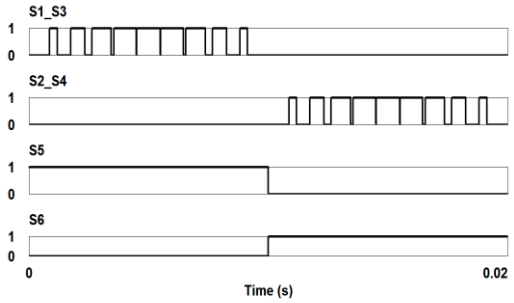
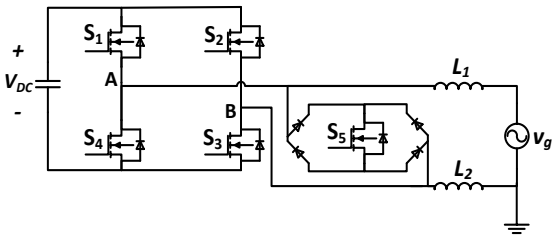


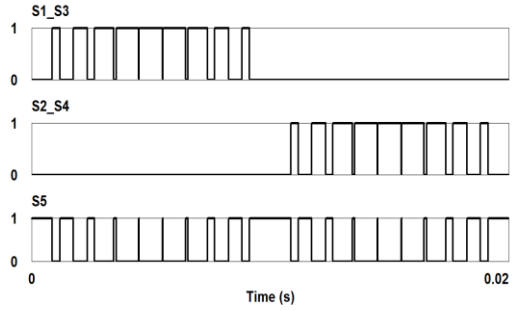
(c)



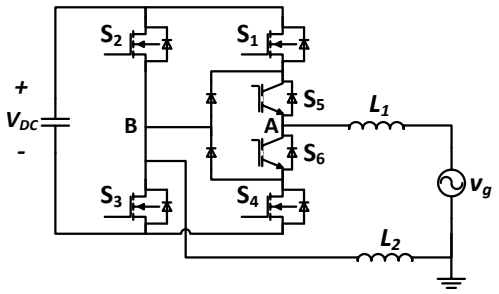
PWM of (a), (b) and (c)



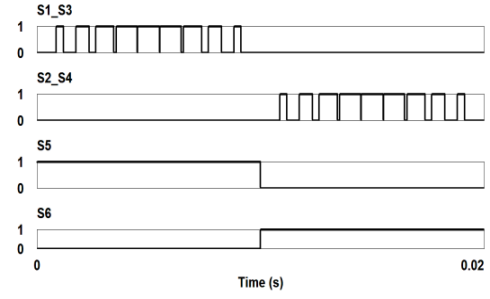
(d)



PWM of (d)



(e)



PWM of (e)

Figure 2.14: Existing HERIC topologies: (a) HERIC-I [35] ,[36] ,[47], (b) HERIC-II [36], (c) HERIC-III [52], (d) HERIC-IV [61] and (e) HERIC-V [60]

The principle of leakage current reduction with AC-decoupling network microinverters (HERIC) is providing an alternative path for the inductors current during the freewheeling stages (stages (b) and (d) of Figure 2.15, taking HERIC-I as an illustration example). Thus, maintaining the CM voltage at $½V_{DC}$ during the whole grid cycle.

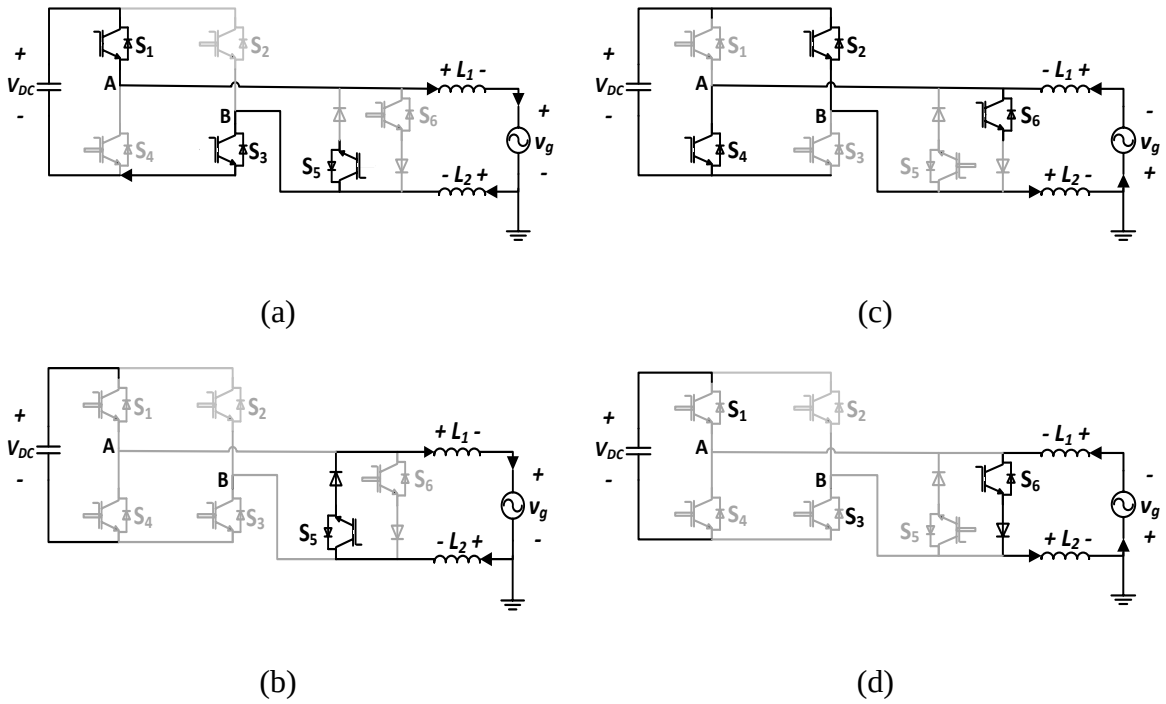


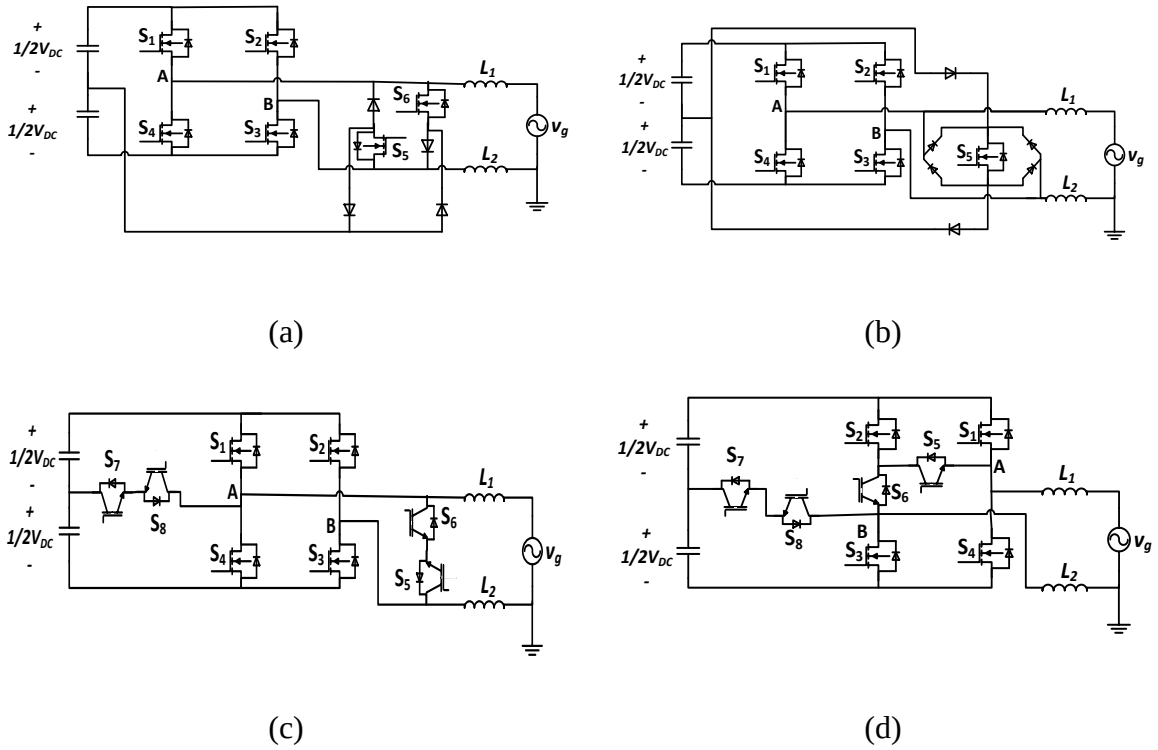
Figure 2.15: HERIC-I operation modes [35], [48]: (a) and (b) equivalent circuits in the positive half cycle, (c) and (d) in the negative half cycles

Even though, these microinverters' performance, compared to DC-based microinverters, has improved regarding the power losses, they still lack the ability to eliminate the current that is produced by the resonance effect of the transistors' junction capacitance. Therefore, similar to what happened with DC-based Neutral Point Clamped

microinverters, similar clamping topologies of AC-based microinverters were introduced in the literature.

b. AC-Based Neutral Point Clamped

Further modification applied to AC-based decoupling microinverters to cancel the effect of junction capacitance is achieved by inserting clamping cell to the microinverter. This clamping cell would also reduce the unexpected high frequency component of the CM voltage and further reduces the leakage current RMS value [25]. In addition, NPC AC-based microinverters are expected to be more preferred since, as discussed earlier, the efficiency of AC-based microinverters is superior to that of DC-based ones [25]. Furthermore, the AC-based microinverters proved to be more cost-effective compared to the DC-based microinverters [25]. Similar to DC-based decoupling network microinverters, the clamping cell can be produced either by active switches or diodes. Therefore, the previously proposed HERIC microinverters can be modified to implement HERIC NPC microinverters (Figure 2.16). As shown in Figure 2.16, four different topologies of HERIC microinverters are modified to achieve Active or Passive NPC microinverter. Notice that the Active NPCs, here, are using a similar clamping function of the T-type or Coenergy inverters [62]. Furthermore, the PWM applied with the Passive-NPC HERIC types in this section are the same as the non-neutral point clamped types. On the other hand, the extra switches that are deployed for the active clamping function use low frequency gate signals. Specifically, switch S_7 is shorted during the positive half cycle and S_8 switch gate signal is complementary to S_7.



(a) (b)

(c) (d)

Figure 2.16: Existing HERIC Neutral Point Clamped microinverters (a) HERIC-I Passive NPC [25], (b) HERIC-IV Passive NPC [25], [53] (c) HERIC-II Active NPC , and (d) HERIC-III Active NPC

Here, the leakage current elimination methodology is similar to HERIC designs. The only difference is the usage of clamping cells to assure that the CM voltage is kept constant at ½V_{DC} during the freewheeling stages and provide an alternative path for the inductors current. As an example of illustration, let us study the operation modes of HERIC-I Passive NPC of Figure 2.16 (a). The corresponding operation modes, shown in Figure 2.17, are expected to generate insignificant leakage current level. Specifically, for stage (b) and (d) of Figure 2.17, the clamping diodes maintain constant voltage drop on each split capacitor; consequently, the CM voltage is constant during all operation modes.

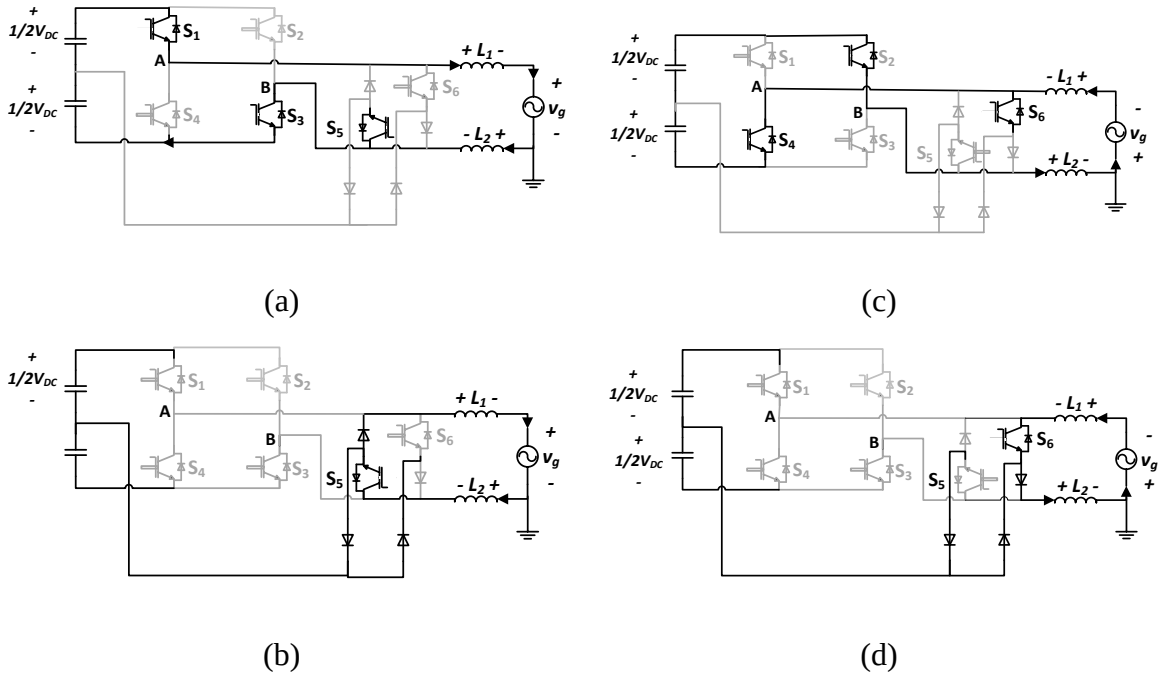


Figure 2.17: HERIC-I Passive NPC microinverter operation modes [25]: (a) and (b) equivalent circuits in the positive half cycle, (c) and (d) in the negative half cycles

2.1.3.2. Elimination of Leakage Current without Active Switches Modification

The publications [44], [63], [64] showed that the leakage current could be bypassed by introducing a CM conducting path to the microinverter without using extra active switches. Additionally, this reduction in the number of active components enhances the reliability and the lifetime of the system [63], [64]. Specifically, [63], [64] designed an LC filter to eliminate the leakage current. Similarly, [44] used an LCL filter to reduce the leakage current and more complex filters are possible to reduce the leakage current such as LLCL configuration [65]. The authors of [44], [63], [64] used 4-switch full-bridge topology with standard unipolar PWM. In [63], [64] the LC filter used is split into two identical parts and the negative DC terminal is connected to the midpoint of the two split

capacitors of the LC filter to provide a conduction path to the CM current (Figure 2.18). The differential mode is not affected because of the symmetrical filter configuration [63], [64]. Nevertheless, connecting the midpoint of the two output split capacitors to the midpoint of the two series DC-link capacitors would also reduce the leakage current [44], [65]. Unlike, the leakage current mitigation techniques with active switches modifications, reactive power flow is possible with the configuration in Figure 2.18, because of standard unipolar modulation usage. This is crucial because grid-tied PV systems with a rating below 3.68kW must attain Power factor (PF) between 0.95 leading and 0.95 lagging to improve the grid voltage stability [66], [67]. Additionally, using the microinverter in VAR mode at night would be difficult because precharging the DC-link capacitor from the grid requires the freewheeling diodes to operate as full-bridge rectifier [68], and this is difficult with the modification applied to mitigate the leakage current in the methods suggested by adding extra active circuitry [67].

The analysis is little different than subsection 2.1.1. For example, with this mitigation method, the parasitic elements of the grid are not neglected. The grid parasitic elements are the negative grid terminal resistance (R_E), the positive terminal grid inductance (L_{g1}) and the negative terminal grid inductance (L_{g2}) as in Figure 2.18. However, the EMI filter and Z_{GcGd} are neglected as in the previous analysis in subsection 2.1.1 which leads to the simplified CM equivalent circuit of Figure 2.19.

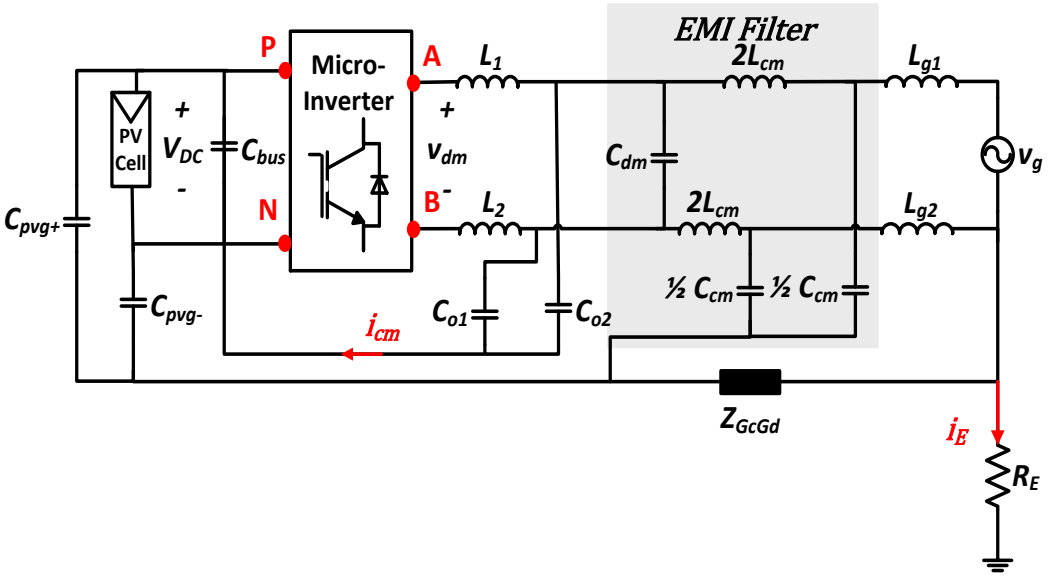


Figure 2.18: Transformerless PV microinverter configuration with parasitic elements representation and the CM filter [63], [64]

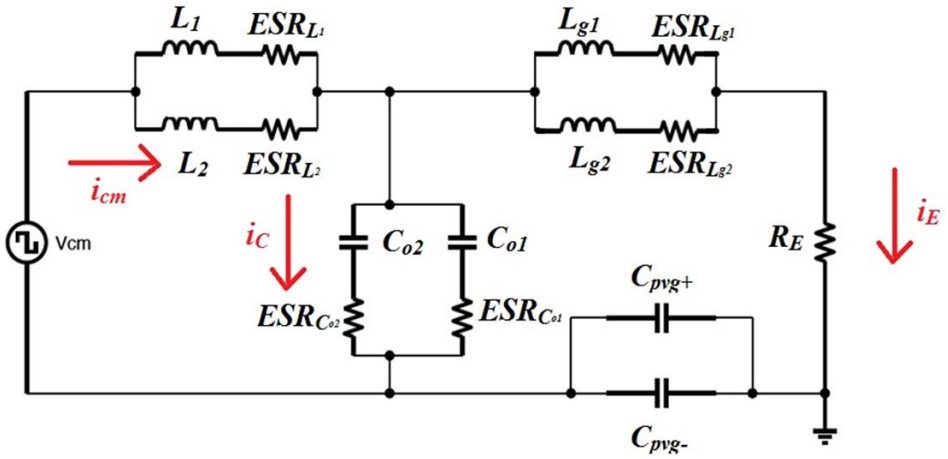


Figure 2.19: CM equivalent circuit of the microinverter with the CM filter (midpoint of the two output split capacitors is connected to the negative DC bus)

Effective reduction in the ground leaking current is expected even with the standard unipolar modulation that has the worst CM performance. The additional two split capacitors provide a low impedance path to the CM current. Specifically, the aim is to

reduce i_E (Figure 2.19). In more details, i_E is determined in (2.10) by current division rule and neglecting the ESR of all the inductances and capacitances.

$$i_E = i_{cm} \frac{Z_{Co1} // Z_{Co2}}{Z_{Co1} // Z_{Co2} + Z_{pvg+} // Z_{pvg-} + Z_{Lg1} // Z_{Lg2} + R_E} \tag{2.10}$$

Since i_{cm} is at the switching frequency, then most of the CM current will flow at the higher capacitance branch. Meaning that, the split capacitors provide an easier path for the CM current and $i_c \gg i_E$. For instance, a capacitor in range of micro-farads would be sufficient to reduce the ground leaking current (since the parasitic capacitances of the PV panel are in the range of several nano-farads). Nevertheless, the parasitic element of the grid must be taken into consideration.

The ground leaking current would be small with stiff AC grids. This is due to the fact that R_E is large in the range of 10Ω to 15Ω [18], [63], [69], [70]. It further increases the impedance of the ground leaking current loop and most of the current is bypassed by the split capacitors. On the other hand, with weak grids, the R_E is unpredictable [63]. Considering the worst case scenario, when the point of resonance occurs between the $Z_{pvg+} // Z_{pvg-}$ and $Z_{Lg2} // Z_{Lg2}$ at the switching frequency, the ground leaking loop would possess low impedance path. Consequently, the ground leaking current would be significant. In this case small CM choke can be installed to shift the point of resonance at the switching frequency of the ground leaking loop. This CM choke is small in size because of the high frequency operation. According to [63], in extreme cases, grounding the frame of the PV panel through a small resistance would be effective in reducing the leakage current.

On the other hand, considering the configuration that connects the midpoint of the two split capacitors to the midpoint of the two series DC-link capacitors as in Figure 2.20 [44], [65].

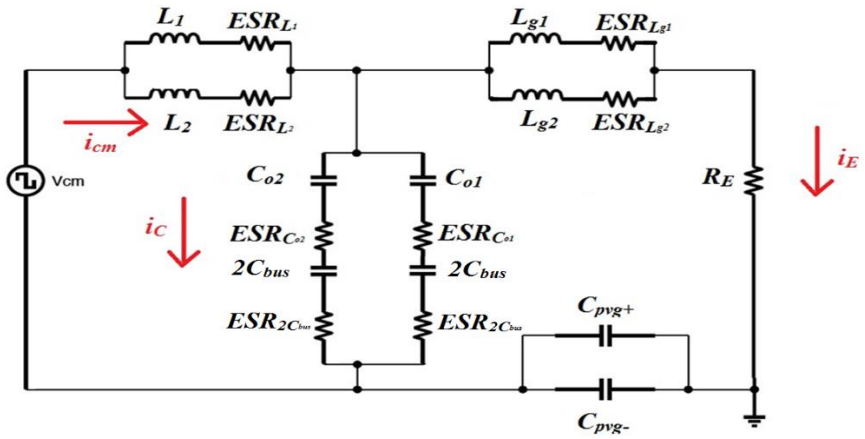


Figure 2.20: CM equivalent circuit of the microinverter with the CM filter (midpoint of the two split capacitors is connected to the midpoint of the two series DC-link capacitors (C_{bus}=2C_{bus}+2C_{bus})

The performance regarding the leakage current reduction is slightly worse in the configuration that connects to the midpoint of the two output split capacitors to the midpoint of the two series DC-link capacitors compared to connecting to the midpoint of the two output split capacitors to the negative DC bus terminal. This is because the CM bypassing branch has lower capacitance in Figure 2.20 compared to Figure 2.19. Nonetheless, i_c is still always greater than i_E; thus, the ground leaking current is insignificant.

2.2. Double Grid Frequency Power Ripples Review

This subsection explores the connection between the double grid frequency power ripples in single phase systems with the size of the DC-link capacitor. Specifically, elaboration on the 2nd order harmonic ripples generation phenomena will be presented along with the mitigation methods. Besides, only transistorless schemes will be reviewed because many possible solutions exist for decoupling these power ripples in the literature. All these solutions in [71] use extra active switches and energy storage devices. Therefore, it is crucial to provide a transistorless technique to eliminate the power pulsation because the reduction in the number of active components enhances the reliability and the lifetime of the system and this is one of the thesis objectives.

2.2.1. Double Grid Frequency Power Ripples and DC-Link Capacitor Size

When the injected current into the grid by the microinverter is sinusoidal; the single-phase instantaneous power is composed of an average term with an additional double grid-frequency pulsating term as in (2.11):

$$p_{AC}(t) = \frac{V_g I_g}{2} cos(\varphi) + \frac{V_g I_g}{2} cos(2(2\pi f_o)t - \varphi) \tag{2.11}$$

Where V_g is the peak grid voltage, I_g is the peak grid current, f_o is the nominal grid frequency and $cos(\varphi)$ is the power factor. Assuming that the power factor is unity the instantaneous power is as in (2.12):

$$p_{AC}(t) = \frac{V_g I_g}{2} + \frac{V_g I_g}{2} cos(2(2\pi f_o)t) \tag{2.12}$$

The power that is drawn from the PV panel is governed by the MPPT and it is kept constant at $P_{PV} = P_{DC}$. Additionally, ignoring losses in the conversion stages the PV panel power is equal to average AC output power $P_{PV} = P_{AC}$. Graphing the AC instantaneous power injected into the grid and the DC instantaneous power delivered by the PV panel would indicate why a capacitor is needed (Figure 2.21)

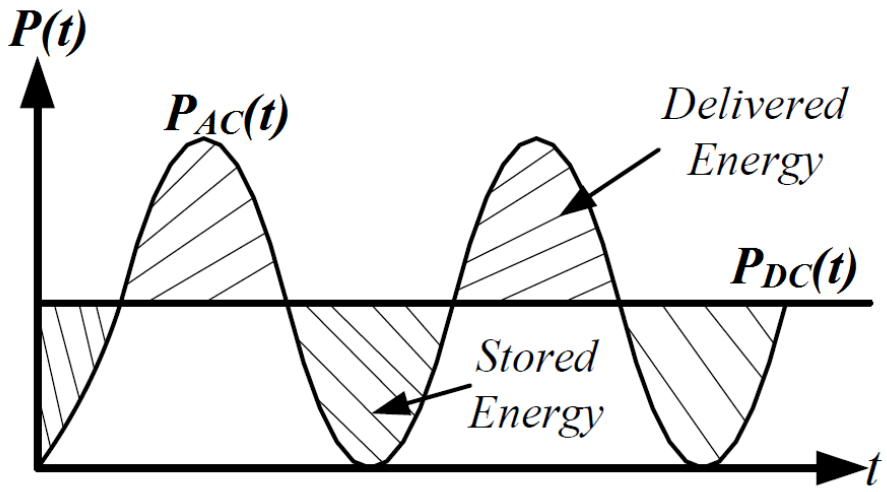


Figure 2.21: Instantaneous power in the system and the total power processed by the decoupling capacitor

The double grid frequency power pulsation affects the PV system performance. For instance, these power ripples affect the MPPT algorithm because it makes the voltage and current measurements time varying; therefore, power ripples reduce the efficiency of the MPPT controller. Nevertheless, the classical solution to minimize the pulsating power is to use large unreliable electrolytic capacitors [71], [72]. Besides, the value of the decoupling capacitor capacitance can be determined by calculating the amount of energy

that is needed to be stored. In more details, finding the area of the shaded region that represents the energy stored in the DC-link capacitor during half of the grid cycle (Figure 2.22) would lead to finding a relation between the required DC-link capacitor size and ripple content.

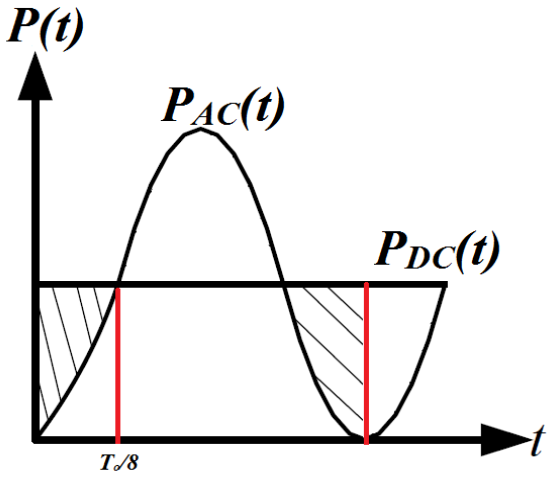


Figure 2.22: AC-side power (output power) and DC-side power (PV side power) waveforms

So the energy stored in the DC-link capacitor during half of the grid cycle is:

$$E_{C_{DC-link}} = 2\int_0^{\frac{T_o}{8}} (P_{DC}(t) - P_{AC}(t))\, dt = C_{DC-link}\int_{V_C(min)}^{V_C(max)} V_c\, dV$$

$$\frac{T_o}{4}P_{DC} - \int_0^{\frac{T_o}{8}} \frac{V_g I_g}{2}\sin^2(2\pi f_o t)\ dt = \frac{C_{DC-link}}{2}(V_C(max)^2 - V_C(min)^2)$$

Since $P_{PV} = P_{DC} = \frac{V_g I_g}{2}$; then the value of the DC-link capacitor is:

$$C_{DC-link} = \frac{V_g I_g}{2\pi f_o (V_C(max)^2 - V_C(min)^2)} \quad (2.13)$$

Also, it is known that the maximum and minimum capacitor voltages ($V_C(max)$ and $V_C(min)$) can be expressed as:

$$V_C(max) = V_c(DC) + \frac{\Delta V_c}{2} \quad (2.14)$$

$$V_C(min) = V_c(DC) - \frac{\Delta V_c}{2} \quad (2.15)$$

Inserting (2.14) and (2.15) in (2.13) results in the following equation for the DC-link capacitance:

$$C_{DC-link} = \frac{P_{PV}}{2\pi f_o V_C(DC)\, \Delta V_C} \quad (2.16)$$

Where $C_{DC\text{-}link}$ is the decoupling DC-link capacitor capacitance, P_{PV} is the PV input power, $V_C(DC)$ is the DC voltage level across the DC-link capacitor and ΔV_C is the maximum allowable peak-to-peak voltage ripples across the DC-link capacitor.

Moreover, plotting ΔV_c as a function of the $C_{DC\text{-}link}$ for 600W H-Bridge type microinverter that is synchronized with 240Vrms/50Hz grid shows clearly the issue of the DC link capacitor size. Thus, to have an acceptable level of voltage ripples the DC-link capacitor value is in the range of mF (Figure 2.23); hence, making the adoption of reliable polypropylene film capacitor impossible at the DC side since mF range film capacitor is extremely expensive [26].

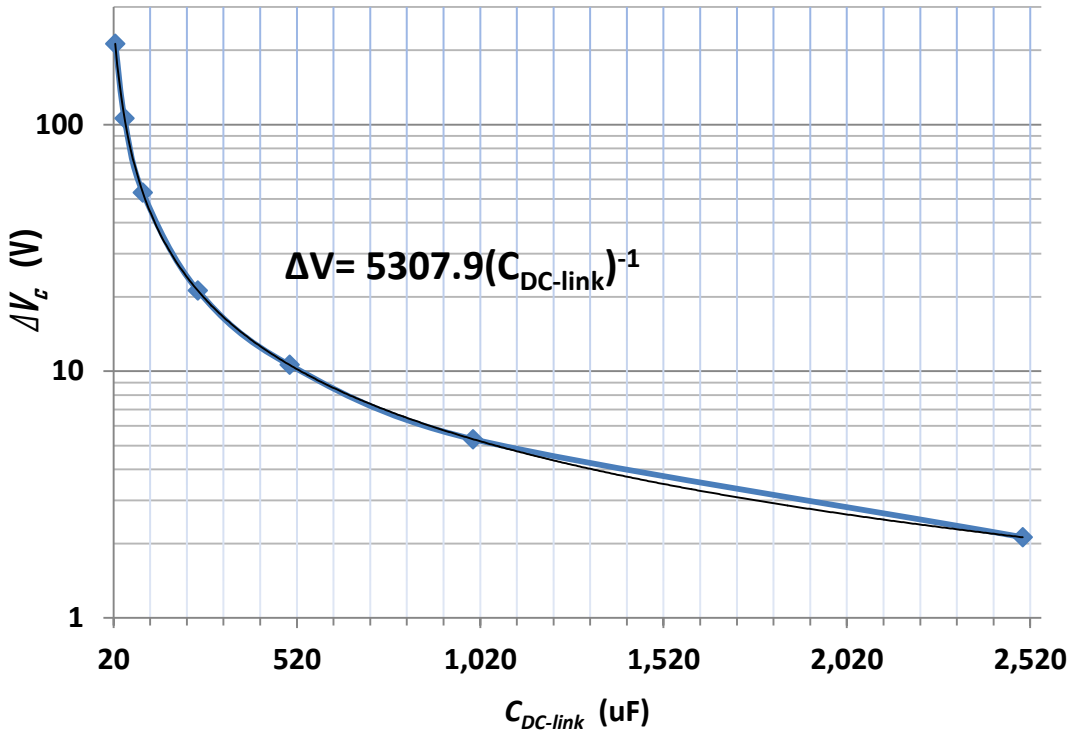


Figure 2.23: The DC-link voltage ripple vs. the DC link capacitance value for the 600W H-Bridge microinverter (The y-axis is in logarithmic scale)

2.2.2. Input Capacitance Reduction Methods and Power Decoupling Control

2.2.2.1. Differential Microinverter Configurations

Generally, transistorless power decoupling techniques can be realize with any configuration that includes two capacitors in the AC output loop; because the location of decoupling the 2nd order power harmonic is in the two output capacitors instead of the classical DC-link capacitor. Therefore, any differential inverter or microinverter configuration is suitable to decouple the second order power ripples. Specifically,

differential inverters or microinverters are realized by connecting two elementary DC-DC converters differentially with the utility grid as in Figure 2.24.

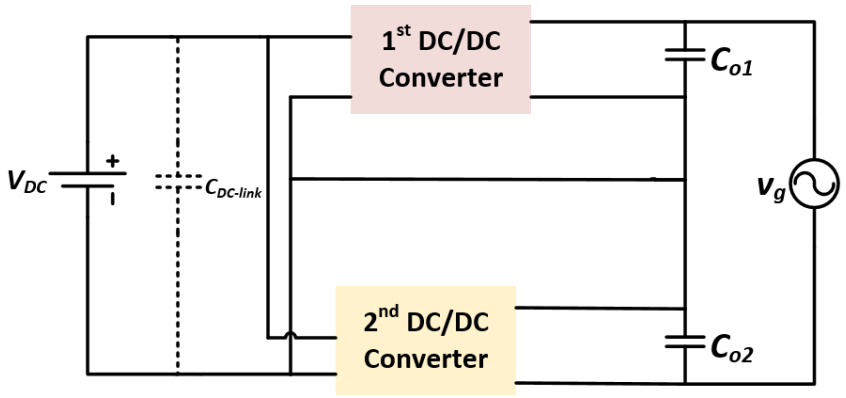
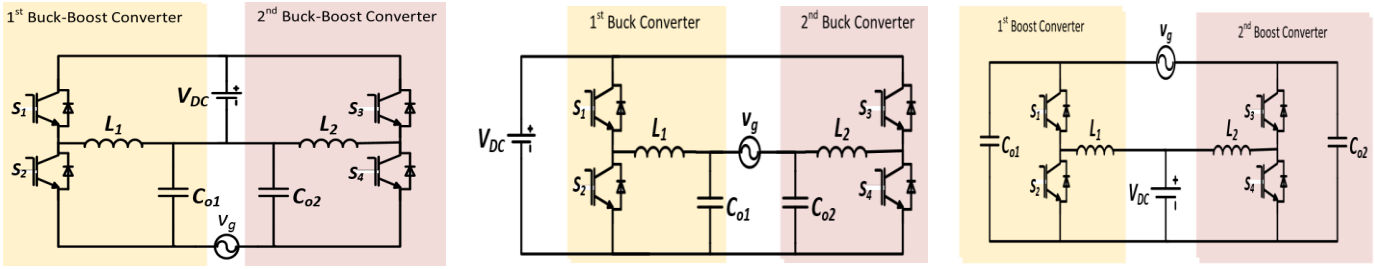


Figure 2.24: General differential microinverter configuration

And the existing differential microinverters are the following (Figure 2.25):



(a) (b) (c)

Figure 2.25: Existing differential microinverters: (a) Buck-Boost type, (b) Buck type and (c) Boost type

To illustrate how the power decoupling scheme works and how it reduces the input capacitance requirement. Investigation of the conventional differential Buck

microinverter (Figure 2.26) operation is discussed and then the power decoupling scheme is illustrated.

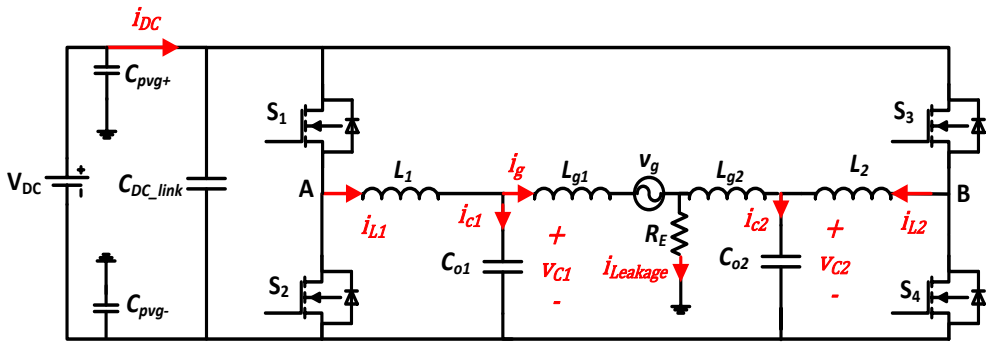


Figure 2.26: Differential Buck microinverter (with grid parasitic elements and the PV terminals stray capacitances)

2.2.2.2. Differential Buck Microinverter Operation

The task here is to find an expression for the instantaneous voltages across the two output capacitors and the instantaneous DC current drawn from the PV source. Therefore, applying KVL at the loop of the common coupling terminals of the microinverter with the grid as in Figure 2.27 will serve the purpose. Note that, $i_{Leakage}$ is at the switching frequency and it is very low; so it can be assumed to be zero in the analysis.

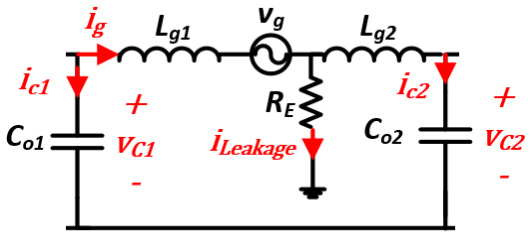


Figure 2.27: Microinverter point of common coupling with the grid loop

In normal operation, the KVL is in (2.17):

$$v_{c1} - v_{L_{g1}} - v_{L_{g2}} - v_g - v_{c2} = 0 \tag{2.17}$$

Since L_{g1} and L_{g2} are small; $v_{L_{g1}}$ and $v_{L_{g2}}$ are small compared to other voltages in (2.17) [73]. Therefore, (2.17) is approximated to be (2.18):

$$v_{c1} - v_g - v_{c2} = 0 \tag{2.18}$$

According to [73], [74], the voltages across the two output capacitors are given in (2.19) and (2.20):

$$v_{c1} = \frac{V_{DC}}{2} + \frac{v_g}{2} \tag{2.19}$$

$$v_{c2} = \frac{V_{DC}}{2} - \frac{v_g}{2} \tag{2.20}$$

Where v_g is equal to $V_g sin(2\pi f_o t)$ and V_{DC} is the DC-link voltage. Now to derive a term for the supplied DC current; knowing that the instantaneous input power is equal to the microinverter output loop power including the output capacitors instantaneous power as in (2.21):

$$p(t)_{c1} + p(t)_{c2} + p(t)_g = p(t)_{DC} \tag{2.21}$$

Therefore, the general term of the DC supplied current when $C_{o1}=C_{o2}=C$ and unity power factor is expressed in (2.22) [73], [74] :

$$i_{DC} = \frac{V_g I_g}{2V_{DC}} + \frac{V_g}{2V_{DC}} \sqrt{I_g^2 + \frac{1}{4}(2\pi f_o)^2 C^2 V_g^2}\, cos[2(2\pi f_o)t + \theta] \tag{2.22}$$

Where $\theta = tan^{-1}(\frac{\pi f_o C V_g}{I_g})$

Notice in (2.22), without any power decoupling control the supplied instantaneous current is composed of two frequencies: one at zero frequency and another term at $2f_o$. The second order ripple is the unwanted term – classically decoupled with large DC-link capacitors- and needed to be decoupled with control techniques.

2.2.2.3. Basic Power Decoupling Technique

The basic idea that can be applied to decouple the 2nd order power ripples is to force the instantaneous power on the two output capacitors to have a term that cancels out the double power ripples.

$$v_{c1} = \frac{V_{DC}}{2} + \frac{V_g sin(2\pi f_o t)}{2} + v_{inject} \tag{2.23}$$

$$v_{c2} = \frac{V_{DC}}{2} - \frac{V_g sin(2\pi f_o t)}{2} + v_{inject} \tag{2.24}$$

In other words, injecting voltages to the two filter capacitor as in (2.23) and (2.24) by circulating some CM current that satisfies the differential equation (2.25) would successfully decouple the power ripples.

$$v_{c1} C_{o1} \frac{dv_{c1}}{dt} + v_{c2} C_{o2} \frac{dv_{c2}}{dt} = -\frac{V_g I_g}{2} cos(2(2\pi f_o)t) \tag{2.25}$$

(2.25) is solved theoretically in the literature when $C_{o1}=C_{o2}=C$ and v_{inject} have the form of (2.26) after compensating the 2nd order power ripples [63].

$$v_{inject} = \sqrt{-\frac{V_g I_g}{8\pi f_o C} sin(2(2\pi f_o)t) - \frac{V_g^2}{8} cos(2(2\pi f_o)t) - \frac{V_g^2}{8} + A} - \frac{V_{DC}}{2} \qquad (2.26)$$

Where A is an arbitrary constant that makes the term under the root to be positive. However, the solution obtained for v_{inject} has not only second order harmonics but also multiple even harmonics. Meaning that, compensating the 2nd order power ripples results in injecting extra unwanted higher order even harmonics [73].

2.2.3. Power Decoupling Schemes in Differential Microinverters

Even though, the theoretical transistorless power decoupling analysis seems to be straightforward. However, the application of this methodology faces multiple issues and many factors need to be considered. For instance, there is a limitation on the two output capacitors voltage that depends on the differential microinverter topology as in (Table 2.1). In addition, some proposed controls in the literature to mitigate the power ripples use capacitors voltage reference estimation that makes the control scheme rely highly on the system parameters and not autonomous, such as, the control scheme proposed in [75]. Another author suggested a control scheme that is autonomous based only by forcing the high frequency contents of the supplied DC current to be zero [76]

Table 2.1: The two output capacitors voltage limitation with different configurations

Capacitors output voltage limitation	Inverter type
$0 < v_{c1} < V_{DC}$ $0 < v_{c2} < V_{DC}$	Buck
$0 < v_{c1}$ $0 < v_{c2}$	Buck-Boost
$V_{DC} < v_{c1}$ $V_{DC} < v_{c2}$	Boost

However, they overlooked the nonlinearities in the DC current loop this makes their method unreliable with Boost type or Buck-Boost type [77]. Also, the control scheme purposed in [63] depends highly on estimating the inductors current of the two buck converters. Figure 2.28 shows two of the proposed power decoupling control schemes from the literature. Both control schemes shown in Figure 2.28 estimate two duty cycles to inject a sinusoidal current into the grid and eliminate the power ripples. Specifically, the addition of the Differential Mode duty cycle (d_{DM}) to the Common Mode duty cycle (d_{CM}) gives the duty cycle of the first converter (S_1 & S_2). On the other hand, the subtraction of d_{DM} from d_{CM} gives the duty cycle of the second converter (S_3 & S_4). Note that the duty cycles here are sinusoidal references. The modification of the control (Figure 2.28 (a)) compared to (Figure 2.28 (b)) is that the CM duty-cycle is estimated using the ripples of the DC supply current. Specifically, forcing the ripple content of the DC supply current to be zero with Proportional Resonance (PR) controllers. These PR controllers are tuned at at $2f_o$ and $4f_o$.

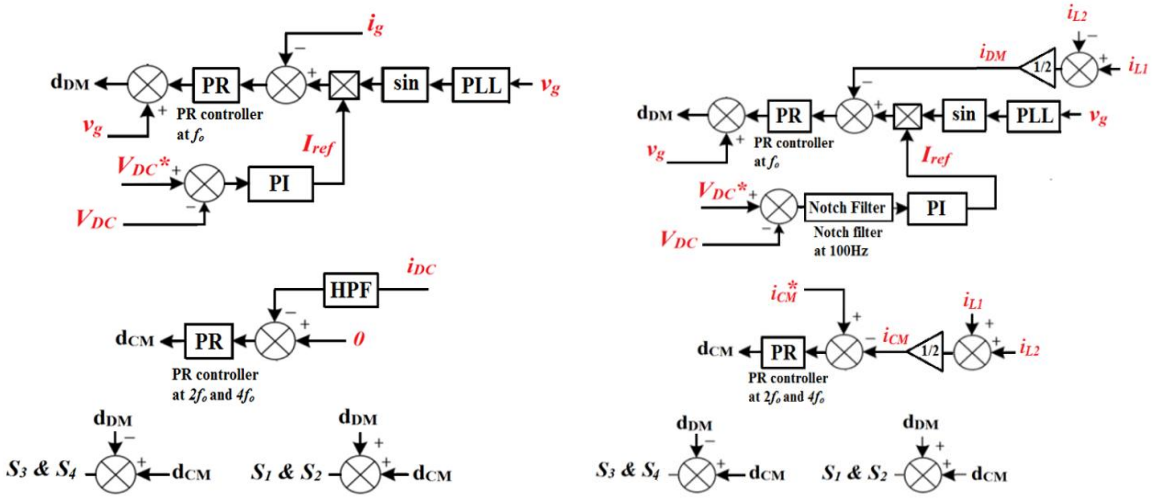


Figure 2.28: Existing transistorless power decoupling control schemes: (a) autonomous control scheme [77], and (b) non-autonomous control scheme [63]

The benefit of the controller (Figure 2.28 (a)) is that the ripple content of DC supply current reference is zero; consequently, no complex calculation needed to estimate the reference for the CM controller. On the other hand, the CM controller in Figure 2.28 (b) needs to compute the required CM current reference after estimating the required CM injected voltage to the two output capacitors with equation (2.26). However, the control scheme in Figure 2.28 (a) needs complex feedback linearization in case it was used with the differential Boost type or Buck-Boost type. Nevertheless, both control schemes must be modified when considering realistic mismatch between the two output capacitors. In other words, if the two output capacitors have different capacitances the control scheme needs to be adjusted. Fortunately, paper [78] analyzed the power decoupling control in Figure 2.28 (a) for a differential Buck inverter with intentional mismatch between the two

output capacitors; they suggested that both the CM and the DM PR controllers must be tuned at f_o, $2f_o$, $3f_o$ and $4f_o$ would successfully decouple the 2nd order harmonic power ripples. Notice in Figure 2.28 the grid voltage is feedforwarded after the f_o PR controller; the purpose of the feedforward is to treat the grid voltage as a disturbance and improve the control scheme stability in case the inverter is connected to a weak-grid [79].

Chapter 3 : Comparison Study

In this chapter, a comparison study will be conducted to evaluate the performance of the different existing microinverter configurations regarding two aspects: (i) the amount of the circulating leakage current and (ii) the possibility to decouple transisorlessly- without any additional semiconductor switches and energy storage devices- the 2nd order power ripples. The comparison is based on PSIM software with these parameters shown in Table 3.1.

Table 3.1 Parameters used in the study of the leakage current

V_{DC}`	V_g		f_o	f_s
$120\sqrt{2}$ V	120 Vrms		50 Hz	16 kHz
$C_{pvg-}=C_{pvg+}$	$C_{bus}= C_{DC-Link}$	C_o*	$L_1=L_2$	P_o
1.5 nF	3 mF	60 μF	0.85 mH	600 W

*LC common mode current elimination filter $C_o/2= C_{o1}= C_{o2}$

3.1. Conventional Configuration with Different PWM Schemes Simulation

As expected in the literature review, the simulation of the conventional 4-Switch microinverter configuration with the different PWM schemes (Figure 2.5) in PSIM; showed that the bipolar modulation (Figure 2.5 (b)) has low leakage current circulation but as discussed earlier that it possess very high losses. Also, the size of the filter is large because the ripples in the output current are around f_s and not $2f_s$ as in any unipolar modulation. On the other hand, all unipolar modulations (Figure 2.5 (c), (d) and (e))

leakage current is large. Unipolar modulation deteriorates the CM performance of the system and causes a large amount of leakage current circulation because of the zero level voltage in the microinverter unfiltered output. Figure 3.1 shows the circulation leakage current of the different PWM schemes with the 4-Switch microinverter:

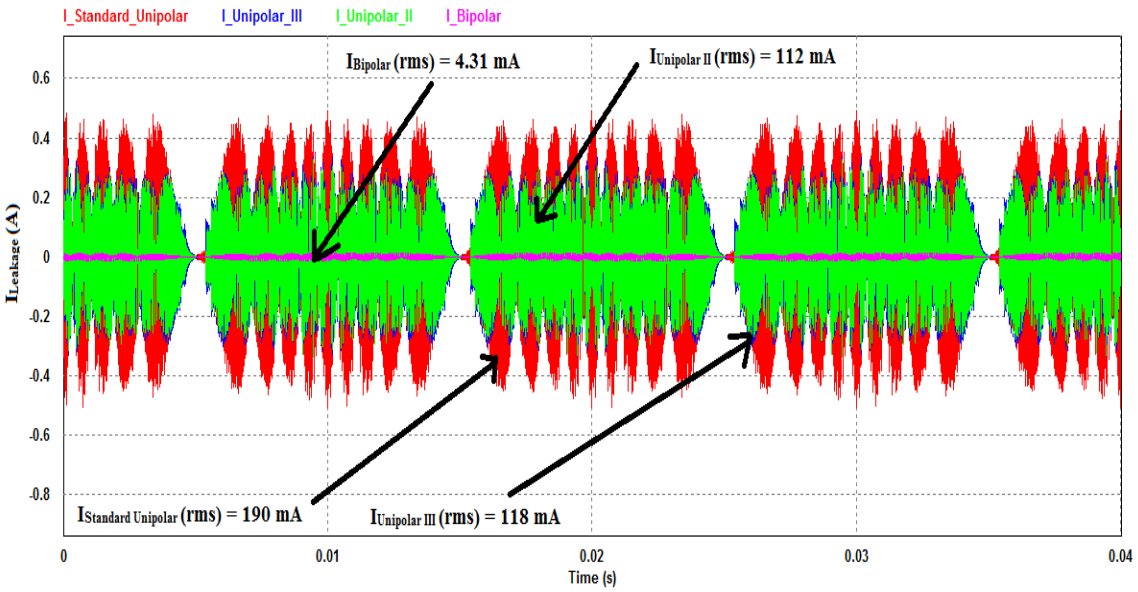


Figure 3.1: Existing 4-Switch microinverters leakage current with different PWMs in PSIM

3.2. DC-Based Decoupling Network Type Simulation

The leakage current reduction with DC decoupling network micrionverters (Figure 2.8 and Figure 2.9) is based on disconnection the parasitic capacitance from the microinverter during the zero level voltage generation. Nonetheless, it turns out that it is not enough to eliminate the leakage current completely because of the transistor junction capacitance resonance phenomena. Hence, NPC types were introduced (Figure 2.12). As expected the leakage current with H5 and H6 is reduced compared to the unipolar

modulation but their NPC configuration reduces the leakage current significantly (Figure 3.2). However, the conduction losses are high because in three of these configuration since four switches are in conduction mode.

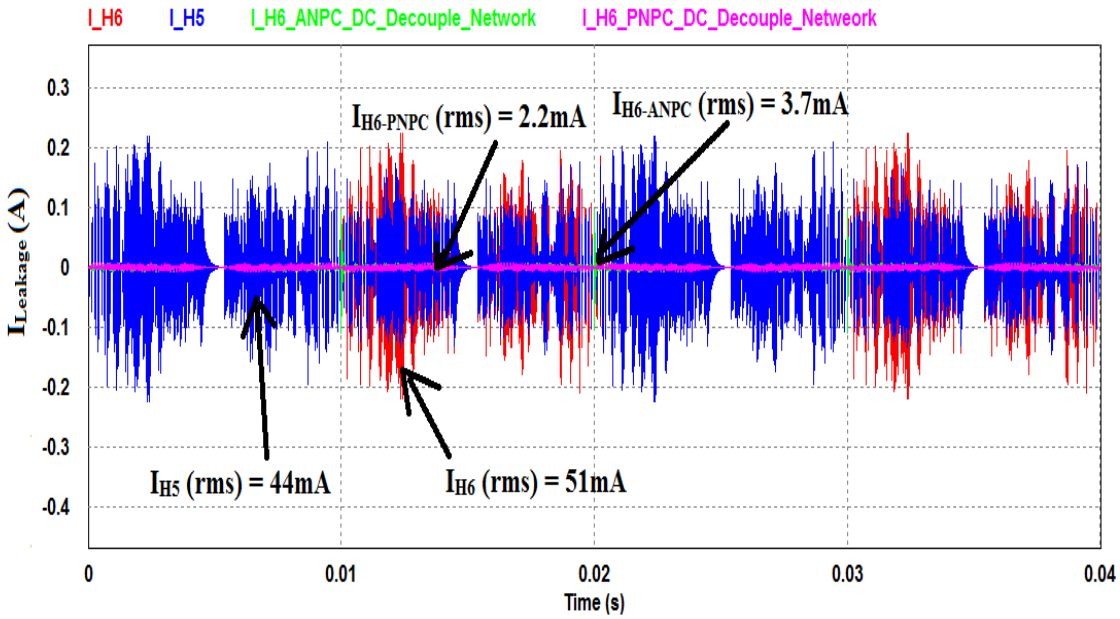


Figure 3.2: Leakage current generated by different DC-decoupling network microinverters

3.3. AC-Based Decoupling Network Type Simulation

The AC decoupling network topologies reduce the leakage current by disconnecting the microinverter from the PV source during the zero voltage level generation at the AC side. These topologies (Figure 2.14) often called HERIC because of its high efficiency compared to the DC type since 2 switches are maximally in conduction state during all the operation modes. However, the lacked the ability to eliminate the leakage current due

to transistor capacitance resonance; thus, NPC types were introduced (Figure 2.16). The leakage current RMS value is less than 2.5mA with the HERIC NPCs (Figure 3.3)

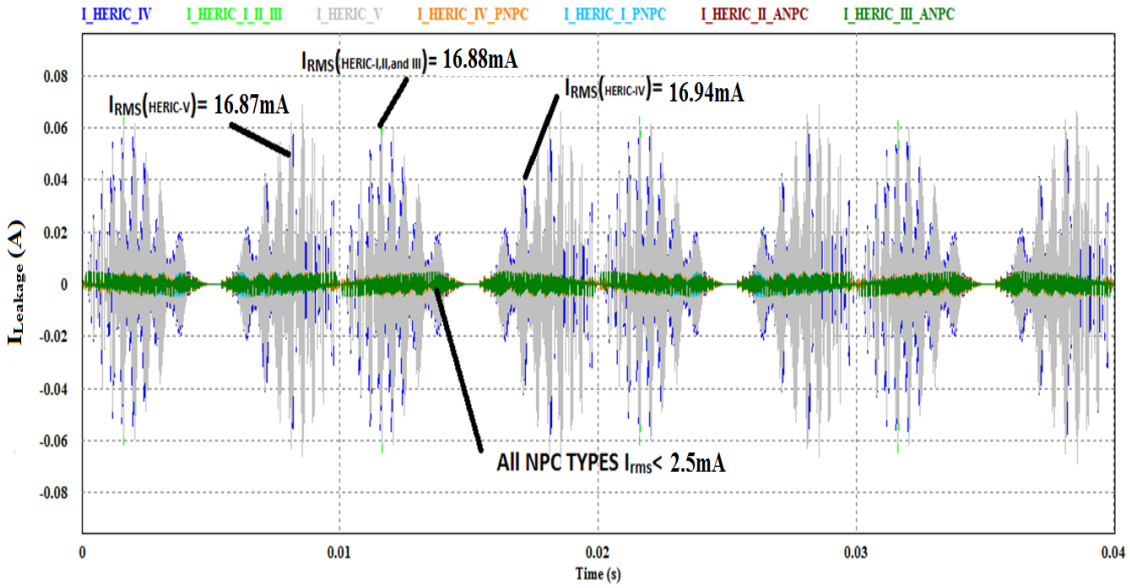


Figure 3.3: Leakage current generated by different HERIC (AC decoupling network) microinverters

3.4. LC CM Filter Simulation

This method does not require any extra active switches to reduce the leakage current. Here the CM current is bypassed and circulates back to the negative terminal of the microinverter making the amount of the leakage current insignificant. The simulation showed a significant reduction in the circulation leakage current less than 1mA as in Figure 3.4.

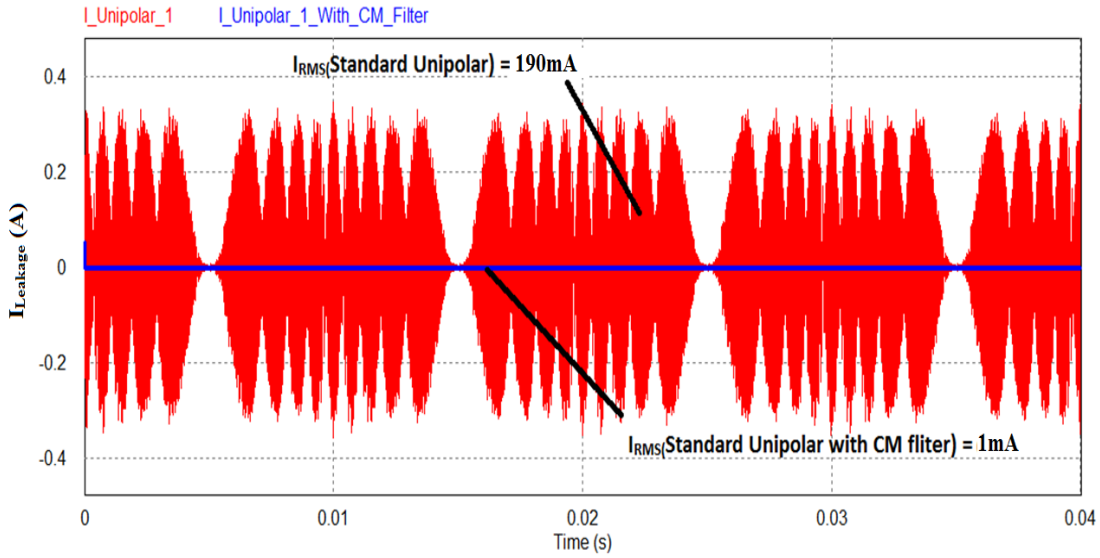


Figure 3.4: Leakage current with LC CM passive filter compared to the conventional H-bridge microinverter with standard unipolar modulation

3.5. Comparison Study Conclusion

The CM operation of the different transformerless microinverter topologies simulated with PSIM software under the same technical and loading conditions showed that the family of NPC microinverters has the lowest leakage current circulation. Even though the bipolar microinverter has very small leakage current, it is not practical to use since its output exhibits high filtering requirements and high losses. Additionally, the methods to reduce the leakage current are classified into DC-decoupling networks, AC-decoupling networks, and CM current filtering. It was found that the AC decoupling networks (HERIC) possess lower losses. Therefore, the best performing microinverters regarding leakage current reduction and efficient operation are the HERIC NPC types. Figure 3.5

shows the vast differences between various topologies' leakage current RMS values simulated under exactly the same technical and loading conditions (Table 3.1).

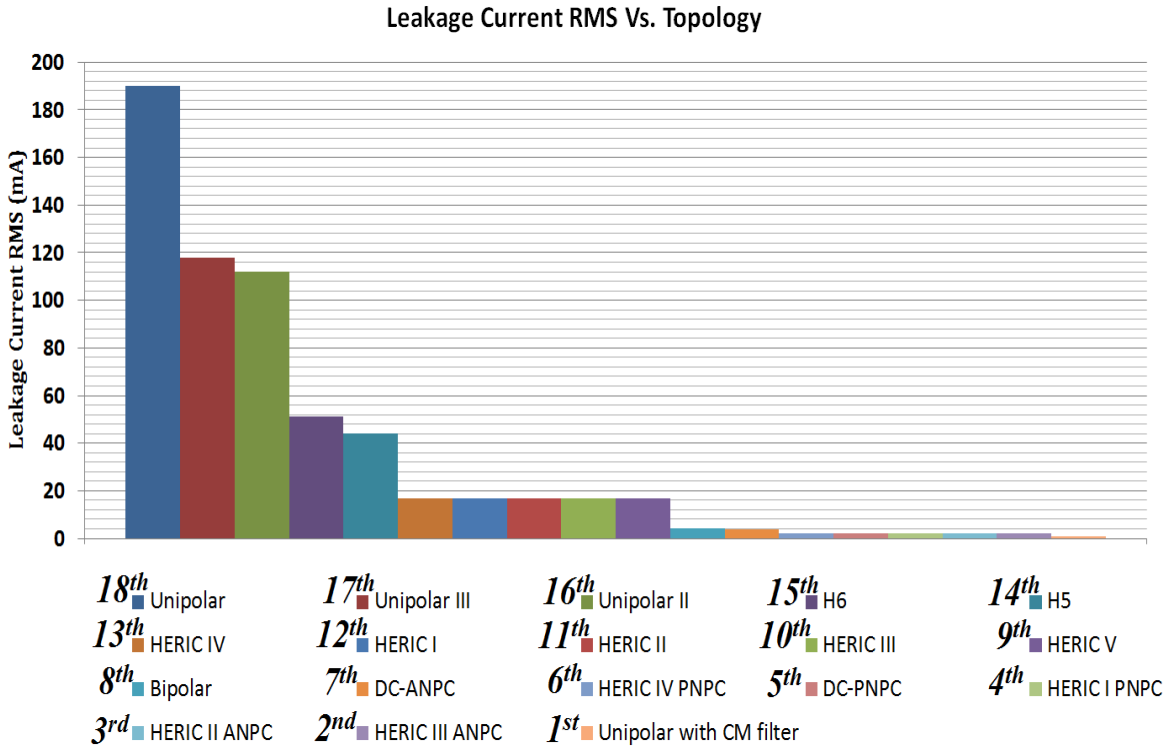


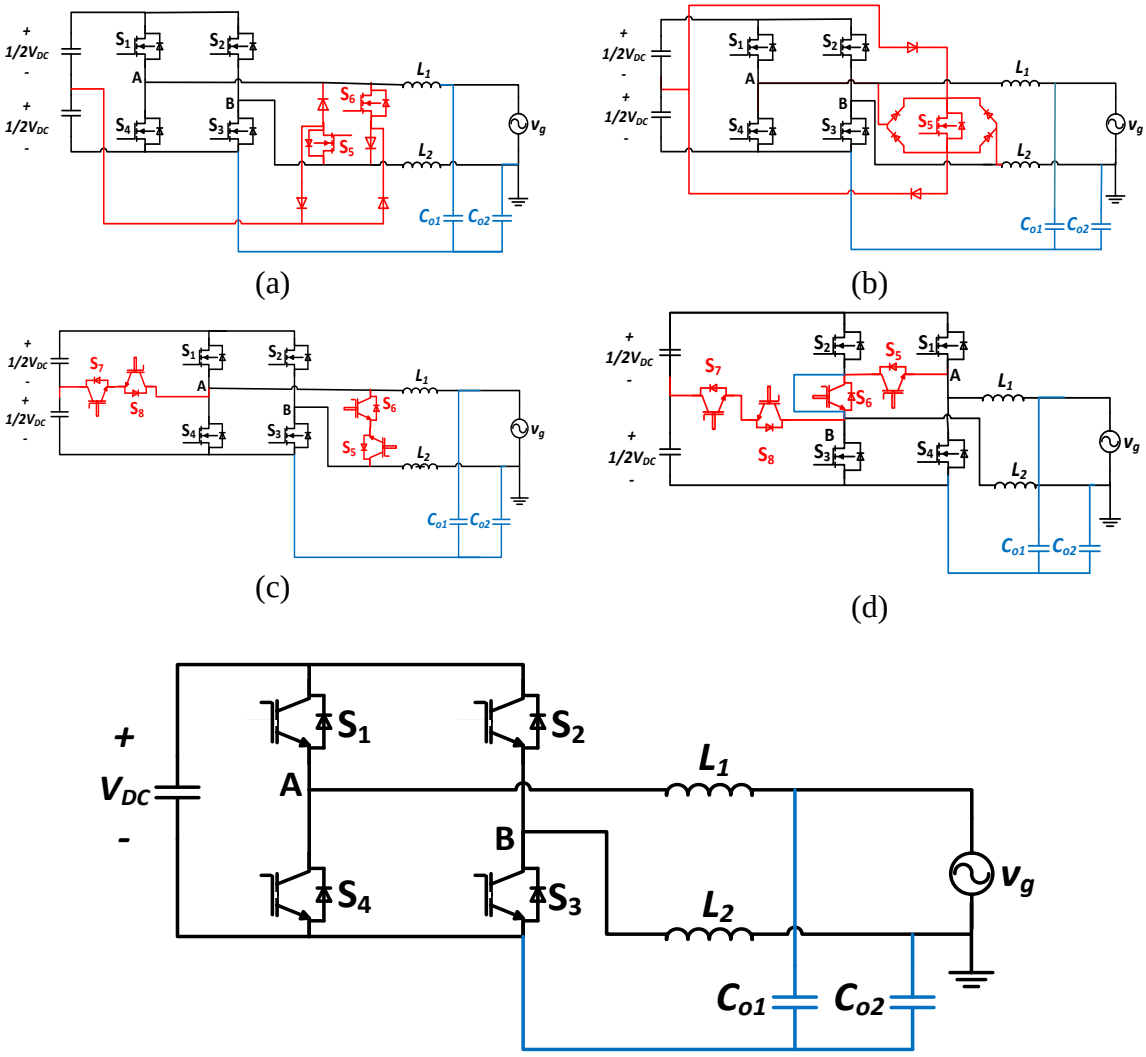
Figure 3.5: Ranking of topologies based on their leakage current RMS values

Even though the leakage current reduction methods using active circuitry are found to be useful, their operation under non-unity power factor is problematic. In other words, injecting or absorbing reactive power to or from the grid is difficult due to their control strategy. However, the most recent results obtained using the special LC filter to reduce the ground leaking current provided the lowest leakage current circulation with the noisiest type of modulation while reactive power flow control is also possible.

Specifically, the leakage current can reach values below 1mA with the LC CM current bypass filter.

3.6. Topology Modification to Eliminate the Power Ripples

As mentioned earlier, any configuration that includes two capacitors in the AC output loop could decouple the 2nd order power ripples transistorlessly. In addition, since the results of the simulation showed that HERIC NPCs are the best regarding the leakage current mitigation; modifying their configuration to make the configuration able to decouple the power pulsation transistorlessly possible would be beneficial. However, modifying their output filter so transistorless power decoupling techniques can be applicable would be useless; since the extra two capacitors that must be placed to decouple the pulsating power would also deviate the most of CM current from the ground leaking loop and all HERIC NPCs would transform to a configuration similar to the differential buck microinverter after cancelling the useless bidirectional switch between point A and B and the clamping cell (Figure 3.6). In other words, the power decoupling capacitors addition to the HERIC NPCs or even the DC-based NPCs transforms the microinverter to the differential buck configuration that is discussed in details in subsection 2.2.2. Moreover, the differential buck would be the best choice to decouple the power pulsation and reduce the circulating leakage current.



Equivalent of (a), (b), (c) and (d)

Figure 3.6: Power decoupling output capacitors addition to the HERIC NPC types and its equivalent configuration

Chapter 4 : Design Methodology

The evaluation of the different configurations based on the simulation showed that the differential buck microinverter has the lowest leakage current circulation and it is capable of decoupling the second order power ripples with the minimum number of switches. However, power decoupling scheme of this configuration is well discussed in [63], [64], [76], [77], [78] but with LC output filter and without resonance damping consideration. Thus, this thesis the leakage current and the switchless power decoupling techniques in differential buck microinverter are explored with these two control schemes:

i) passive resonance damping and

ii) active resonance damping.

The differential buck configuration is selected because autonomous power decoupling scheme with the differential boost or buck-boost needs complex feedback linearization [77]. Also, any other differential configuration such as Cuk or SEPIC makes the system order high and complicated. Besides, when the grid side parasitic inductance is considered the differential buck can be viewed as an unstable LCL filter because of the resonance peak [79]. Figure 4.1 shows the differential buck configuration with LCL filter used in this study and Table 4.1 indicates the rating of the configuration and the utility grid type.

Table 4.1: Parameters used in the modeling and design stage

V_{DC}	v_g	f_o	f_s	P_o
400 V	240 V_{RMS}	50 Hz	30 kHz	600 W

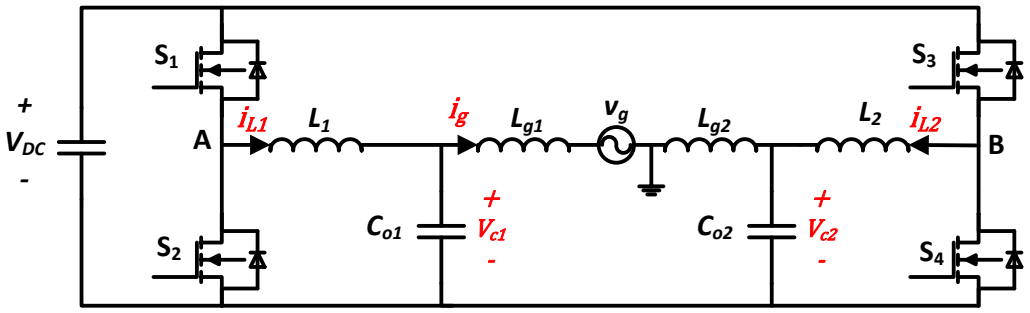


Figure 4.1. The differential buck configuration with LCL filter

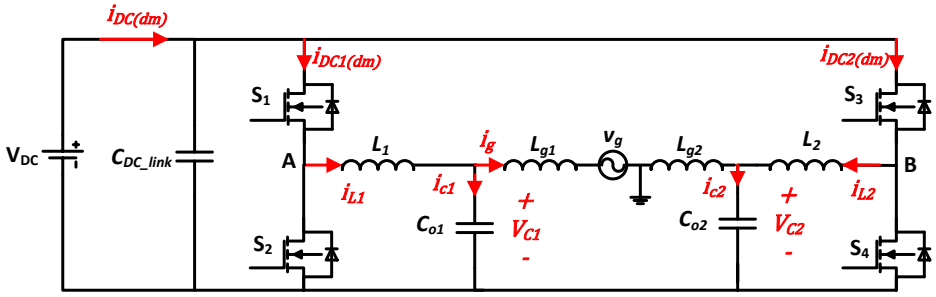
Chapter 5 : Modelling and Microinverter Control

This chapter is divided into two sections: (i) Differential buck with passive resonance damping control and (ii) Differential buck with active resonance damping control. Each controller is composed of an outer voltage regulation loop and two inner parallel loops to decouple the power ripples and inject a sinusoidal current into the grid. However, there will be no elaboration regarding the outer voltage regulation loop since it is elementary and could be regulated with simple PI controller as suggested in [80]. Similarly, there will be no elaboration on single phase PLL as it is well described in [81].

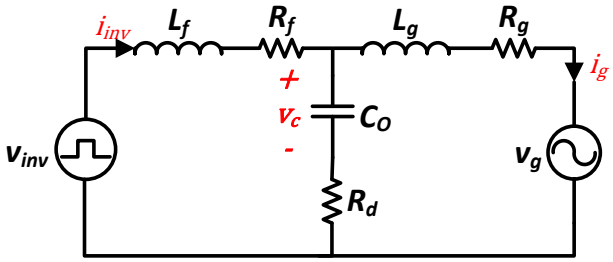
5.1. Differential Buck with LCL Passive Resonance Damper

5.1.1. Filter Design

In the differential mode (DM) the symmetrical LCL filter with the differential buck configuration (Figure 4.1) can be redrawn to show the detailed DM model as Figure 5.1. Also, the parameters in Figure 5.1 (b) are derived as shown in Table 5.1.



(a)



(b)

Figure 5.1: Differential Buck LCL filter equivalent circuit in the DM: (a) detailed DM model and (b) simplified model

Table 5.1: Differential Buck with LCL equivalent parameters in the DM

Parameters	
$L_f = L_1 + L_2$	$C_o = \frac{C_{o1}\, C_{o2}}{C_{o1} + C_{o2}}$
$R_f = R_{L_1} + R_{L_2}$	$R_d^* = R_{C_{o1}} + R_{C_{o2}} + R_{Damping}$
$L_g = L_{g1} + L_{g2}$	$i_{inv} = \frac{i_{L_1} - i_{L_2}}{2}$ and i_g
$R_g = R_{L_{g1}} + R_{L_{g2}}$	$v_{inv} = v_{AB} = v_A - v_B$ and $v_C = v_{c_1} - v_{c_2}$

*R_d includes the ESR of the two capacitors and additional damping resistor that could be added to avoid the resonance phenomena with LCL filters

Applying superposition principle; two transfer functions exist for the injected grid current, i_g. Specifically, the transfer function $G_1(s) = \frac{i_g(s)}{v_{inv}(s)}$ is given in (5.1) and the transfer function $G_2(s) = \frac{i_g(s)}{v_g(s)}$ is given in (5.2).

$$G_1(s) = \frac{i_g(s)}{v_{inv}(s)} = \frac{i_{inv}(s)}{v_{inv}(s)} \frac{i_g(s)}{i_{inv}(s)} \quad \text{when } v_g(s) = 0$$
$$= \frac{sC_oR_d + 1}{s^3C_oL_fL_g + s^2C_o(L_fR_d + L_gR_d + L_fR_g + L_gR_f) + s(L_f + L_g + C_oR_dR_f + C_oR_dR_g + C_oR_fR_g) + R_f + R_g} \tag{5.1}$$

$$G_2(s) = \frac{i_g(s)}{v_g(s)} = -\frac{1}{Z_{Total}} \quad \text{when } v_{inv}(s) = 0$$
$$= -\frac{s^2L_fC_o + sC_o(R_d + R_f) + 1}{s^3C_oL_fL_g + s^2C_o(L_fR_d + L_gR_d + L_fR_g + L_gR_f) + s(L_f + L_g + C_oR_dR_f + C_oR_dR_g + C_oR_fR_g) + R_f + R_g} \tag{5.2}$$

From (5.1) and (5.2) it is obvious that the grid current (i_g) depends on the microinverter output voltage (v_{inv}) and the grid voltage (v_g). Nevertheless, grid connection standards allow harmonic distortion introduced by the grid voltage. As a result, the LCL filter design considers only (5.1) as the filter transfer function. Also, the filter must attenuate the first switching harmonic that appears in the grid current spectrum to less than 0.3% of the rated current. Precisely, the first switching harmonics that appears in the grid current is $2m_f - 1$ because it is a unipolar modulation; where $m_f = \frac{f_{sw}}{f_o}$ is the frequency modulation index. The consideration that must be taken into account when designing the LCL filter can be summarized in the flowchart in Figure 5.2 based on the guideline provided in [82], [83]:

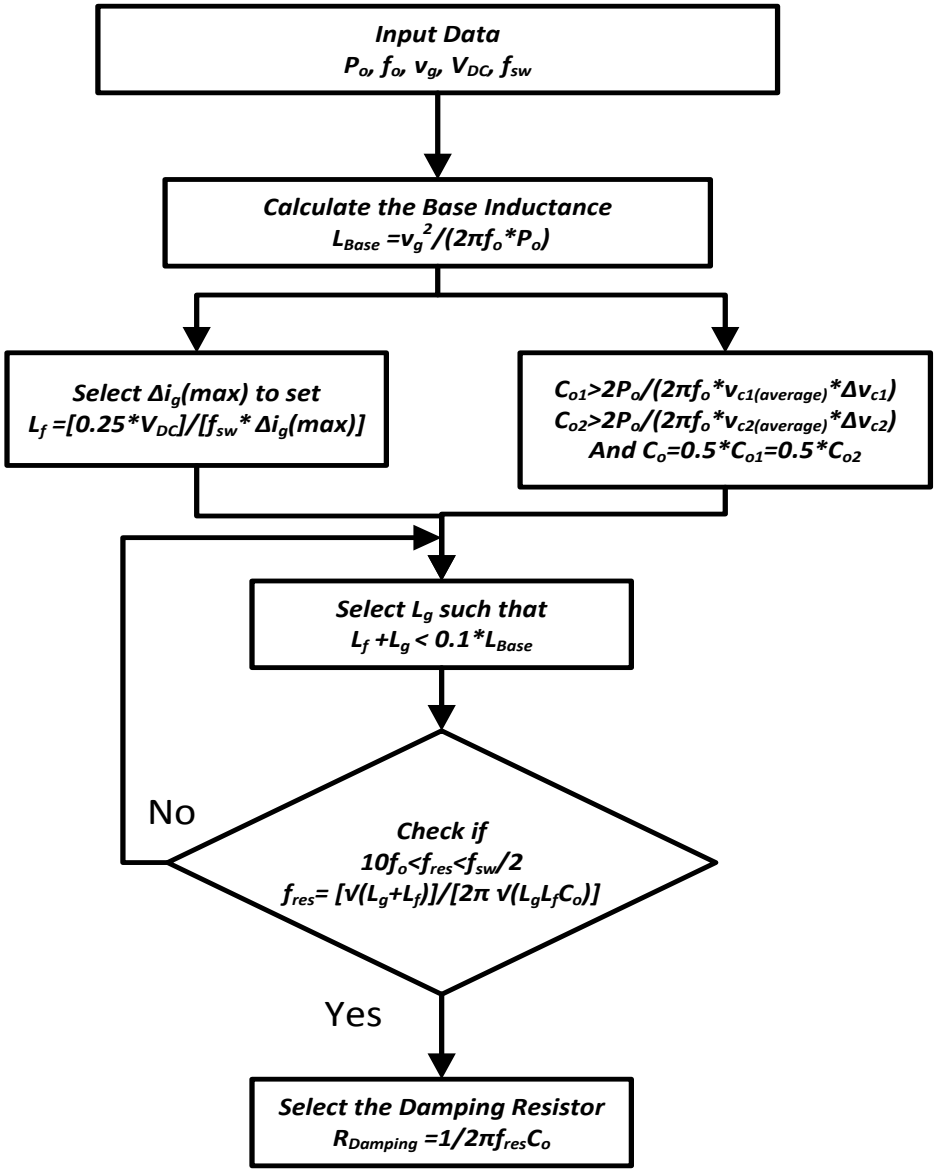


Figure 5.2: Flowchart for LCL filter with Differential buck parameters selection

Figure 5.2 is slightly modified compared to the conventional LCL filter flowchart of [82], [83]; specifically, the selection of the output capacitor C_o is based on the minimum allowable ripples in the two output split capacitors C_{o1} and C_{o2}. The average

voltage of the two capacitors is $V_{C1(average)} = V_{C2(average)} = \frac{1}{2}V_{DC}$ and the minimum ripple is equal to $\Delta V_{C1} = \Delta V_{C2} = V_{DC}$ so power decoupling can be achieved successfully. Moreover, Table 5.2 summarizes the overall LCL filter parameters that are selected.

Table 5.2: Selected LCL filter Parameters

$L_f = L_1 + L_2$	$L_g = L_{g1} + L_{g2}$	$C_o = C_{o1}/2 = C_{o2}/2$	$R_g = R_{g1} + R_{g2}$	$R_f = R_{L1} + R_{L2}$	$R_d = R_{co1} + R_{co2} + R_{damping}$
2mH	0.1mH	60uF	24mΩ	26mΩ	3.4mΩ +0.8Ω

Note these values are selected based on actual existing components; each component datasheet is attached in the appendix.

5.1.2. Controllers Design

The microinverter is controlled through 3 controllers: DM controller to inject a sinusoidal current into the grid, CM controller to decouple the 2nd order power harmonics at the AC side and DC-bus voltage regulation controller that estimates the reference current. However, PLL and DC-bus regulation are not discussed. Therefore, this section is divided into three subsections (i) DM controller, (ii) CM controller and (iii) Overall control.

5.1.2.1. DM controller

Prior to the design of the DM loop compensator; the plant model of the microinverter in the differential mode must be derived. Combining (5.1) and (5.2) gives the expression in (5.3) for the injected grid current in the Laplace domain.

$$i_g(s) = G_1(s)v_{inv}(s) + G_2(s)v_g(s)$$

$$i_g(s) = G_1(s)\left[v_{inv}(s) - v_g(s)\,\frac{s^2L_fC_o + sC_o(R_d + R_f) + 1}{sC_oR_d + 1}\right] \quad (5.3)$$

Since the magnitude of the term $\frac{s^2L_fC_o+sC_o(R_d+R_f)+1}{sC_oR_d+1}$ is unity and its phase is zero at $s=j2\pi f_o$ the extra term that is multiplied by the grid voltage can be approximated to be 1. As a result, the grid current equation (5.3) can be approximated as in (5.4):

$$i_g(s) \approx G_1(s)[v_{inv}(s) - v_g(s)] \quad (5.4)$$

Then, the DM controller block diagram is shown in Figure 5.3

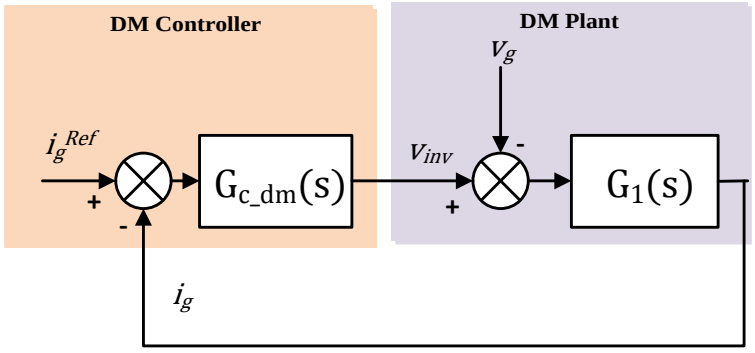


Figure 5.3: DM controller and the microinverter DM plant

Since the current injected into the grid is sinusoidal; PI controllers are incapable of tracking sinusoidal references without steady state errors [84], [85]. Nonetheless, Proportional Resonance (PR) controllers are introduced to track non-DC components efficiently since they produce an infinite gain at a specific resonance frequency [84], [85]. The transfer function of the PR controller is shown in (5.5).

$$G_{PR}(s) = k_P + k_R \frac{s}{s^2 + (2\pi f_o)^2} \quad (5.5)$$

Where k_p is the proportional gain, k_R is the resonance gain and f_o is the nominal grid frequency. Note that in (5.5) only one resonance controller gain is considered and the addition of extra resonance controllers at different frequencies such as 3rd or 5th harmonic is possible to eliminate these harmonics [81]. Nevertheless, the ideal PR controller (5.5) causes instability because of its infinite gain and infinite bandwidth [86]; therefore, non-ideal PR controllers are adopted as in (5.6):

$$G_{c\_dm}(s) = G_{PR\,(non-ideal)}(s) = k_{P_{dm}} + k_{R_{dm}} \frac{s}{s^2 + 2\zeta(2\pi f_o)\, s + (2\pi f_o)^2} \quad (5.6)$$

Where ζ sets the bandwidth around the AC fundamental frequency usually set to be 0.001 [86]. Also, the non-ideal PR controller is realizable by digital systems [84].

Simple manipulation could be done to derive the closed loop transfer function of the system in Figure 5.3 and show how to avoid grid voltage feedforward. Specifically, modifying the system in Figure 5.3 to be as in Figure 5.4 shows that the grid current is expressed as in (5.7):

$$i_g(s) = i_g^{Ref}(s) \frac{G_{c\_dm}(s) G_1(s)}{1 + G_{c\_dm}(s) G_1(s)} - v_g(s) \frac{1}{G_{c\_dm}(s)} \quad (5.7)$$

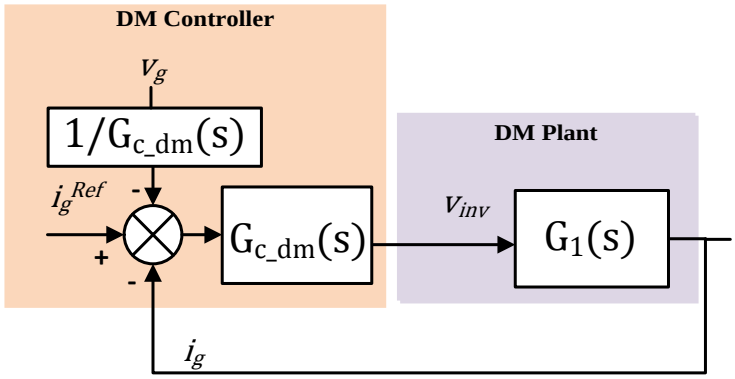


Figure 5.4: Modified DM control

Now if the controller gain $G_{c\_dm}(s)$ is infinity at the fundamental the term that is multiplied by $i_g^{Ref}(s)$ $(\frac{G_{c\_dm}(s)G_1(s)}{1+G_{c\_dm}(s)G_1(s)})$ will reach 1. On the other hand, the grid voltage disturbance multiplication term $\frac{1}{G_{c\_dm}(s)}$ will reach zero and (5.7) will be as (5.8) in case of high controller gain:

$$i_g(s) = i_g^{Ref}(s) \tag{5.8}$$

In other words, the grid voltage feedforward is not necessary and it is neglected. The PR compensator parameters can be obtained using (5.9):

$$T(s) = G_{c\_dm}(s)G_1(s) = \left(K_{P_{dm}} + k_{R_{dm}(f_o)}\frac{s}{s^2 + 2\zeta(2\pi f_o)\,s + (2\pi f_o)^2}\right) * \left(\frac{sC_oR_d + 1}{s^3C_oL_fL_g + s^2C_o(L_fR_d + L_gR_d + L_fR_g + L_gR_f) + s(L_f + L_g + C_oR_dR_f + C_oR_dR_g + C_oR_fR_g) + R_f + R_g}\right) \tag{5.9}$$

Table 5.3 indicate the controller gain to yield -180^o phase margin and unity gain

Table 5.3: PR compensator parameters

$K_{P_{dm}}$	$k_{R_{dm}(f_o)}$	ζ^*
3	20000	0.001

*Non-ideal PR controller factor [86]

5.1.2.2. CM controller

As discussed in the literature review section that the CM controller works independently from the DM controller. This can be illustrated by observing the DM voltage and the CM voltage on the two capacitors C_{o1} and C_{o2} of Figure 4.1 (a) as in (5.10) and (5.11):

$$\begin{aligned} v_{C1}(t) - v_{C2}(t) &= \left[\frac{V_{DC}}{2} + \frac{V_{DC}}{2}(d_{cm} + d_{dm})\right] - \left[\frac{V_{DC}}{2} + \frac{V_{DC}}{2}(d_{cm} - d_{dm})\right] = d_{dm}V_{DC} \\ &= (L_{g1} + L_{g2})\frac{di_g}{dt} + v_g(t) \end{aligned} \tag{5.10}$$

$$v_{C1}(t) + v_{C2}(t) = \left[\frac{V_{DC}}{2} + \frac{V_{DC}}{2}(d_{cm} + d_{dm})\right] + \left[\frac{V_{DC}}{2} + \frac{V_{DC}}{2}(d_{cm} - d_{dm})\right] = V_{DC} + d_{cm}V_{DC} \tag{5.11}$$

Notice that the differential voltage (5.10) does not contain the CM duty cycle (d_{cm}). In other words, the grid current is not affected by the CM duty cycle. In addition, the CM voltage does not contain any information about the DM duty cycle (d_{dm}) and the term $d_{cm}V_{DC}$ in (5.11) is used to create ripples opposite to the ripples in the DC-link capacitor. The DM duty cycle (d_{dm}) is obtained in the previous subsection with the PR controller. In this subsection, illustration of the CM controller will be explored. Prior to designing the CM loop compensator the plant of the microinverter in the CM must be developed. Using (5.11) the microinverter CM equivalent circuit of Figure 4.1 can be visualized as follows (Figure 5.5)

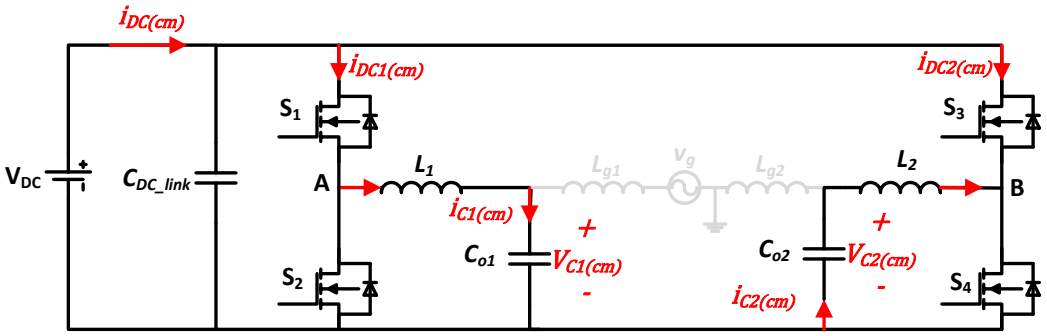


Figure 5.5: CM equivalent circuit of the differential buck microinverter

Deriving an expression for the supply DC current is mandatory to obtain the plant of the CM controller. Each microinverter leg is viewed and a separate buck converter that is connected differentially to the grid. Therefore, the sum of the DC currents flowing in each leg of the microinverter gives the supply current (i_{DC}) drawn from the PV as (5.12):

$$\begin{aligned} i_{DC1}(s) &= (d_{cm} + d_{dm})\, i_{L1}(s) = (d_{cm} + d_{dm})\left(i_g(s) + sC_{o1}v_{c1}(s)\right) \\ i_{DC2}(s) &= (d_{cm} - d_{dm})\, i_{L2}(s) = (d_{cm} - d_{dm})\left(-i_g(s) + sC_{o2}v_{c2}(s)\right) \\ i_{DC}(s) &= i_{DC1}(s) + i_{DC2}(s) \end{aligned} \tag{5.12}$$

Note that the inductor currents are related to the grid current and the capacitor current by applying KCL at the two point of the common coupling with the grid. Further manipulation of (5.12) results in (5.13)

$$i_{DC}(s) = [2i_g(s) + sC(v_{c1}(s) - v_{c2}(s))]d_{dm} + sC(v_{c1}(s) - v_{c2}(s))d_{cm} \tag{5.13}$$

Note that the expression in (5.13) is derived using identical capacitors (C_{o1}=C_{o2}=C). Now relating the expression in (5.13) to the capacitors CM voltage and the DM voltage can be achieved by inserting (5.14) and (5.15) in (5.13)

$$v_{c_{cm}}(s) = \frac{v_{c1}(s) + v_{c2}(s)}{2} \tag{5.14}$$

$$v_{c_{dm}}(s) = \frac{v_{c1}(s) - v_{c2}(s)}{2} \tag{5.15}$$

The DC source current relation with the capacitors CM and DM voltages is expressed in (5.16).

$$i_{DC}(s) = [2i_g(s) + s2Cv_{c_{dm}}(s)]d_{dm} + [s2Cv_{c_{cm}}(s)]d_{cm} \tag{5.16}$$

(5.16) can be further simplified by relating the CM and DM voltages to the capacitors CM and DM current as in equation (5.17)

$$i_{DC} = \left[2i_g(s) + 2i_{c_{dm}}(s)\right]d_{dm} + [2i_{c_{cm}}(s)]d_{cm} \tag{5.17}$$

(5.17) indicates that the DC supply current is affected by the CM and the DM duty cycles and it can be decomposed to two currents (5.18)

$$i_{DC_{dm}}(s) = \left[2i_g(s) + 2i_{c_{dm}}(s)\right]d_{dm}$$

$$i_{DC_{cm}}(s) = [2i_{c_{cm}}(s)]d_{cm} \tag{5.18}$$

$$i_{DC} = i_{DC_{dm}}(s) + i_{DC_{cm}}(s)$$

The term that is due to the DM in (5.17) can be treated as a disturbance. However, there is a huge issue with this expression since the relation between the supply DC current and the CM duty cycle is non-linear due the multiplication with the capacitor CM current $i_{c_{cm}}(s)$. Typical solution to solve the non-linearity in the CM plant model is to linearize the model by multiplying it the inverse of the non-linear term prior the plant model as in (Figure 5.6). In other words, the CM controller is composed of a PR controller tuned at $2f_o$ and $4f_o$, a feedforward control of the disturbance caused by the contribution of the

$i_{DC_{dm}}(s)$ to the $i_{DC_{cm}}(s)$ and reciprocal of the nonlinear term $(2i_{c_{cm}}(s))$. In addition, since the goal is to reduce the ripples caused by the power ripples in the AC output the DC supply current is filtered with high pass filter tuned at *20Hz* and a unity feedback is taken to construct the error signal (Figure 5.6).

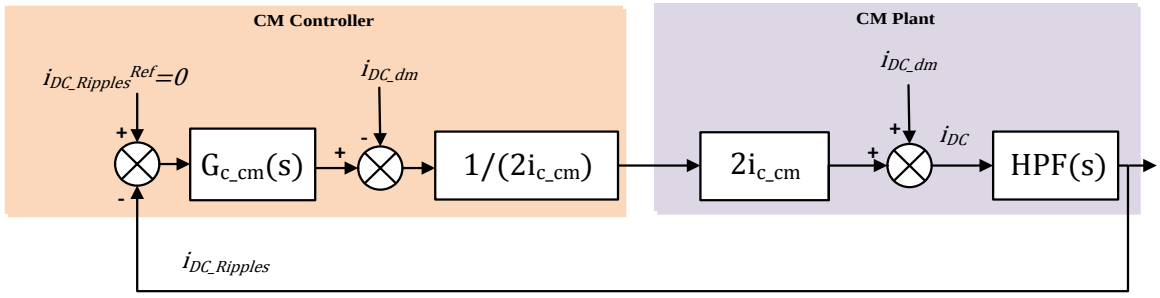


Figure 5.6: CM controller and the CM plant

The issue with the CM controller is that when the error on the DC supply current ripples $(e(s))$ is not zero initially the error will converge to zero exponentially. However, instead of forcing the ripples on the DC current to zero; the controller can reject the disturbance caused by the DM mode contribution. In other words, the feedforward of the disturbance $i_{DC_{dm}}(s)$ is removed and the controller dynamic will become as (5.19)

$$e(s)G_{c\_cm}(s) = i_{DC_{dm}} \tag{5.19}$$

The open loop and closed loop transfer functions are shown in (5.20) and (5.21) respectively:

$$G_{OL}(s) = G_{c\_cm}(s)\,HPF(s) \tag{5.20}$$

$$G_{CL}(s) = \frac{G_{c\_cm}(s)\,HPF(s)}{1 + G_{c\_cm}(s)\,HPF(s)} \tag{5.21}$$

And the gains selected for the CM controller are in (Table 5.4)

Table 5.4: CM controller gains

$K_{p_{cm}}$	$K_{R_{cm(2f_o)}}$	$K_{R_{cm(4f_o)}}$	ζ^*
0.001	450	160	0.001

*Non-ideal PR controller factor [86]

5.1.3. Overall Control with Passive Resonance Damper

The overall controller structure is illustrated in Figure 5.7. The controller is composed of inner current loop that estimates the CM and DM duty cycles and the outer loop regulates the DC bus voltage. Usually, the inner loop is much faster that the outer loop. Notice that the feedforward of the grid voltage and the contribution of the capacitors DM current to the supply DC current are neglected; since high controller gain removes the necessity of disturbance feedforward.

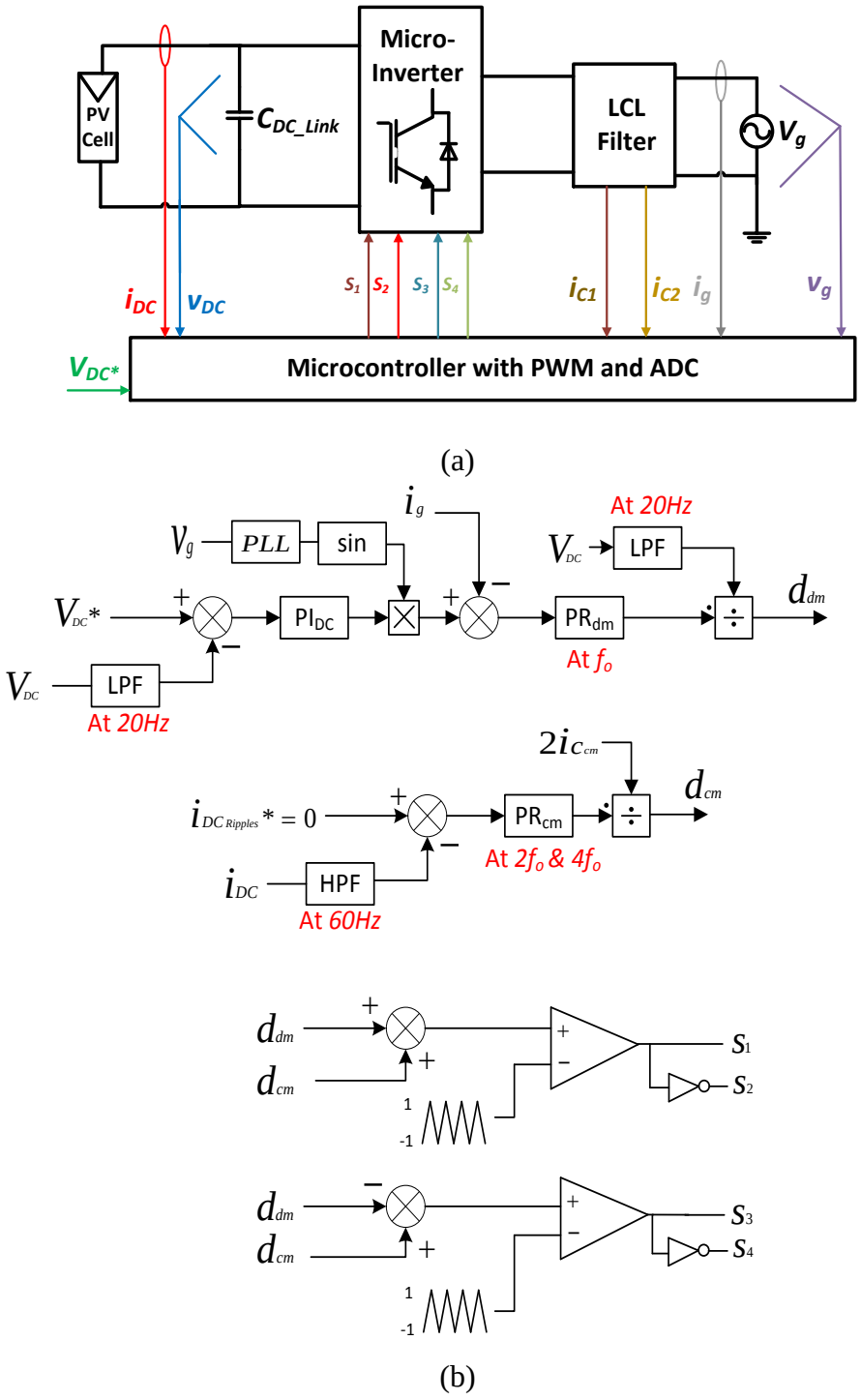


Figure 5.7: Passive resonance damping overall control structure differential buck microinverter: (a) Sensors and microinverter block diagram and (b) detailed controller structure

5.2. Differential Buck with LCL with Active Resonance Damper

One issue with the passive damper control scheme that was discussed in the previous section is that when an unexpected delay is considered the linearization $\frac{1}{2i_{c_{cm}}(s)}$ distorts the CM duty cycle estimation. In addition, when the $i_{c_{cm}}(s)$ is zero the linearization term goes to infinity. Also, the damping resistor introduces large inevitable losses and reduces system efficiency. Consequently, here explorations of the differential buck microinverter with small signal analysis to obtain a linearized CM plant.

5.2.1. Small Signal Analysis

The two microinverter legs compose two separate buck converters that are connected differentially to the grid. As indicated in (5.10) and (5.11), each capacitor voltage reaches maximally half the DC-link voltage. Meaning that, the two buck converters are operating around the equilibrium duty cycle (*D=0.5*). This suggests that the switches S1/S2 (converter A) are operating with the duty cycle (5.22) and S3/S4 (converter B) operate at (5.23):

$$D_A = D_{cm} + D_{dm} \tag{5.22}$$

$$D_B = D_{cm} + (1 - D_{dm}) \tag{5.23}$$

Note that the two duty cycles (5.22) and (5.23) are referenced to the top switch of each converter so the bottom switch has an inverted duty cycle. Moreover, small perturbation is applied to the CM and DM duty cycles of both converters around the equilibrium point results in (5.24) and (5.25):

$$\hat{d}_A = \hat{d}_{cm} + \hat{d}_{dm} \tag{5.24}$$

$$\hat{d}_B = \hat{d}_{cm} - \hat{d}_{dm} \tag{5.25}$$

The small signal model of the differential buck configuration is illustrated in Figure 5.8. The small signal modelling approach is similar to the one provided by [87], [88] but considering non-idealities.

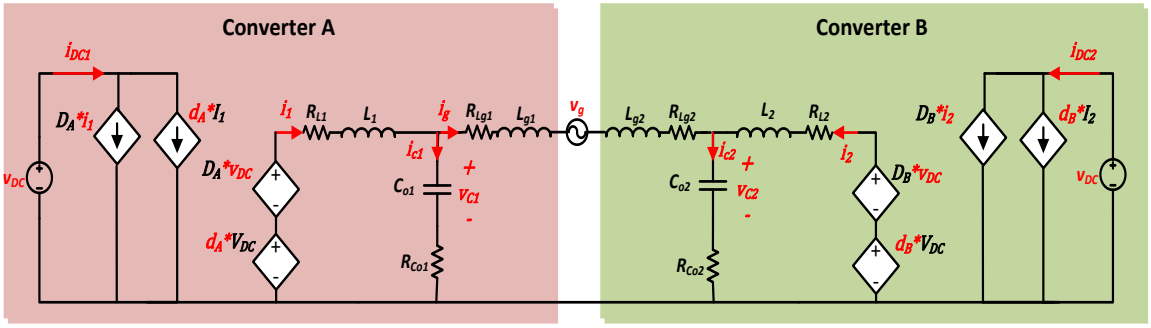


Figure 5.8: Grid connected differential buck small signal model (Red color indicates a perturb value)

Based on the dynamics of the small signal model; derivation of the DM and CM plants are deduced to construct a stable controller that actively damp the resonance peaks. However, a common method to damp LCL resonance peak in conventional inverter is to either feedback the capacitor current with simple proportional gain or feedback the capacitor voltage with high-pass filter in the feedback. Nonetheless, both methods emulate a virtual resistance in parallel with the filter capacitor. Since the controller is producing two duty-cycles ($\hat{d}_{dm}$ and $\hat{d}_{cm}$), both DM and CM plants are resonating. Therefore, feeding-back –with proportional gain in the feedback- the capacitors CM current in the CM plant and capacitors DM current in the DM plant would damp the resonance of both plants. However, because the reduction in the number of sensors is important, the active damping in both the CM and DM plants here is done through

cascading a notch filter prior to the control signal. This methodology reduces the number of sensors required to damp the resonance peaks since the requirement for capacitor current feedback is eliminated. Moreover, from the previous subsection, the DM plant is resonating at the LCL resonance frequency but the CM plant resonance is unknown because the plant is non-linear. Therefore, the small signal analysis is done to find the resonance peak of the CM plant so the notch filter would be tuned at the CM plant resonance peak. In all derivations the assumptions made are in Table 5.5.

Table 5.5: Assumptions in the small signal analysis

Parameters	
$L = L_1 = L_2$	$R_L = R_{L_1} = R_{L_2}$
$C = C_{o1} = C_{o2}$	$R_g = R_{g_1} = R_{g_2}$
$L_g = L_{g1} = L_{g2}$	$R_c = R_{c_{o1}} = R_{c_{o2}}$

Therefore, converter A has this small signal dynamics (5.26) and (5.27):

$$\left(\hat{d}_{cm} + \hat{d}_{dm}\right)V_{DC} = (sL + R_L)\,\hat{i}_1 + \hat{v}_{c1}(1 + sCR_c) \tag{5.26}$$

$$\hat{i}_{c1} = sC\hat{v}_{c1} = \hat{i}_1 - \hat{i}_g \tag{5.27}$$

Similarly, converter B dynamics are expressed in (5.28) and (5.29):

$$\left(\hat{d}_{cm} - \hat{d}_{dm}\right)V_{DC} = (sL + R_L)\,\hat{i}_2 + \hat{v}_{c2}(1 + sCR_c) \tag{5.28}$$

$$\hat{i}_{c2} = sC\hat{v}_{c2} = \hat{i}_2 + \hat{i}_g \tag{5.29}$$

Remember that the term V_{DC} is not changing quickly so it's perturb value $\hat{v}_{DC}$ goes to zero. Consequently, the dependent sources $D_A\hat{v}_{DC}$ and $D_B\hat{v}_{DC}$ that should contribute to (5.26) and (5.28) respectively are shorted. Furthermore, applying KVL at the AC output loop the grid current relation with the two buck output capacitors can be found:

$$\left(2sL_g + 2R_g\right)\hat{i}_g + \hat{v}_g = (\hat{v}_{c1} - \hat{v}_{c2})(1 + sCR_c) \tag{5.30}$$

Substituting (5.27) into (5.26) results in (5.31):

$$V_{DC}\left(\hat{d}_{cm} + \hat{d}_{dm}\right) = (sL + R_L)\,\hat{i}_g + \hat{v}_{c1}(s^2LC + sC(R_c + R_L) + 1) \tag{5.31}$$

Also, inserting (5.29) into (5.28) would results in a similar expression to (5.31) but in relation to $\hat{v}_{c2}$ as (5.32)

$$V_{DC}\left(\hat{d}_{cm} - \hat{d}_{dm}\right) = -(sL + R_L)\,\hat{i}_g + \hat{v}_{c2}(s^2LC + sC(R_c + R_L) + 1) \tag{5.32}$$

The transfer function between the CM perturbed duty cycle ($\hat{d}_{cm}$) and the capacitor CM voltage $\hat{v}_{c_{cm}}$ is achieved by the addition of (5.31) to (5.32). Note that the capacitor CM voltage is defined as (5.14) in the previous subsection (5.1.2.2. CM controller). (5.33) is the transfer function between the CM capacitor voltage and the CM duty cycle.

$$G_{v_{c_{cm}}}(s) = \frac{\hat{v}_{c_{cm}}}{\hat{d}_{cm}} = \frac{V_{DC}}{s^2LC + sC(R_c + R_L) + 1} \tag{5.33}$$

In addition, the output input relation between the capacitor DM voltage $\left(\hat{v}_{c_{dm}}\right)$ and the DM perturbed duty ratio ($\hat{d}_{dm}$) is obtained by the subtraction of (5.31) from (5.32) and substituting equation (5.30). The transfer function obtained is (5.34)

$$G_{v_{c_{dm}}}(s) = \frac{\hat{v}_{c_{dm}}}{\hat{d}_{dm}}_{\hat{v}_g=0} = \frac{(sL_g + R_g)V_{DC}}{s^3CLL_g + s^2C(LR_C + L_gR_C + LR_g + L_gR_L) + s(L + L_g + CR_CR_L + CR_CR_g + CR_LR_g) + R_L + R_g} \tag{5.34}$$

Note that the capacitor DM voltage is defined as (5.15) in the previous subsection (5.1.2.2. CM controller). Furthermore, the transfer function between the grid current and the DM duty cycle derived by inserting (5.34) into (5.30) as in (5.35)

$$G_{i_g}(S) = \frac{\hat{i}_g}{\hat{d}_{dm}\,\hat{v}_g=0} = \frac{(sCR_C + 1)V_{DC}}{s^3CLL_g + s^2C(LR_C + L_gR_C + LR_g + L_gR_L) + s(L + L_g + CR_CR_L + CR_CR_g + CR_LR_g) + R_L + R_g} \quad (5.35)$$

Notice (5.35) is exactly the LCL filter transfer function that was obtained in the previous section (5.1.2.1. DM controller) and it resonates exactly as a conventional LCL filter. Therefore, cascading a notch filter tuned at $f_{res_{dm}} = \frac{1}{2\pi}\sqrt{\frac{L+L_g}{LL_gC}}$ with the plant of the DM would damp the resonance peak. Moreover, extra two transfer functions can be obtained by summing or subtracting (5.27) and (5.29) to yield the expression for the microinverter CM (5.36) and DM (5.37) current

$$G_{i_{inv_{cm}}}(s) = G_{i_{c_{cm}}}(s) = \frac{\hat{i}_{inv_{cm}}}{\hat{d}_{cm}} = \frac{\hat{i}_{c_{cm}}}{\hat{d}_{cm}} = \frac{sCV_{DC}}{s^2LC + sC(R_c + R_L) + 1} \quad (5.36)$$

$$G_{i_{inv_{dm}}}(s) = \frac{\hat{i}_{inv_{dm}}}{\hat{d}_{dm}} = \frac{\left(s^2CL_g + sC(R_g + R_c) + 1\right)V_{DC}}{s^3CLL_g + s^2C(LR_C + L_gR_C + LR_g + L_gR_L) + s(L + L_g + CR_CR_L + CR_CR_g + CR_LR_g) + R_L + R_g} \quad (5.37)$$

The last expression to derive is the DC supply current that had a non-linear equation in the previous section. Thus, according to Figure 5.8 the DC supply current is as (5.40) by the addition of (5.38) to (5.39):

$$\hat{i}_{DC1} = D_A\,\hat{i}_1 + \hat{d}_A\,I_1 = (D_{cm} + D_{dm})\hat{i}_1 + \left(\hat{d}_{cm} + \hat{d}_{dm}\right)I_1 \quad (5.38)$$

$$\hat{i}_{DC2} = D_B\,\hat{i}_2 + \hat{d}_B\,I_2 = (D_{cm} + (1 - D_{dm}))\hat{i}_2 + \left(\hat{d}_{cm} - \hat{d}_{dm}\right)I_2 \quad (5.39)$$

$$\hat{i}_{DC} = (2D_{cm} + 1)\hat{i}_{inv_{cm}} + \hat{d}_{cm}I_{inv_{cm}} + (2D_{dm} + 1)\hat{i}_{inv_{dm}} + \hat{d}_{dm}I_{inv_{dm}} \quad (5.40)$$

Notice that the inductor CM current is exactly equal to the capacitor CM current ($\hat{i}_{inv_{cm}} = \hat{i}_{c_{cm}}$). This can be seen clearly in Figure 5.5. Furthermore, the DC supply current is a function of both the CM and the DM duty cycles. Though, the purpose was to

control the CM duty cycle so the DM duty cycle is treated as a disturbance. The transfer function between the DC supply current and the CM duty cycle is derived by substituting (5.36) into (5.40) and setting $D_{dm} = \hat{d}_{dm} = 0$ as (5.41)

$$G_{i_{DC_{cm}}}(s) = \frac{\hat{i}_{DC_{cm}}}{\hat{d}_{cm}} = \frac{(2D_{cm}+1)sCV_{DC}}{s^2LC + sC(R_c + R_L) + 1} + I_{c_{cm}} \tag{5.41}$$

In case of designing an active damper with capacitor current feedbacks; (5.36) can be used to damp the resonance in the CM control loop. Also, it is crucial to find the transfer function between the capacitors DM current and the DM duty cycle; so by subtracting (5.27) from (5.29) and inserting them into (5.34) the result is (5.42)

$$G_{i_{c_{dm}}}(s) = \frac{\hat{i}_{c_{dm}}}{\hat{d}_{dm}}_{\hat{v}_g=0} = \frac{(s^2CL_g + sCR_g)V_{DC}}{s^3C\,L\,L_g + s^2C\,(L\,R_C + L_gR_C + L\,R_g + L_gR_L) + s(L + L_g + C\,R_CR_L + C\,R_CR_g + C\,R_LR_g) + R_L + R_g} \tag{5.42}$$

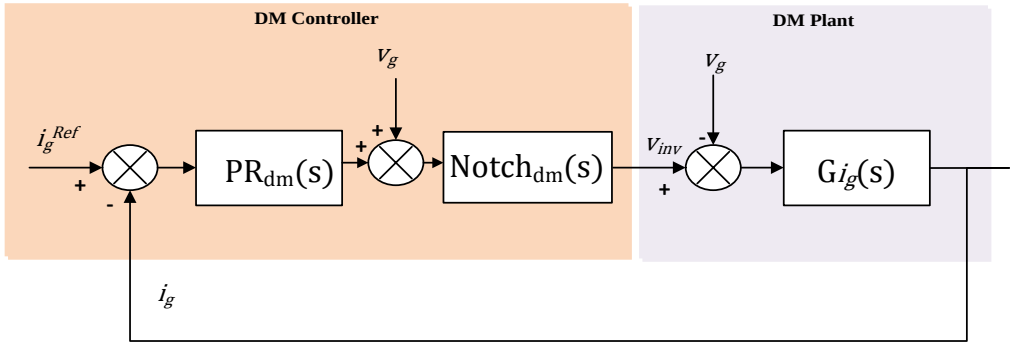
Hence, feeding back the capacitor DM current can damp the resonance that occurs in the DM loop in case of damping with capacitor current. In addition, two extra transfer function can be derived: (i) to convert the DM capacitor current to the grid current (5.43) by dividing (5.35) by (5.42) and (ii) to convert the CM capacitor current to the supply CM current (5.44) by dividing (5.41) by (5.36)

$$\frac{\hat{i}_g}{\hat{i}_{c_{dm}}} = \frac{sCR_C + 1}{s^2CL_g + sCR_g} \tag{5.43}$$

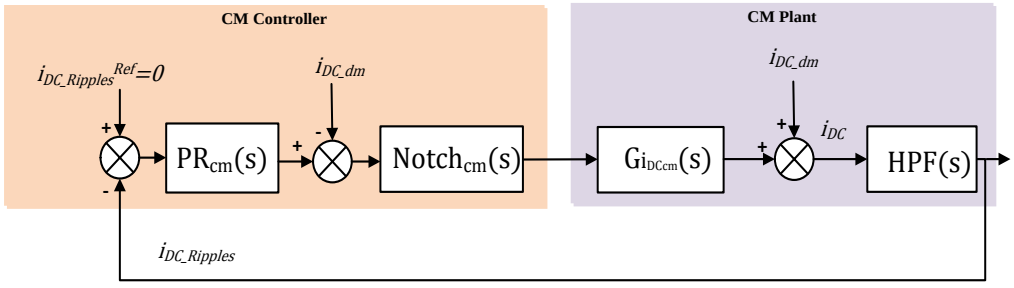
$$\frac{\hat{i}_{DC_{cm}}}{\hat{i}_{c_{cm}}} = (2D_{cm}+1) + I_{c_{cm}}\frac{s^2LC + sC(R_c + R_L) + 1}{sCV_{DC}} \tag{5.44}$$

In case of damping through capacitor current feedback, the controller can be designed using (5.36), (5.42), (5.43) and (5.44). Note that all four transfer functions have a resonance peak that affects the system stability. Alternatively, (5.41) indicates that the

CM plant resonance depends on microinverter side inductance and the output capacitors; thus, the CM notch filter must be tuned at $f_{res_{cm}} = \frac{1}{2\pi\sqrt{LC}}$ to damp the resonance. Finally, the CM & DM controller structures with plant model are shown in Figure 5.9.



(a)



(b)

Figure 5.9 Active damper controller detailed models: (a) DM controller and (b) CM controller

Note that with grid-side inductance deviation due to different grid interfacing; DM resonance deviate and therefore, the DM notch filter must be adaptive. On the other hand, the CM notch filter is not affected by grid-side inductance variation so no requirement for adaptive design. Also, the feedforward disturbance can be avoided in CM and DM plants with high controller gains as in subsection 5.1 analysis. Furthermore, the open loop and

closed loop transfer functions are shown in (5.45), (5.46), (5.47) and (5.48) of both DM and CM:

$$G_{OL_{dm}}(s) = PR_{dm}(s)\, Notch_{dm}(s)\, G_{i_g}(s) \tag{5.45}$$

$$G_{CL_{dm}}(s) = \frac{PR_{dm}(s)\, Notch_{dm}(s)\, G_{i_g}(s)}{1 + PR_{dm}(s)\, Notch_{dm}(s)\, G_{i_g}(s)} \tag{5.46}$$

$$G_{OL_{cm}}(s) = PR_{cm}(s)\, Notch_{cm}(s)\, G_{i_{DC_{cm}}}(s)\, HPF(s) \tag{5.47}$$

$$G_{CL_{cm}}(s) = \frac{PR_{cm}(s)\, Notch_{cm}(s)\, G_{i_{DC_{cm}}}(s)\, HPF(s)}{1 + PR_{cm}(s)\, Notch_{cm}(s)\, G_{i_{DC_{cm}}}(s)\, HPF(s)} \tag{5.48}$$

The gains selected are in Table 5.7 based on the components values of Table 5.6.

Table 5.6: Active damper components

L	L_g	C	R_g	R_L	R_c
1mH	0.05mH	120uF	12mΩ	13mΩ	1.7mΩ

Note these values are selected based on actual existing components; each component datasheet is attached in the appendix.

Table 5.7: Controller gains

$K_{p_{cm}}$	$K_{R_{cm(2f_o)}}$	$K_{R_{cm(4f_o)}}$
0.001	450	160
$K_{P_{dm}}$	$k_{R_{dm}(f_o)}$	ζ^*
3	20000	0.001

*Non-ideal PR controller factor [86]

5.2.2. Overall Control with Active Resonance Damper

The overall controller structures with active resonance damping are illustrated in Figure 5.10 which is similar to Figure 5.7. The only difference is the cascaded two notch filters and the removal of the feedback linearization term in the CM plant. CM notch filter is not affected by the grid inductance variation, while the DM notch filter is highly dependent on grid inductance variation. Therefore, there has to be some estimation method to adaptively vary the DM notch filter center frequency. Moreover, the feedforward of the disturbances such as the grid voltage and DC DM supply currents are neglected because of the high controller's gain. Only 4 sensors are needed to control the microinverter; specifically, the measurements needed are grid current, grid voltage for PLL, DC supply current and DC link voltage.

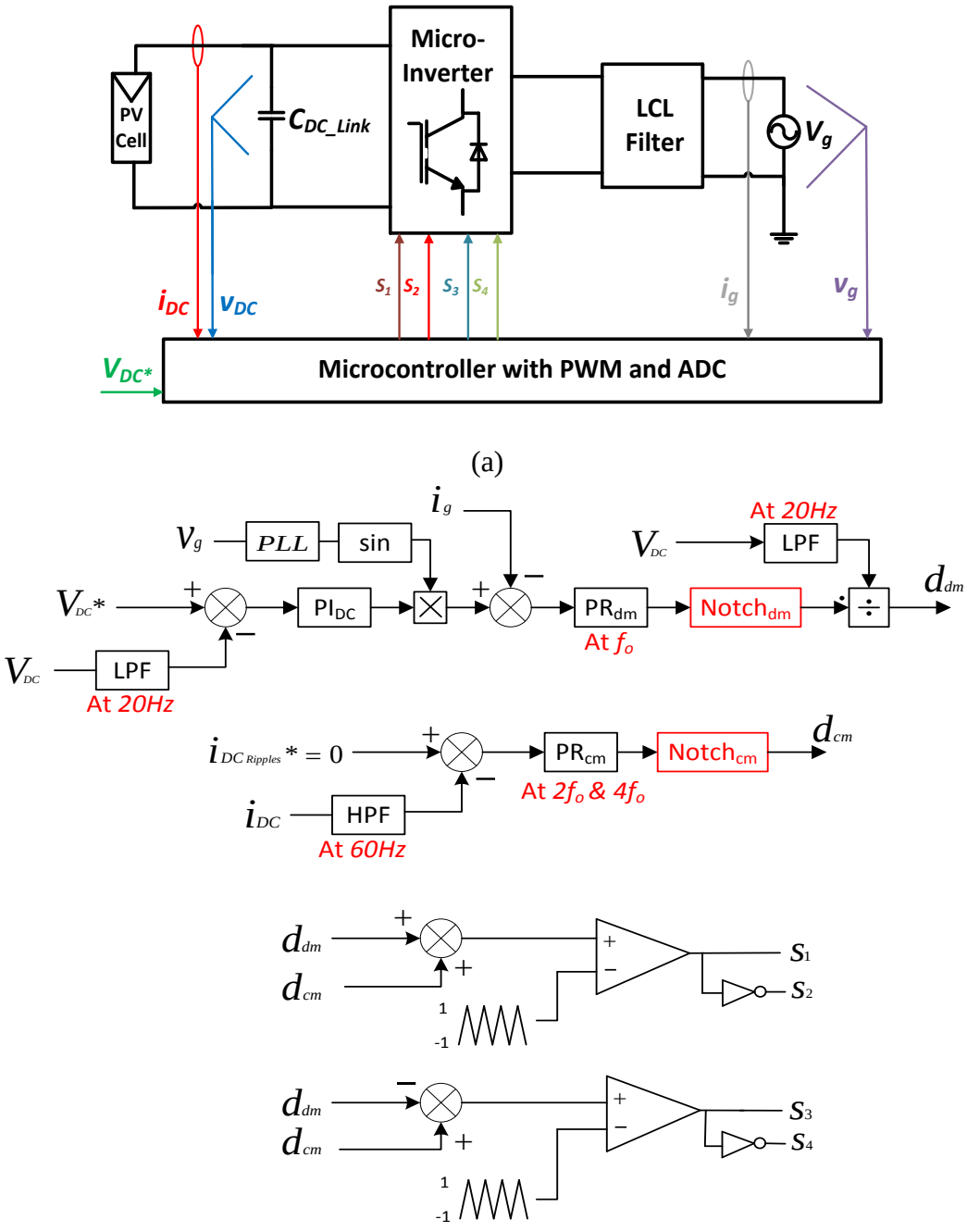


Figure 5.10: Active resonance damping control structure with differential buck microinverter: (a) Sensors and microinverter block diagram and (b) detailed controller structure

Chapter 6 : Simulation

This chapter discusses the simulation of both proposed control schemes using PSIM software tools. A 600W prototype is simulated under non-ideal conditions. Non-idealities include the on-state resistance, the voltage threshold of the MOSFET, the internal resistance of each element, and the delay consideration of the PWM. Moreover, the internal resistances and MOSFET on-state resistance ($R_{DS(ON)} = 300m\Omega$) are obtained from the components datasheets. In addition, a realistic PWM delay is considered to be 150% of the controller sample time T_s. Note in all simulations the DC-link capacitor $c_{DC-Link}$ is 60uF film capacitor. Without any power decoupling control, the DC voltages ripples should be around *50V*. In addition, to observe the ground leaking current, the parasitic capacitors between the PV terminals to the ground are selected to be $c_{pvg+} = c_{pvg-} = 20nF$. Furthermore, the negative grid terminal resistance R_E is *10*Ω since the microinverter is connected to a *240V$_{RMS}$/50Hz* stiff-grid. Also, based on the two proposed controllers, this chapter is divided into two sections: (i) passive resonance damping control simulation and (ii) active resonance damping control simulation.

6.1. Passive Resonance Damper Control Simulation

The simulation carried out in PSIM with these components values (Table 6.1). Notice the extremely small DC-Link capacitor ($c_{DC-Link}$) and the exaggerated PV terminal stray capacitances (c_{pvg+} and c_{pvg-}). The small DC-Link capacitor is used to illustrate the power decoupling scheme impact on the DC bus voltage ripples. Also, the exaggerated

value of the PV stray capacitances to show the enormous reduction in the ground leakage current.

Table 6.1 component values used in PSIM simulation (Passive Damper Control)

$L = L_1 = L_2$	$L_g = L_{g_1} = L_{g_2}$	$C = C_{o_1} = C_{o_2}$	$R_g = R_{g_1} = R_{g_2}$	$R_L = R_{L_1} = R_{L_2}$
1mH	0.05mH	120uF	12mΩ	13mΩ

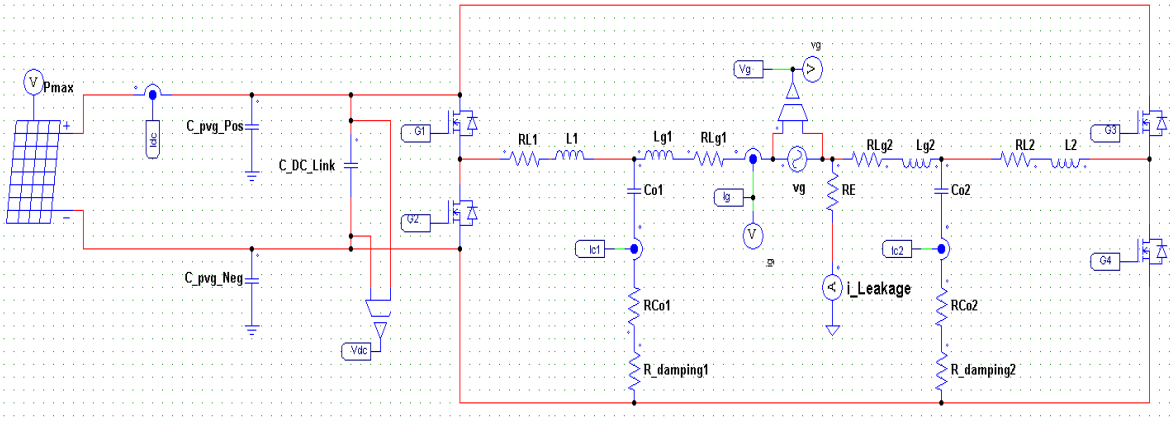
$R_c = R_{co_1} = R_{co_2}$	$R^*_{damping}$	$c_{pvg+} = c_{pvg-}$	R_E	$R^{**}_{DS(ON)}$	$c_{DC-Link}$
1.7mΩ	0.4Ω	20nF	10Ω	300mΩ	60uF

* One $R_{damping}$ is connected in series with each output capacitor

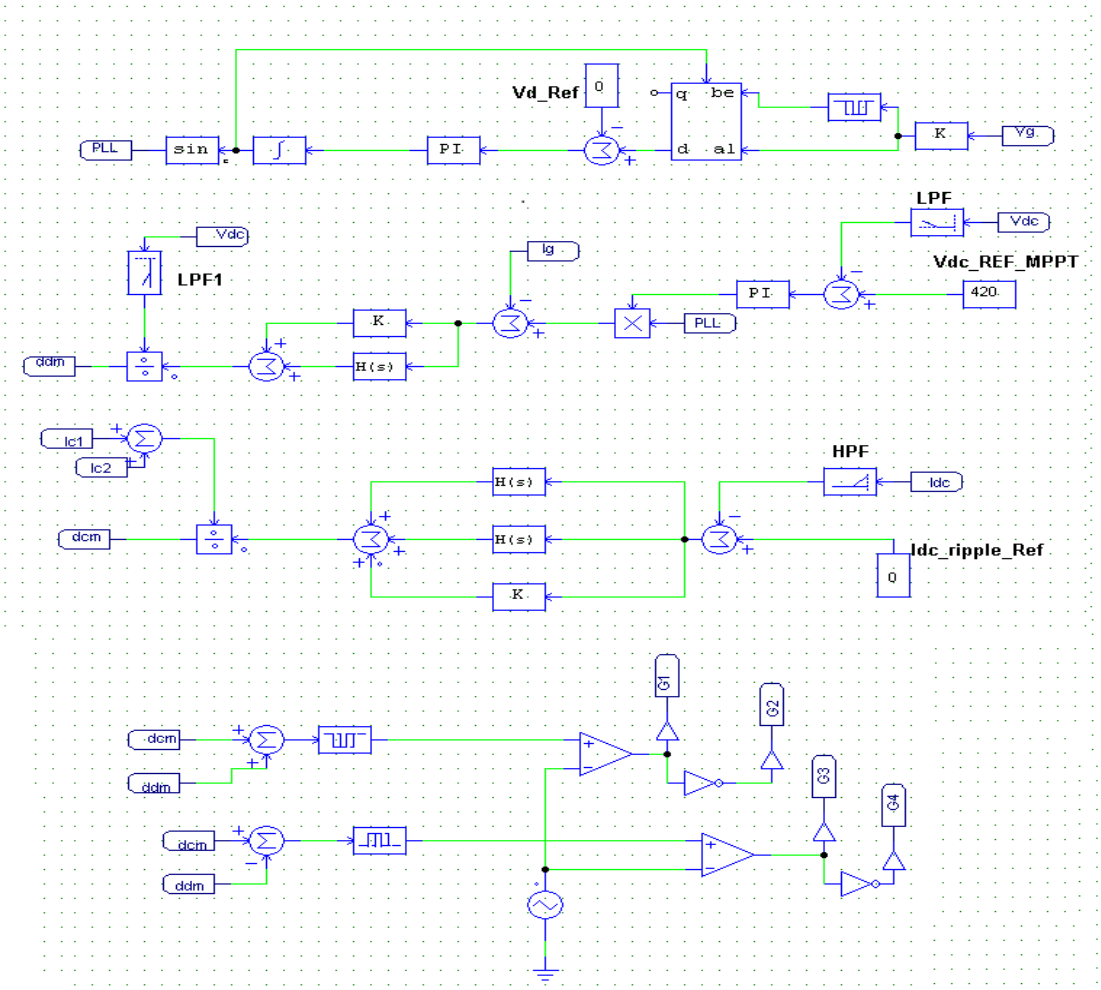
** $R_{DS(ON)}$ is the MOSFET on-state resistance

6.1.1. PSIM Set-up (Passive Resonance Damping)

The system set-up in PSIM is shown in (Figure 6.1). As discussed earlier, the controller is composed of two parallel inner loops for power decoupling and current control and outer voltage regulation loop (Figure 6.1 (b)). Additionally, single-phase PLL is shown in Figure 6.1 (b) to estimate grid voltage angle. The modulation used is unipolar since each H-bridge leg has its own reference (Figure 6.1 (b)).



(a)



(b)

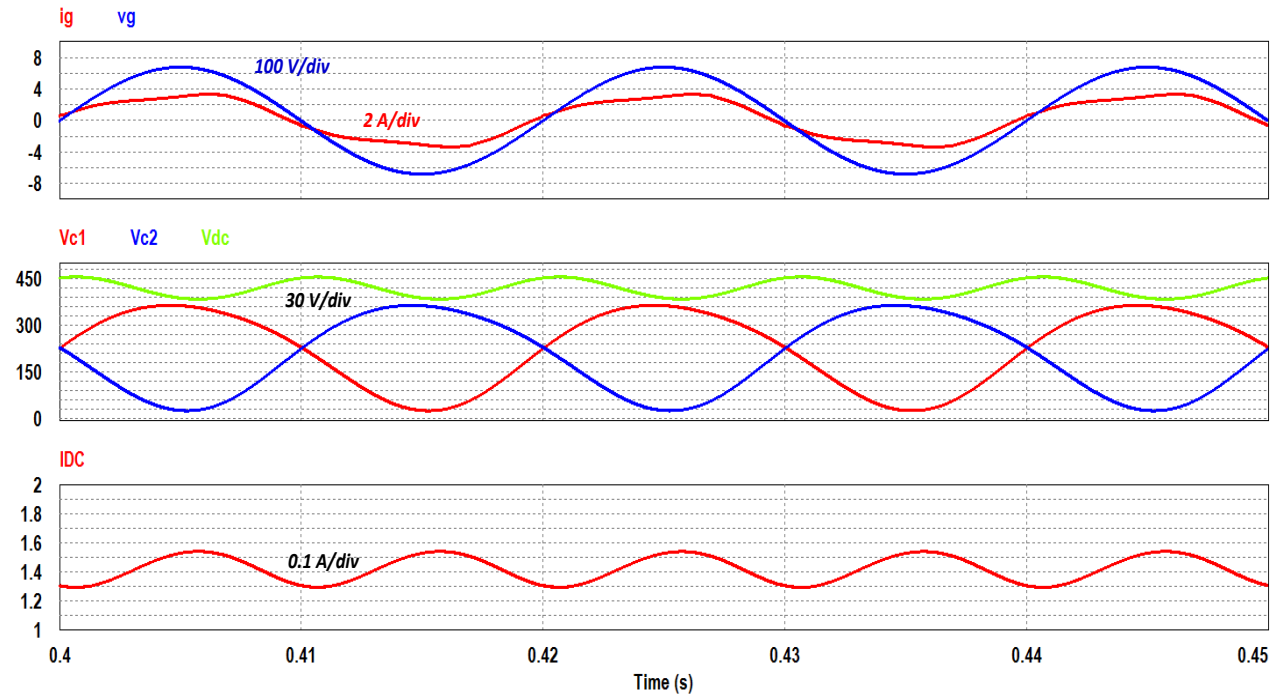
Figure 6.1: System set-up in PSIM (Passive damper control): (a) circuit set-up and (b) controller structure.

Simulating the set-up in Figure 6.1 and by observing the different waveforms; performance evaluation of the system efficiency, leakage current RMS value and the DC link ripples will be conducted in the next subsection. Another comparison will be carried out with activation and deactivation of the power decoupling controller to observe the significance of the power decoupling control.

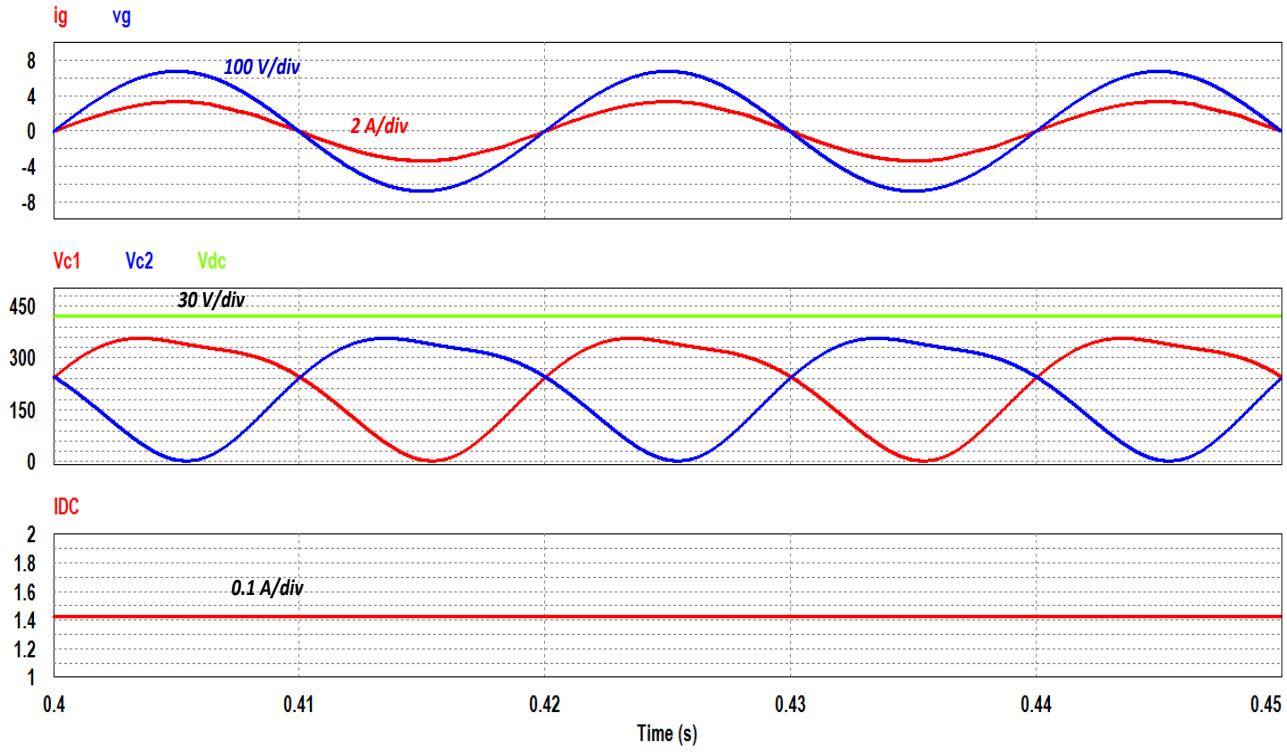
6.1.2. Waveforms Observation (Passive Resonance Damping)

6.1.2.1. Waveforms With and Without Power Decoupling Control

Essential waveforms are observed with and without the power decoupling control. The essential waveforms are the grid current (i_g), DC-link voltage (V_{DC}), output capacitors voltages ($v_{c1}$and v_{c2}) and the DC supply current (i_{DC}). Figure 6.2 indicates the effect of the power decoupling controller.



(a)



(b)

Figure 6.2: Essential waveforms (Passive damper control): (a) without power decoupling control and (b) with power decoupling control

Notice in Figure 6.2 (b) the DC supply current and the DC voltage are constant. Thus, the grid current is sinusoidal. On the other hand, Figure 6.2 (a) the ripples on the DC link voltage are around 50V and the DC supply current has 2^{nd} order current harmonics. Consequently, without the power decoupling control, the grid current is distorted by 2^{nd} order harmonics. Note the disappearance of 2^{nd} order power ripples in Figure 6.2 (b) is due to the injected CM voltage in the two output capacitors (see the capacitor voltages are not pure sinusoidal in Figure 6.2 (b)). The significance of these results is that it allows a smaller DC-Link capacitor (film type) that would enhance the reliability and lifetime of the system. Furthermore, since film capacitor sensitivity to temperature variation is less compared to electrolytic type; using power decoupling control in microinverter that are usually installed outside would boost their lifetime.

6.1.2.2. Leakage Current Waveform with Power Decoupling Control

After illustrating the benefits of the power decoupling control and how it impacts the input capacitance requirement. Let us explore the other objective which is the amount of the ground leaking current. The ground leaking current RMS value is very low around 4mA (Figure 6.3). Remember, that the parasitic PV capacitances c_{pvg+} and c_{pvg-} values are extremely exaggerated (20nF); as mentioned earlier these values were selected for testing purposes.

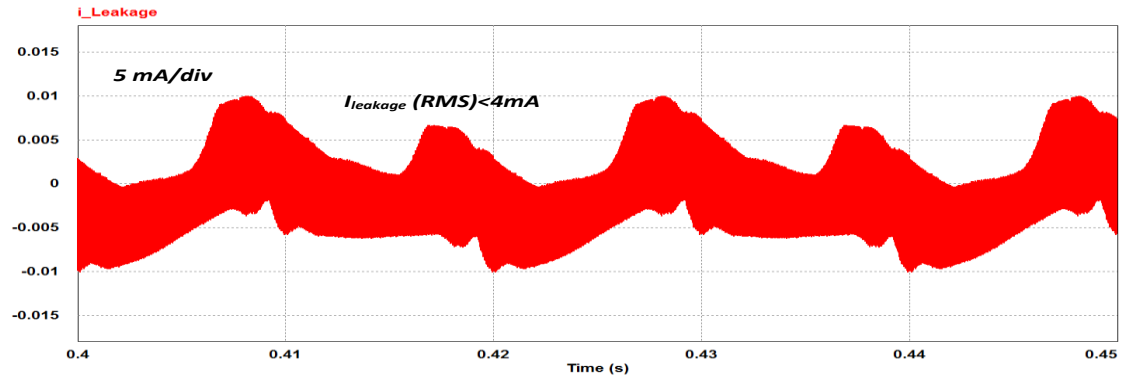


Figure 6.3: Ground leaking current with power decoupling control (Passive damper control)

6.1.3. Efficiency of the System (Passive Resonance Damping)

The last part of the objective was to maintain the high efficiency. However, most of the losses are due to the additional two damping resistors as in Figure 6.1. Still, these two damping resistors are crucial and removing them makes the grid current non-sinusoidal as in Figure 6.4.

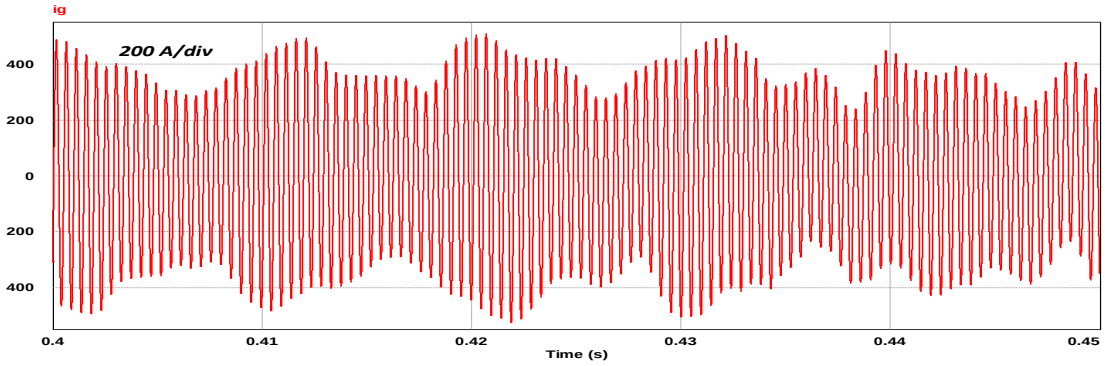


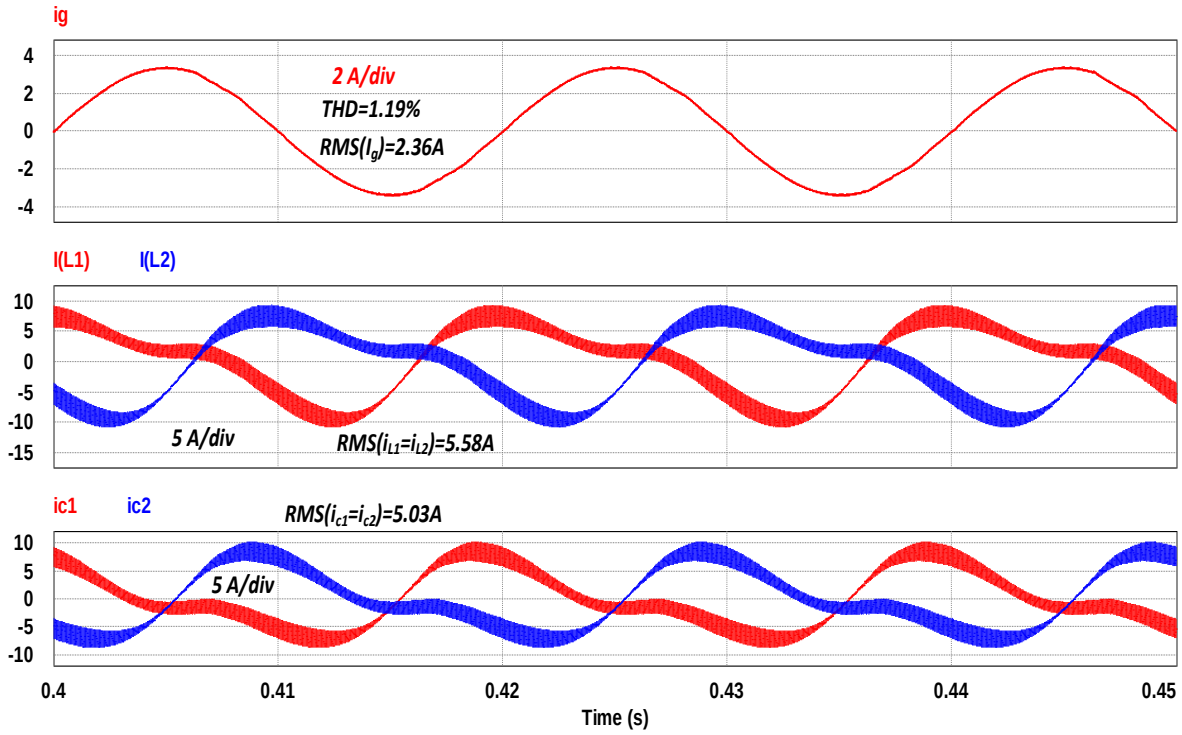
Figure 6.4: Effect of removing the damping resistors on the grid current

In other words, the damping resistors that cause most of the efficiency deterioration stabilized the system. Moreover, to calculate the efficiency of the system precisely let us observe each LCL filter component current waveforms and measure the current RMS value (Figure 6.5 (a)) or alternatively measure the average of the instantaneous output power (Figure 6.5 (b)).

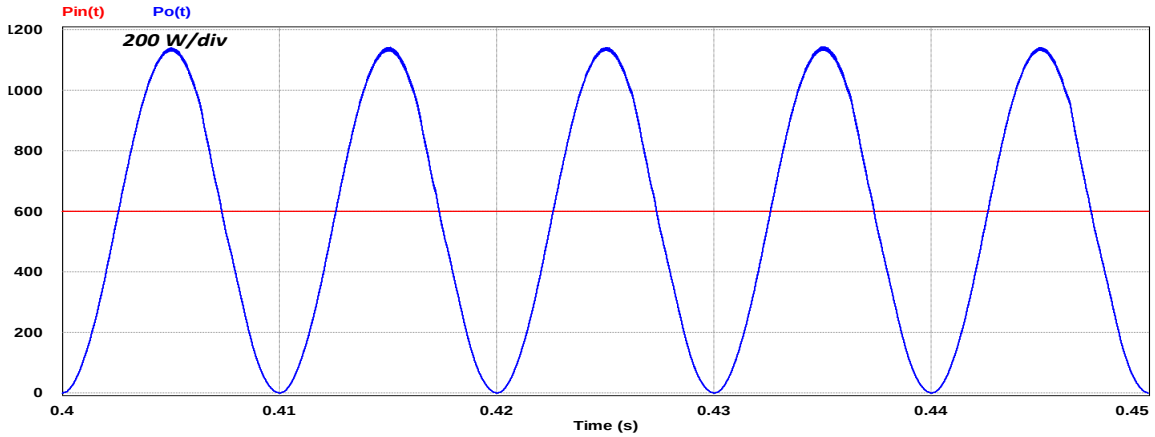
Table 6.2: Currents RMS values and power losses (Passive damper control)

$i_{c_1}(RMS) = i_{c_2}(RMS)$	$i_{L_1}(RMS) = i_{L_2}(RMS)$	$i_{L_{g_1}}(RMS) = i_{L_{g_2}}(RMS) = i_g(RMS)$
5.03A	5.58A	2.36A
$P_{Loss}(c_1 \& c_2)$	$P_{Loss}(L_1 \& L_2)$	$P_{Loss}(L_{g_1} \& L_{g_2})$
20.33W	0.81W	0.13W
$P_{Loss}(MOSFET)$	$P_{in}(Average)$	$P_{out}(Average)$
12.33W	600W	566.4W
η%	94.40%	

The 12.33W loss due to MOSFETs can be calculated using the guideline provided by [20] but with considering the two modes duty cycles. Notice the capacitor high RMS current value; this caused most of the system losses around 3.38% because of the high inevitable damping resistors that are in series with the capacitors. Also, the MOSFETs losses are around 2.06% of the total losses. Consequently, next subsection will discuss how the active damper would reduce the losses that were due damping only. MOSFETs losses are not tackled since the switching frequency is high and IGBT usage would deteriorate the system performance.



(a)



(b)

Figure 6.5: Efficiency calculation waveforms (Passive damper control): (a) Currents waveforms and (b) instantaneous output power waveform compared to the instantaneous input power

6.2. Active Resonance Damper Control Simulation

The simulation carried out in PSIM with these components values (Table 6.3). Most component values are similar to the previous section except the removal of the damping resistors. In other words, the task here is to improve the efficiency of the system.

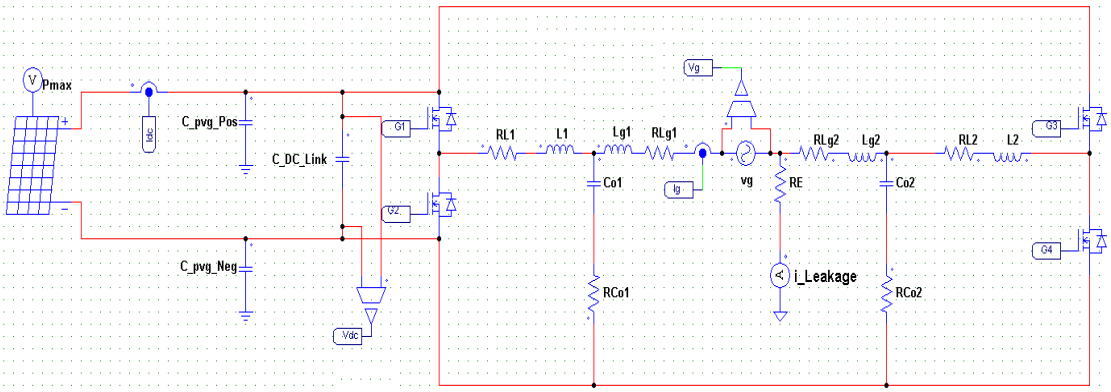
Table 6.3: component values used in PSIM simulation (Active Damper Control)

$L = L_1 = L_2$	$L_g = L_{g_1} = L_{g_2}$	$C = C_{o_1} = C_{o_2}$	$R_g = R_{g_1} = R_{g_2}$	$R_L = R_{L_1} = R_{L_2}$
1mH	0.05mH	120uF	12mΩ	13mΩ
$R_c = R_{co_1} = R_{co_2}$	$R^*_{DS(ON)}$	$c_{pvg+} = c_{pvg-}$	R_E	$c_{DC-Link}$
1.7mΩ	300mΩ	20nF	10Ω	60uF

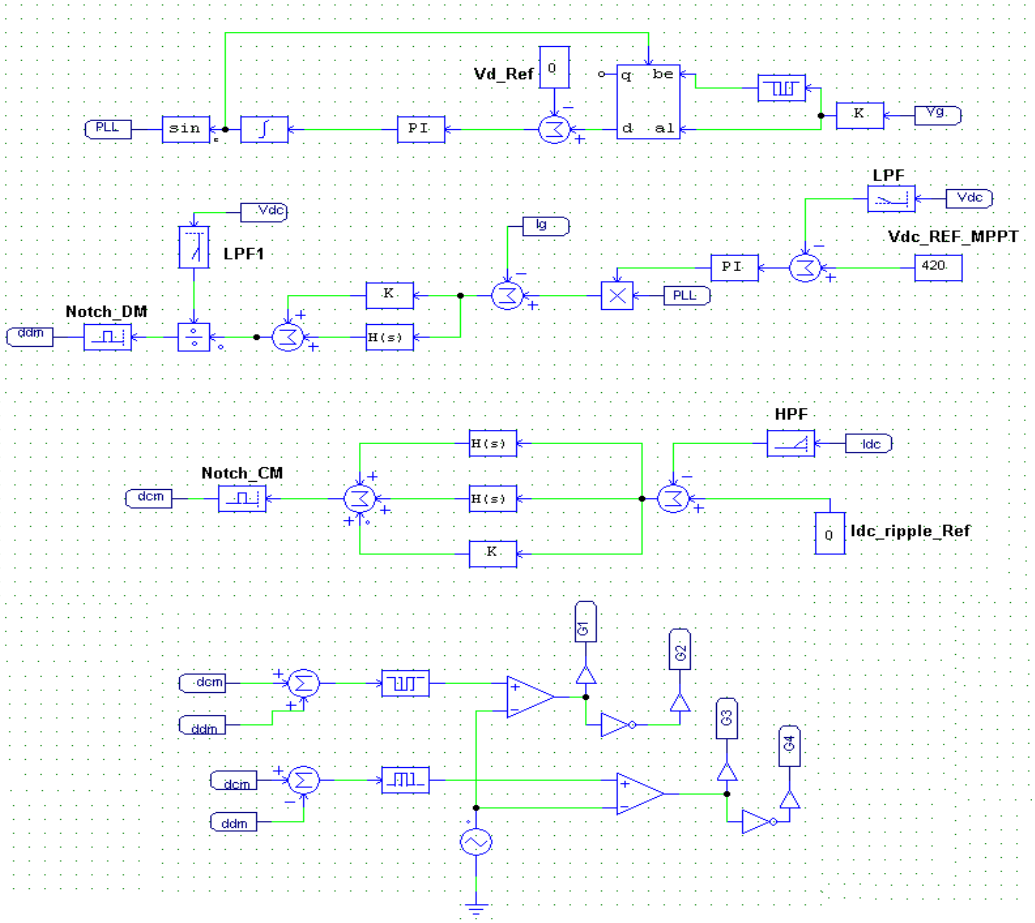
*$R^*_{DS(ON)}$ is the MOSFET on-state resistance

6.2.1. PSIM Set-up (Active Resonance Damping)

The control scheme is similar to the previous subsection. The difference is that the number of sensors is reduced to only 4 sensors (Figure 6.6 (a)), the removal of the damping resistors (Figure 6.6 (a)) and the cascaded two notch filters Figure 6.6 (b). These notch filters are tuned at each plant resonance frequency.



(a)



(b)

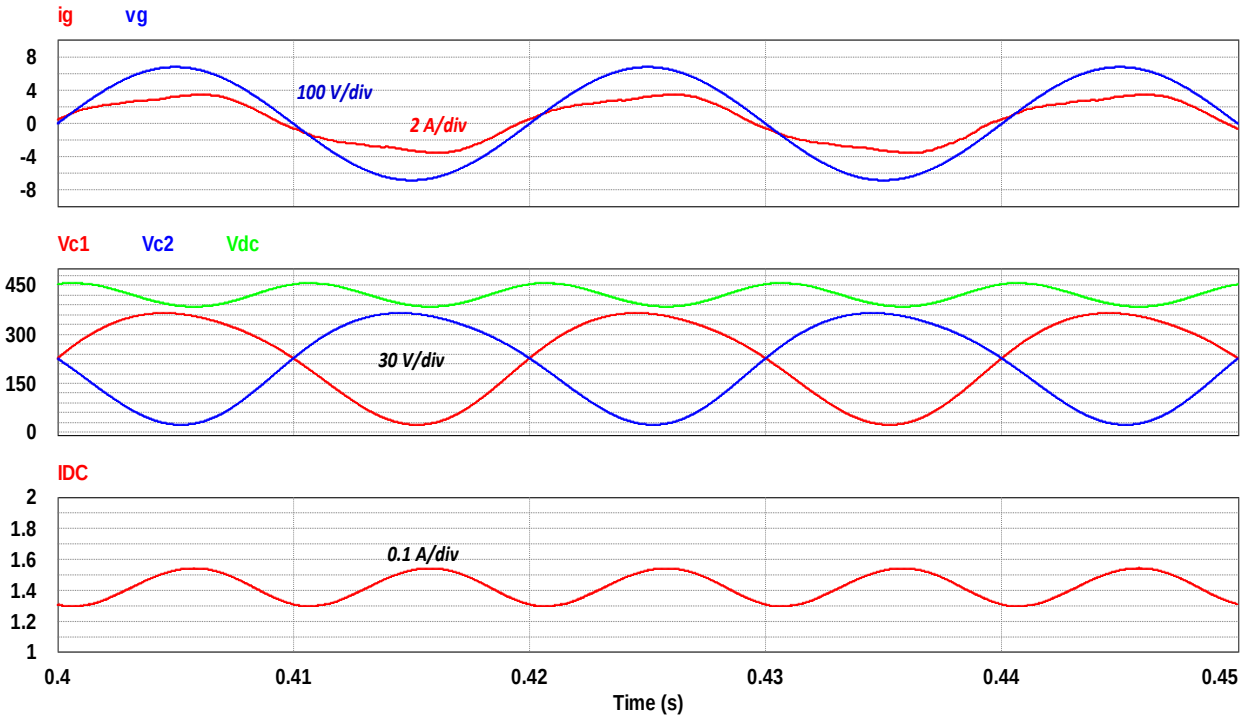
Figure 6.6: System set-up in PSIM (Active Damper Control): (a) Circuit set-up and (b) controller structure.

Simulating the set-up in Figure 6.6 and by observing the different waveforms; performance evaluation of the system efficiency, leakage current RMS value and the DC link ripples will be conducted in the next subsection. Also, the effect of grid-side inductance variation and the notch filter removal on the grid current is observed.

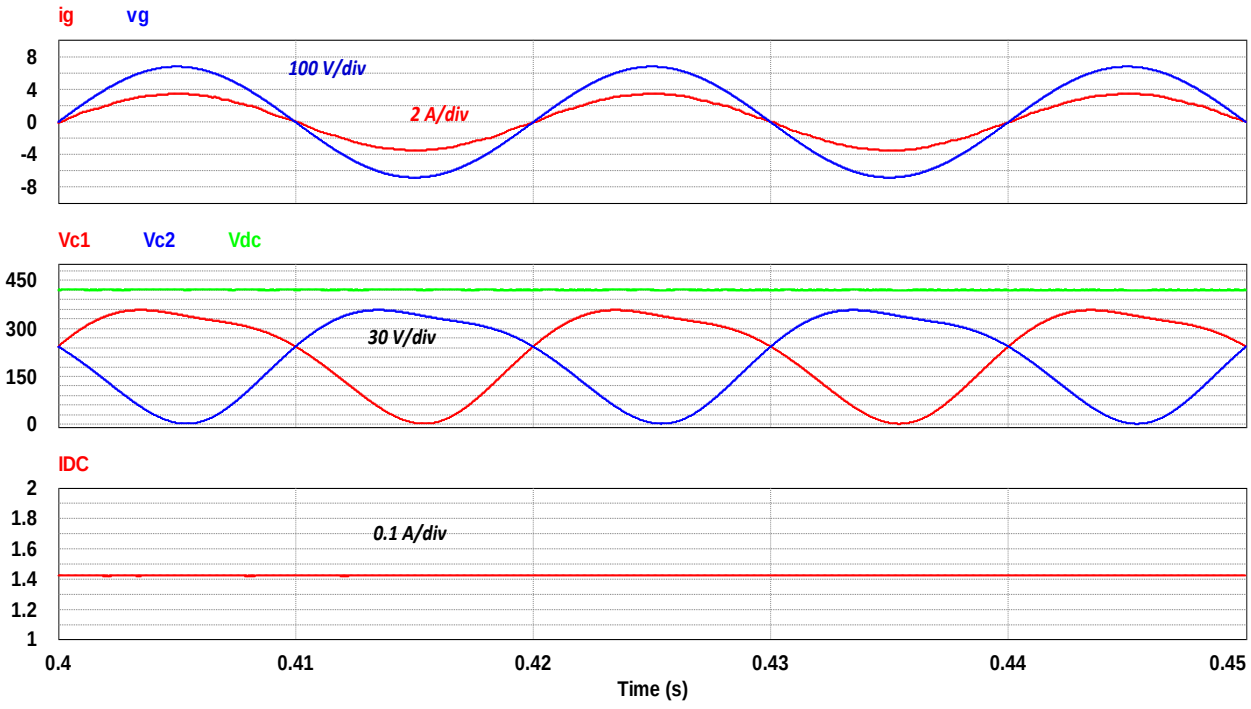
6.2.2. Waveforms Observation (Active Resonance Damping)

6.2.2.1. Waveforms With and Without Power Decoupling Control

Essential waveforms are observed with and without the power decoupling control. The essential waveforms are the grid current (i_g), DC-link voltage (V_{DC}), output capacitors voltages ($v_{c1}$and v_{c2}) and the DC supply current (i_{DC}). Figure 6.7 indicates the effect of the power decoupling controller. Similar to the passive damper control section, without power decoupling control the grid-current is superimposed by 2nd order harmonics in Figure 6.7 (a). The difference between the passive and active damping is that the RMS value of the grid current increased. Meaning that, it is expected that with active damping the efficiency will rise. Also, the significance of this results Figure 6.7 (b) is the smaller reliable DC-Link capacitor could be used to improve the system reliability.



(a)



(b)

Figure 6.7: Essential waveforms (Active damper control): (a) without power decoupling control and (b) with power decoupling control

6.2.2.2. Ground Leaking Current Waveform

The second part of the thesis objective is also met with this control; since the RMS value of the ground leaking current is less than 3mA. This is a substantial result because the stray capacitances are exaggerated 20nF and the leakage current is still low Figure 6.8.

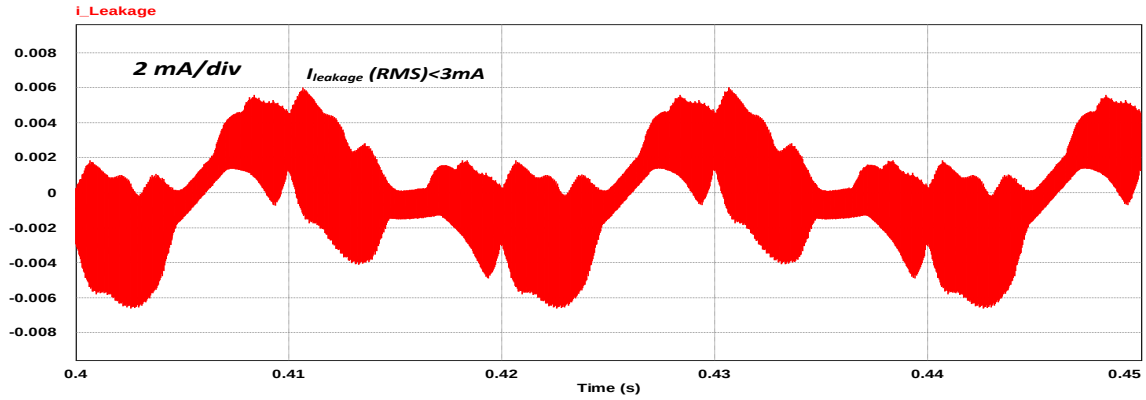
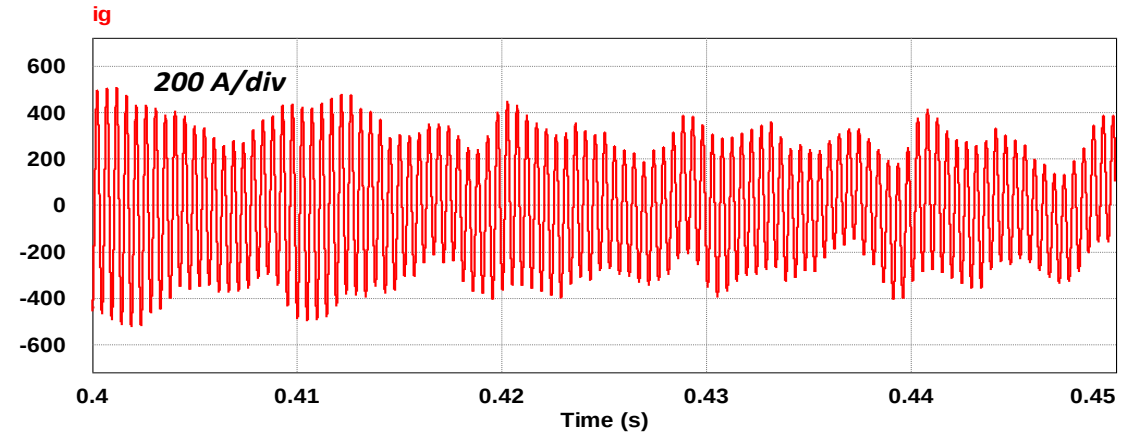


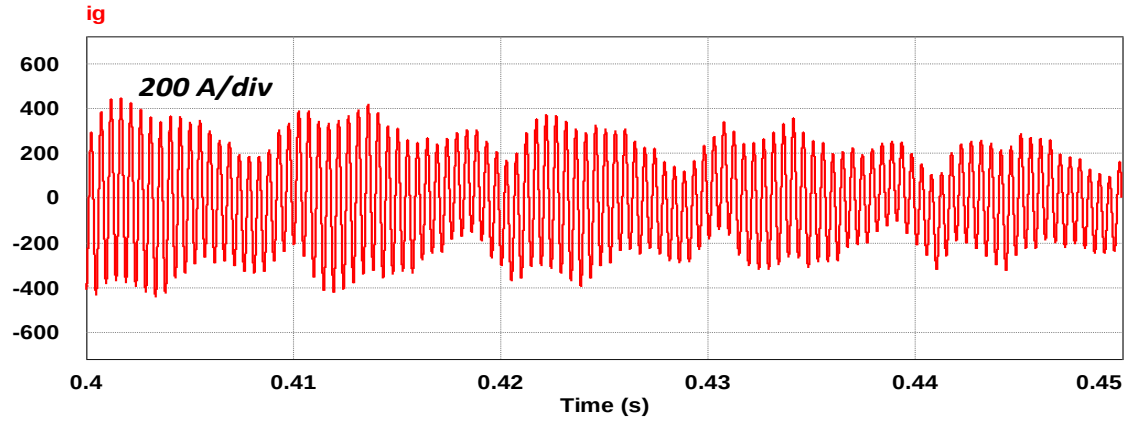
Figure 6.8: Ground leaking current with power decoupling control (Active damper control)

6.2.2.3. Effect of Notch Filter

In active resonance damping control, the notch filters are essential. Precisely, eliminating both or one of the notch filters would result in a resonating grid current; thus, confirming the theoretical analysis done in 5.2. The effect of notch filters removal on the grid current waveform is summarized in Figure 6.9: (a) both notch filters removal, (b) DM notch filter removal and (c) CM notch filter removal.



(a)



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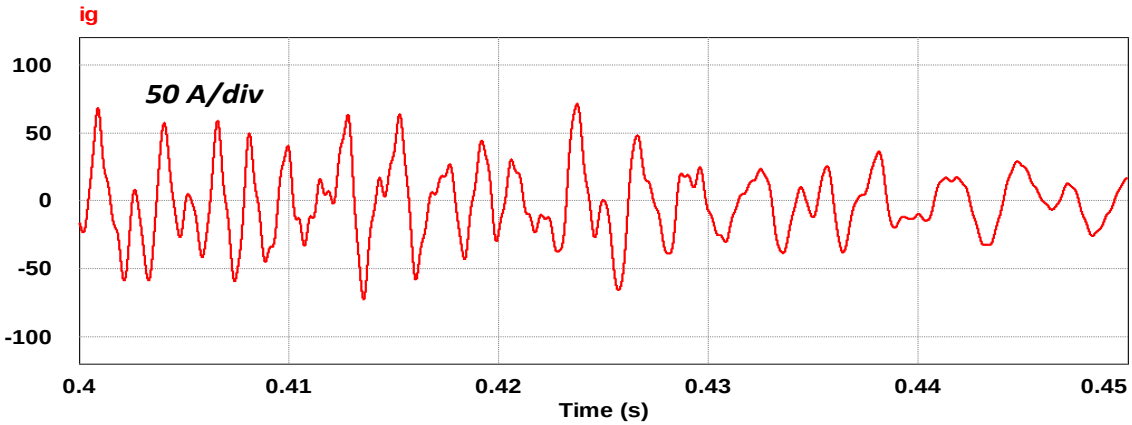
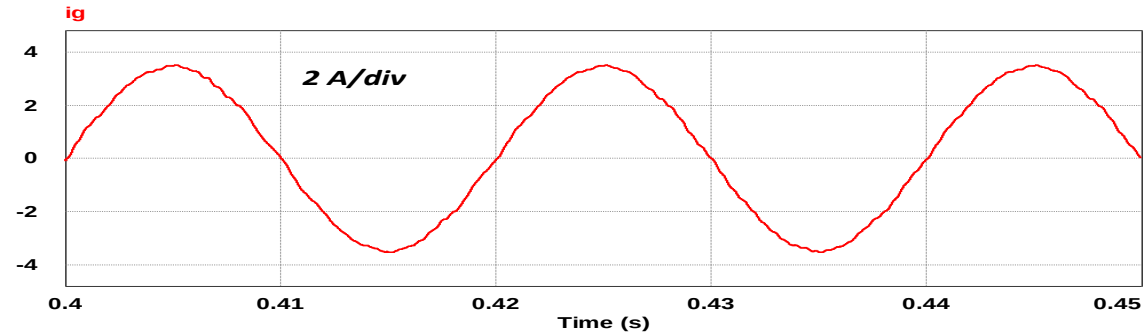


(c)

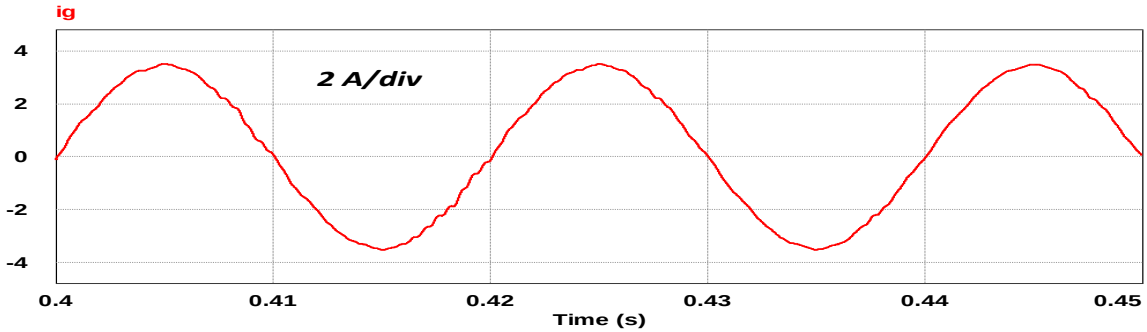
Figure 6.9: Effect of removing resonance damping notch filters on grid current: (a) DM and CM notch filters removal, (b) DM notch filter removal and (c) CM notch filter removal

6.2.2.4. Effect of Grid-Side Inductance Variation

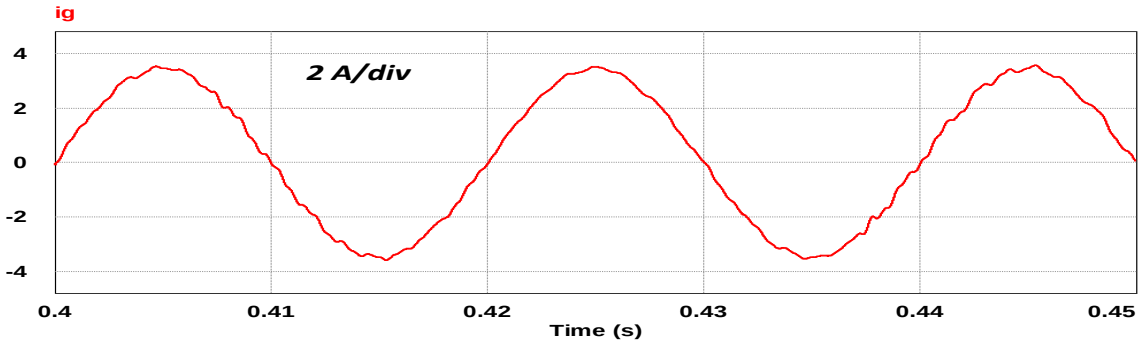
Interfacing with different grids, results in unexpected variation in grid-side inductance. Unfortunately, this grid-side inductance variation deviates the DM resonance frequency. Consequently, affecting the system stability. A common solution is to design the DM notch filter with adaptive configurations. Meaning that, there should be an estimation of the grid-side inductance prior to control activation. However, in our design, the DM notch filter center frequency is little lower than the LCL resonance frequency and the filter bandwidth is large. As a result, grid-side inductance variation effect would be limited. Figure 6.10 shows the grid-side inductance increase relation with the grid current THD%. As illustrated earlier in 5.2.2, the CM notch filter is not affected by grid-side inductance variation.



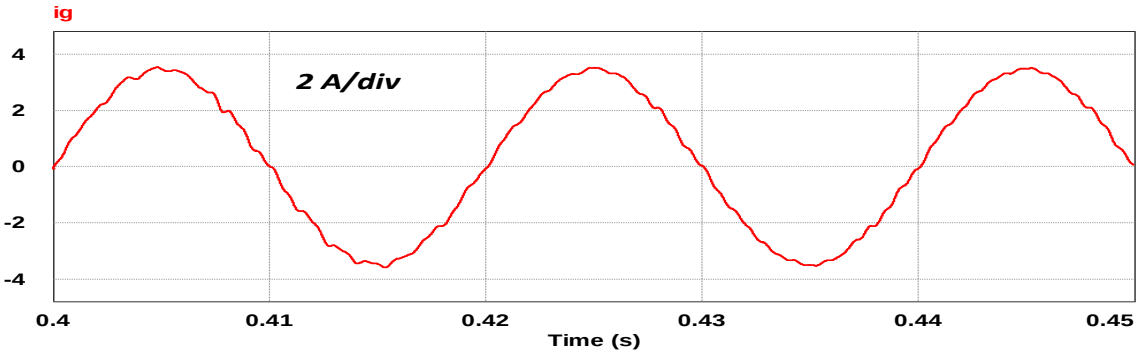
(a) THD=1.68%



(b) THD=2.19%



(c) THD=2.23%



(d) THD=2.61%

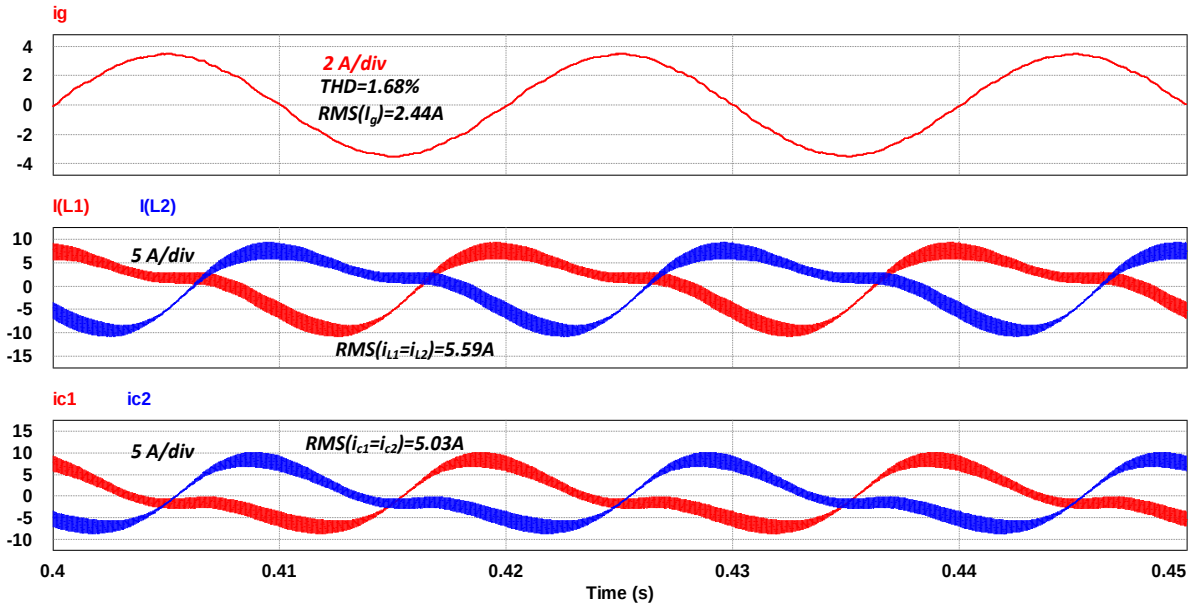
Figure 6.10: Effect of grid-side inductance increase on the grid current: (a) 0% increase, (b) 25% increase, (c) 50% increase and (d) 100% increase

6.3. Efficiency of the System (Active Resonance Damping)

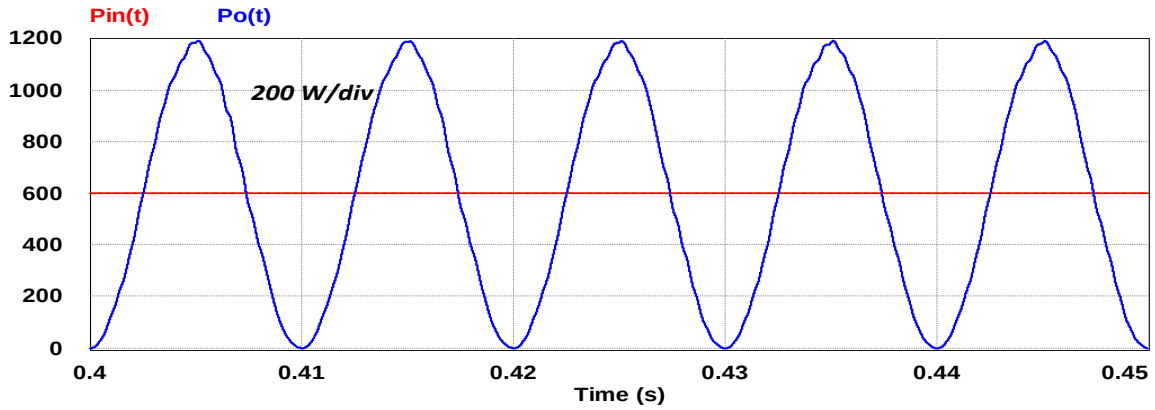
The efficiency of the system improved enormously - around 20W increase in output power- with active resonance damping control. This is due to passive damping resistor avoidance. The losses are calculated by observing different current waveforms and measuring their RMS values. Specifically, Figure 6.11 and Table 6.4 summarize the overall results regarding system efficiency.

Table 6.4: Currents RMS values and power losses (Active damper control)

$\boldsymbol{i_{c_1}(RMS) = i_{c_2}(RMS)}$	$\boldsymbol{i_{L_1}(RMS) = i_{L_2}(RMS)}$	$\boldsymbol{i_{L_{g_1}}(RMS) = i_{L_{g_2}}(RMS) = i_g(RMS)}$
5.03A	5.59A	2.44A
$\boldsymbol{P_{Loss}(c_1 \& c_2)}$	$\boldsymbol{P_{Loss}(L_1 \& L_2)}$	$\boldsymbol{P_{Loss}(L_{g_1} \& L_{g_2})}$
0.086W	0.81W	0.14W
$\boldsymbol{P_{Loss}(MOSFET)}$	$\boldsymbol{P_{in}(Average)}$	$\boldsymbol{P_{out}(Average)}$
13.36W	600W	585.6W
$\boldsymbol{\eta}$%	97.6%	



(a)



(b)

Figure 6.11: Efficiency calculation waveforms (Active damper control): (a) Currents waveforms and (b) instantaneous output power waveform compared to the input power

Chapter 7 : Conclusion & Future Work

7.1. Conclusion

This thesis presented a transformerless microinverter that has enhanced: (i) safety, (ii) reliability and (iii) efficiency. An evaluation study conducted to test the existing microinverter configurations performance regarding two aspects: (i) the amount of the circulating leakage current and (ii) the possibility to decouple transisorlessly the second order harmonic power ripples. The study concluded that the differential buck DC/AC converter has the lowest leakage current circulation and it is capable of decoupling the second order harmonic power ripples with the minimum number of switches. In other words, the differential buck configuration is the most reliable and safe design that can be adopted in the DC/AC conversion stage of the non-isolated microinverter.

The differential buck is controlled in two simultaneous operating modes: (i) DM to inject a sinusoidal current into the gird and (ii) CM to decouple the power ripples in the AC-side. Nevertheless, in grid-connected PV applications the differential buck configuration with LC or LCL output filter requires proper resonance damping control. Besides, it turns out that the resonance occurs in both modes. Thus, this thesis proposed two resonance damping control schemes with the LCL differential buck microinverter:

(i) Passive resonance damping control

(ii) Active resonance damping control

The passive control was based on feedback linearization techniques and passive damping through resistors series connection, they decreased the efficiency of the DC/AC

conversion stage ($\eta\% = 94.4\%$) and required 6 sensors. In contrast, the active control was based on cascading two notch filters and required 4 sensors only. The two damping notch filters center frequencies were obtained after modeling the non-ideal differential buck microinverter with small signal analysis. Contrary to the passive control, the active damping control improved the efficiency of the system ($\eta\% = 97.6\%$), but increased the grid current THD. The proposed techniques for improving the efficiency, reliability, and low leakage current in microinverter, were validated through extensive simulation of a 600W microinverter model using non-ideal components.

7.2. Future Work

This thesis focused mainly on designing, modeling, and controlling the DC/AC converter stage of the non-isolated microinverter in grid-connected applications. The thesis work could be expanded in many ways. For instance, test the controllers and filters on HIL system. Then, build a prototype and implement the proposed techniques. The other option is to design adaptive notch filters that are based on online methods to estimate the grid-side inductance prior the control activation (online estimation of the resonance frequency in case of weak-grid connection). It is also possible to extend the design to consider a realistic components mismatch in contrast to the actual analysis which assumed symmetrical microinverter elements. Further work can include the MPPT controller and DC/DC converter.

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APPENDIX

A1: Components

The simulations of Chapter 6 were based on existing components. The components selected for both –Active and Passive - control schemes of the differential buck DC/AC converter are similar (Figure A1.1); the only difference is that the passive control needs two additional damping resistors in series with the each output capacitor and two extra current sensors. The extra two sensors are for sensing the output capacitors current. Note that, because of the CM operation the microinverter-side inductance (L_1 and L_2), the two output capacitors (C_{o1} and C_{o2}) and the MOSFETs ratings increased compared to conventional inverter.

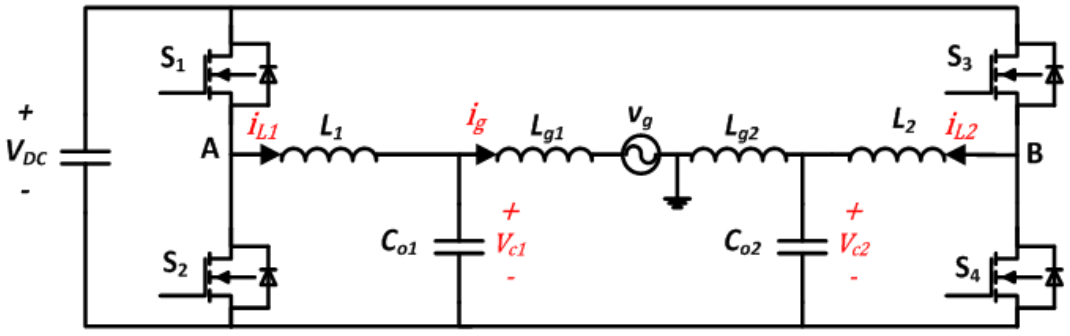


Figure A1.1: Differential buck microinverter

The list below summarizes the components used:

- DC/AC MOSFET (STB18NM80): *800V*, *17A*, $R_{DS(ON)}$ =300*m*Ω, V_{SD}=*1.6V* and $R_{GS(th)} = 4V$.

- Microinverter-side inductance (Hammond 195C20): *600V, 20A,* $L_1 = L_2$ *=1mH,* and $R_{L1} = R_{L2}$ *= 13m*Ω
- Grid-side inductance (Bourns 5711-RC): *600V, 9.5A,* $L_{g1} = L_{g2}$ *=50uH,* and $R_{Lg1} = R_{Lg2}$ *= 12m*Ω
- Output film capacitor (TDK B32778J1127K000): *1300V, 58.5A,* $C_{o1} = C_{o2} = 120uF$, $R_{C_{o1}} = R_{C_{o2}}$ *= 1.7m*Ω
- DC-Link film capacitor (TDK B32778J0606K000): *1100V, 34.5A,* $C_{DC\_Link} = 60uF$, $R_{C_{DC\_Link}}$ *= 4.1m*Ω

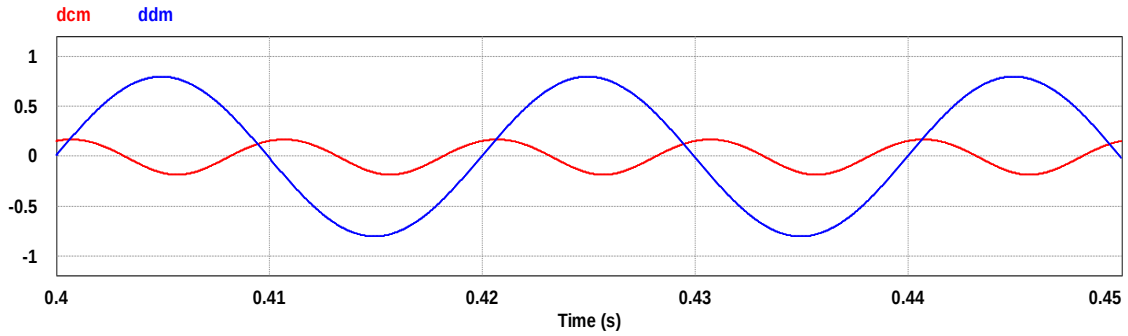
Notice the high ratings of the reliable film capacitors; even with small capacitance value.

A2: Waveforms

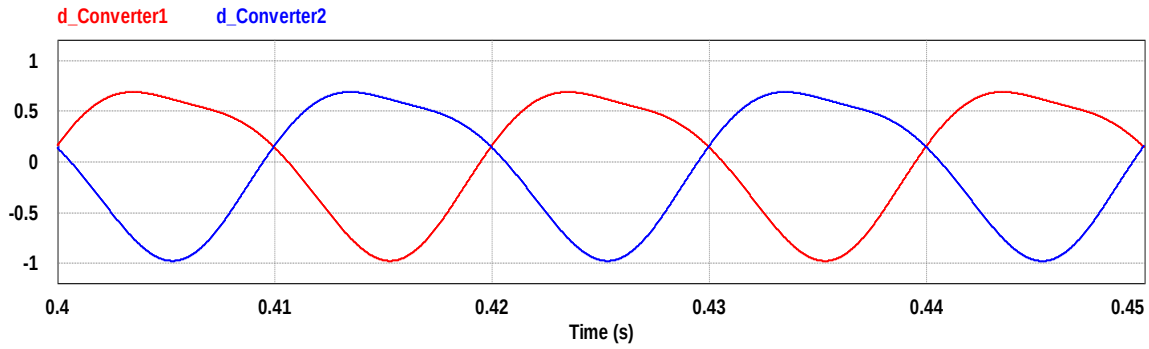
Appendix 2 shows all waveforms. The waveforms are viewed for a time window of 0.05sec; specifically, from t=0.40 sec to t=0.45 sec. Waveforms are not restricted to voltage and current only; duty cycles are also observed.

A2.1. Passive Resonance Damping Controller Waveforms

A2.1.1. Duty Cycles



(a)



(b)

Figure 0.2: Duty cycles (Passive): (a) DM and CM duty cycles, and (b) each microinverter leg duty cycle

A2.1.2. Currents

A2.1.2.1. AC currents

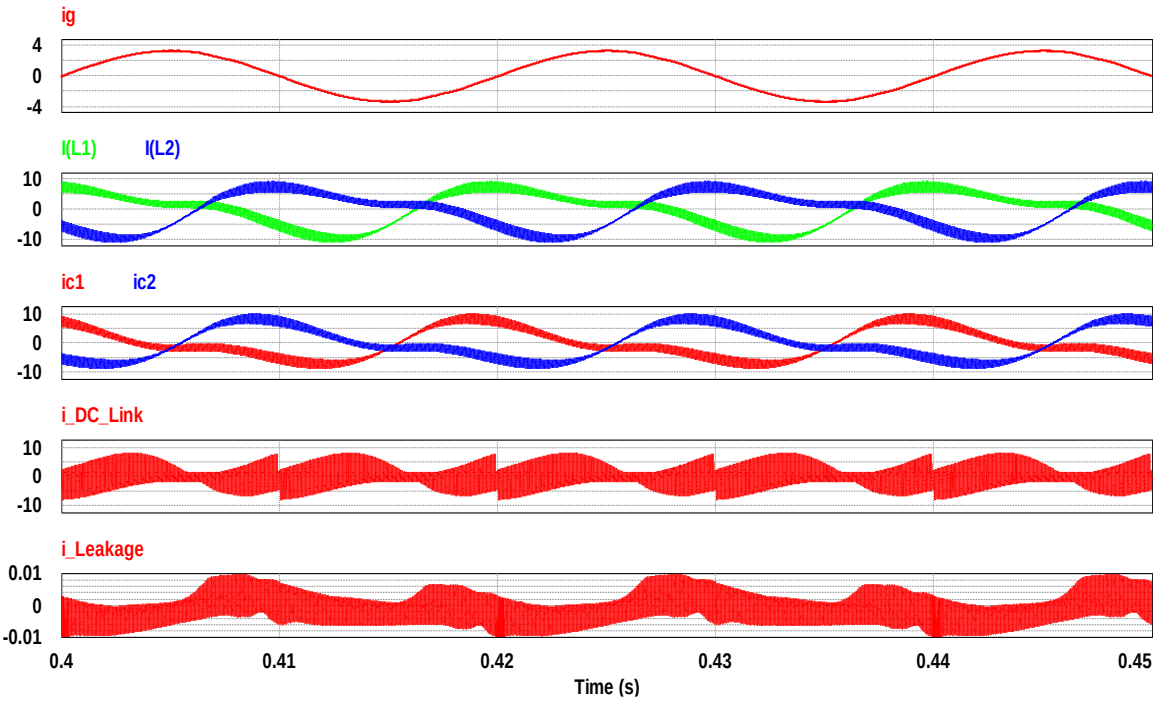


Figure A2.3: AC Current waveforms (Passive): i_g (2 A/div), i_{L1} (5 A/div), i_{L2} (5 A/div), i_{C1} (5 A/div), i_{C2} (5 A/div), i_{DC_Link} (5 A/div) and $i_{Leakage}$ (2 mA/div)

A2.1.2.2. DC Current

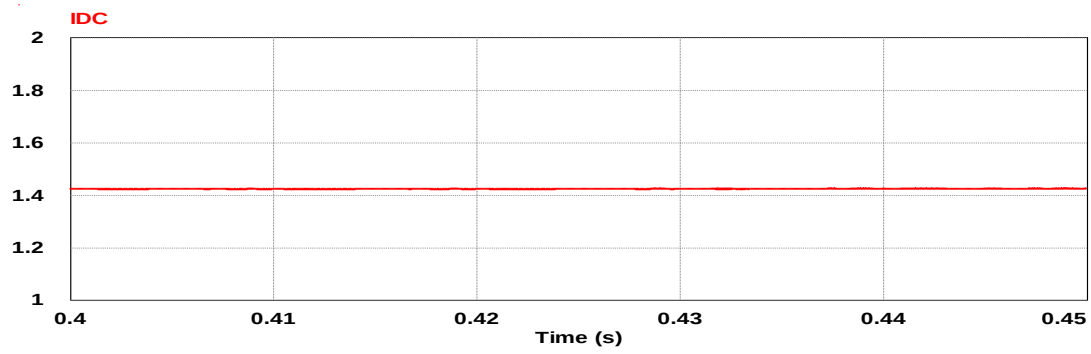


Figure A2.4: DC supply current (Passive) (0.2 A/div)

A2.1.3. Voltages

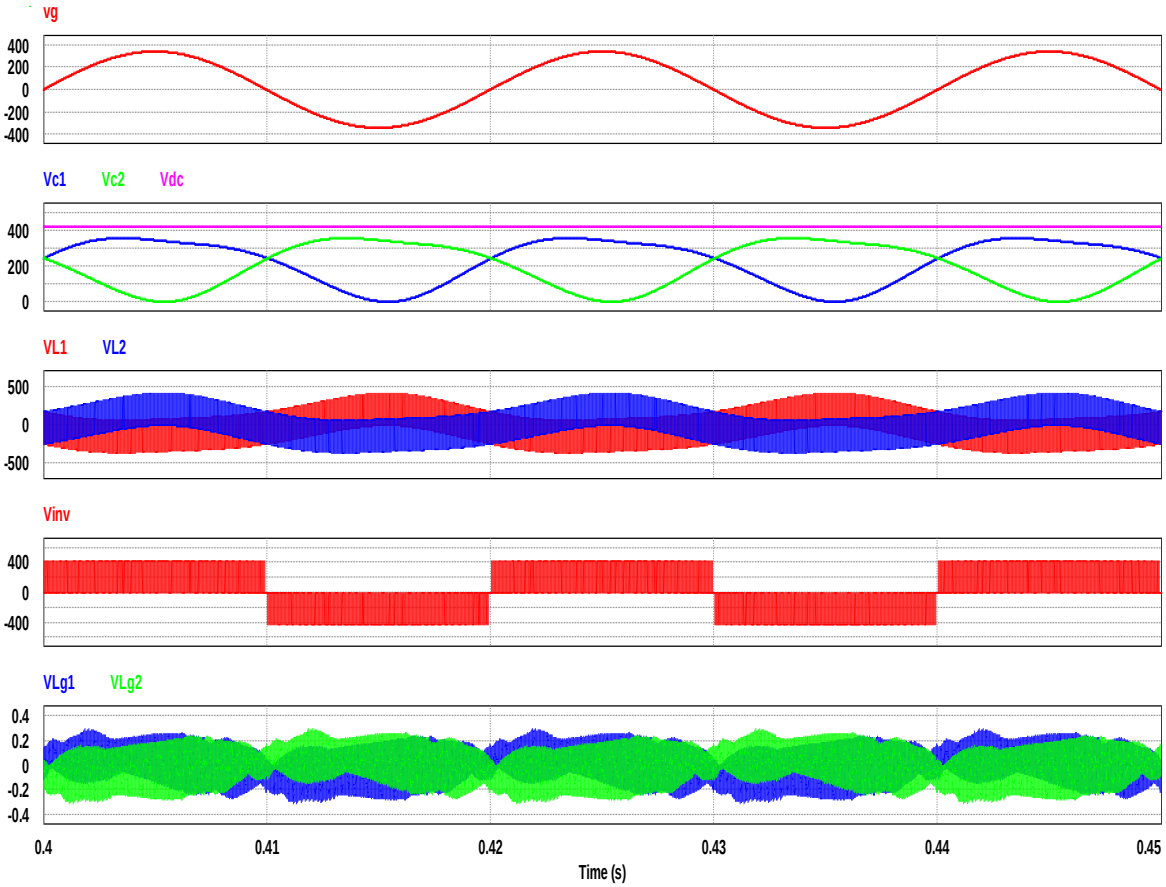
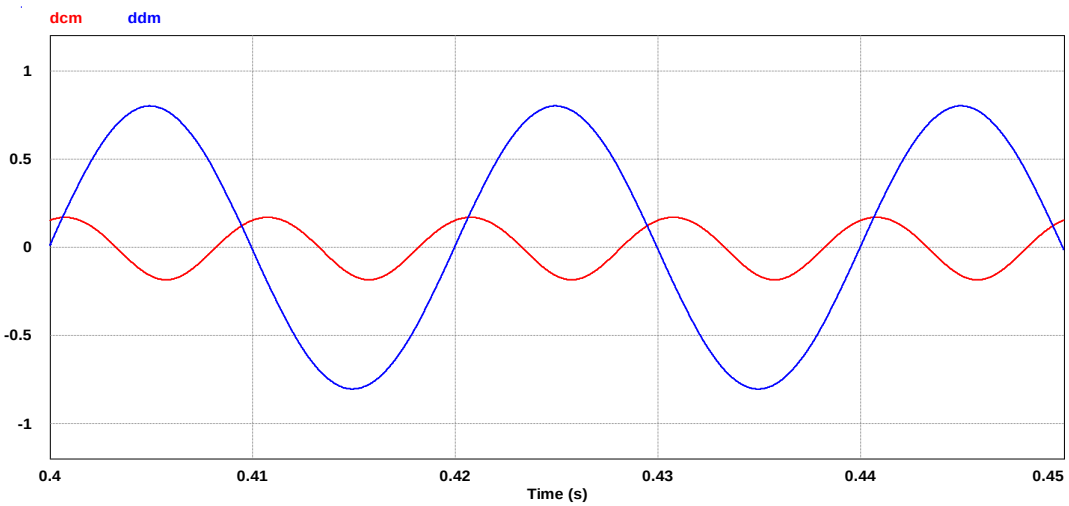


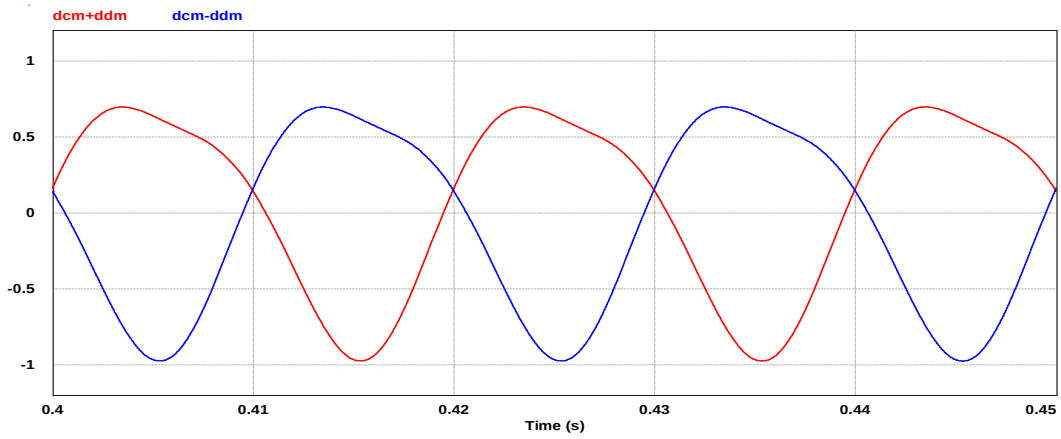
Figure 0.5: Voltage waveforms (Passive): v_g (200 V/div), v_{C1} (100 V/div), v_{C2} (100 V/div), V_{DC} (100 V/div), v_{L1} (500 A/div), v_{L2} (500 V/div) and v_{inv} (200 V/div), v_{Lg1} (0.2 V/div) and v_{Lg2} (0.2 V/div)

A2.2. Active Resonance Damping Controller Waveforms

A2.2.1. Duty cycles



(a)



(b)

Figure 0.6: Duty cycles (Active): (a) DM and CM duty cycles, and (b) each microinverter leg duty cycle

A2.2.2. Currents:

A2.2.2.1. AC currents

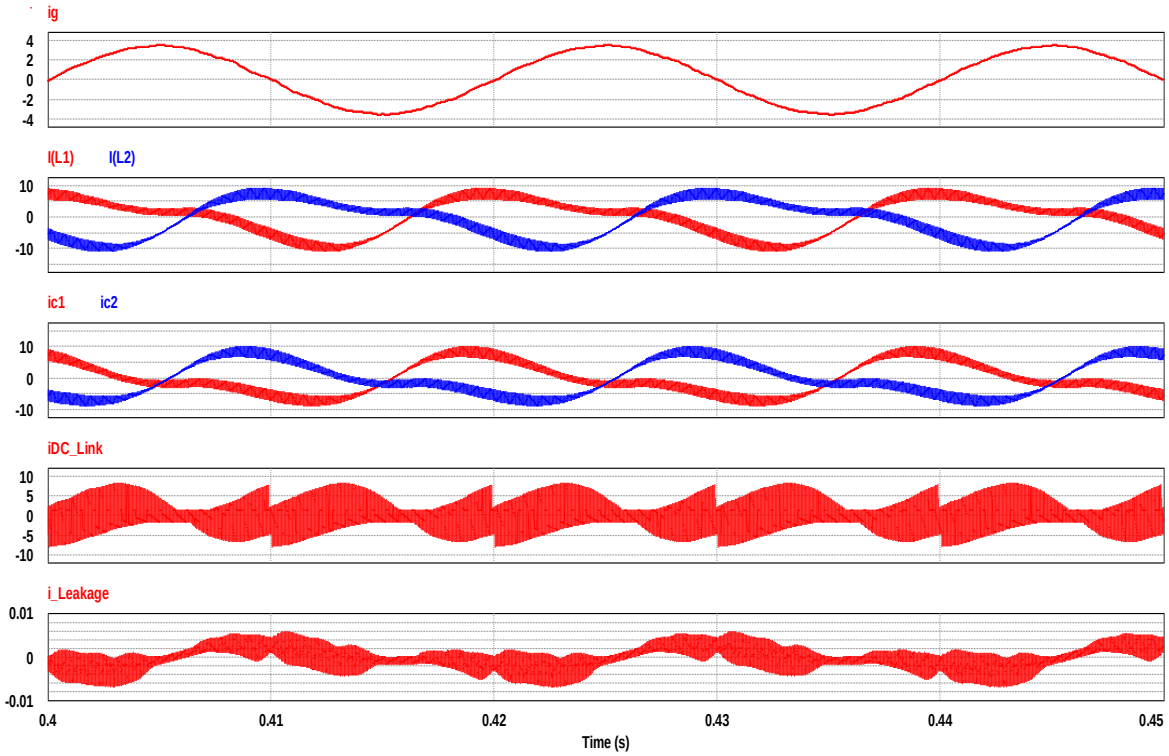


Figure A2.7: AC Current waveforms (Active): i_g (2 A/div), i_{L1} (5 A/div), i_{L2} (5 A/div), i_{C1} (5 A/div), i_{C2} (5 A/div), i_{DC_Link} (5 A/div) and $i_{Leakage}$ (2 mA/div)

A2.2.2.2. DC currents

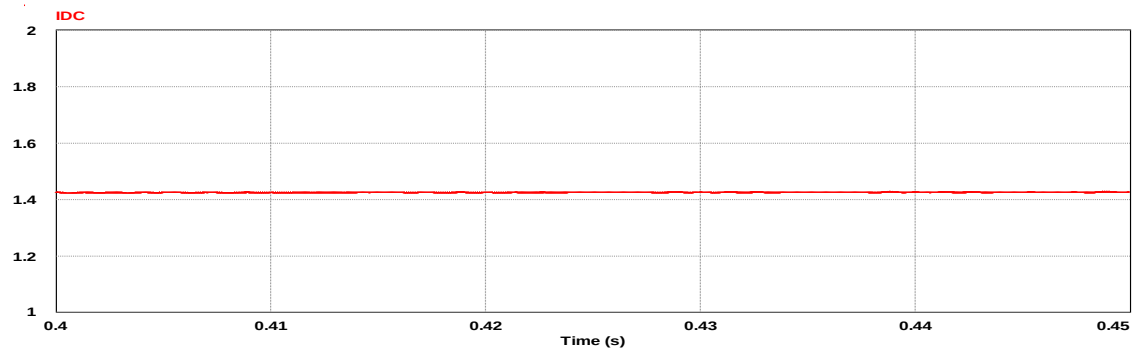


Figure 0.8: DC supply current (Active) (0.2 A/div)

A2.2.3. Voltages

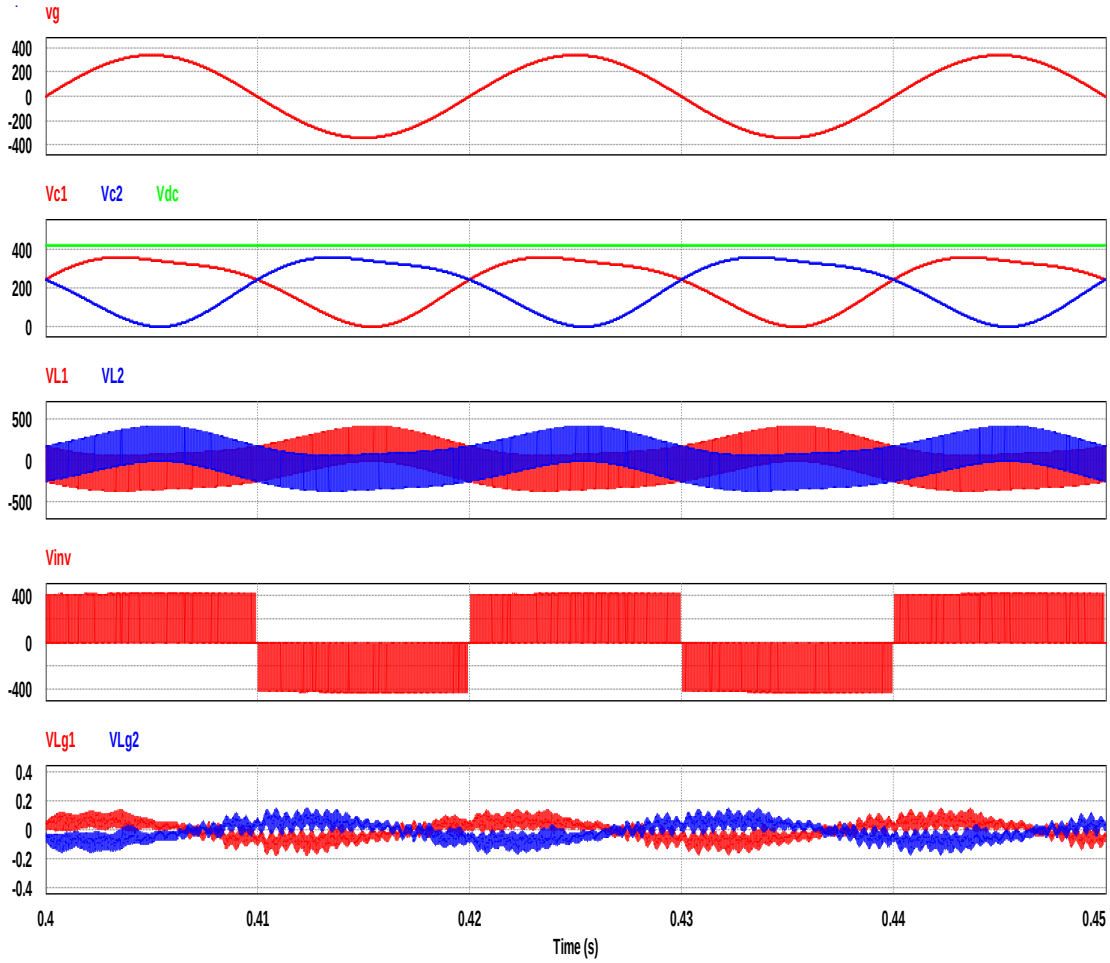


Figure A2.9: Voltage waveforms (Active): v_g (200 V/div), v_{C1} (200 V/div), v_{C2} (200 V/div), V_{DC} (200 V/div), v_{L1} (500 A/div), v_{L2} (500 V/div) and v_{inv} (200 V/div), v_{Lg1} (0.2 V/div) and v_{Lg2} (0.2 V/div)