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ORIGINAL RESEARCH

A hybrid half-bridge submodule-based DC–DC modular multilevel converter with a single bidirectional high-voltage valve

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Abstract

Modular Multilevel Converters (MMCs) are promising candidates for high-voltage high-power applications. The main challenge of the MMCs is the zero-frequency operation. To achieve a successful DC–DC conversion process with balanced capacitors' voltages with limited voltage ripple, this paper suggests the employment of the conventional two-leg half-bridge submodule-based MMC structure in conjunction with a single bidirectional high-voltage (HV) valve across the low-voltage side. In the suggested structure, the HV valve is controlled on and off to ensure energy equalization for the MMC arms. In addition, soft-switching for the HV valve is proposed to reduce the switching losses. Detailed illustration and design of the proposed concept are presented. Simulation and experimentation results are elucidated to show the effectiveness of the proposed DC–DC hybrid MMC. The results showed efficient performance of the suggested converter.

1 | INTRODUCTION

The electric power transfer between two or more locations can be achieved via AC or DC technology [1]. Recently, with the high penetration of renewable energy resources, the need for DC transmission is significantly increased. The DC–DC converter is the main element in the DC grids to interconnect two DC voltages with different levels with bidirectional power flow capability. The main challenge is to implement high-voltage high-power DC–DC converters to meet the requirements of the high-voltage DC grids [2].

Modular Multilevel Converters (MMCs) are promising candidates in high-voltage high-power applications [3–7] due to their modularity, scalability, and redundancy [8–10]. The operation of conventional DC–AC MMC is based on having a bipolar arm current, which allows charging and discharging of the arm capacitors during the operation to keep them bounded in a particular voltage window. The main challenge is the operation of conventional MMCs under low-output frequency, where the capacitor voltage ripple of the involved submodules (SMs) is inversely proportional to the output frequency [11–13]. On the other hand, the DC–DC operation of the conventional MMC fails to keep the voltages of the capacitors balanced due to having a unipolar arm current in this condition, which allows just charging or discharging of the involved arm capacitors according to the arm current direction leading to energy drift of the converter upper and lower arms, that is, capacitors voltages divergence [14].

For isolated DC–DC high-power converters, DC–AC MMCs can be employed to interconnect two different DC voltage levels via applying the Dual Active Bridge (DAB) concept [15, 16]. For the non-isolated DC–DC MMCs, different techniques have been presented in literature to ensure successful DC–DC conversion. Some of these techniques use the conventional structure with high-frequency AC current injection within the converter arms [17, 18]. In this technique, the switches of the involved SMs suffer from over-current stresses and increased power losses [18], that is, proper control of the injected AC circulating current is essential to ensure operation with enhanced efficiency. In [19], the polyphase cascaded-cell modular DC–DC converter concept has been proposed, where the structure is similar to the operation of the MMC for polyphase DC–AC conversion. However, the AC voltages and currents are employed to ensure energy equalization conditions for the converter arms, which requires a relatively large number of semiconductor devices.

In [20, 21], conventional MMC legs are employed along with energy equalization modules (EEMs) to ensure energy equalization of the converter arms. The EEMs used extra semiconductor devices and isolating transformers affecting the converter cost. In [22], a modified MMC has been presented, where distributed semiconductor switches are used to enable the parallel connection between the arms capacitors. In this technique, boosting capability is associated with the operation that elevates the SM capacitors' voltage above the nominal voltage level.

In [23], the arm current reversal concept has been presented for one-leg half-bridge SM-based DC–DC MMC, where two successive stages are employed, namely, the DC–AC stage to generate square wave AC output voltage and AC–DC rectification stage. Both stages are based on half-bridge SMs. The DC–AC stage requires bulk DC capacitors, but the AC–DC stage requires small DC capacitors as the small DC capacitor is used as a snubber circuit to clamp the voltage of the half-bridge SM, not to store the energy to be delivered to the load [24]. On the other hand, DC–DC hybrid MMCs have been proposed in literature to accomplish the DC–DC conversion process successfully, while employing MMC Half-bridge or full-bridge SMs in conjunction with HV valves.

In [25, 26], different versions of self-balanced non-isolated hybrid DC–DC MMC for medium-voltage DC grids have been presented. The main drawback of this approach is the high current stresses at the common low-voltage cell. In [27], different versions of DC–DC hybrid MMCs employing half-bridge SMs or full-bridge SMs in conjunction with HV-valves have been presented with a soft-switching operation for the involved HV vales. In the presented approaches, a relatively large number of HV valves are employed. In [28], the arm interchange concept has been presented in two stages. This approach requires a relatively large number of semiconductor devices and HV valves. In addition, the employed HV valves increase the converter losses due to their relatively high conduction and switching losses. In [29], the aforementioned arm current reversal approach has been employed, but the second stage half-bridge SMs (4 arms) are replaced by series-connected switches-based HV valves (4 valves). The valves are operated under zero-voltage switches to reduce the converter switching losses, that is, enhance the converter efficiency. In addition, zero-voltage switching of the HV valve makes the design of voltage equalization elements for the valve series-connected switches easier compared to the hard-switching option [30]. However, still, a relatively large number of HV valves are needed.

This paper proposes a hybrid DC–DC MMC converter to connect two different DC voltage levels: the high-voltage side (HVS) and the low-voltage side (LVS). The proposed converter consists of conventional two-legs (H-bridge) half-bridge SM-based MMC in conjunction with a single bidirectional HV valve connected across the low-voltage side. The HV valve is controlled on and off to ensure energy equalization among the involved arms. The HV valve is turned off during the conventional operation of MMC, where the capacitors' voltages start to diverge due to the unipolar arm currents, while it turned-on during the equalization period at which the arm capacitors are connected in parallel to ensure the energy equalization among the converter arms.

The main contributions of the presented converter are:

- Proposing a Hybrid DC–DC MMC converter with a single bidirectional HV valve, that is, a reduced number of HV valves are employed compared to the other existing hybrid DC–DC MMC,
- A methodology to operate the involved HV valve under soft-switching is presented which reduces the switching losses.

The main advantage of the proposed converter is employing the conventional MMC legs with HB-SMs and a single bidirectional HV valve to perform DC–DC conversion process with balanced capacitors' voltages with limited voltage ripple, that is, operating with a reduced number of HV valves compared to the existing hybrid DC–DC MMCs. On the other hand, the main disadvantage of the proposed approach is that the current stresses during the equalization period are high due to the parallel connection of different branches having different initial voltages. This necessitates the employment of switches with a proper pulsed current rating to withstand current during the equalization period.

The following sections present detailed illustrations, design, and assessment of the proposed converter. The methodology of soft-switching for the involved HV valve is also presented. A simulation model for the proposed converter is built to show the dynamic behavior of the converter during different conditions. Finally, a down-scaled prototype for the proposed converter has been implemented for experimental validation.

2 | DC–DC CONVERSION OF THE CONVENTIONAL MMC

In the two-leg-based MMC converter shown in Figure 1, each leg has upper and lower arms (u_1 and L_1 for leg1) and (u_2 and L_2 for leg2). Each arm has N cascaded half-bridge SMs, each rated at V_{dc}/N in series with arm inductance (L_{a}), where V_{dc} is the input DC voltage. Each SM has a positive or zero output voltage state. The positive voltage state (V_{dc}/N) can be achieved by turning on the upper IGBT of the SM, while the zero-voltage state is achieved by turning on the lower IGBT of the SM. Each arm SMs are controlled to generate unipolar arms voltages, where if the desired output voltage average, namely, V_{o} is defined to be a constant value of (αV_{dc}) where α is less than unity; the corresponding arms voltage references are given by;

$$v_{u1} = v_{L2} = 0.5\,V_{dc} - 0.5V_o = 0.5V_{dc}\,(1-\alpha) \quad (1)$$

$$v_{L1} = v_{u2} = 0.5V_{dc} + 0.5V_o = 0.5V_{dc}(1+\alpha) \quad (2)$$

where v_{uk} and v_{Lk} are the upper and lower arm voltage references of the k^{th} leg, where $k = 1$ or 2 and V_o is the desired average output voltage, that is, $\alpha = V_{\mathrm{o}}/V_{\mathrm{dc}}$. The arm currents can be expressed in terms of output current as follows;

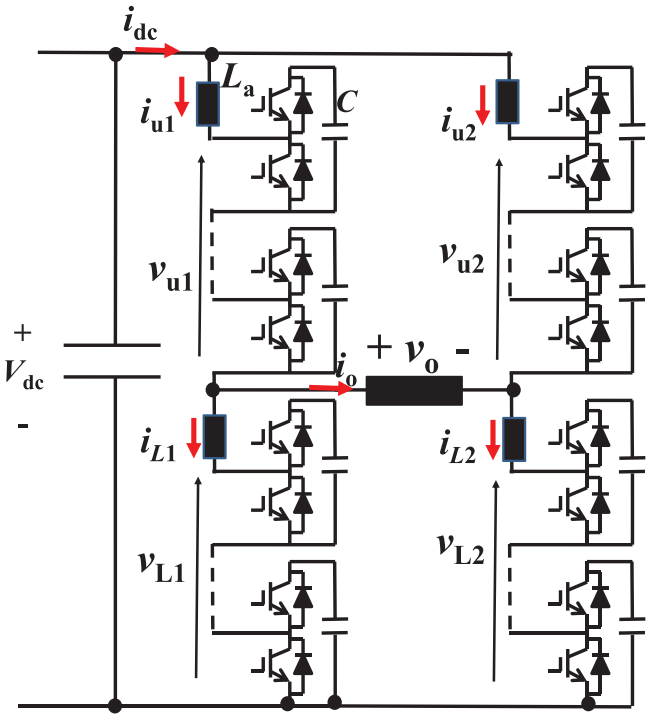


FIGURE 1 Conventional two-leg half-bridge SM-based MMC.

$$i_{u1} = i_{L2} = 0.5\, i_o\,(\alpha + 1) \tag{3}$$

$$i_{u2} = i_{L1} = 0.5\, i_o\,(\alpha - 1) \tag{4}$$

where i_{uk} and i_{Lk} are the upper and lower arm current of the k^{th} leg, where $k = 1$ or 2, and i_o is the output current.

Unlike the DC–AC conversion process, the arm currents in the DC–DC conversion are unipolar, that is, positive or negative, allowing the arm capacitors to charge or discharge.

As a result, capacitor voltage divergence occurs, and the capacitors voltages cannot be kept bounded within a certain voltage window. To resolve this issue, a new hybrid DC–DC MMC is proposed in this paper, where the conventional structure of MMC, shown in Figure 1, is employed in conjunction with a bidirectional HV-valve to ensure a successful DC–DC conversion process with balanced capacitors voltages with limited voltage ripple.

3 | THE PROPOSED HYBRID DC–DC MMC

A novel hybrid DC–DC MMC is proposed in this work to maintain successful DC–DC operation with balanced capacitors voltages of the MMC shown in Figure 1, where a bidirectional HV valve rated at the HVS voltage level is connected across the output terminals as shown in Figure 2. An inductive output filter (L_f) is connected in series to the LVS (V_{dcL}) to have a smoothed DC current at the LVS (i_{dcL}). This converter can be used effectively in medium-/high-voltage DC grids to

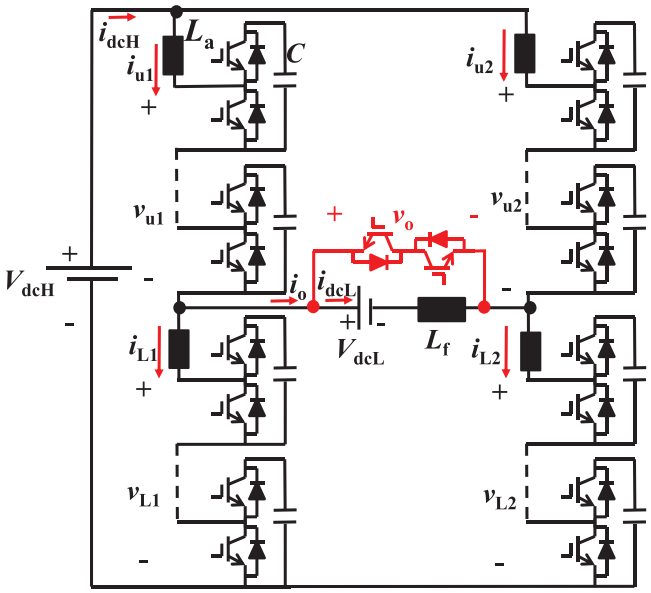


FIGURE 2 The proposed hybrid DC–DC MMC.

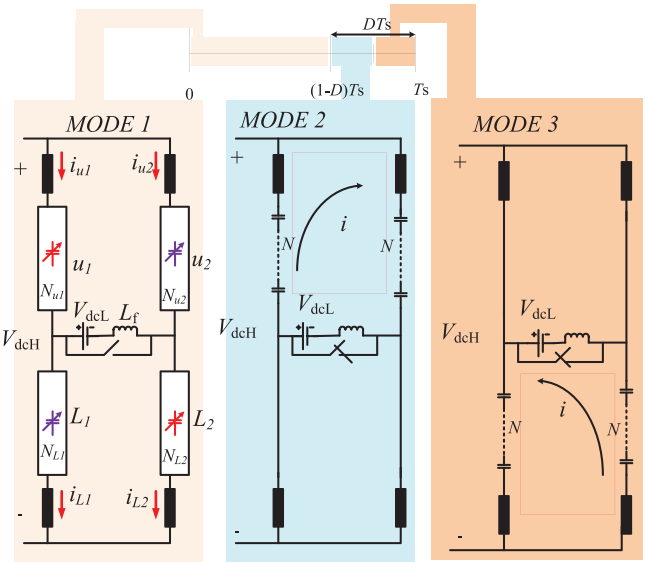


FIGURE 3 Modes of operation without soft-switching of the HV valve.

interconnect between different voltage levels, namely, V_{dcH} and V_{dcL}, as shown in Figure 2, where V_{dcH} is the voltage of the HVS, and V_{dcL} is the voltage of the LVS. The employed HV valve is operated with a moderate switching frequency ($1/T_s$), which is lower than the switching frequency of the employed multilevel modulation technique. The HV valve has a specific low duty cycle, namely, D. The HV valve duty cycle is split equally, as shown in Figure 3, where when the HV valve is turned on, in the first half of turn-on time, all cells of the upper arms are activated while the lower arms are deactivated. As a result, the capacitors of the upper arms are connected in parallel, enabling energy transfer between arms (energy equalization). In the second half of the turn-on time of the high-voltage valve, the upper arms cells are deactivated, while

all cells of the lower arms are activated to enable the parallel connection of lower arms and energy transfer. To ensure successful operation, small arm inductance should be employed to ensure fast energy equalization between upper/lower arms. Nevertheless, as a result, arm current spikes are associated with the operation due to the equalization action.

It has to be noted that the capacitor voltage ripple in the proposed approach depends on a predefined frequency of the equalization process; whereas this frequency increases, the capacitor voltage ripple decreases, but the converter switching loss increases.

3.1 | Operation without soft-switching of HV valve

To ensure capacitors voltages equalization, the operation of the converter is divided into three modes of operation, as shown in Figure 3, which are defined as follows;

Mode 1: (1-*D*)T_s > t ≥ 0

During this mode, the HV valve is turned off. This mode lasts for (1-*D*)T_s, where *D* and T_s are the duty cycle and switching periodic time of the involved HV valve. In this mode, the conventional control of MMC with the desired dc output voltage references is applied, where based on Figure 2, for an average output voltage reference of αV_{dc}, the upper and lower arm voltage references are given by;

$$v_{u1} = v_{L2} = \frac{V_{dc}}{2}(1-\alpha),\quad v_{L1} = v_{u2} = \frac{V_{dc}}{2}(1+\alpha) \tag{5}$$

The corresponding arm currents in this mode are given by;

$$i_{u1} = i_{L2} = \frac{i_o}{2}(\alpha+1),\quad i_{u2} = i_{L1} = \frac{i_o}{2}(\alpha-1) \tag{6}$$

Based on Figure 2, if the output current is positive, based on (6), the currents i_{u1} and i_{L2} will be positive, while the currents i_{u2} and i_{L1} will be negative. As a result, the upper capacitors of the first leg and lower capacitors of the second leg are charged, that is, their voltages increase above the nominal value of capacitor voltage, namely, V_{dcH}/N, while the upper capacitors in the second leg and lower capacitors in the first leg are discharged, that is, their voltages decrease below the nominal value of capacitor voltage. As a result, capacitor voltage divergence occurs, and the capacitor voltages of (u_1 and L_2) arms will be higher than those of (u_2 and L_1) arms at the end of this mode. At the end of this mode, the summation of capacitor voltages in the upper arm is higher than V_{dcH}, while the summation of capacitor voltages in the lower arm is less than V_{dcH}.

Mode 2: (1−0.5*D*)T_s > *t* ≥ (1−*D*)T_s

To avoid divergence of capacitors' voltages, an equalization period is enabled for DT_s duration. The equalization period is divided equally into modes 2 and 3. During mode 2, the HV valve is turned on. Meanwhile, the upper arms of both legs are connected in parallel, and the lower arms are bypassed, which allows energy transfer between the converter upper arms. In mode 2, the arm with higher capacitor voltage (u_1) pushes the current to the arm with lower capacitor voltage (u_2) during this mode, which results in arm current reversal in both arms compared to mode 1, that is, bipolar arm currents are obtained by applying the equalization period, which results in energy equalization of the involved arms. To achieve that and ensure fast equalization, relatively small arm inductors should be employed.

The corresponding equivalent circuit is shown in Figures 4a and 4b in the time-domain and s-domain, respectively. Based on the aforementioned illustration of mode 1, the initial inductor currents for mode 2 are given by;

$$i_{u1(0)} = \frac{i_o}{2}(\alpha+1) \tag{7}$$

$$i_{u2(0)} = \frac{i_o}{2}(\alpha-1) \tag{8}$$

It is clear that for a positive output current, $i_{\mathrm{u1(0)}}$ is positive, and $i_{\mathrm{u2(0)}}$ is negative. On the other hand, the initial capacitor voltages are given by;

$$V_{Cu1(0)} = V_{dcH} + \Delta V_a \tag{9}$$

$$V_{Cu2(0)} = V_{dcH} - \Delta V_a \tag{10}$$

where ΔV_a is the total deviation of the summation of arm capacitor voltages from V_{dcH} at the end of mode 1. The corresponding expressions of arm currents in *s*-domain are given by;

$$I_{U1}(s) = \frac{\left(\frac{V_{dcH}}{s} + L_a i_{u1(0)} - \frac{V_{Cu1(0)}}{s}\right)}{\left(sL_a + \frac{N}{sC}\right)} \tag{11}$$

$$I_{U1}(s) = \frac{\left(\frac{-\Delta V_a}{L_a} + i_{u1(0)}s\right)}{\left(s^2 + \frac{N}{CL_a}\right)} = \sim \frac{\frac{-\Delta V_a}{L_a}}{\left(s^2 + \frac{N}{CL_a}\right)} \tag{12}$$

that is,

$$I_{U1}(s) \sim = \frac{-\Delta V_a}{\sqrt{\frac{NL_a}{C}}}\frac{\omega}{(s^2+\omega^2)} \tag{13}$$

where $\omega = \sqrt{N/CL_a}$. Similarly,

$$I_{U2}(s) \sim = \frac{\Delta V_a}{\sqrt{\frac{NL_a}{C}}}\frac{\omega}{(s^2+\omega^2)} \tag{14}$$

The currents in time-domain are given by;

$$I_{u1}(t) \sim = \frac{-\Delta V_a}{\sqrt{\frac{NL_a}{C}}}\sin(\omega t) \tag{15}$$

$$I_{u2}(t) \sim = \frac{\Delta V_a}{\sqrt{\frac{NL_a}{C}}}\sin(\omega t) \tag{16}$$

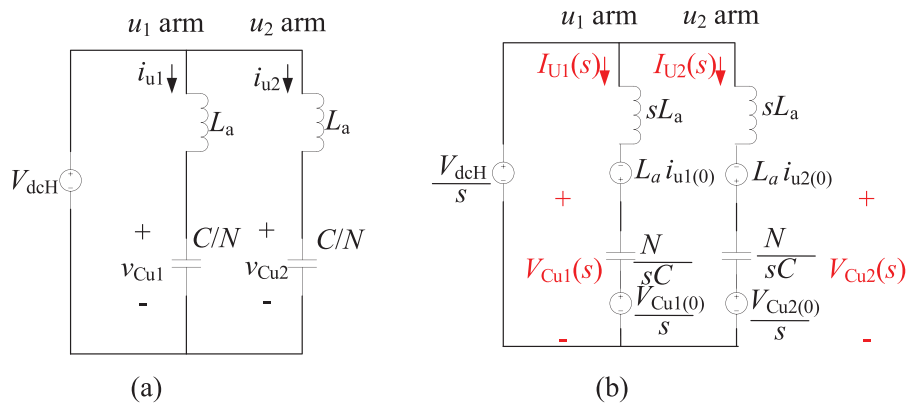


FIGURE 4 Equivalent circuit during mode 2 of the proposed approach. (a) In time-domain and (b) in s-domain.

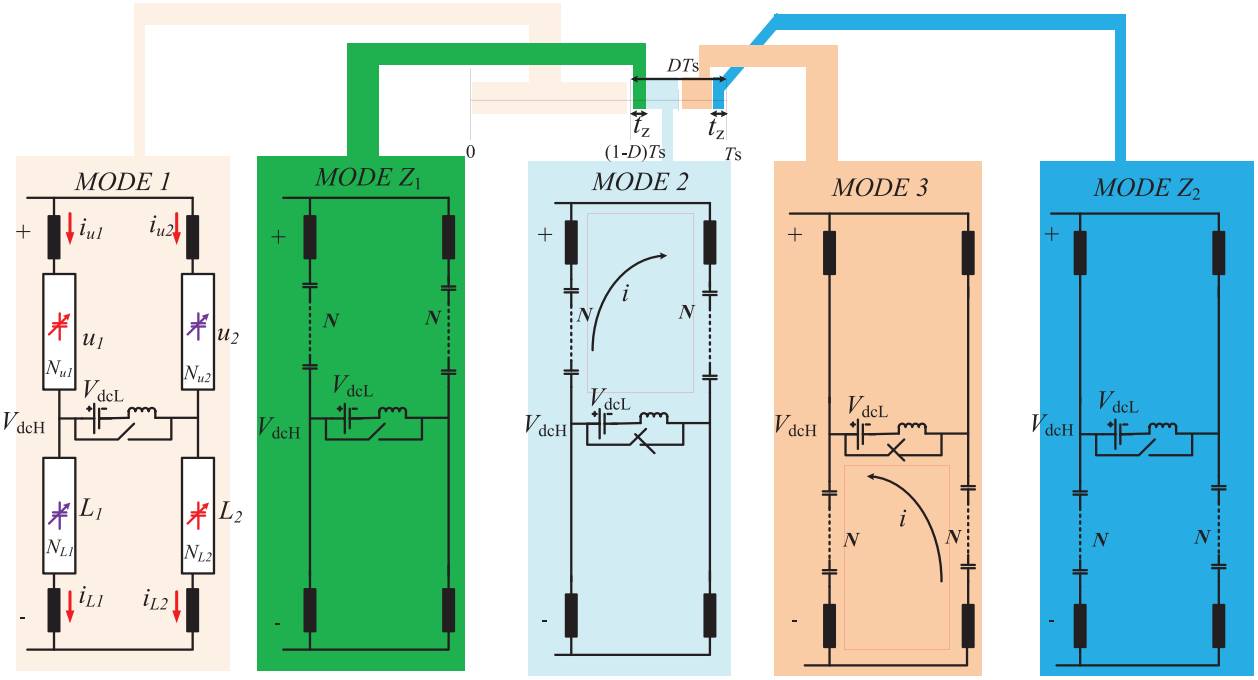


FIGURE 5 Modes of operation with soft-switching of the HV valve.

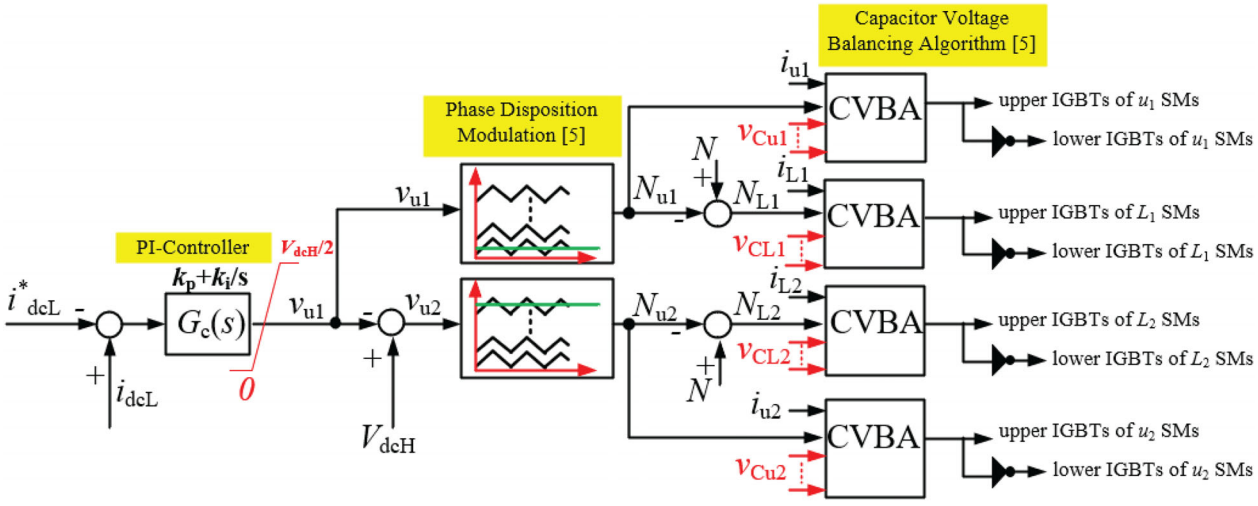


FIGURE 6 Closed-loop control of the proposed hybrid DC–DC MMC during Mode 1.

TABLE 1 Gate pulses of the involved IGBTS during the different operating modes in the presented approach.

	Mode1	Mode z_1	Mode 2	Mode 3	Mode z_2
Upper IGBTs of u_1 SMs	Based on Figure 6	ON	ON	OFF	OFF
Lower IGBTs of u_1 SMs	Based on Figure 6	OFF	OFF	ON	ON
Upper IGBTs of L_1 SMs	Based on Figure 6	OFF	OFF	ON	ON
Lower IGBTs of L_1 SMs	Based on Figure 6	ON	ON	OFF	OFF
Upper IGBTs of u_2 SMs	Based on Figure 6	ON	ON	OFF	OFF
Lower IGBTs of u_2 SMs	Based on Figure 6	OFF	OFF	ON	ON
Upper IGBTs of L_2 SMs	Based on Figure 6	OFF	OFF	ON	ON
Lower IGBTs of L_2 SMs	Based on Figure 6	ON	ON	OFF	OFF
HV Valve	OFF	OFF	ON	ON	OFF

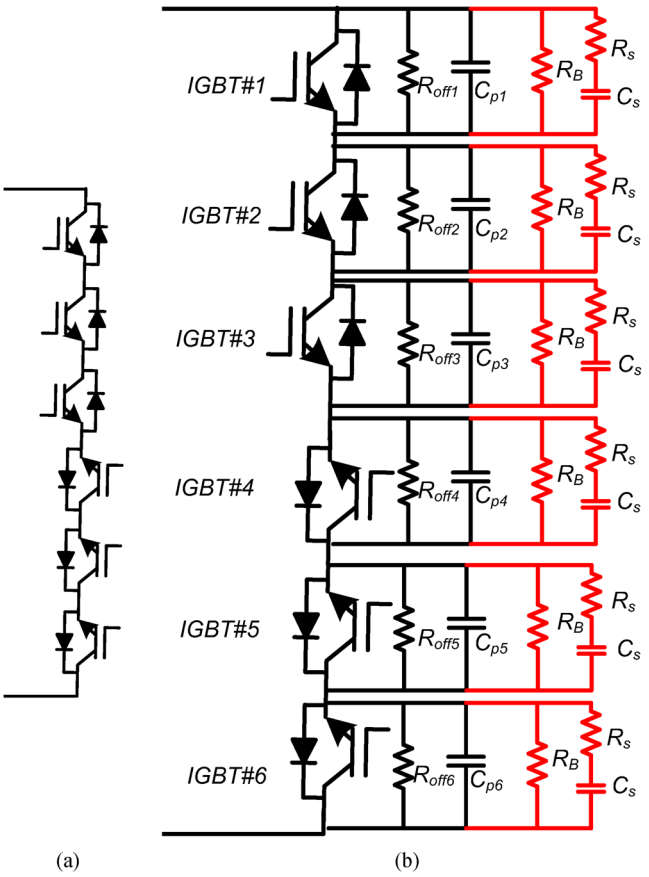


FIGURE 7 Series-connected IGBT-based bidirectional HV valve. (a) Structure, and (b) static and dynamic voltage-sharing elements (R_B, R_s, and C_s).

Based on (15) and (16), it is clear that the current is reversed in u_1 and u_2 at mode 2 compared to mode 1, which results in capacitor voltage equalization. To ensure having just one-half cycle of the current, that is, unipolar current, the circuit parameters should be adjusted such that the arm currents reach zero at the end of this mode. Similarly, for mode 3, but with lower arms.

Mode 3: $T_s > t \geq (1-0.5D)T_s$

During mode 3, the lower arms of both legs are connected in parallel while the upper arms are bypassed, as shown in Figure 3, to equalize the energy of the converter lower arms, where the arm with higher capacitor voltage (L_2) pushes the current to the arm with lower capacitor voltage (L_1) during this mode, that is, the arm currents in this mode is opposite to the arm current directions of mode 1, which results in capacitor voltage equalization in both lower arms (energy equalization) in mode 3.

The aforementioned modes (modes 1, 2, and 3) should be repeated continuously with the operation, which results in a successful DC–DC conversion process with balanced and bounded capacitor voltages. It has to be noted that the hard switching of the bidirectional HV valve significantly affects the converter efficiency. To enhance the operation, soft-switching of the HV valve can be employed, as illustrated in the following subsection.

3.2 | Operation with soft-switching of HV valve

To enable the soft-switching operation of the involved HV valve, two additional modes, namely, mode Z_1 and mode Z_2, should be added to the aforementioned modes (1, 2, and 3), as shown in Figure 5. The five modes for the operation with soft-switching of the HV valve can be summarized as follows;

Mode 1: $(1-D)T_s > t \geq 0$: In this mode, the conventional control of MMC with the desired dc output voltage references as described in section II-B is applied.

Mode Z_1: $t_z+(1-D)T_s > t \geq (1-D)T_s$: All SMs of the upper arms are activated, while all SMs of the lower arms are deactivated (bypassed), which forces zero voltage across the HV valve before turning it on, that is, soft-switching is achieved.

Mode 2: $(1-0.5D)T_s > t \geq t_z+(1-D)T_s$: The HV valve is turned on, and the u_1 arm pushes the current to u_2 arm, which results in energy equalization of the converter upper arms.

Mode 3: $T_s-t_z > t \geq (1-0.5D)T_s$: The HV valve is kept closed, and all SMs of the lower arms are activated, while all SMs of the upper arms are deactivated (bypassed). During this

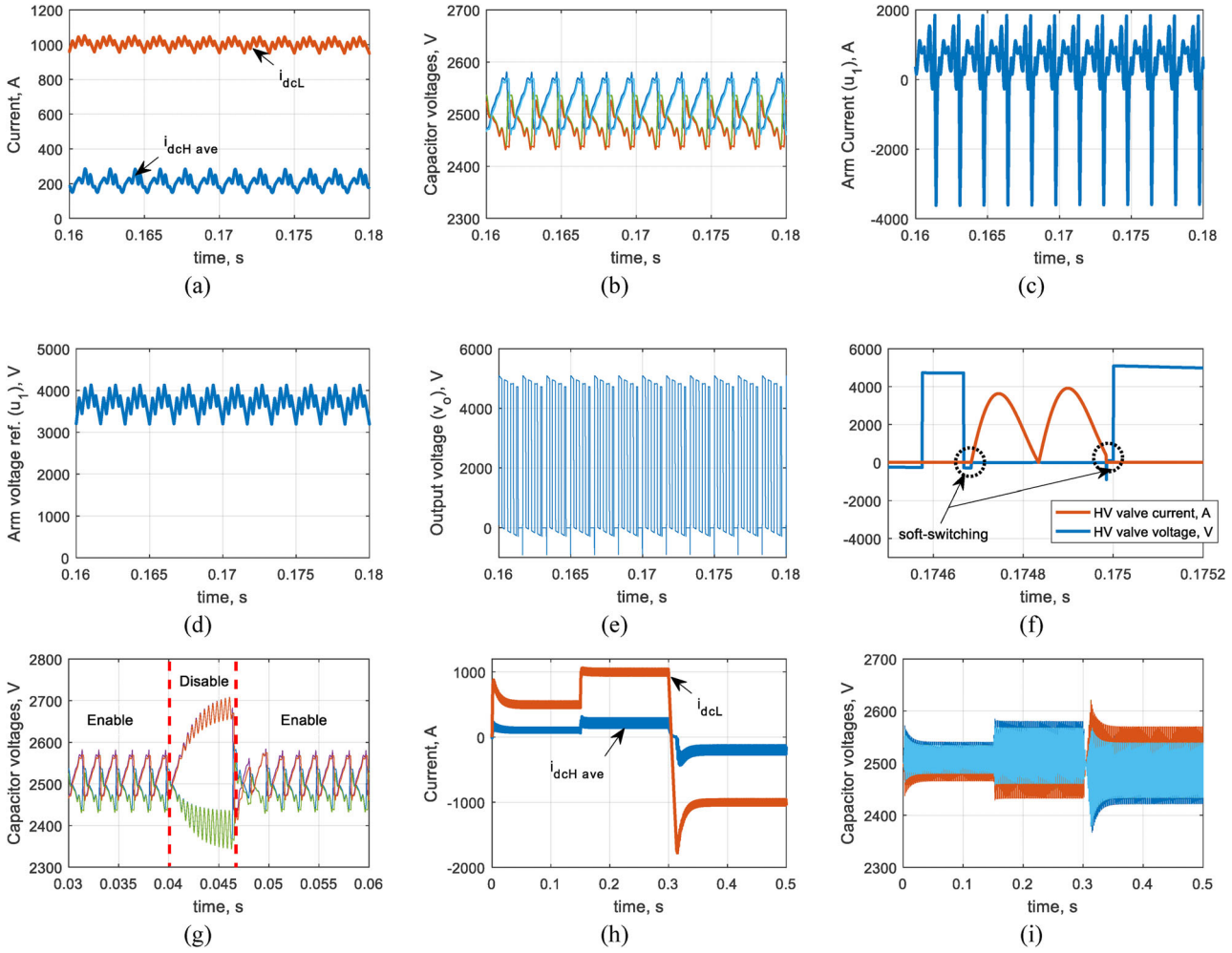


FIGURE 8 Simulation results (a)–(g) are at $i^*_{dcL} = 1$ kA, (h) and (g) are at multi-step i^*_{dcL} (a) currents at the LVS and HVS, (b) capacitors voltages, (c) currents of the upper arms, (d) u_1 arm voltage reference, (e) u_1 arm voltage reference along with the converter output voltage, (f) the current and voltage of the HV valve at the switching instant, (g) effect of disabling the proposed approach on capacitor voltage variation, (h) currents at the LVS and HVS, and (i) capacitor voltage variation during loading and power flow reversal.

mode, the L_2 arm pushes the current to L_1 arm, which results in energy equalization of the converter's lower arms.

Mode Z_2: $T_s > t \geq T_s - t_z$: The HV valve is turned off, where the voltage across it after turning it off is almost zero, that is, soft-switching is achieved. These modes should be repeated continuously with the operation.

4 | CLOSED-LOOP CONTROL AND DESIGN

4.1 | Closed-loop control

The closed-loop controller of the proposed hybrid DC–DC MMC during mode1 is shown in Figure 6, where the current at the LVS, namely, i_{dcL}, is controlled to follow its reference value (i^*_{dcL}) which may be positive or negative. In the case of positive i^*_{dcL}, the power flow is from the HVS to the LVS, while negative i^*_{dcL} indicates that the power flow is from the LVS to the HVS, that is, the proposed DC–DC converter provides bidirectional power transfer between the involved HVS and LVS.

The current error is fed to a suitable controller with a transfer function $G_c(s)$ to generate the proper voltage reference of the upper arm of the first leg, namely, v_{u1}. In the presented work proportional-integral controller (PI) is used where $G_c(s) = (k_p + k_i/s)$, where k_p and k_i are the proportional and integral gain of the PI controller. The parameters are tuned in the presented work via try and error technique.

After extracting the suitable upper arm voltage of the first leg (v_{u1}), the voltage reference of the upper arm of the second leg (v_{u2}) can be estimated as the summation of v_{u1} and v_{u2} equals V_{dcH}. By employing one of the multi-level modulation techniques, the suitable number of SMs to be activated in arms u_1 and u_2, namely, N_{u1} and N_{u2}, respectively, can be estimated. In the presented work, the phase disposition (PD) modulation technique is employed, where the extracted upper arm voltages (v_{u1} and v_{u2}) are compared with N in-phase carriers but shifted in level [5] to extract the suitable number of SMs to be activated in the upper arms, namely, N_{u1} and N_{u2} as shown in Figure 6.

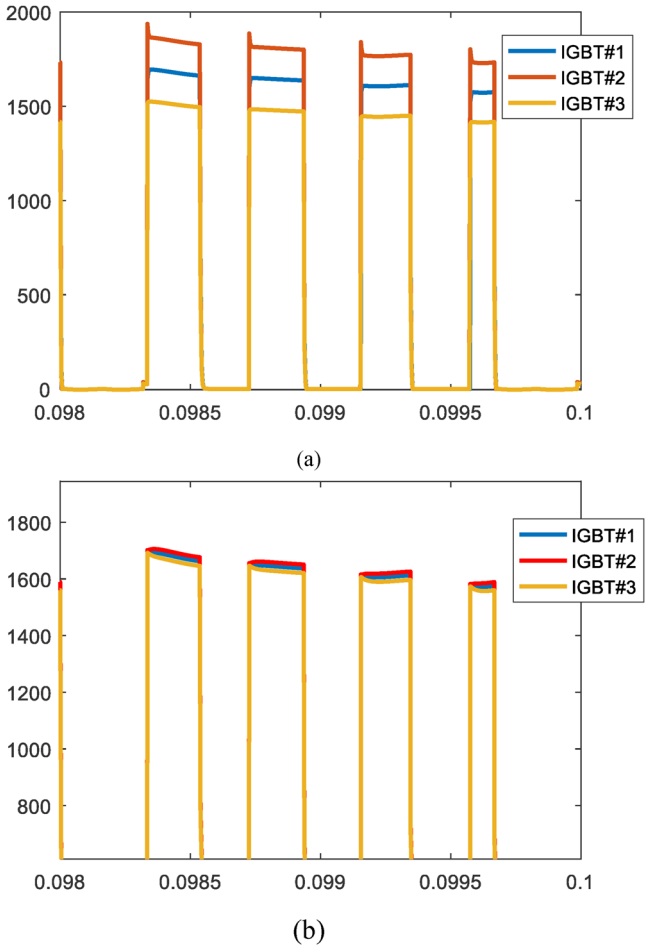


FIGURE 9 Effect of off-state resistance mismatch and parasitic capacitances mismatch on the voltage distribution among the series-connected IGBTs of HV valve (IGBTs# 1,2 and 3). (a) Without employing static and dynamic voltage sharing elements, and (b) with employing static and dynamic voltage sharing elements.

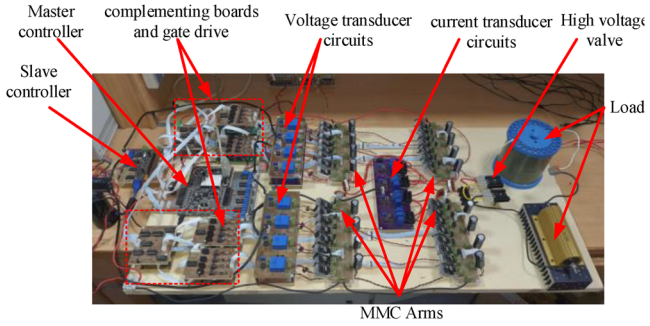


FIGURE 10 Experimental setup.

Then the suitable number of SMs to be activated in lower arms (N_{L1} and N_{L2}) can be extracted simply as the summation of the activated SMs in the upper and lower arm in the same leg equals N, where N is the number of SMs in each arm.

Based on Figure 6, the arm currents (i_{u1}, i_{u2}, $i_{L1,}$ and i_{L2}), capacitor voltages in each arm ($[V_{Cu1}]_{Nx1}$, $[V_{Cu2}]_{Nx1}$, $[V_{CL1}]_{Nx1}$ and $[V_{CL2}]_{Nx1}$) as well as the number of SMs to be activated in each arm (N_{u1}, N_{u2}, $N_{L1,}$ and N_{L2}) are fed to the conventional Capacitor Voltage Balancing Algorithm (CVBA), presented in [5], to decide which arm SMs will be activated, and which will be bypassed based on the arm current direction and capacitors voltages levels. As for positive arm current, SMs with lower capacitor voltage are activated and vice versa, as presented in [5]. Based on that, the gate pulses of the SMs IGBTs can be generated during mode 1, as shown in Figure 6.

The generated pulses are fed to the involved IGBTs during mode 1, which lasts for $(1-D)T_s$, then the modes shown in Figure 5 are enabled sequentially (one by one) with the defined time interval of each mode. The suitable gate pulses of involved SMs IGBTs and the HV valve during each mode are defined in Table 1. The modes are repeated continuously to ensure balanced capacitor voltages with limited voltage ripple during the DC–DC conversion process.

4.2 | Assessment of the proposed converter versus other existing converters

In this subsection, a comparison between the proposed hybrid MMC-based DC–DC converter and other existing converters in literature is held for assessment.

The comparison is tabulated in Table 2. The comparison shows that the proposed converter has a reasonable count of IGBTs and a reduced number of HV valves. In addition, it has the ability to operate the involved HV valve under soft switching.

4.3 | Passive component design

In this subsection, the design of the passive components, such as the SM capacitance, arm inductor, and output filter inductor, is provided as follows;

4.3.1 | SM capacitance

During mode 1, the SMs capacitors are charged/discharged during $(1-D)T_s$ duration according to the arm current direction. For u_1 arm, the basic relation between the capacitor current and voltage is given by;

$$i_c = \frac{Cdv_c}{dt} \rightarrow i_{u1}\ \frac{v^*_{u1}}{V_{dcH}} = \frac{C\,\Delta v}{(1-D)\,T_s} \tag{17}$$

where i_{u1} and v^*_{u1} are the arm current and the arm voltage reference of u_1 arm, respectively, and Δv is the capacitor voltage ripple. For the defined accepted capacitor voltage ripple, Δv, the suitable SM capacitance can be expressed by;

$$C = i_{u1}\ \frac{v^*_{u1}\ (1-D)\,T_s}{V_{dcH}\,\Delta v} \tag{18}$$

It has to be noted that the HV valve duty cycle, namely, D, is limited to less than 20% to reduce the negative impact of the

TABLE 2 Comparison between the proposed hybrid modular DC–DC converters versus other existing converters.

	Proposed converter	Ref. [28]	Ref. [22]	Ref. [27], series 2L with switches at HVS	Ref. [21]
Voltage at HVS	V_{dcH}	V_{dcH}	V_{dcH}	V_{dcH}	V_{dcH}
Type of SMs	HBSMs	FBSMs	HBSMs	FBSMs	HBSMs
No. of SMs per arm	N	N	N	N	N
Total No. of SMs (also, No. of SMs DC capacitors)	$4N$	$4N$	$4N$	$3N$	$4N$
Voltage rating of the SMs	V_{dcH}/N	$V_{dcH}/2N$	BV_{dcH}/N, $B>1$	V_{dcH}/N	V_{dcH}/N
No. of SMs IGBTs	$\mathbf{8N}$	$16N$	$8N$	$12N$	$8N$
Voltage rating of SM IGBTs and SM capacitors	V_{dcH}/N	$V_{dcH}/2N$	BV_{dcH}/N	V_{dcH}/N	V_{dcH}/N
No. of arm inductors	4 × (μH range)	4× (μH range)	4× (mH range)	3 × (mH range)	4× (mH range)
No. of HV Valves	1 (bidirectional)	2 (unidirectional)	–	6 (unidirectional)	–
HV Valve voltage rating	V_{dcH}	V_{dcH}	–	V_{dcH}	–
HV valve structure	Series-connected IGBTs	Series-connected HBSMs	–	Series-connected IGBTs	–
Soft-switching ability	**Yes**	No	No	Yes	No
Additional components	–	2 arm inductors in (μH range) for HV valves	$4(N+1)$ IGBTs×BV_{dcH}/N	–	$4N$ IGBTs×$2V_{dcH}/N$ + $2N$ Isolating transformers

equalization period on the smoothness of the output current, as the output voltage is zero during the equalization period. It is worth mentioning that the modulation index does not affect the value of the duty cycle D, that is, a fixed duty cycle (D) is defined for the operation irrelevant to the modulation index.

4.3.2 | Arm inductor (L_a)

The MMC arm inductor MMC is chosen to ensure almost zero/very-low current at the end of the equalization process to avoid sudden change of arm currents when returning to the normal operating modes.

To ensure that the equalization process duration should equal the periodic time of the LC circuit response, that is;

$$DT_s - 2\,t_z = 2\pi\sqrt{L_aC/N} \tag{19}$$

That is, the proper arm inductance is given by;

$$L_a \cong N\left(\left(DT_s - 2t_z\right)/2\pi\right)^2/C \tag{20}$$

4.3.3 | Output L-filter (L_f)

To have smoothed current at the LVS (i_{dcL}), proper inductance (L_f) should be chosen carefully to ensure an acceptable current ripple at the LVS. To achieve that, the impedance of the inductor at the HV valve switching frequency should be much higher than the equivalent load resistance (R_{eq}) seen at the LVS, assuming that the power flow is from the HVS to LVS, that is, $R_{eq} = V^2_{dcL}/P$; where P is the injected power to the LVS. Hence, the proper output filter inductance is given by;

$$L_f >> R_{eq}T_s/(2\pi) \tag{21}$$

4.3.4 | Numerical example

For 2 MW, 10 kV/2 kV, DC–DC MMC with four SMs per arm (i.e. V_{dcH} = 10 kV, V_{dcL} = 2 kV, i_{dcL} = 1kA, and $i_{dcH\,ave.}$ = 200 A, i_{u1} = 600 A, v_C = 2500 V, v_{u1} = 4 kV), if the HV valve duty cycle, D, is 0.2 and its switching time, T_s, is 1/600 s, while $t_z = 0.01T_s$. With the help of (18), suitable capacitance can be estimated for voltage ripples less than 10% ($\boldsymbol{\Delta v} < 250$ V), that is, C > 1.28 mF. Then with the help of (20), the proper arm inductance is $L_a \cong 3\ \mu$H for a capacitance of 3 mF. Finally, with the help of (21), proper output filter inductance can be estimated, where $R_{eq} = (2\text{ kV})^2/2\text{ MW} = 2\Omega$, that is, $L_f >> 0.5$ mH.

4.4 | Bidirectional HV valve implementation

The involved bidirectional HV valve in the proposed topology is implemented using series-connected IGBTs as shown in Figure 7a. Each IGBT has an off-state resistance (R_{off}) and a parasitic capacitance (C_p). Having series-connected IGBTs with different off-state resistances and parasitic capacitances will lead to unequal voltage distribution among them. To ensure equal voltage sharing of the involved IGBTs, proper balancing resistances (R_B) are connected across the IGBTs for static voltage sharing (equal voltage sharing at steady state), and

RC snubber circuits (R_s, C_s) are connected as well across the involved IGBTs for dynamic voltage sharing (equal voltage sharing during transients). The static and dynamic voltage equalization elements are shown in Figure 7b.

Based on [31], the proper static resistance, R_B is given by (22) where R_{off} is the nominal off-state resistance of IGBTs, while the proper snubber capacitor and snubber resistance are given by (23) and (24) respectively; where I_o is the switch current before turning it off, t_f is needed time for current to decay from I_o to zero (assuming a linear decrease of current during its turn-off interval), V_{Css} is the steady state capacitor voltage, and T_{on} is the minimum turn-on time of the involved IGBTs.

$$R_B \cong \frac{R_{off}}{10} \tag{22}$$

$$C_s \cong \frac{I_O\, t_f}{2V_{Css}} \tag{23}$$

$$R_s << \frac{T_{on}}{5C_s} \tag{24}$$

In the following section, the effect of voltage equalization elements for a given case study is presented.

5 | SIMULATION

5.1 | Investigation of converter performance

A 2MW, 10 kV/2 kV hybrid DC–DC MMC simulation model with four SMs per arm rated at 2.5 kV is employed. Based on the aforementioned numerical example for $D = 0.2$, $T_s = 1/600$ s, the following parameters are defined $C = 3$ mF, $L_a = 2.5\ \mu$H with an internal resistance of 0.02 Ω, and $L_f = 10$ mH. The phase disposition modulation technique is employed with a switching frequency of 2.4 kHz to generate the number of SMs activated in the involved arms during mode 1 for the given arm voltage references. The proposed soft-switching operation of the involved HV valve is applied where t_z of $0.01T_s$ is defined. The current at the LVS (i_{dcL}) is controlled using PI-Controller with gain constants of ($k_p = 10$, $k_i = 1000$). For a current reference of 1kA, the corresponding results are shown in Figure 8a–f. Figure 8a shows the DC current at LVS (i_{dcL}) and the average HVS current. To ensure drawing this current from the HVS, a proper passive second-order LC-filter with proper damping should be employed at the HVS terminals. Figure 8b shows the voltages of the involved capacitors. The capacitors' voltages are kept in a certain voltage window when the proposed concept is applied. The currents of the involved upper arms are shown in Figure 8c, where the shown current impulses are due to the parallel connection of capacitors during the equalization period. Figure 8d shows the voltage reference of the u_1 arm generated from the employed current controller, while the converter output voltage, v_o, is shown in Figure 8e. The current and voltage of the HV valve during the switching instant are shown in Figure 8f, where the soft-switching is achieved.

To show the effectiveness of the proposed concept, the proposed technique is enabled, then disabled, then enabled again at 1 kA current reference. The corresponding capacitors voltages variation is shown in Figure 8 g, where the capacitors' voltages are well-balanced and bounded when the proposed technique is enabled, but when the proposed concept is disabled and conventional MMC control is applied (Mode 1 only), the capacitors' voltages deviate, and DC–DC conversion process fails. Finally, to show the proposed converter's dynamic behaviour and bidirectional power flow capability, a multi-step current reference (i^*_{dcL}) is defined, where a step change from 0.5kA to 1kA, then another step-change from 1kA to −1kA are applied. The corresponding simulation results are shown in Figures 8 h and i where the current i_{dcL} is well regulated, and the power flow is reversed successfully. The capacitor voltages are balanced and bounded with a limited voltage ripple.

5.2 | Voltage equalization elements of HV valve

In this subsection, the design and effect of static and dynamic voltage sharing elements for the series-connected IGBTs-based bidirectional HV valve are presented, where six IGBTs are employed to implement the bidirectional HV valve as shown in Figure 7a. To show the effect of switches mismatch on the voltage distribution among them with the operation, six IGBTs with different off-state resistances of 6 MΩ ± 10%, and different parasitic capacitances of 0.4 pF ± 30% are employed. To design proper static and dynamic voltage-sharing elements, Equations (22)–(24) are used. The proper static voltage sharing resistor R_B is approximately equals 6MΩ/10 = 600kΩ, where 6MΩ is the nominal off-state resistances of the involved IGBTs. Then assuming that $I_o = 10$ A (soft-switched valve), $t_f = 10$ ns, and steady-state capacitor voltage of 1670 V for the defined case study, the proper snubber capacitance $C_s = 30$ pF. Finally, for $T_{on} = 0.2(1/600)$, the selected snubber resistance is 20kΩ. The voltage distribution among the employed series-connected switches with no voltage equalization elements is shown in Figure 9a, while the voltage distribution with the designed static and dynamic voltage-sharing elements is shown in Figure 9b.

The results show that due to off-state resistances mismatch and parasitic capacitances mismatch of the series-connected IGBTs, there is an unequal voltage distribution among them when no voltage equalization elements are used. On the other side, after considering the voltage equalization elements, the voltage is distributed equally among the series-connected IGBTs which ensures safe operation during steady state as well as transient instants.

6 | EXPERIMENTAL VALIDATION

A down-scaled prototype of the proposed hybrid DC–DC MMC with four SMs per arm, shown in Figure 10, has been

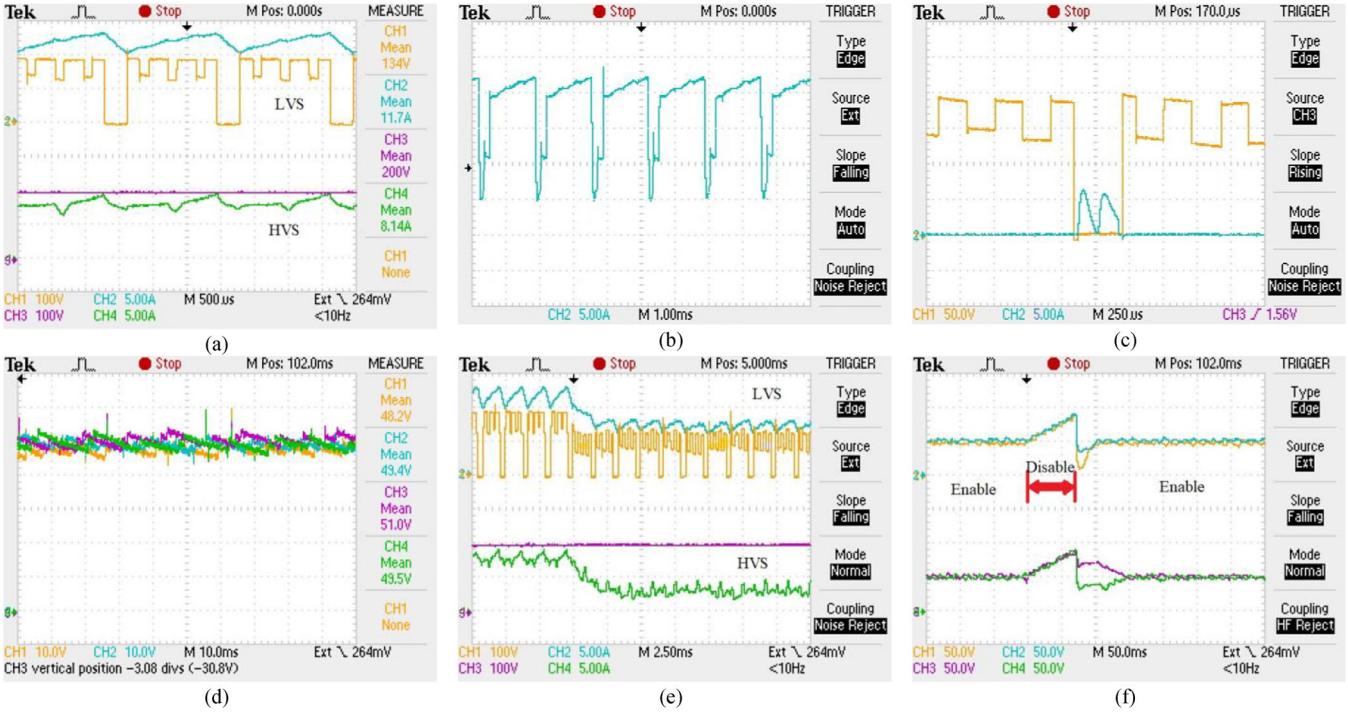


FIGURE 11 Experimental results. (a) Output voltage and current at HVS and LVS, (b) arm current (u_1), (c) HV valve voltage and current with applying the proposed soft-switching methodology, (d) capacitor voltages, (e) dynamic performance of the HVS and LVS quantities (voltage and current at each side) due to loading variation, and (f) effect of the proposed equalization approach on the capacitors' voltages.

TABLE 3 Experimental parameters.

Parameter	Value
Input voltage (HVS)	200 V
PD carrier frequency	2400 Hz
HV valve switching frequency	600 Hz
Number of SMs per arm	4
Inductive Load at LVS	$10\Omega + 11\text{mH}$ with ESR$\sim = 1.2\Omega$
Arm inductance	20 μH
Arm capacitance	680 μF
HV valve duty cycle, D	0.2
SMs switches	MOSFETs (IPW60R070C6)
HV valve switches	IGBTs (60N90)
Digital controller	Master:PSoC(CY8C5868AXI-LP035) Slave:PSoC (CY8CKIT-059)
Gate drivers	Optically isolated (HCPL-3120)

implemented for experimental verification. The parameters of the experimental setup are given in Table 3.

The experimental setup has been run at an output voltage reference of 135 V, enabling the soft-switching of the involved bidirectional HV valve. The corresponding recorded experimental results are shown in Figure 11. Figure 11a shows the voltage and current at HVS as well as LVS, while Figure 11b shows the corresponding upper arm current of the first leg (u_1), where the shown current notches in the arm current waveform are due to the parallel connection between capacitors during the equalization period. Figure 11c shows the voltage and current of the involved HV valve, which only carries current during the equalization period. It is clear that soft-switching is associated with the operation, which reduces the complexity of series-connected devices to implement the HV valve as well as decreases the switching losses of the HV valve, which has a positive effect on the converter efficiency.

Figure 11d shows the corresponding variation of capacitor voltages, where balanced and bounded capacitor voltages are achieved thanks to the proposed equalization technique. To show the dynamic performance of the proposed hybrid DC–DC MMC, the voltage and current at HVS and LVS have been recorded before and after load change. The corresponding waveforms are shown in Figure 11e.

To show the effectiveness of the proposed equalization technique, the converter is run while enabling the equalization technique; then the technique is disabled, and the MMC is operated under conventional control, then the equalization technique is re-enabled again. The corresponding capacitors voltages variation is shown in Figure 11f, where the capacitors voltages are balanced when the equalization technique is enabled. While capacitors' voltages diverge, and energy drift starts when the equalization technique is disabled

To validate the operation under variable power levels, including the power reversal condition, a 100 V DC-link has been employed at the low-voltage side, that is, $V_{\text{dcL}} = 100$ V is employed, while the high-voltage side voltage level is kept at 200 V. The current at the low-voltage side is controlled to

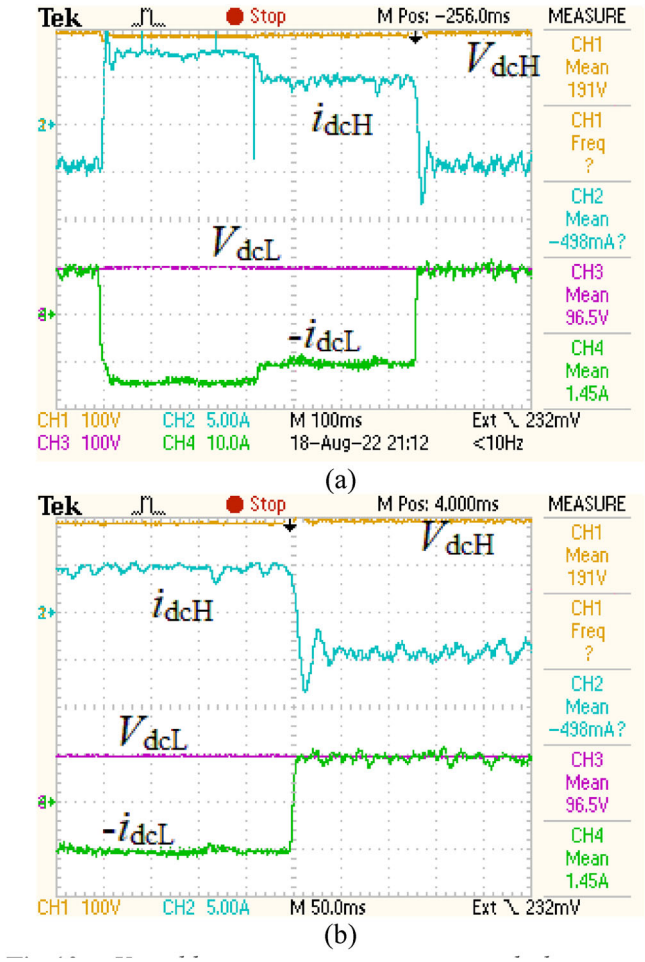


FIGURE 12 Variable power operation, including power reversal condition. (a) Changing the power level at the HV side from +1.5 kW to +1 kW to −1 kW and (b) a zoomed-in view of the power reversal condition (+1 kW to −1 kW).

transfer 1.5 kW, then 1 kW from the high-voltage side to the low-voltage side, then 1 kW is transferred from the low-voltage side to the high-voltage side, that is, the power at the high-voltage side is controlled to be +1.5 kW then +1 kW then −1 kW to ensure a bidirectional power flow feature for the proposed configuration. The corresponding experimental results are shown in Figure 12. Figure 12a shows the voltage and current levels at both sides are presented for the aforementioned power profile (+1.5 kW→+1 kW→-1 kW), while Figure 12b shows the zoomed-in view of the power reversal condition (+1 kW to −1 kW).

It is clear that the current level on both sides can be controlled and reversed successfully. Finally, Figure 13 shows the efficiency variation of the proposed Hybrid DC–DC MMC versus loading, where the output voltage reference is changed while keeping the same load resistance. The efficiency curve shows that the efficiency of the down-scaled prototype is relatively high, where maximum efficiency is above 96%. The efficiency is expected to be higher at higher voltages and power levels, that is, in real-scale operation.

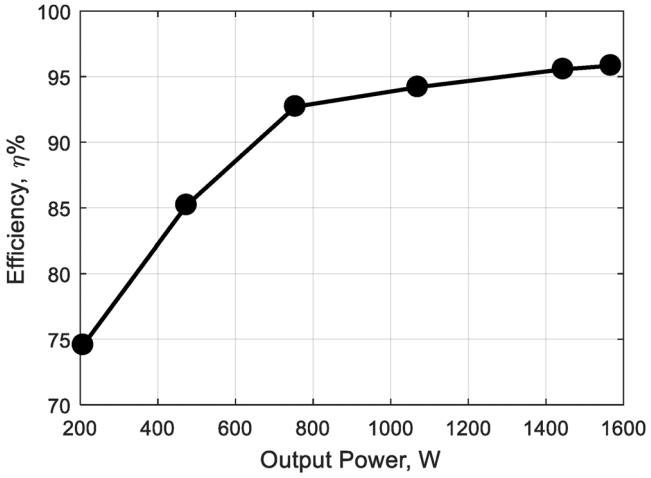


FIGURE 13 Experimental efficiency versus loading.

TABLE 4 Simulation parameters of the assessment models.

	AC voltage injection	Proposed approach
DC voltage at the HV side	10 kV	10 kV
Submodule capacitance	3.3 mF	3.3 mF
Arm inductance	25 μH	2.5 μH
Load impedance	100 mH + 10 ohm	100 mH + 10 ohm
Desired current at LV side	150 A	150 A
HV valve switching	–	600 Hz, 20% Duty
AC injected voltage	3.8 kV pk, 600 Hz	–
Carrier frequency	2400 Hz	2400 Hz

7 | ASSESSMENT OF THE PROPOSED APPROACH

This section presents an assessment of the proposed approach, where its performance is compared with the high-frequency AC voltage injection technique. Two simulation models have been built, one for the high-frequency sinusoidal AC voltage injection and the other for the proposed approach. The parameters of both models are summarized in Table 4. In the AC voltage injection approach, high-frequency (HF) sinusoidal voltage is injected in the upper arms with a magnitude of 3800 V (0.38 p.u) and frequency of 600 Hz, while identical voltage with 180° phase shift is injected in the lower arms. The corresponding simulation results for the AC injection approach as well as the proposed approach, are shown in Table 5. Based on the presented results, it is clear that the same currents are achieved at the low voltage side, but the rms value of the arm currents in the proposed approach are lower compared to the high-frequency AC voltage injection method, similarly for the circulating current in both approaches. Finally, both approaches have balanced capacitors voltages which vary approximately at the same voltage window. Both approaches have acceptable performance, but at lower current stresses when the proposed approach is employed.

TABLE 5 Simulation results of assessment models.

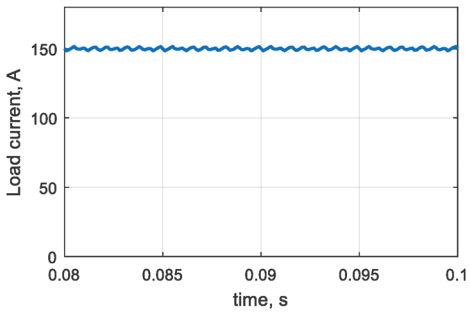
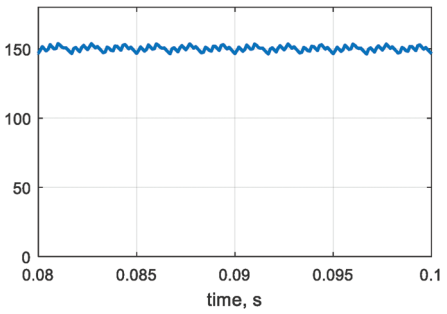
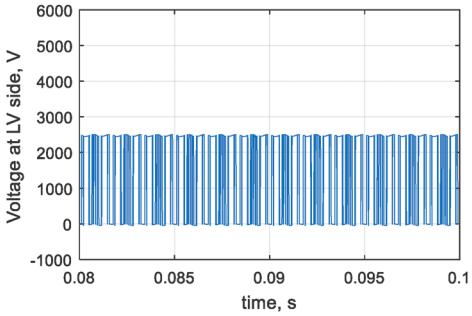
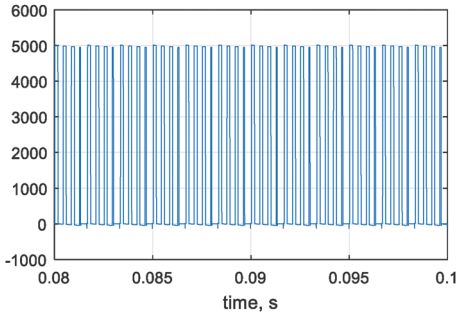
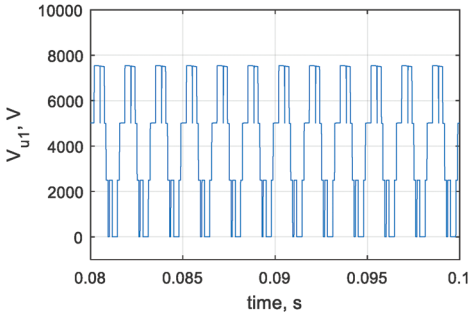
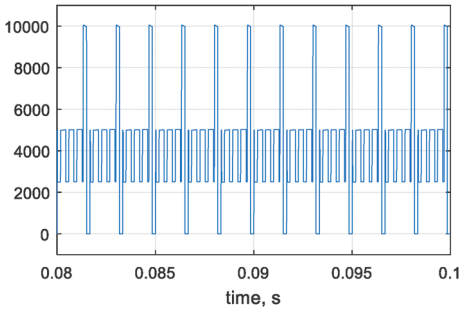
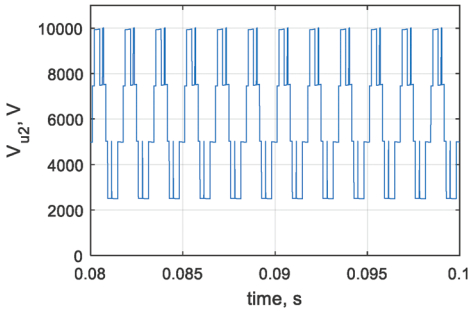
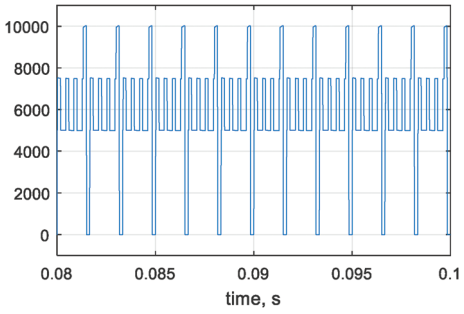
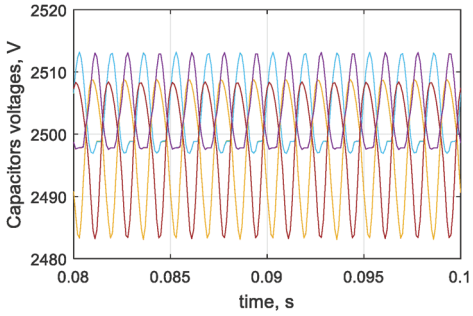
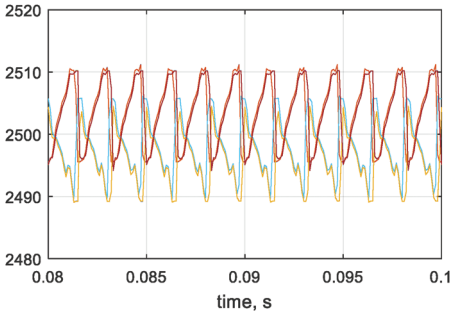
	HF sinusoidal AC voltage injection	The proposed approach
Current at LV side		
Voltage at LV side		
U1 arm voltage		
U2 arm voltage		
Capacitor voltages		

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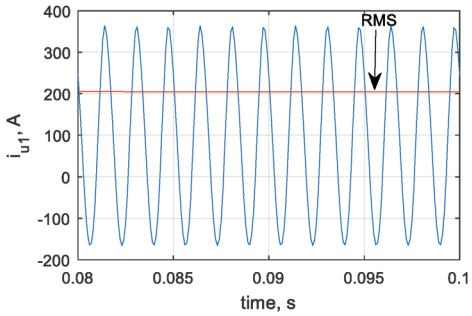
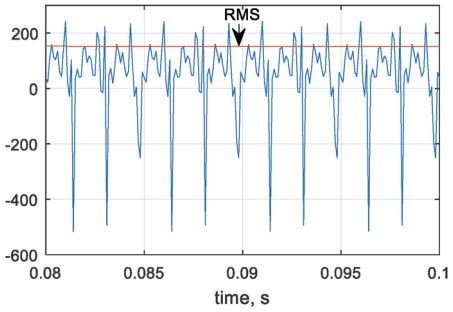
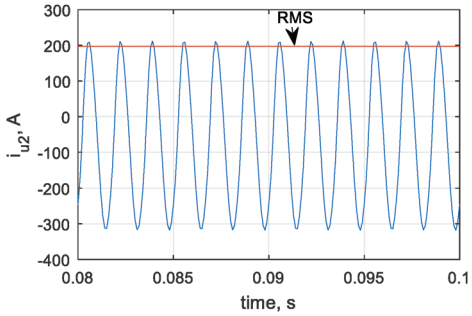
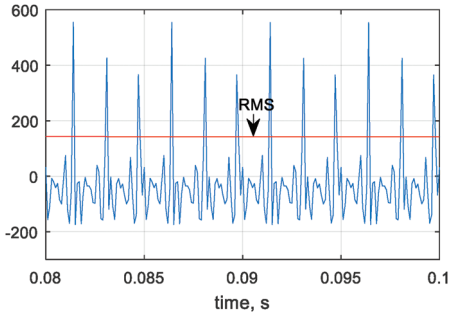
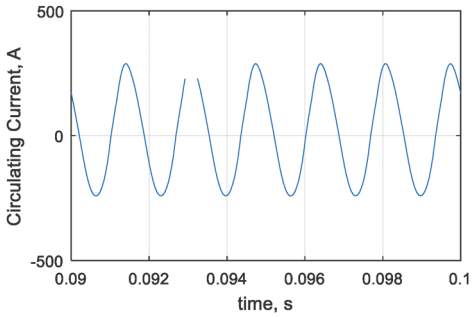
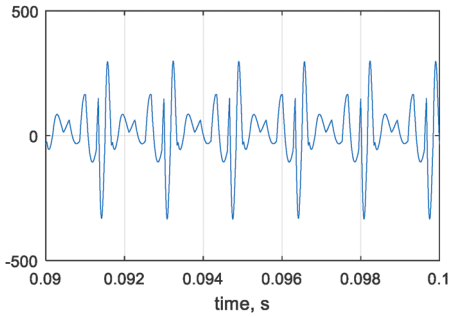
TABLE 5 (Continued)

	HF sinusoidal AC voltage injection	The proposed approach
U_1 arm current		
U_2 arm current		
Circulating current		

8 | CONCLUSION

Here, a new bidirectional hybrid DC–DC MMC has been proposed for DC grid applications. The converter consists of conventional half-bridge SMs-based legs, where two legs are needed, along with a bidirectional HV valve connected between the mid-points of the MMC legs. The HV valve is used to ensure operation with balanced and bounded capacitors voltages with the DC–DC conversion processes. The operation of the proposed architecture is divided into two periods. The first one is operating the MMC converter with conventional control with the defined dc output voltage while the HV valve is turned off, which results in capacitor voltage divergence due to unipolar arm currents. To restore capacitor voltage to its nominal voltage level, an equalization period is enabled for a predetermined time. In the equalization period, the involved HV-valve is turned on, and a parallel connection between arms capacitors is enabled. A soft-switching of the series-connected IGBTs-based bidirectional HV valve is highlighted, in addition, the design of the required static and dynamic voltage sharing elements for the series-connected IGBTs is highlighted and tested as well in the presented work. The proposed approach's current stresses are lower when compared to the high-frequency sinusoidal AC voltage injection approach. The presented simulation and experimental results show the viability and high efficiency of the proposed converter. It is worth mentioning that the same concept can be investigated for DC–DC conversion but with DC fault-blocking capability feature and DC to low-frequency AC conversion.

AUTHOR CONTRIBUTIONS

Ahmed Elserougi: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Writing – original draft, Writing – review and editing; Ibrahim Abdelsalam: Investigation, Resources, Software, Validation; Ahmed Massoud: Conceptualization, Project administration, Resources, Supervision, Writing – review and editing.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

FUNDING INFORMATION
None.

DATA AVAILABILITY STATEMENT
The data that support the findings of this study are available from the corresponding author upon reasonable request.

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