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Deep reinforced learning-based inductively coupled DSTATCOM under load uncertainties

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Abstract
Concerning the power quality issues in the power distribution network due to load uncertainties and improper impedance matching of the inductances, deep reinforced learning (DRL)-based inductively coupled DSTATCOM (IC-DSTATCOM) is proposed. First, by analyzing the impedance matching principle, the expression of source, load and filter current is derived with the help of inductive filtering transformer. And second, an individual DRL subnet structure is accumulated for each phase using mathematical equations to perform the better dynamic response. A 10-kVA, 230-V, 50-Hz prototype direct coupled distributed static compensator (DC-DSTATCOM) and IC-DSTATCOM experimental setup is buit to verify the experimental performance under uncertainties of loading. The IC-DSTATCOM is augmented better dynamic performance in terms of harmonics curtailment, improvement in power factor, load balancing, potential regulation, etc. The benchmark IEEE-519-2017, IEC-61727 and IEC-61000-1 grid code are used to evaluate the effectiveness of the simulation and experimental study.

Keywords DRL algorithm · IC-DSTATCOM · DC-DSTATCOM · PCC

List of symbols

w_{pa}, w_{pb} and w_{pc}	Weighting values of active component of load current
w_{qa}, w_{qb} and w_{qc}	Weighting values of reactive component of load current
u_{pa}, u_{pb} and u_{pc}	In phase unit voltage template
u_{qa}, u_{qb} and u_{qc}	Quadrature unit voltage template
w_{cp} and w_{cq}	Output of DC and AC side PI controller
w_{sp} and w_{sq}	Total active and reactive components
w_a	Mean active weight
w_r	Mean reactive weight
i_{ra}, i_{rb} and i_{rc}	Total reactive weight
v_{sa}, v_{sb} and v_{sc}	Supply voltages
i_{la}, i_{lb} and i_{lc}	Load currents
i_{sa}, i_{sb} and i_{sc}	Supply currents
i_{aa}, i_{ab} and i_{ac}	Total active weight
i^*_{sa}, i^*_{sb}, i^*_{sc}	Reference supply currents

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1 Introduction

DC-DSTATCOM has achieved a great success in terms of shunt compensation for the PDN. There are several suggested improvements which are being considered to improve the performance of the DC-DSTATCOM [1–3]. The prime objectives such as harmonics curtailment, improvement in

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PF, load balancing and potential regulation are considered [4, 5]. The drawbacks of DC-DSTATCOM have raised the important concern-related issues due to the flow of short-circuit current at point of common coupling (PCC), poor protection and thermal issues [6, 7]. Considering the medium- and long-term development plan for "automotive industry" regulated by Ministry of Industry and Information Technology, it is encouraged for the development of IC-DSTATCOM.

1.1 Review of the literature and research background

In order to improve the above issues, three-phase three-wire Star/Delta/Star transformer is integrated with DC-DSTATCOM in the PDN [8–10]. The influence of the inductive transformer permits the inductance balancing in the PDN to analyze the system stability. Moreover, it provides the roboustness against the load variation over wide range. Apart from these, low-order harmonic obtained from the filter is suppresses effectively. The equivalent inductance of the source, load and filter side is maintain equal by using impedance matching principle for maximum power transfer. The feasibility of inductive transformer is anlayzed in terms of shunt compensation including additional features as discussed above.

To mitigate the shunt compensation issues, different types of neural network (NN) control algorithms are employed [11–24]. These algorithms such as Kernel Hebbian least mean square [11], Levenberg–Marquard backpropagation [12], Hebbian least mean square [13], sparse least mean square [14], adaptive control [15], recurrent neural network [16, 17], CFNN-AMF [18], neuro fuzzy learning [19], neural network [20–22], predictive control [23] and PNK-LMF [24] are reported for PQ conditioning. Most of the NN techniques proposed do not possess the perfect tuned weight which makes the inaccurate PQ performance. In the present work, the following improvements are proposed by using the DRL algorithm.

(i) This proposed DRL technique is constructed the biological relation among the input, target and previous weight neurons to obtain the tuned weight.
(ii) This tuned weight permits the inductive transformer and interfacing impedances for system protection with better PQ improvement.
(iii) Apart from this, it also performs smooth operation among analog and digital signals for d-SPACE 1104 application

However, some of the shortcomings, such as premature convergence and solutions, are not suitable for a competent planning framework (CPF). Hence, all the practical concerns, such as voltage and current profile, reliability, economic and environmental aspects, are very important for consideration. For designing a CPF, an unsupervised machine learning technique is required. Motivated by the several advantages such as excellent weight learning principle, adaptive capability, faster convergence, tracking capability and real-time application, DRL is selected for the generating of switching pulses. Also, it maintains the proper coordination in between input and neurons irrespective of parameter variation. It performs high transmission rate between the assigned input and expected output using multilayer network features in a short period.

1.2 Novelty and contribution

In order to achieve a CPF, IC-DSTATCOM is incorporated for unbalanced PDN to improve the shunt compensation with suitable protection and reliable operation. The major contributions are mortified in this way:

(i) The aspects such as reliability, financial, environmental and technical benefits are considered for CPF model.
(ii) An accurate CPF-based PDN for both balanced and unbalanced loading is designed in the time domain.
(iii) The IFT is deployed with the DSTATCOM as a perfect matching impedance device for nonlinear systems, which is also an integral part of controlling the shunt compensation as per acceptable limits.
(iv) The DRL algorithm is deployed to improve the PQ solution with reduced computational complexities.

1.3 Workflow of the study

The remaining part of this study are as follows: A brief introduction of the literature review, motivation, novelty and contribution is described in Sect. 1. Section 2 presents an overview of the PQ assessment, circuit description of IC-DSTATCOM, modeling of IFT and design of DRL algorithm. Section 3 describes the detailed implementation of DRL algorithm for the switching signal generation. The simulation study of the proposed topology and DC-DSTATCOM is presented to analyze the performance under the different case studies. Experimental results are presented to validate the effectiveness of the simulation study in Sect. 5. Finally, the summary of the conclusion is highlighted in Sect. 6.

2 Overview of the PQ assessment

The computer business equipment and manufacturing association (CBEMA) assessment is surveyed by the National

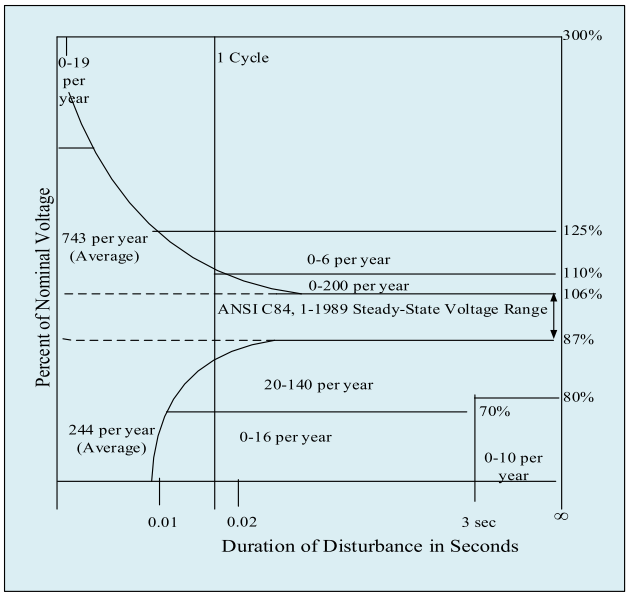


Fig. 1 CBEMA curves for PDN faults versus voltage and duration

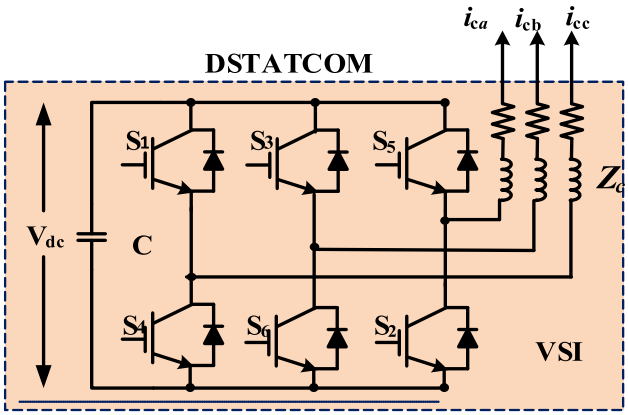


Fig. 2 Two-level self-supported capacitor-supported VSI-based DSTATCOM

Power Laboratory, Canadian Electrical Association and Electric Power Research Institute. Reviewing the assessment, the cause and effect of faults and loading are considered which is exposed in Fig. 1. To reach this level of coverage of PQ solution, DRL-based IC-DSTATCOM is analyzed.

2.1 Circuit description of the IC-DSTATCOM

The DC-DSTATCOM consists of a balanced three-phase supply, DSTATCOM and nonlinear load. But, the IC-DSTATCOM consists of a balanced three-phase supply, IFT-based DSTATCOM and three-phase nonlinear load.

The VSI-based DSTATCOM is considered at the point of common coupling (PCC) of PDN which is shown in Fig. 2. The arrangement of the 3P3W PDN with DC-DSTATCOM and IC-DSTATCOM is shown in Figs. 3 and 4, respec-

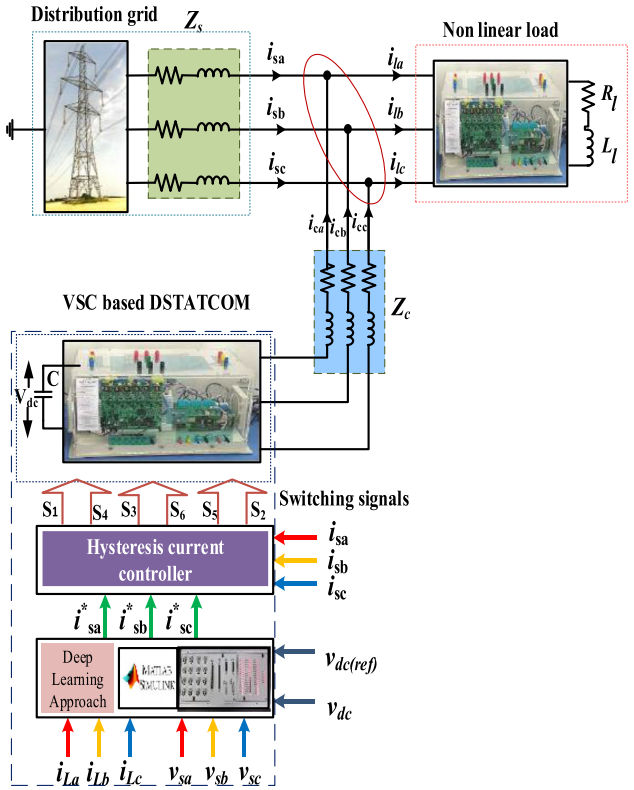


Fig. 3 PDN with DC-DSTATCOM

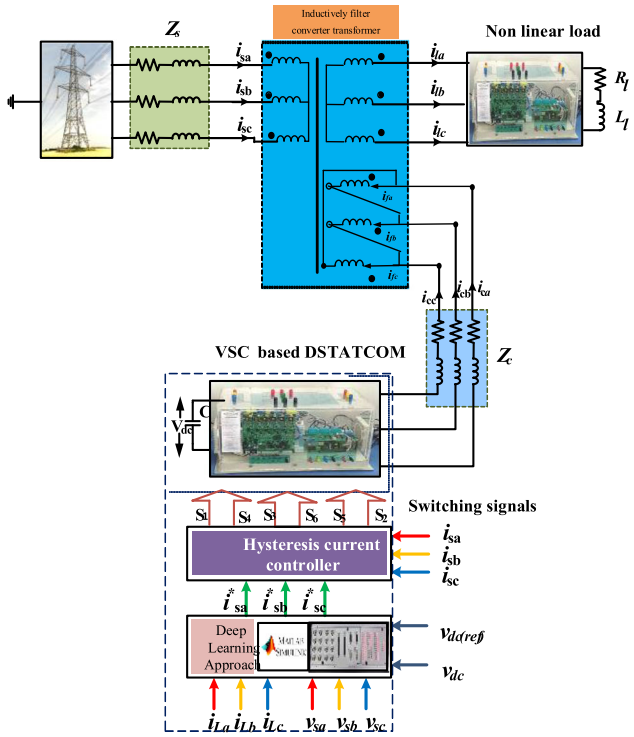


Fig. 4 PDN with IC-DSTATCOM

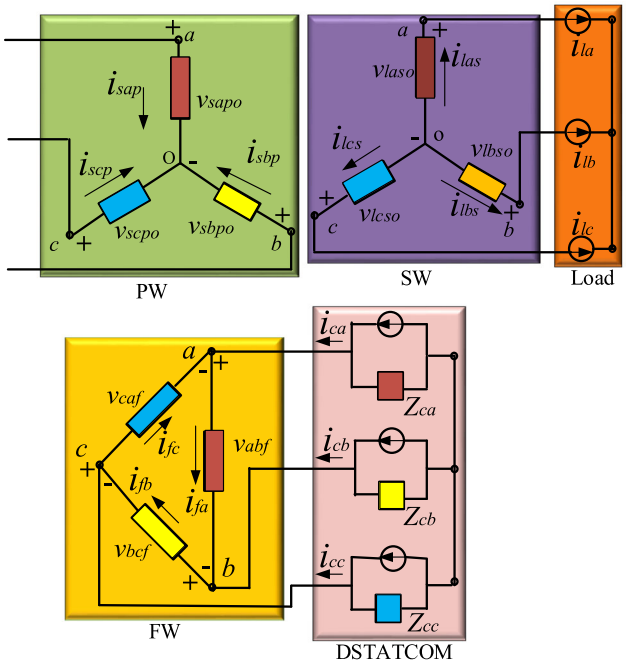


Fig. 5 Equivalent circuit of proposed IC-DSTATCOM

tively. The switching pulses of both DC-DSTATCOM and IC-DSTATCOM are generated by using DRL algorithm.

2.2 Modeling and designing of IFT

Figure 5 shows the proposed IC-DSTATCOM's winding structure. The suggested IC-DSTATCOM is connected through the IFT. Among the three windings, the filtering winding (FW) is connected to the DSTATCOM, the secondary winding (SW) is connected to the load and the primary winding (PW) is connected to the grid. The IFT is designed to maintain the same voltage among grid, load and DSTATCOM. The following subsections discuss the in-depth mathematical model of the IFT and its filtering mechanism. Here N_1, N_2 and N_3 are three turns of the IFT, Z_p is the primary winding impedance, Z_s is the series impedance and Z_g is the line impedance. So, $Z_g = Z_s + Z_p$. But Z_o is the filter side winding impedance, Z_c is the compensator impedance and Z_f is the tertiary winding impedance. So, $Z_g = Z_c + Z_f$.

The voltage balance equation of PW, SW and FW can be expressed as follows,

$$\begin{cases} N_1 i_{sap} + N_2 i_{las} + N_3 i_{caf} = 0 \\ N_1 i_{sbp} + N_2 i_{lbs} + N_3 i_{cbf} = 0 \\ N_1 i_{scp} + N_2 i_{lcs} + N_3 i_{ccf} = 0 \end{cases} \tag{1}$$

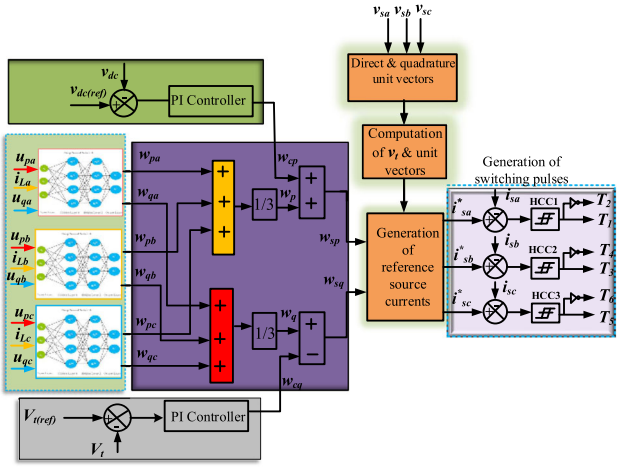


Fig. 6 Design of DRL-based IC-DSTATCOM/DC-DSTATCOM

According to Kirchhoff's current law (KCL), the current equations in the primary side of the IFT are written as

$$\begin{cases} i_{sap} = \left(v_{sa} - v_{sapo}\right)/Z_{sa} \\ i_{sbp} = \left(v_{sb} - v_{sbpo}\right)/Z_{sb} \\ i_{scp} = \left(v_{sc} - v_{scpo}\right)/Z_{sc} \end{cases} \tag{2}$$

According to KCL, the current equations in the secondary side of the IFT (load side) are written as

$$\begin{cases} i_{la} = i_{las} + i_{caf} \\ i_{lb} = i_{lbs} + i_{cbf} \\ i_{lc} = i_{lcs} + i_{cbf} \end{cases} \tag{3}$$

The current balance equations are shown below:

$$\begin{cases} i_{sap} + i_{sbp} + i_{scp} = 0 \\ i_{las} + i_{lbs} + i_{lcs} = 0 \\ i_{caf} + i_{cbf} + i_{ccf} = 0 \end{cases} \tag{4}$$

The total compensating current equations at filter side are written as

$$\begin{cases} i_{caf} = i_{ca} + i_{fa} \\ i_{cbf} = i_{cb} + i_{fb} \\ i_{ccf} = i_{cc} + i_{fc} \end{cases} \tag{5}$$

2.3 Design of DRL structure

The equivalent circuit of the IFCT is shown in Fig. 5. Also, the complete structure of DRL to generate the switching signals is presented in Fig. 6. Here S_1, S_2, … S_6 are represented by different controlled switching devices for all three phases. The corresponding flowchart for obtaining the tuned weight

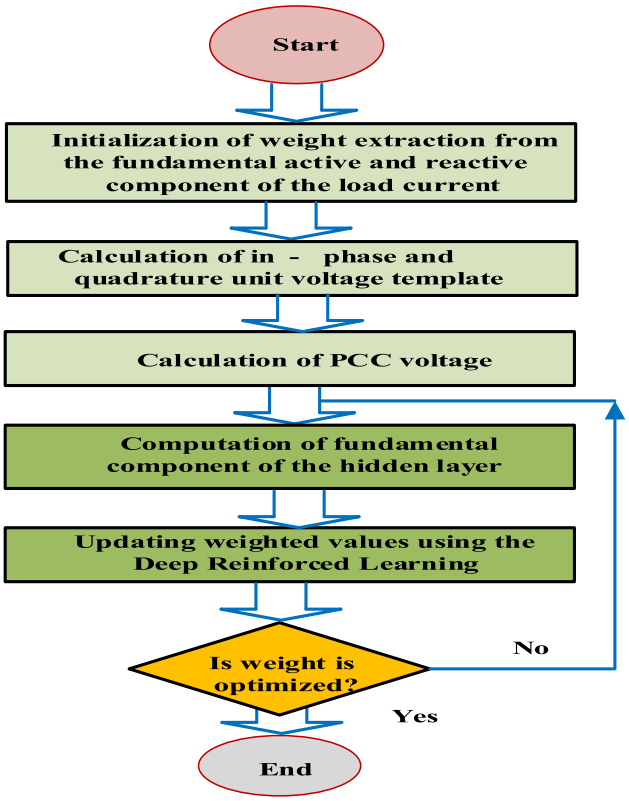


Fig. 7 Flowchart for obtaining the tuned weight using DRL principle

is shown in Fig. 7. The primary, load and filtering currents are represented by i_{p}, i_{l} and i_{f}, respectively. The compensator impedance is denoted by Z_{c}. The DRL algorithm is described in the later section in detail.

3 DRL algorithm

Having three input layers, three computational layers are Boltzmann machine to generate latent featured and vector encoded weights, and three output layers are provided for conditional probability density function (CPDF) oriented updated weight. Here j is considered as the neurons in the hidden layer, and "i" is the neurons in the computational layer.

The DRL algorithm is used to extract the reactive component of load current ($w_{\mathrm{q}a}$, $w_{\mathrm{q}b}$ and $w_{\mathrm{q}c}$) which are expressed by the following equation:

$$W_{\mathrm{q}a}^{n} = \alpha\gamma u_{\mathrm{q}a}(n)\, i_{\mathrm{l}a}(n) \frac{\mathrm{d}e_{\mathrm{q}a}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{q}a}(n-1) + b_j^i w_{\mathrm{q}a}(n-1) \tag{6}$$

whereas $e_{\mathrm{q}a}(n) = \alpha\left\{i_{\mathrm{lq}a}(n) - i_{\mathrm{lq}A}(n)\right\}$

$$W_{\mathrm{q}b}^{n} = \alpha\gamma u_{\mathrm{q}b}(n)\, i_{\mathrm{l}b}(n) \frac{\mathrm{d}e_{\mathrm{q}b}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{q}b}(n-1) + b_j^i w_{\mathrm{q}b}(n-1) \tag{7}$$

$$W_{\mathrm{q}c}^{n} = \alpha\gamma u_{\mathrm{q}c}(n)\, i_{\mathrm{l}c}(n) \frac{\mathrm{d}e_{\mathrm{q}c}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{q}c}(n-1) + b_j^i w_{\mathrm{q}c}(n-1) \tag{8}$$

Similarly, the DRL algorithm is used to extract the active component of load current ($w_{\mathrm{p}a}$, $w_{\mathrm{p}b}$ and $w_{\mathrm{p}c}$) which are expressed by the following equation:

$$W_{\mathrm{p}a}^{n} = \alpha\gamma u_{\mathrm{p}a}(n)\, i_{\mathrm{l}a}(n) \frac{\mathrm{d}e_{\mathrm{p}a}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{p}a}(n-1) + b_j^i w_{\mathrm{p}a}(n-1) \tag{9}$$

whereas $e_{\mathrm{p}a}(n) = \alpha\left\{i_{\mathrm{lp}a}(n) - i_{\mathrm{lp}A}(n)\right\}$

$$W_{\mathrm{p}b}^{n} = \alpha\gamma u_{\mathrm{p}b}(n)\, i_{\mathrm{l}b}(n) \frac{\mathrm{d}e_{\mathrm{p}b}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{p}b}(n-1) + b_j^i w_{\mathrm{p}b}(n-1) \tag{10}$$

$$W_{\mathrm{p}c}^{n} = \alpha\gamma u_{\mathrm{p}c}(n)\, i_{\mathrm{l}c}(n) \frac{\mathrm{d}e_{\mathrm{p}c}(n)}{\mathrm{d}t} h_k^{i-1} - w_{\mathrm{p}c}(n-1) + b_j^i w_{\mathrm{p}c}(n-1) \tag{11}$$

The reactive average value is given as

$$w_{\mathrm{r}} = \frac{w_{\mathrm{q}a} + w_{\mathrm{q}b} + w_{\mathrm{q}c}}{3} \tag{12}$$

Similarly, active average value is calculated as

$$w_{\mathrm{a}} = \frac{w_{\mathrm{p}a} + w_{\mathrm{p}b} + w_{\mathrm{p}c}}{3} \tag{13}$$

The direct unit voltage templates ($u_{\mathrm{p}a}$, $u_{\mathrm{p}b}$ and $u_{\mathrm{p}c}$) are calculated from phase voltages (v_{sa}, v_{sb}, v_{sc}) and PCC voltage (v_t) which are given by:

$$u_{\mathrm{p}a} = \frac{v_{sa}}{v_{\mathrm{t}}}, \quad u_{\mathrm{p}b} = \frac{v_{sb}}{v_{\mathrm{t}}}, \quad u_{\mathrm{p}c} = \frac{v_{sc}}{v_{\mathrm{t}}} \tag{14}$$

Similarly, the quadrature unit voltage templates ($u_{\mathrm{q}a}$, $u_{\mathrm{q}b}$ and $u_{\mathrm{q}c}$) are expressed by:

$$u_{\mathrm{q}a} = \frac{u_{\mathrm{p}b} + u_{\mathrm{p}c}}{\sqrt{3}}, \quad u_{\mathrm{q}b} = \frac{3u_{\mathrm{p}a} + u_{\mathrm{p}b} - u_{\mathrm{p}c}}{2\sqrt{3}}, \quad u_{\mathrm{q}c} = \frac{-3u_{\mathrm{p}a} + u_{\mathrm{p}b} - u_{\mathrm{p}c}}{2\sqrt{3}} \tag{15}$$

where v_t can be expressed as

$$v_{\mathrm{t}} = \sqrt{\frac{2\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)}{3}} \tag{16}$$

The proportional–integral (PI) controller processes the v_{de} signal for controlling the constant dc bus voltage which can be expressed as follows:

$$w_{\mathrm{cp}} = k_{pa} v_{\mathrm{de}} + k_{ia} \int v_{\mathrm{de}} \mathrm{d}t \tag{17}$$

where $v_{\mathrm{de}} = v_{\mathrm{dc\ (ref)}} - v_{\mathrm{dc}}$; $v_{\mathrm{dc(ref)}}$ is the reference DC link voltage, and v_{dc} is the actual DC link voltage.

The total active weight of the reference source current can be given in the form

$$w_{\mathrm{sp}} = w_{\mathrm{a}} + w_{\mathrm{cp}} \tag{18}$$

The PI controller processes the v_{te} signal for controlling the constant ac bus voltage which can be expressed as follows:

$$w_{\mathrm{cq}} = k_{\mathrm{pr}} v_{\mathrm{te}} + k_{\mathrm{ir}} \int v_{\mathrm{te}} \mathrm{d}t \tag{19}$$

where $v_{\mathrm{te}} = v_{\mathrm{t\ (ref)}} - v_{\mathrm{t}}$; $v_{\mathrm{t(ref)}}$ is the reference PCC voltage, and v_{t} is the actual PCC voltage.

Similarly, the total active weight of the reference source current can be given in the form

$$w_{\mathrm{sq}} = w_{\mathrm{r}} - w_{\mathrm{cq}} \tag{20}$$

By multiplying the active power current component by the in phase unit voltage template, the reference source current active component is given as follows:

$$i_{aa} = w_{\mathrm{sp}} u_{\mathrm{pa}},\ i_{ab} = w_{\mathrm{sp}} u_{\mathrm{pb}},\ i_{ac} = w_{\mathrm{sp}} u_{\mathrm{pc}} \tag{21}$$

Similarly, reference source reactive components are obtained as

$$i_{ra} = w_{\mathrm{sq}} u_{qa},\ i_{rb} = w_{\mathrm{sq}} u_{qb},\ i_{rc} = w_{\mathrm{sq}} u_{qc} \tag{22}$$

The following equation formulates the reference source currents

$$i_{sa}^* = i_{aa} + i_{ra}, \quad i_{sb}^* = i_{ab} + i_{rb}, \quad i_{sc}^* = i_{ac} + i_{rc} \tag{23}$$

The error signals in between actual and the reference source currents are processed by the hysteresis current controller (HCC). The HCC is used to turned OFF and turned ON as indicated in Figs. 3, 4 and 5.

3.1 Simulation results of DC-DSTATCOM

The simulation study of the DC-DSTATCOM in PDN is analyzed to show the effectiveness and feasibility in Fig. 8(i). This observation was obtained in response to the balanced nonlinear uncontrolled rectifier loading between 0.55 and 0.75 s. In Fig. 8(i), all the subplots are source voltage and source current, source current, source voltage and load current, compensating current, DC link voltage are arranged in the order of top to bottom wise. The THD% of the source current is reduced to 4.51, which is depicted in Fig. 8(ii). Figure 8(iii) displays the load current THD% 27.90. The PF is improved to 0.94 as shown in Fig. 8(iv). But, the PF is the load side is shown in Fig. 8(v). Moreover, 671.6 V DC link voltage is achieved for voltage regulation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures better power to end-users in the PDN.

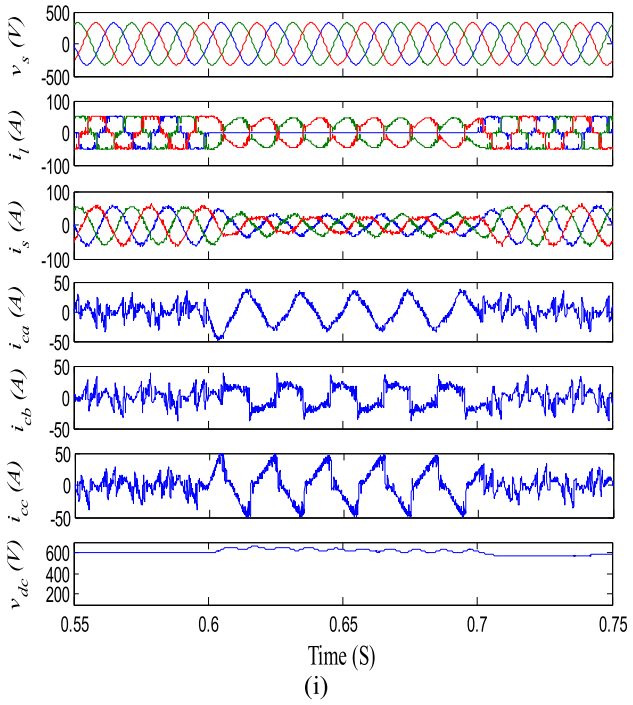
3.2 Simulation results of IC-DSTATCOM

The simulation study of the IC-DSTATCOM in PDN is analyzed to show the effectiveness and feasibility in Fig. 9(i). This observation was obtained in response to the balanced nonlinear uncontrolled rectifier loading between 0.55 and 0.75 s. In Fig. 9(i), all the subplots are source voltage and source current, source current, source voltage and load current, compensating current, DC link voltage are arranged in the order of top to bottom wise.

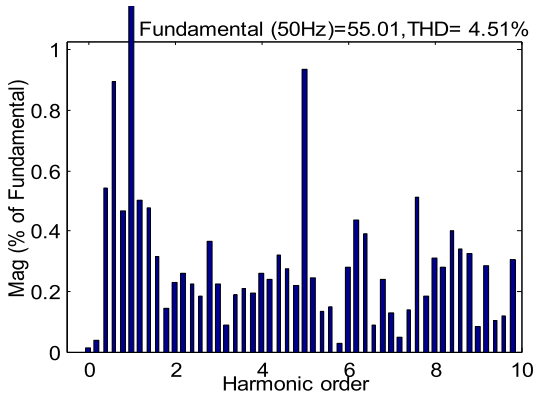
The THD % of the supply current is reduced to 4.51 due to the compensation depicted in Fig. 9(ii). Figure 9 iii shows that the load current THD % is 27.90. The source side PF is improved to 0.94 as depicted in Fig. 9(iv), whereas the load side is shown in Fig. 9(v). Furthermore, an appropriate voltage regulation of 671.6 V controls the DC link voltage under this observation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures better power to end-users in the PDN.

The above performance are made by considering the internal weighting factor for the two case studies which are shown in Fig. 10. The stability margin for the PI controller is selected by considering the suggested blue color parameter for both cases, which is shown in Fig. 11. The transfer function of PI controller used in the DC side is given by $g(s) = K_{ia} + \frac{K_{ia}}{s}$ where $0 \leq K_{pa} \leq 10$ and $0 \leq K_{ia} \leq 1$.

To improve the stability performance, the frequency response is analyzed by considering the first-order function. The optimal parameter is selected from frequency response subjected to the given constraints. Furthermore, the obtained THD profile by using both the techniques is shown in Fig. 12. A comprehensive technical comparison between IC-DSTATCOM and DC-DSTATCOM considering the power loss calculation, components, cost and their merits/demerits is presented in Tables 2 and 3.



(i)



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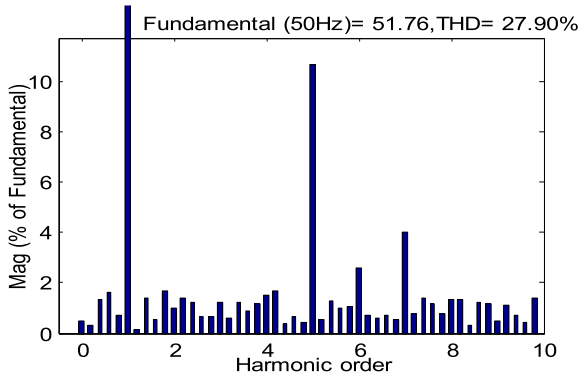
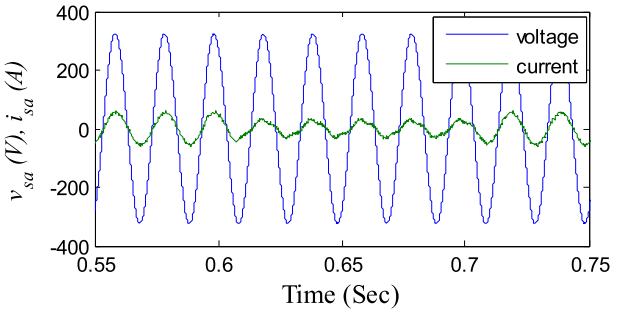


(iii)

Fig. 8 **i** Simulated waveforms of system performance for DC-DSTATCOM, **ii** source current THD under DC-DSTATCOM, **iii** load current THD under DC-DSTATCOM, **iv** a-phase source side PF and **v** a-phase load side PF



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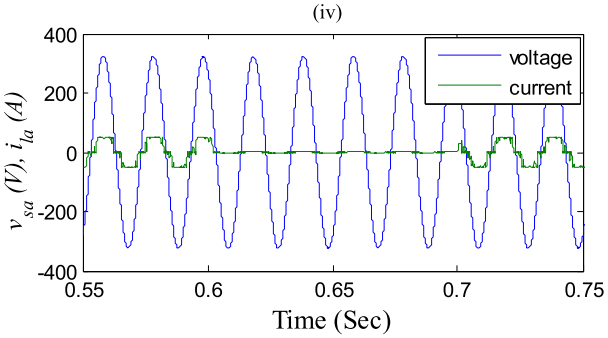


(v)

Fig. 8 continued

4 Experimental analysis

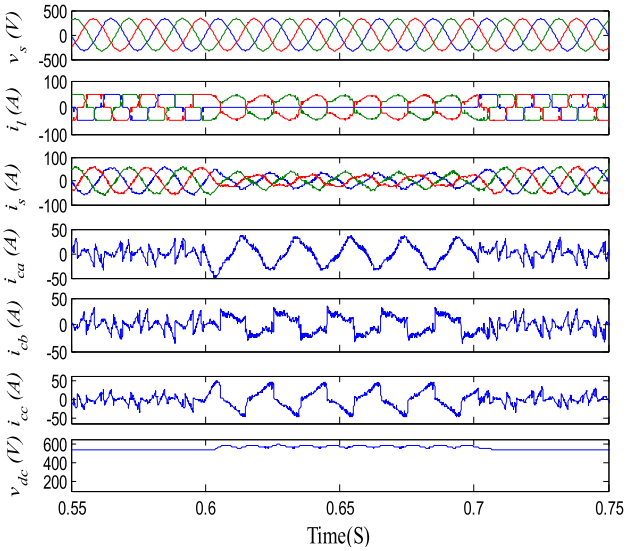
To further validate the proposed system, the prototype is developed. The experimental photograph is shown in Fig. 13. The insulated gate bipolar transistors (IGBTs) switching devices are used for the intelligent PM300DSA060 power module. The control strategy was implemented using data acquisition cards created by dSPACE and compatible with MATLAB/Simulink in a general control application. The MathWorks Real-Time Workshop and the dSPACE Real-Time Interface (RTI) automatically generate the real-time code [25–29].

This makes it possible to program I/O boards into the processor board. The output board was the DS 510001DWO, and the input board was the dSPACE DS 2004A/D. The switching frequency 20 kHz is selected based on the IGBTs used in the setups. The experimental analysis shows all the cases shown in the simulation analysis using DC-DSTATCOM and IC-DSTATCOM. The steady-state and dynamic experimental results are recorded by Siglent SDS1104X-E Super Phosphor Oscilloscope. All presented observations are performed on the same experimental setups without changing the system parameters.

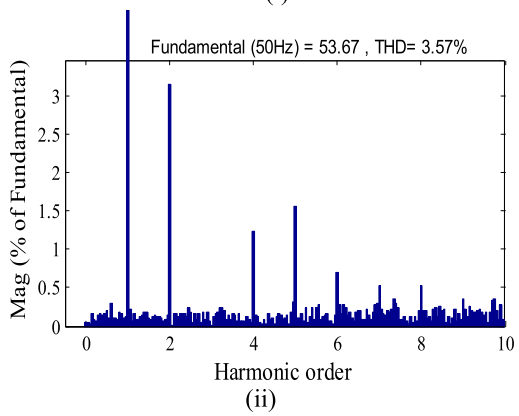
The prototype was verified for two different scenarios: DC-DSTATCOM and IC-DSTATCOM.

Case: A Dynamic performance of DC-DSTATCOM

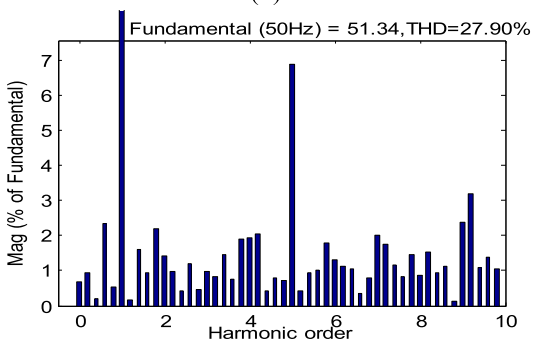
This section presents the experimental results to claim the practical implementation of DC-DSTATCOM using the DBLN technique. The recorded results are presented to



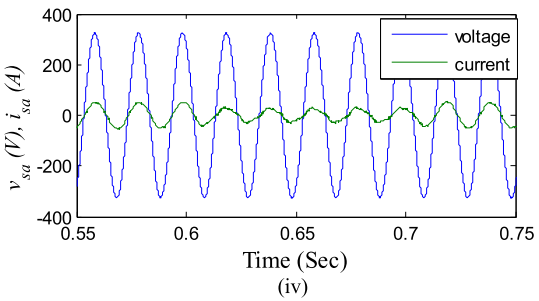
(i)



(ii)

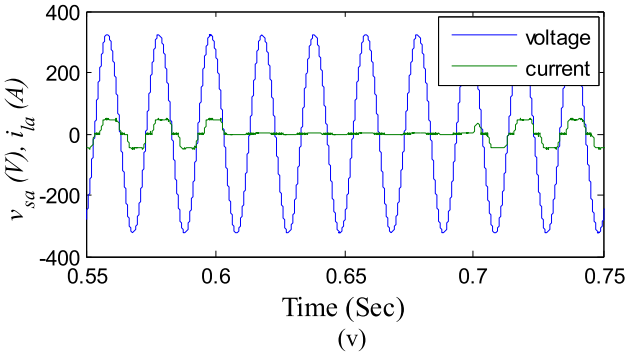


(iii)



(iv)

Fig. 9 **i** Simulated waveforms of system performance with IC-DSTATCOM, **ii** source current THD under IC-DSTATCOM, **iii** load current THD under IC-DSTATCOM, **iv** a-phase source side PF and **v** a-phase load side PF



(v)

Fig. 9 continued

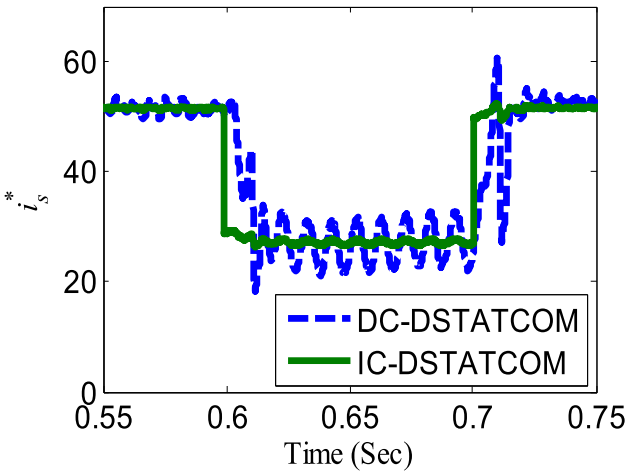


Fig. 10 Internal weighting factor for the source current

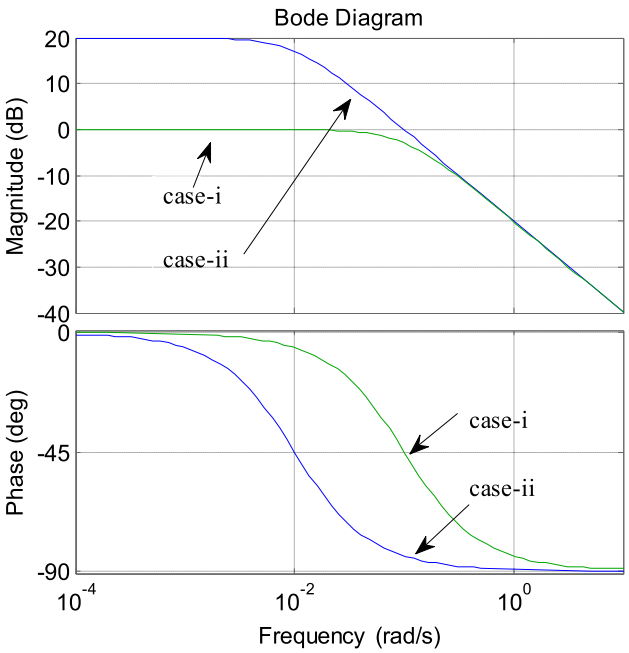


Fig. 11 Frequency response (simulated) of the sensitivity function for the PI controller with variable proportional gains: **i** $K_{pa} = 10$ (green) and $K_{ia} = 1$ (green), **ii** $K_{pa} = 10$ (blue) and $K_{ia} = 0.1$ (blue) (color figure online)

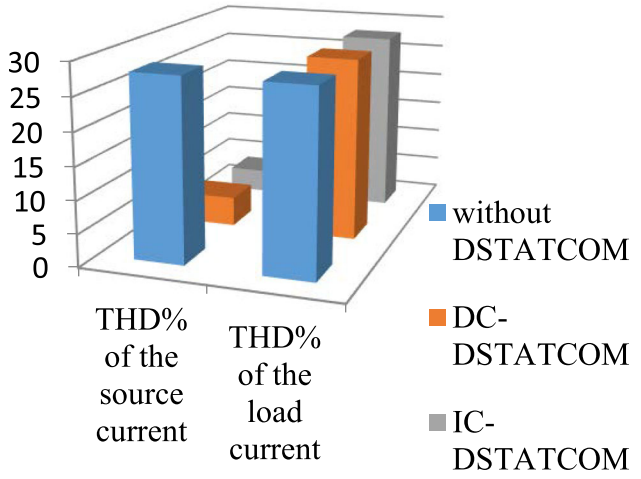


Fig. 12 THD profile obtained from experimental setup

Table 1 Simulation configuration parameters

Sl. no.	Symbol	Definition	Value
1	v_s	Three-phase source voltage	230 V/phase
2	f_s	Frequency	50 Hz
3	R_s	Source resistance	0.5 Ω
4	L_s	Source inductance	2 mH
5	K_{pr}	AC proportional controller	0.2
6	C_{dc}	Capacitor	2000 μF
7	K_{pa}	DC proportional controller	0.01
8	K_{ia}	DC integral controller	0.05
9	v_{dc}	DC link voltage	600 V
10	R_c	VSC resistance	0.25 Ω
11	L_c	VSC inductance	1.5 mH
12	K_{ir}	AC integral controller	1.1

Table 2 Simulated results of DC-DSTATCOM and IC-DSTATCOM

Sl. no.	Performance parameter	DC-DSTATCOM	IC-DSTATCOM
1	i_s (A), %THD	55.01, 4.51	53.67, 3.57
2	v_s (V), %THD	321.4, 2.23	321, 1.42
3	i_l (A), %THD	51.76, 27.90	51.34, 27.90
4	Power factor	0.94	0.99
5	v_{dc} (V)	671.6	605.6

observe the dynamic performance of the controller from 0.55 to 0.75 s. Here, the dynamic state is chosen by switching off "a" phase load with the help of a circuit breaker (CB) from 0.6 to 0.7 s. The balanced and undistorted 440 V (Line-Line) supply voltage is considered and shown in Fig. 14(i). The sinusoidal supply current for three phases of magnitude 55 A

Table 3 Performance comparison between DC-DSTATCOM and IC-DSTATCOM

Sl. no.	Issues	DC-DSTATCOM	IC-DSTATCOM
1	Shunt compensation	Acceptable	Better
2	PF correction	Good	Better
3	Computational burden	High	Medium
4	Estimation speed	Low	High
5	Weight convergence	More than one cycle	Less than one cycle
6	Transient response	Slow	Fast
7	Error in steady state	Moderate	Less
8	Power loss	More	Less
9	Component cost and maintenance	More	Acceptable

Fig. 13 Experimental setup of the DRL controlled IC-DSTATCOM

is shown in Fig. 14(ii). As can be seen, the "a," "b" and "c" phases distorted the load current with its magnitude 50 A depicted in Fig. 14(iii). The compensating current contains that harmonics spike along with DC link voltage is shown in Fig. 14(iv). The source side PF 0.97 is achieved by considering phase "a" supply voltage and current as shown in Fig. 14(v). This result verifies the resistive behavior of the system; voltage and current are sinusoidal, and both are in phase.

But, the load side PF 0.84 is achieved by considering phase "a" load voltage and current, as shown in Fig. 14(vi). During this time, the self-braced capacitor experiences a significant amount of voltage that oscillates around 640 V and satisfies voltage regulation.

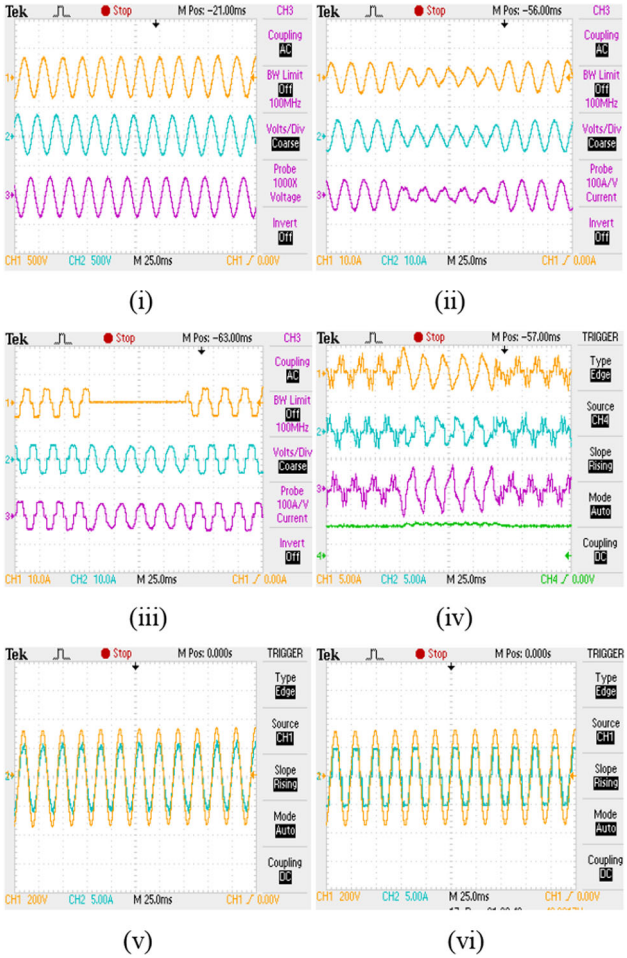


Fig. 14 **i** Source voltage, **ii** source current, **iii** load current, **iv** compensator current with DC link voltage, **v** a-phase source PF and **vi** a-phase load PF using DRL-based DC-DSTATCOM

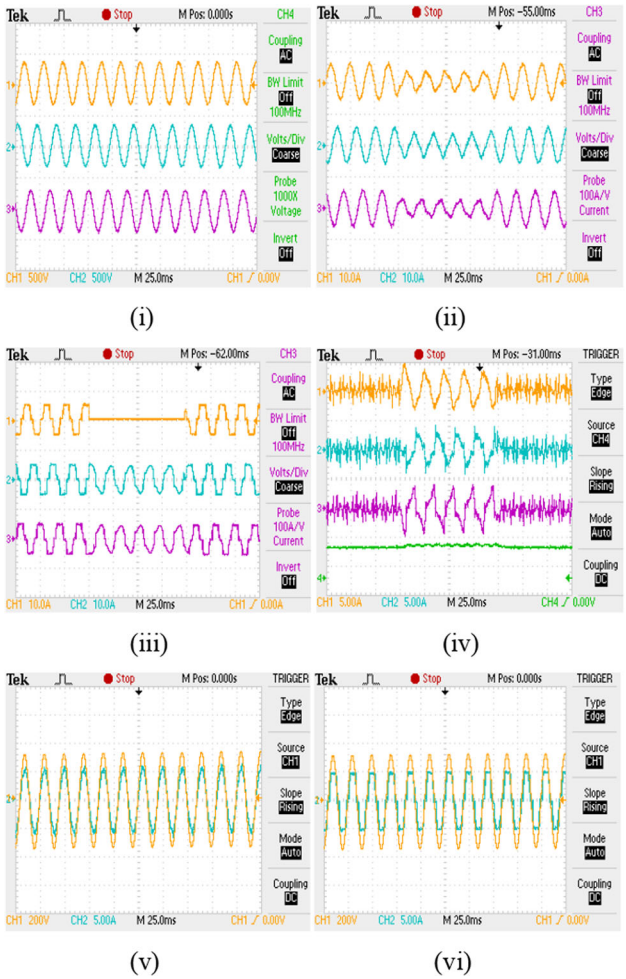


Fig. 15 **i** Source voltage, **ii** source current, **iii** load current, **iv** compensator current with DC link voltage, **v** a-phase source PF and **vi** a-phase load PF using DRL-based IC-DSTATCOM

Moreover, it is observed that the PCC voltage is maintained at a reference level of 317 V irrespective of load switching, which also achieves voltage balancing.

Case: B Dynamic performance of IC-DSTATCOM

This section presents the experimental results to claim the practical implementation of DC-DSTATCOM using the DBLN technique. The recorded results are presented to observe the dynamic state performance of the controller from 0.55 to 0.75 s. Here, the dynamic state is chosen by switching off "a" phase load with the help of a circuit breaker (CB) from 0.6 to 0.7 s. The balanced and undistorted 440 V (Line-Line) supply voltage is considered and shown in Fig. 15(i). The sinusoidal supply current for three phases of magnitude 55 A is shown in Fig. 15(ii). As can be seen, "a," "b" and "c" phases distorted the load current with its magnitude 50 A depicted in Fig. 15(iii). The compensating current contains that harmonic spike along with DC link voltage is shown in Fig. 15(iv).

The source side PF 0.97 is achieved by considering phase "a" supply voltage and current as shown in Fig. 15(v). This result verifies the resistive behavior of the system; voltage and current are sinusoidal, and they are in phase. But, the load side PF 0.84 is achieved by considering phase "a" load voltage and current as shown in Fig. 15(vi). During this time, the self-braced capacitor experiences a significant amount of voltage that oscillates around 580 V and satisfies voltage regulation.

Moreover, it is observed that the PCC voltage is maintained at a reference level of 317 V irrespective of load switching, which also achieves voltage balancing. As shown from Fig. 16, DC link voltage is obtained 542 V and 600 V under balanced and unbalanced loading conditions under DRL controlled IC-DSTATCOM algorithm, respectively. Whereas 580 V and 640 V are obtained under DRL controlled DC-DSTATCOM under different loading conditions, respectively.

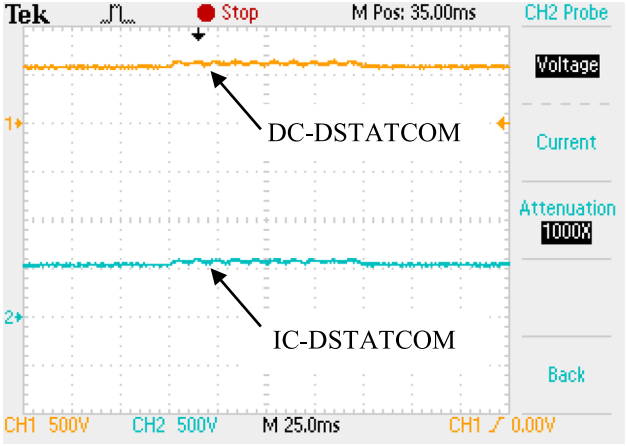


Fig. 16 DC link voltage profile using DRL-based DC-DSTATCOM and IC-DSTATCOM

5 Conclusion

In this paper, this DRL algorithm is designed and implemented for the IC-DSTATCOM to demonstrate the PQ solution under uncertainties of PDN loading.

The superiorities obtained from both the simulation and experimental studies are as follows:

- Improved PF at source side with balanced, sinusoidal, distortion-free source current is obtained.
- Significant THD harmonic reduction 3.57% is achieved by using IC-DSTATCOM as per IEEE-519-2017, IEC-61727 and IEC-61000-1 grid code.
- The DC link voltage is regulated in the range of ± 10% dynamically, which attains 542 V and 600 V using DRL controlled IC-DSTATCOM algorithm under different conditions.
- The switching stress across the switches is reduced due to less variation of DC link voltage under load switching. Hence, the life time and efficiency of the IC-DSTATCOM can be increased.
- Moreover, 13.11% reduced rating of IC-DSTATCOM are observed, demonstrating the reliability and suitability for practical distribution

Author contributions Dr. Mrutyunjaya Mangaraj has conducted the experimental analysis Prof. S M Muyeen has reviewed the paper and supervised the research as required Prof. B Chitti Babu has analyzed the MATLAB simulation study for the different scenarios Dr. N Toushif Khan has written the overall manuscript based upon simulation and experimental study Dr. S Singh has contributed for overall correction and formatting as per journal guidelines Dr. A Chakravarty cross-checked the grammatical error and plagiarism.

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Data availability The raw processed data required to reproduce the above findings cannot be shared at this time due to legal/ethical reasons.

Declarations

Conflict of interest Authors have no conflicts of interest to disclose that are relevant to the content of this work.

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