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Single-phase hybrid multilevel inverter topology with low switching frequency modulation techniques for lower order harmonic elimination

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Abstract: A new single-phase asymmetrical multilevel inverter (MLI) is presented in this study. The proposed topology generates a staircase output voltage waveform with a maximum number of levels using less number of components compared to several existing and recent topologies. The basic module consists of a combination of two isolated DC sources with ten switches that produce all the possible number of levels. Other advantages of the proposed MLI include improved output voltage performance and a low blocking voltage of the switches. The low switching frequency pulse width modulation (LSF-PWM) technique has been used for the generation of gate pulses. In the LSF technique, selective harmonic elimination (SHE) and fundamental switching frequency PWM techniques have been discussed for the better output voltage waveform. The optimised switching angles with SHEPWM has been calculated using particle swarm optimisation considering the different combination of the elimination of lower order harmonics. Simulation work was carried out using MATLAB/SIMULINK, and a prototype was implemented to validate the proposed MLI module. Simulation and experimental results have been provided in the study to show the performance of the proposed topology with these modulation techniques.

1 Introduction

Multilevel inverters (MLIs) are presently one of the most received attention in power electronics converters. MLIs have several advantages compared to conventional two-level inverter like lower total harmonic distortion (THD), better fundamental component, able to generate high voltage using lower voltage rating power devices, low dv/dt, higher efficiency etc. In a MLI, different step voltages are generated to form a staircase waveform that resembles a sinusoidal waveform by using different DC link voltages produced by DC voltage sources and/or capacitors. MLIs are used in a wide range of applications including solar PV systems, motor drives, HVDC systems [1–5]. The design of MLIs mainly depends on the number of output voltage levels required, THD, voltage stress across switches, the number of DC voltage links and components used [6–8]. In general, MLIs are classified as (i) neutral point clamped (NPC) invented in 1981 [9], (ii) flying capacitor (FC) presented in early 1990 [10] and (iii) cascade H-bridge (CHB) reintroduced in 1996 [11]. All three classical MLI topologies require more components as the number of levels increases which increases the size, cost, and control complexity of the topologies. To overcome these problems, several new topologies with a reduced number of components have been proposed. Hybrid inverters are the commonly proposed MLIs. It comprises of two parts, i.e. the first part is a DC–DC converter which generates several levels of output in one polarity, and the second part is an H-bridge which works as a polarity changer. Both parts combine to generate a multilevel voltage with dual polarity at the output [12–20]. The main problem with such configuration is that the H-bridge switches need to be of high voltage rating. Several topologies have been proposed in this configuration. A bidirectional MLI is proposed in [14]. This topology includes the H-bridge for polarity change and requires three DC sources to generate seven levels. In [16] the proposed MLI involves a five-level DC–DC converter and H-bridge. It uses four capacitors to obtain nine levels of the output voltage. A switched-capacitor (SC) MLI is presented in [17] but it also requires the use of an H-bridge with two DC sources and one capacitor to generate seven levels at the output. An MLI based on a modified H-bridge basic unit is presented in [19]. By cascading the H-bridge units, more levels can be generated but not all possible levels from the DC links available.

Modular multilevel inverter (MMC) is categorised as a new MLI topology [21–24]. However, in the MMC topologies, the number of components is higher. They also suffer from the problems of circulating currents. MLIs based on cascaded MLIs have received more attention due to its simplicity and modularity. Cascaded MLIs are divided into two groups: symmetrical MLIs having an equal magnitude of DC voltage sources and asymmetrical MLIs having different values of DC voltage sources. By opting for asymmetrical configuration, more number of levels

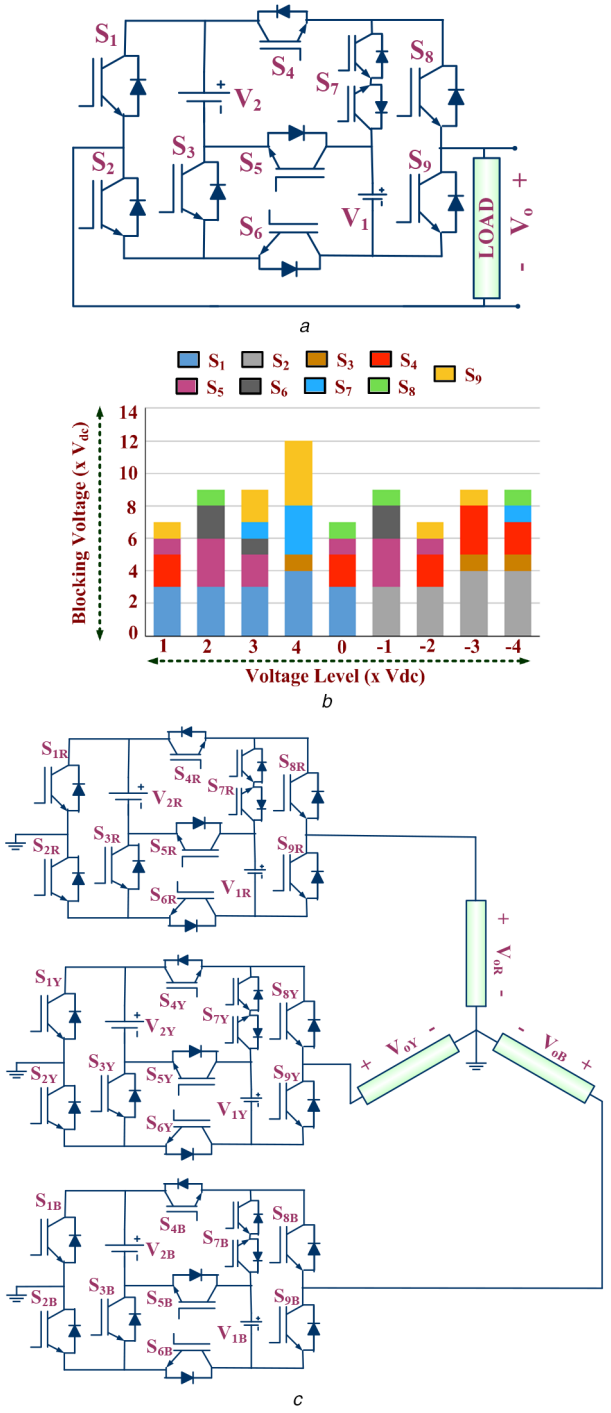

Fig. 1 *Proposed MLI*

(a) Circuit diagram, ***(b)*** Voltage stress across the switches, ***(c)*** Three-phase configuration

can be generated, compared to its symmetrical configuration with the same number of components and DC links. However, the asymmetrical topologies have the problem of unbalance power-sharing among the voltage sources because of differences in magnitude. Also, the number of redundant switching states is reduced as the higher number of levels are generated using a lower number of components [25].

Several asymmetrical MLIs have been reported in the literature. The E-type MLI module is presented in [26]. In this, four DC voltage sources were used to generate 13 levels. The cascading of two such modules produces 25 levels of the output voltage. However, eight DC isolated sources are required. The improved version of E-type is the square T (ST) type [27]. In ST-type, 4 DC voltage sources are used to generate 17 levels compared to only 13 levels for the E-type. Both E-type and ST-type MLIs generate both polarities without using H-bridge, but both topologies require more number of DC sources to generate 13 and 17 levels, respectively. Similarly, Odeh *et al*. [28] presented the MLI for nine levels using three isolated DC sources. Topology in [29] generates nine-level output voltage by employing one DC voltage source and two capacitors. It uses 11 power devices with higher blocking voltage ratings.

In this paper, a single-phase asymmetrical MLI is proposed, comprising an arrangement of switches and DC voltage sources to generate the maximum number of levels from multiple DC links. In the proposed MLI module, two DC sources are used with ten switches to generate $3^2 = 9$ levels, i.e. four positive levels, four negative levels, and zero. Both polarities are generated inherently in the proposed module without using H-bridge. The cascade connection of two or more modules is also possible to generate more number of levels and higher output voltage. In Section 2, the topology of the proposed MLI is discussed in detail. Section 3 gives the comparison of the proposed MLI with other existing topologies, and Section 4 describes the modulation technique used. Simulation and experimental results with a suitable application of the proposed topology have been discussed in Section 5. The conclusion is given in Section 6.

2 Proposed MLI topology

2.1 Power circuit and operation

Fig. 1*a* shows the circuit configuration of the proposed MLI module. It comprises of eight unidirectional switches, one bidirectional switch, and two DC sources. Each unidirectional switch (unidirectional for voltage and bidirectional conduction for current) comprises an IGBT with its antiparallel-diode connected. The bidirectional switch (bidirectional for voltage and current) comprises two unidirectional switches. DC sources are arranged in the tertiary configuration. For tertiary configuration $V_2/V_1 = 3$. With this configuration, nine levels (9L) can be generated which includes four positive levels, four negative levels, and zero. The important feature of this topology is its ability to create different voltage levels for both polarities without using an H-bridge circuit. The switches are connected in such a manner that their anti-parallel diodes do not become forward bias that can cause short-circuiting of the sources. The switches in each of the following groups (S_1, S_2, S_3), (S_3, S_5, S_6), (S_4, S_5, S_7), (S_3, S_4, S_6, S_7) and (S_7, S_8, S_9) are not turn ON simultaneously, otherwise, it will short circuit of the DC sources. The switching state for the proposed topology is selected such that it takes into consideration all conditions and requires the least dead band to avoid short-circuiting of sources. Fig. 1*b* shows the individual voltage stress of switches and total standing voltage (TSV) for each level. TSV is the sum of maximum blocking voltage calculated for each switch with all output voltage levels considered. Lower TSV reduces the cost of the switch. From Fig. 1*b*, it is clear that TSV is not the same for the same level in positive and negative polarity. This is because of the asymmetrical design of the MLI. Fig. 1*c* shows the three-phase configuration of the proposed topology. Table 1 shows the different switching states of the proposed MLI and Figs. 2 and 3 show the operation of the proposed MLI for different positive and negative voltage levels, respectively.

From Table 1, the number of turn ON of a switch in a half cycle is only once or twice. Therefore, it reduces the switching losses of the module for the low-frequency PWM technique, which is adopted in this paper. For low-frequency MLI, the selection of switches mainly depends on the blocking voltage and ON-state current handling capabilities. The topology structure determines the blocking voltage of each switch.

2.2 Module extension

A modular extension of the proposed topology can be used to generate more number of levels. Two or more modules can be connected in a cascaded connection as shown in Fig. 4. Fig. 4 shows the cascade connection of two modules. Module A generates $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$ and zero voltage levels. Module B can be configured to generate two distinct sets of voltage levels as

Table 1 Switching table for the proposed nine-level MLI

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o ($\times V_{dc}$)
0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	1	1	0	1
0	1	1	1	0	0	1	0	1	2
0	1	1	1	0	0	0	1	0	3
0	1	0	1	1	1	0	1	0	4
1	0	0	1	0	0	0	1	0	0
1	0	0	1	0	0	1	0	1	−1
1	0	1	0	0	1	1	1	0	−2
1	0	1	0	0	1	0	0	1	−3
1	0	0	0	1	0	0	0	1	−4

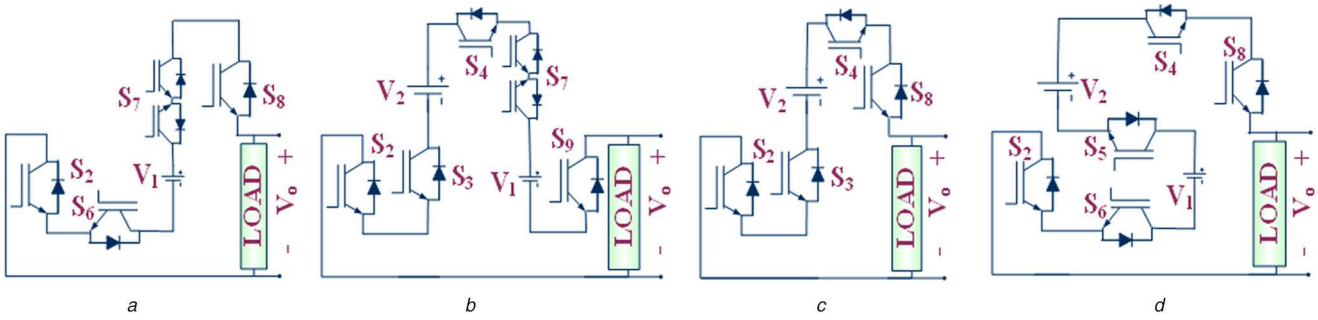

Fig. 2 *Different switching states for generation of positive levels*
(a) $V_o = V_{dc}$, ***(b)*** $V_o = 2V_{dc}$, ***(c)*** $V_o = 3V_{dc}$, ***(d)*** $V_o = 4V_{dc}$

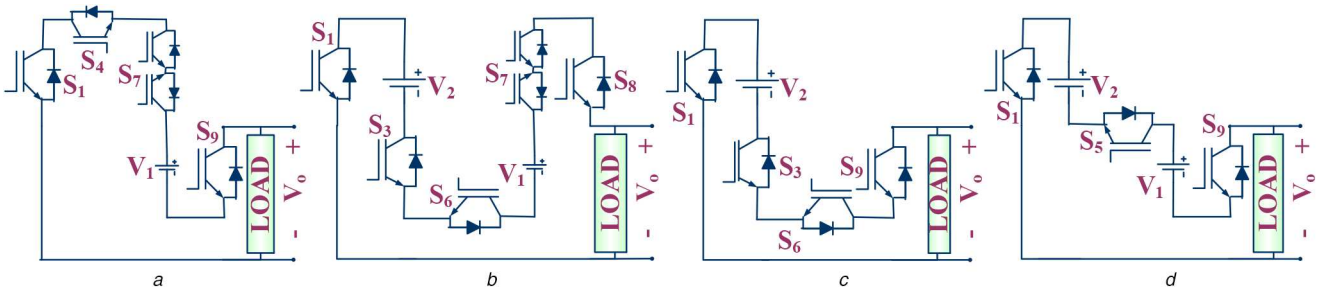

Fig. 3 *Different switching states for generation of negative levels*
(a) $V_o = -V_{dc}$, ***(b)*** $V_o = -2V_{dc}$, ***(c)*** $V_o = -3V_{dc}$, ***(d)*** $V_o = -4V_{dc}$

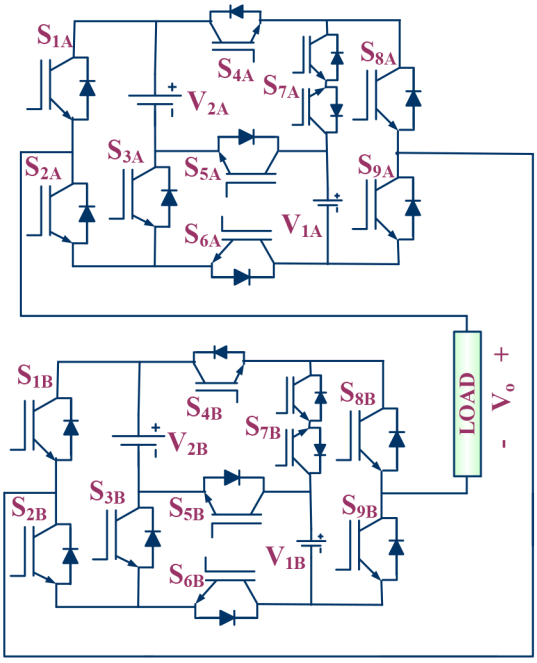

Fig. 4 *Cascade connection of two modules*

Table 2 Configuration of two modules for 17 levels

X_1	X_2								
	−4	−3	−2	−1	0	1	2	3	4
−4	−8	−7	−6	−5	−4	−3	−2	−1	0
−3	−7	−6	−5	−4	−3	−2	−1	0	1
−2	−6	−5	−4	−3	−2	−1	0	1	2
−1	−5	−4	−3	−2	−1	0	1	2	3
0	−4	−3	−2	−1	0	1	2	3	4
1	−3	−2	−1	0	1	2	3	4	5
2	−2	−1	0	1	2	3	4	5	6
3	−1	0	1	2	3	4	5	6	7
4	0	1	2	3	4	5	6	7	8

Table 3 Configuration of two modules for 81 levels (mode II)

X_1	X_2								
	−36	−27	−18	−9	0	9	18	27	36
−4	−40	−31	−22	−13	−4	5	14	23	32
−3	−39	−30	−21	−12	−3	6	15	24	33
−2	−38	−29	−20	−11	−2	7	16	25	34
−1	−37	−28	−19	−10	−1	8	17	26	35
0	−36	−27	−18	−9	0	9	18	27	36
1	−35	−26	−17	−8	1	10	19	28	37
2	−34	−25	−16	−7	2	11	20	29	38
3	−33	−24	−15	−6	3	12	21	30	39
4	−32	−23	−14	−5	4	13	22	31	40

Table 4 Equations of modules for cascade connection

	Based on cascaded connections	Based on no. of levels $N = 8k + 1$
no of levels	3^{2k}	N
no of switches	10k	$5(N-1)/4$
no of drivers	9k	$N + (k-1)$
no of DC sources	2k	$(N-1)/4$
TSV	25k	$25(N-1)/8$

Table 5 Output levels of modules for cascade connections

Module A	Module *K*th	
	Mode I	Mode II
$V_{1k} = V_{dc}$, $V_{2k} = 3\ V_{dc}$	$V_{1(k+1)} = V_{dc}$, $V_{2(k+1)} = 3\ V_{dc}$	$V_{1(k+1)} = 3\ V_{2k}$, $V_{2(k+1)} = 3\ V_{1(k+1)}$
output levels: 0,	output levels: 0,	output levels: 0,
$\pm V_{dc}$, $\pm 2\ V_{dc}$,	$\pm V_{dc}$, $\pm 2\ V_{dc}$,	$\pm 3^k V_{dc}$, $\pm 2*3^k V_{dc}$,
$\pm 3\ V_{dc}$, $\pm 4\ V_{dc}$	$\pm 3\ V_{dc}$, $\pm 4\ V_{dc}$	$\pm 3*3^k V_{dc}$, $\pm 4*3^k V_{dc}$

given in Tables 2 and 3 where $X_1 = V_{A1A2}/V_{dc}$ and $X_2 = V_{B1B2}/V_{dc}$. In both tables, the magnitude of the output voltage is given for each pair of X_1 and X_2 values. From Table 2, if module B generates zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$ voltage levels, then 17 level output voltage will appear across the load (Mode I). If module B generates zero, $\pm 9V_{dc}$, $\pm 18V_{dc}$, $\pm 27V_{dc}$ and $\pm 36V_{dc}$, then the cascade configuration will produce 81 levels of output voltage (Mode II).

Table 4 shows the equations of the voltage levels, number of switches, driver circuits, DC voltage sources required and TSV for the proposed cascade MLI where k is the number of modules connected in cascade. Table 5 gives the output voltage levels of different modules connected in cascade with the selection of magnitude of input voltages for all modules.

3 Comparative study

The proposed topology is compared with some recent and similar asymmetrical MLI. Table 6 compares the proposed MLI with several recent nine-level inverters topologies based on the number of switches, DC sources, capacitors, TSV etc. From Table 6, the proposed topology and topology of [13] has the minimum number of power devices, i.e. ten, however, the topology of Bin Arif *et al*. [13] used H-bridge which required higher blocking voltage. As given in Table 6, the required number of switches of higher voltage rating is low, i.e. for the proposed topology, three switches of $4V_{dc}$ rating are required whereas, in the topologies of [13, 15, 16, 29], four switches of $4V_{dc}$ is required. The lower voltage rating is reflected in terms of the TSV of the topology which is lower for the proposed topology compared to the topologies of [13, 15, 20, 29]. The topology proposed in [28] has minimum TSV but uses three voltage sources for the same number of voltage levels which limits its acceptability. The proposed MLI requires the least number of DC links to produce 9L. Besides, the proposed MLI does not use capacitors, thus problems related to capacitors such as voltage balancing, power losses and cost are not present in the proposed MLI.

The cascade connection of the proposed topology has also been compared with similar topologies. Fig. 5*a* illustrated the variation of the number of switches and Fig. 5*b* shows the variation of the number of DC voltage sources with the output levels of the cascade

Table 6 Comparison of proposed topology with some recent topologies for single module (9 level)

Topology	Switches/diodes/power devices/drivers/DC sources/ capacitor	Blocking voltage (number of power devices) 4 V_{dc}	3 V_{dc}	2 V_{dc}	V_{dc}	TSV (×V_{dc})	Total component	Polarity changer
[13]	10/0/10/10/2/0	4	1	3	2	27	12	H Bridge
[15]	9/2/11/9/1/2	4	0	3	4	26	14	H Bridge
[16]	12/0/12/12/1/4	4	0	0	8	24	17	H Bridge
[20]	12/0/12/12/3/0	3	0	5	4	26	15	H Bridge
[28]	7/4/11/7/3/0	2	0	4	5	21	14	inherent
[29]	10/1/11/8/1/2	4	1	3	1	26	14	inherent
proposed	10/0/10/9/2/0	3	3	1	2	25	12	inherent

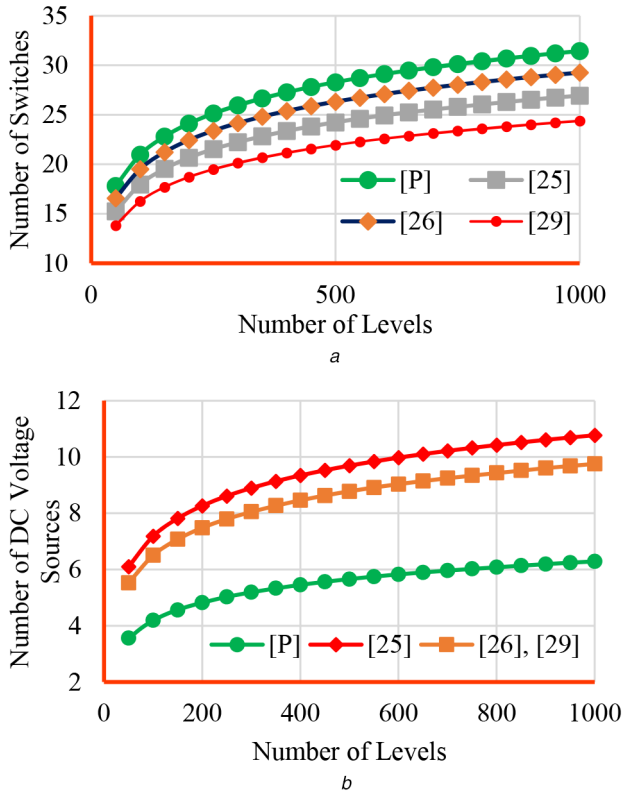

Fig. 5 *Comparison of the cascade connection with*
(a) Number of switches, ***(b)*** Number of DC voltage sources with respect to the number of levels

connection. As the proposed topology has the ability to produce all the available number of levels from the multiple DC voltage sources, the required number of DC voltage source is lower compared to all other topologies as shown in Fig. 5*b*.

4 PWM technique

There are various modulation techniques for MLIs proposed in the literature. Low switching frequency modulation techniques are preferred for MLIs because of having a lower number of transitions in a half cycle, resulting in negligible switching losses. The low switching frequency pulse width modulation (LSF-PWM) technique includes selective harmonic elimination pulse width modulation (SHEPWM), NLCPWM, Half-Height (HH) PWM etc. to generate the pulse width modulated output voltage, [30–35]. In this paper, SHEPWM and NLCPWM techniques have been used for the generation of gate pulses. SHEPWM gives the flexibility of the selection of harmonic order to be eliminated from the output voltage waveform.

4.1 SHEPWM technique

SHEPWM technique is one of the most famous techniques which has been used for the elimination of the lower order harmonics. The presence of lower order harmonics in the output voltage

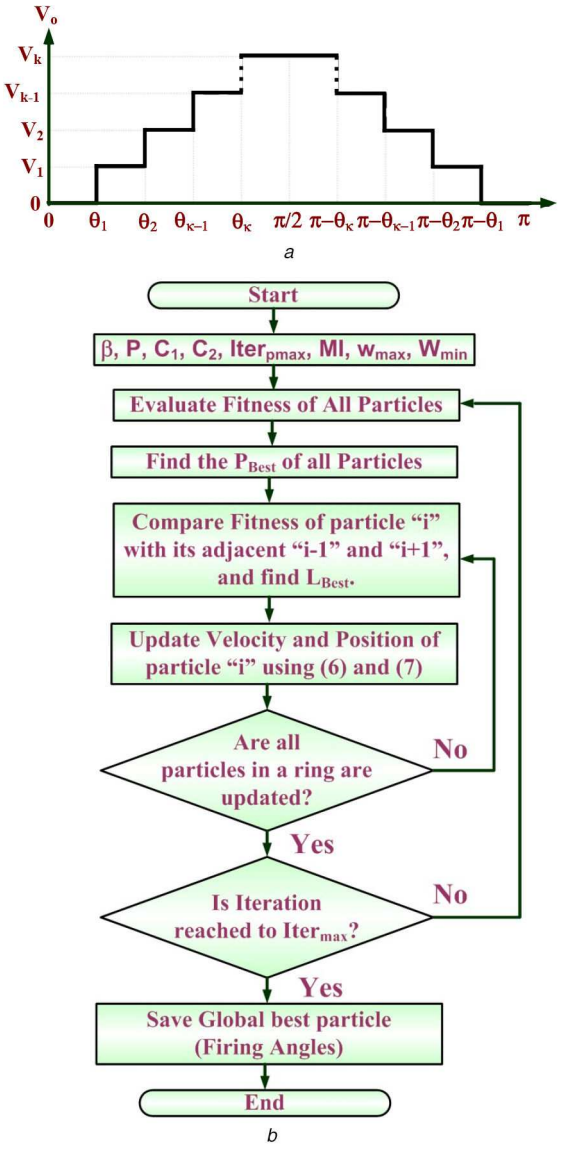

Fig. 6 *Waveform and flowchart*
(a) Staircase modulated output voltage, ***(b)*** Flowchart for PSO algorithm

waveforms reduces the utilisation of the output voltage. Fig. 6*a* shows the staircase output voltage waveform for N number of levels with k number of switching angles. The Fourier series of the output voltage waveform can be expressed as follows:

$$v_o(t) = \frac{a_o}{2} + \sum_{i=0}^{n} \left\{ a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right) \right\} \quad (1)$$

where a_o, a_n, and b_n gives the value of the DC component, even-numbered harmonic and odd-numbered harmonic component and n is the harmonic order. Since the output voltage possesses quarter-

wave symmetry, the value of a_o, a_n, and sine terms of odd harmonics become zero. Therefore, based on quarter-wave symmetry, (1) modifies as:

$$v_o(t) = \sum_{i=1,3,5}^{n} b_n \sin(n\theta_k) \tag{2}$$

where b_n can be expressed as

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{i=1,3,5}^{n} \cos(n\theta_k). \tag{3}$$

For 9L, θ_1, θ_2, θ_3, θ_4 are the switching angles which need to be calculated. For 9L output voltage, three lower-order harmonics can be removed. In this paper, two different sets of harmonics have been eliminated from the output voltage.

4.1.1 Set I (3rd, 5th, and 7th): For a single-phase output voltage, the lower order harmonics are 3rd, 5th, and 7th. The different equation for the elimination of these harmonic order is given as:

$$\left.\begin{aligned} b_1 &= \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] = V_d \\ b_3 &= \frac{4V_{dc}}{3\pi}[\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4)] = 0 \\ b_5 &= \frac{4V_{dc}}{5\pi}[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4)] = 0 \\ b_7 &= \frac{4V_{dc}}{7\pi}[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4)] = 0 \end{aligned}\right\} \tag{4}$$

where $b_1 = V_D$ is the fundamental component that gives the desired output voltage V_D. While b_3, b_5, and b_7 are the harmonic orders which need to be eliminated and made equal to zero. The modulation index m_a is given by

$$m_a = \frac{\pi \times V_d}{4 \times N \times V_{dc}}. \tag{5}$$

For the basic module, 3rd, 5th, and 7th order harmonics are selected for elimination from the output voltage waveform. In the SHEPWM technique, switching angles are calculated using (4) and (5) by maintaining the relationship $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2$. The solution of (4) and (5) gives the switching angle which will be used for the generation of gate pulses. For the proposed inverter, optimised switching angles are calculated using the particle swarm optimisation (PSO) algorithms described in [27]. In PSO, particles are arranged in a ring topology that updates their velocity and position using (6) and (7) respectively

$$v_{i,j}^{t+1} = \left(v_{i,j}^{t} \times w^{t+1}\right) + \begin{bmatrix} C_1 + r_{1j}^{t} \times \\ \left(P_{\text{Best},i}^{t} - x_{i,j}^{t}\right) \end{bmatrix} + \begin{bmatrix} C_2 + r_{2j}^{t} \times \\ \left(L_{\text{Best}} - x_{i,j}^{t}\right) \end{bmatrix} \tag{6}$$

$$x_{i,j}^{t+1} = x_{i,j}^{t} + v_{i,j}^{t+1} \tag{7}$$

where L_{Best} is the local best particle among $i + 1$, i, and $i - 1$, $P_{\text{Best},i}^{t}$ is the personal best position of particle and w^{t+1} is the inertia weight calculated using (8). Table 7 gives the values of control parameters selected for the PSO algorithm

$$w^{t+1} = w_{\max} - \left(\frac{w_{\max} - w_{\min}}{\text{Total number of iterations}} \times \text{current iteration}\right). \tag{8}$$

Fig. 6*b* illustrates the flowchart of the PSO-based algorithm to solve the equation of SHEPWM. Fig. 7*a* shows the variation of switching angles with the modulation index for all four switching angles, i.e. θ_1, θ_2, θ_3, and θ_4. Similarly, the variation of the magnitude of selected harmonic has been shown in Fig. 7*b*. With the selected harmonic orders, the optimised switching gives the lower harmonic values for the modulation index of 0.4–0.9.

Table 7 Control parameter value selected for PSO

Symbol	Quantity	Values
c_1, c_2	acceleration coefficient	2.0
P	swarm size	100
$w_{\min}$	minimum inertia	0.4
$w_{\min}$	maximum inertia	0.9
$\text{iter}_{P\max}$	maximum number of Iterations	500
B	initialisation of swarm	$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4$
m_a	modulation index	$0 < m_a <= 1$

4.1.2 Set II (5th, 7th, and 11th): For a three-phase system, all the triple harmonic orders are eliminated because of three-phase symmetrical connections. Therefore, for the three-phase systems, the lower order harmonics are the 5th, 7th, and 11th. Therefore, (4) modifies as

$$\left.\begin{aligned} b_1 &= \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] = V_d \\ b_5 &= \frac{4V_{dc}}{5\pi}[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4)] = 0 \\ b_7 &= \frac{4V_{dc}}{7\pi}[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4)] = 0 \\ b_{11} &= \frac{4V_{dc}}{11\pi}[\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4)] = 0 \end{aligned}\right\}. \tag{9}$$

The solution of (5) and (9) gives the optimised switching angles. Fig. 7*c* shows the variation of switching angles and Fig. 7*d* depicts the variation of harmonics magnitude with respect to the modulation index.

4.2 Fundamental switching frequency PWM

For a lower number of levels, the SHEPWM technique gives a better performance in the elimination of lower order harmonics, however, as the number of levels becomes high, the computational time required to solve the equations for SHEPWM become more and thus SHEPWM is not a favourable method to be implemented for a higher number of levels. Furthermore, with a higher number of levels, the value of lower order harmonics becomes less, therefore their removal from the output voltage is not of too much importance. Therefore, for a higher number of levels, the fundamental switching frequency PWM technique can be used for the cascade connection of the proposed modules. The calculation of angle θ_k is given by (10)

$$\theta_k = m_a \sin^{-1}\left(\frac{2i-1}{N-1}\right) \tag{10}$$

where m_a is the modulation index and N is the number of levels and $i = 1, 2, \ldots$, and $(N-1)/2$.

5 Results and discussion

Simulation of the proposed module with SHEPWM is carried out by using MATLAB/Simulink software. Table 8 shows the different voltage parameters for three different configurations. For the generation of gate pulses, optimal switching angles are used which are calculated using the method explained in Section 4. Table 9 gives the different switching angles with different modulation indexes which are used for the simulation and hardware results. Fig. 8 illustrates the different output voltage with their respective harmonic spectrum. Figs. 8*a–c* shows the output voltage waveforms for three different modulation indexes with the elimination of 3rd, 5th, and 7th harmonics from the output voltage.

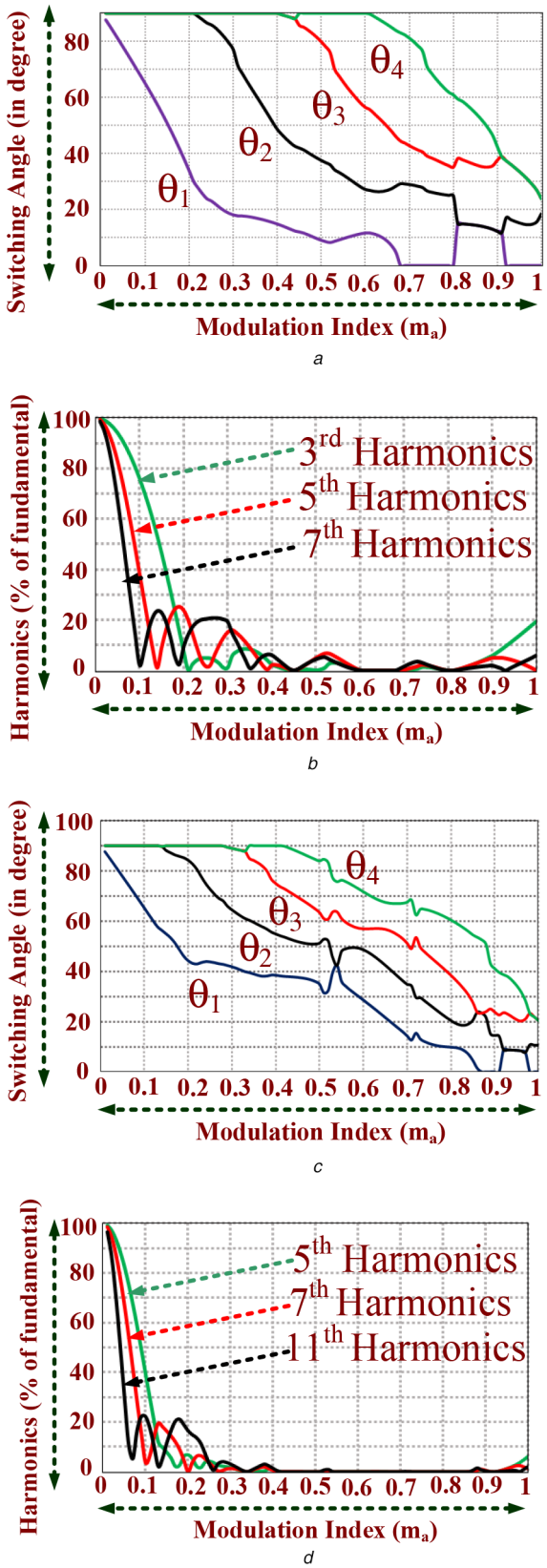

Fig. 7 *Switching angle and harmonics plots*
(a) Switching angles with respect to modulation index with set I, ***(b)*** Harmonic with respect to modulation index with set I, ***(c)*** Switching angles with respect to modulation index with set II, ***(d)*** Harmonic with respect to modulation index with set II

For the lower modulation index, i.e. 0.60, as shown in Fig. 8*a*, the elimination of these selected harmonics is very difficult and a small presence of these harmonics can be noticed from Fig. 8*a*. However, the other two modulation indexes, i.e. 0.65 and 0.80, the selected lower order harmonics are eliminated from the output voltage as depicted in Figs. 8*b* and *c*, respectively. On the same line, the output voltage and their respective FFTs for different modulation indexes have been illustrated in Fig. 8*d*, 9*a* and *b* for Set II which eliminates 5th, 7th, and 11th harmonic orders. Furthermore, the cascading of two modules has also been simulated. With two modules in mode I configuration, 17 level output voltage is achieved and is shown in Fig. 9*c*. Similarly, with mode II, 81 level output voltage waveform is shown in Fig. 9*d*. For the cascade connection, the fundamental switching frequency PWM technique has been used for the gate pulse generation and the FFT of the 17 levels and 81 level output voltage has been shown in Figs. 9*c* and 9*d* respectively. The lower order harmonics for these number of levels are very low as depicted in Figs. 9*c* and *d*, the fundamental switching frequency PWM technique gives an adequate performance in terms of the magnitude of lower order harmonics.

To validate simulation results, experimental tests were carried out with an experimental hardware setup. Fig. 10 shows the experimental setup of the proposed topology. This experimental setup uses IRG4PH40UD power IGBT which includes an antiparallel diode, and dSPACE CP1104 is used to generate the gate pulses for all IGBTs. The gate pulses are passed through a gate driver circuit made up of NXP 74HC04N IC and A3120 optocoupler. Fig. 11 shows the experimental results for the proposed nine-level topology with a different modulation index considering the elimination of 3rd, 5th, and 7th harmonic order. Their respective harmonic spectrum is shown in Fig. 11. As shown from these figures, except for the results at 0.60, the selected harmonic orders are eliminated from the output voltage waveform. Similarly, the output voltage waveform and their respective harmonic spectrum with the elimination of 5th, 7th, and 11th harmonic orders are shown in Fig. 12. The three modulation indexes are 0.60, 0.65, and 0.80. With these three modulation indexes, the selected harmonic order is eliminated from the output voltage waveform.

The proposed topology has also been tested with different types of load. Fig. 13*a* shows the output voltage with its corresponding current waveform with a series-connected resistive-inductive load of $Z = 200$ mH + 40 Ω. In addition to this, the output voltage and current waveform with the change of modulation index with the same load parameter has been depicted in Fig. 13*b*. The modulation index has been changed from 0.80 to 0.65. With this change of modulation index, the peak of the load current changes which can be observed from Fig. 13*b*. Furthermore, the proposed nine-level topology has been tested with the dynamic change of load. Fig. 13*c* illustrates the change of load from no load to $Z =$ 100 Ω, and $Z = 100$ to $Z = 50$ Ω. A zoomed view of the change of load from $Z = 100$ to $Z = 50$ Ω has been shown in Fig. 13*d*. From all these experimental results, the proposed nine-level topology shows its performance in different lading conditions.

The power loss analysis of the proposed 9L topology has been accomplished using PLECS software. PLECS is used to build the thermal model of the proposed topology. Fig. 14*a* shows the variations in efficiency as the load output power is changed. Furthermore, the power loss distribution among different switches has been illustrated in Fig. 14*b*. As evident from Fig. 14*b*, the power loss of two switches, i.e. S_7 and S_8 has a loss-share of 6 and 8% of the total switching losses. The remaining switches have a loss-share of 13–14% of the total power loss.

As the required number of switches for the proposed topology is low, it finds suitable for applications related to renewable energy. Fig. 15 shows the integration of the proposed topology with a solar PV system. The two dc voltage sources are replaced by two DC/DC converter with solar panels. DC/DC converter is used for maximum power point tracking (MPPT). The output voltage of these two solar panels determines the level number. The proposal of a topology for configuration of the tertiary voltage for the output voltage of 9. Therefore, the voltage magnitude of both solar panel is also configured such that $V_2/V_1 = 3$.

6 Conclusion

A new nine-level asymmetrical MLI topology is proposed in this paper. When compared with other topologies, the proposed MLI gives several advantages such as a reduced number of DC voltage

Table 8 Output voltage parameters for simulation and experimental results

No of levels	Module A		Module B		Maximum voltage, V
	V_{1A}, V	V_{1B}, V	V_{2A}	V_{2B}	
9	50	150	—	—	200
17	25	75	25 V	75 V	200
81	5	15	45 V	135 V	200

Table 9 Optimised switching angles

Modulation index	Switching angles				Eliminated harmonics			
	θ_1	θ_2	θ_3	θ_4	3rd	5th	7th	11th
0.50	34.91	51.21	63.40	83.93	-	×	×	×
0.70	9.84	20.38	38.40	60.42	-	×	×	×
0.80	14.31	34.82	51.16	67.48	-	×	×	×
0.60	11.61	27.15	56.43	89.99	×	×	×	—
0.65	8.66	26.82	49.57	85.96	×	×	×	—
0.80	0.01	24.91	35.13	60.90	×	×	×	—

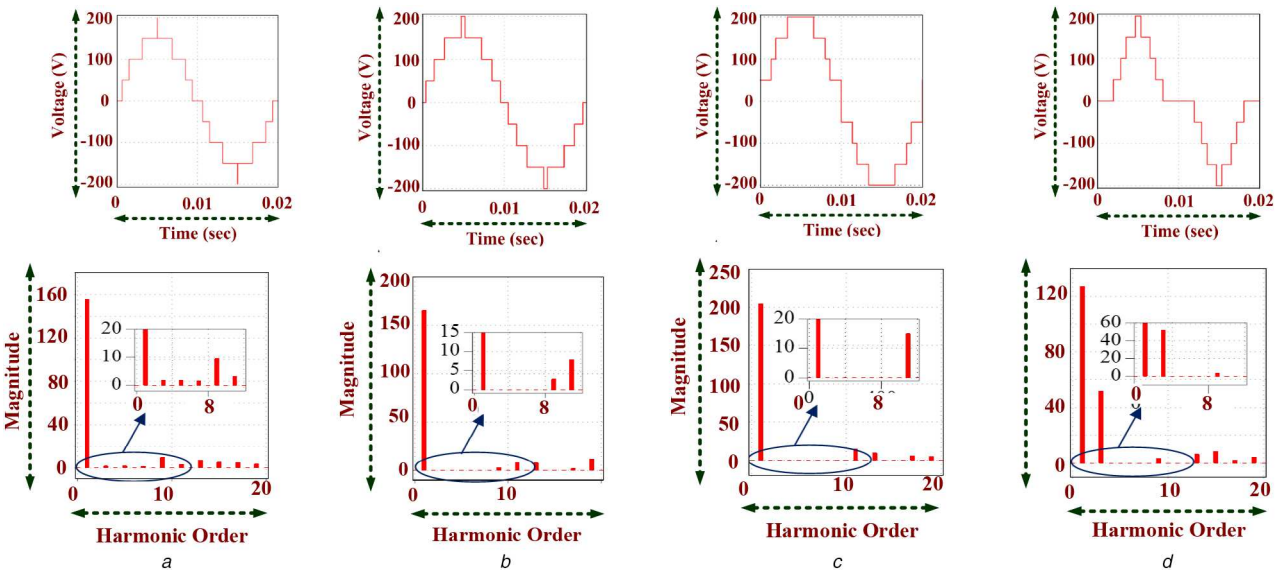

Fig. 8 *Simulation results of the proposed topology with different modulation index and their respective voltage harmonic spectrum (FFT)*
(a) $m_a = 0.60$ (set I), ***(b)*** $m_a = 0.65$ (set I), ***(c)*** $m_a = 0.80$ (set I), ***(d)*** $m_a = 0.50$ (set II)

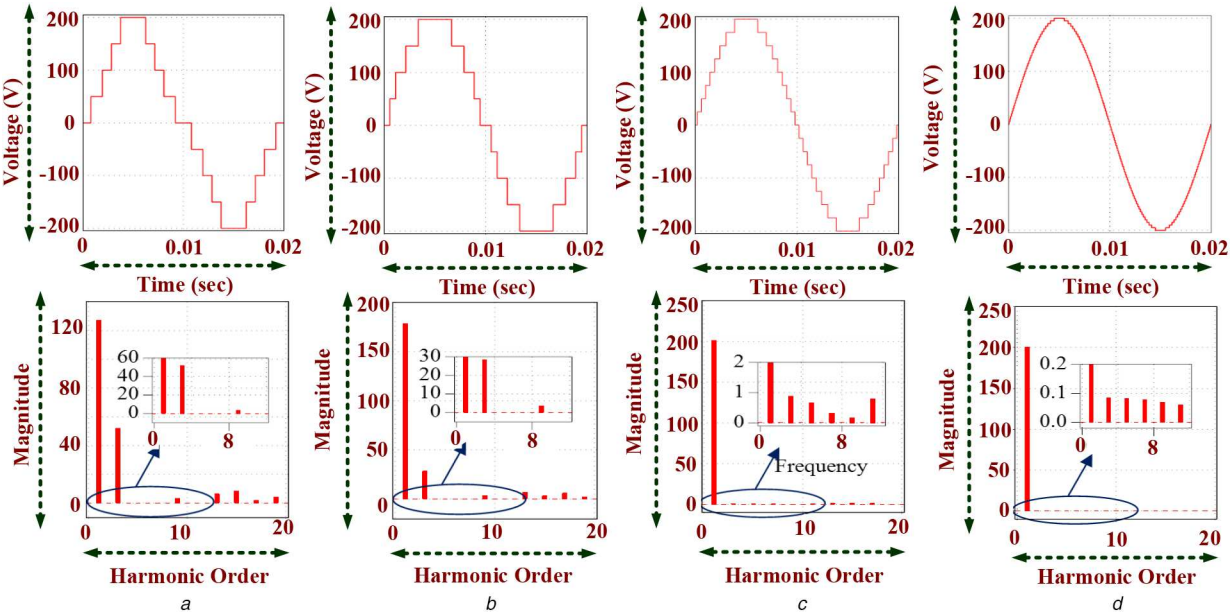

Fig. 9 *Simulation results of the proposed topology with different modulation index and their respective voltage harmonic spectrum (FFT)*
(a) $m_a = 0.70$ (set II), ***(b)*** $m_a = 0.80$ (set II), ***(c)*** Cascaded Connection I, ***(d)*** Cascaded connection II

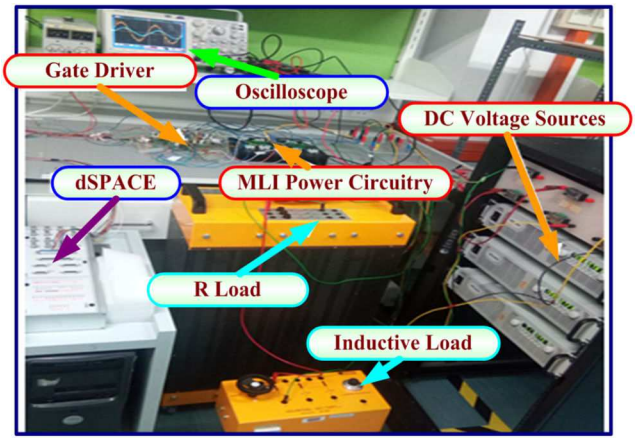

Fig. 10 *Experimental setup of the proposed nine-level topology*

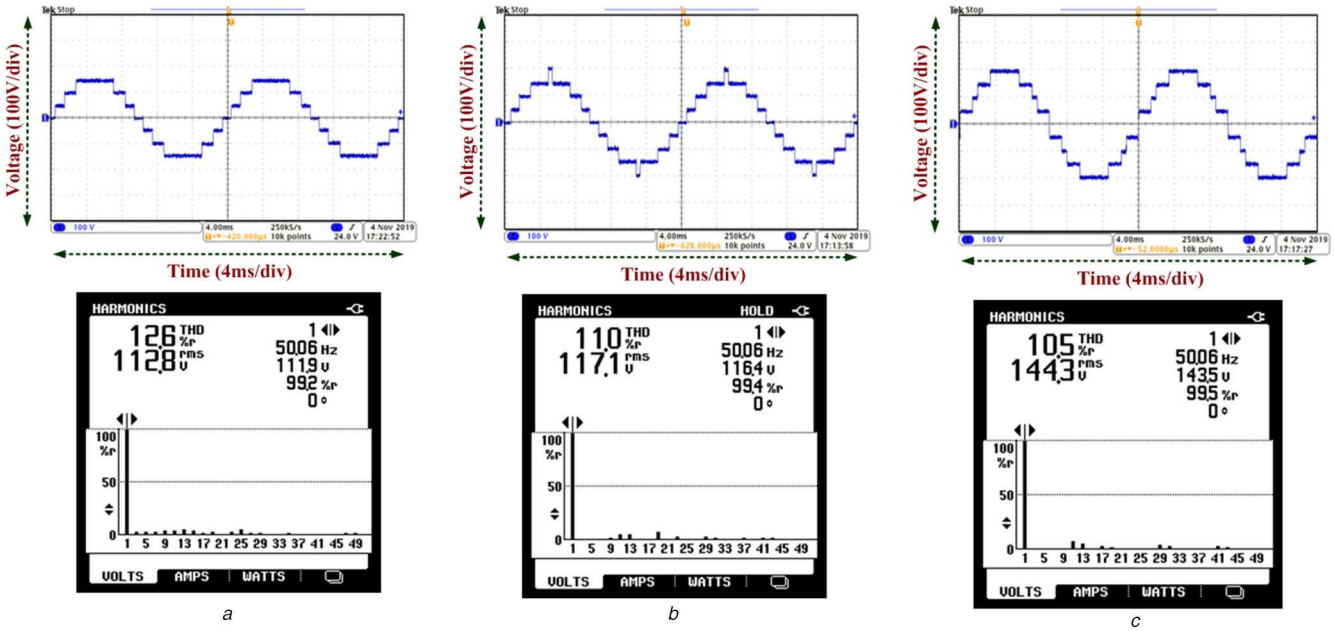

Fig. 11 *Hardware results of the proposed topology with different modulation index and their respective voltage harmonic spectrum (FFT)*
(a) $m_a = 0.60$ (set I), ***(b)*** $m_a = 0.65$ (set I), ***(c)*** $m_a = 0.80$ (set I)

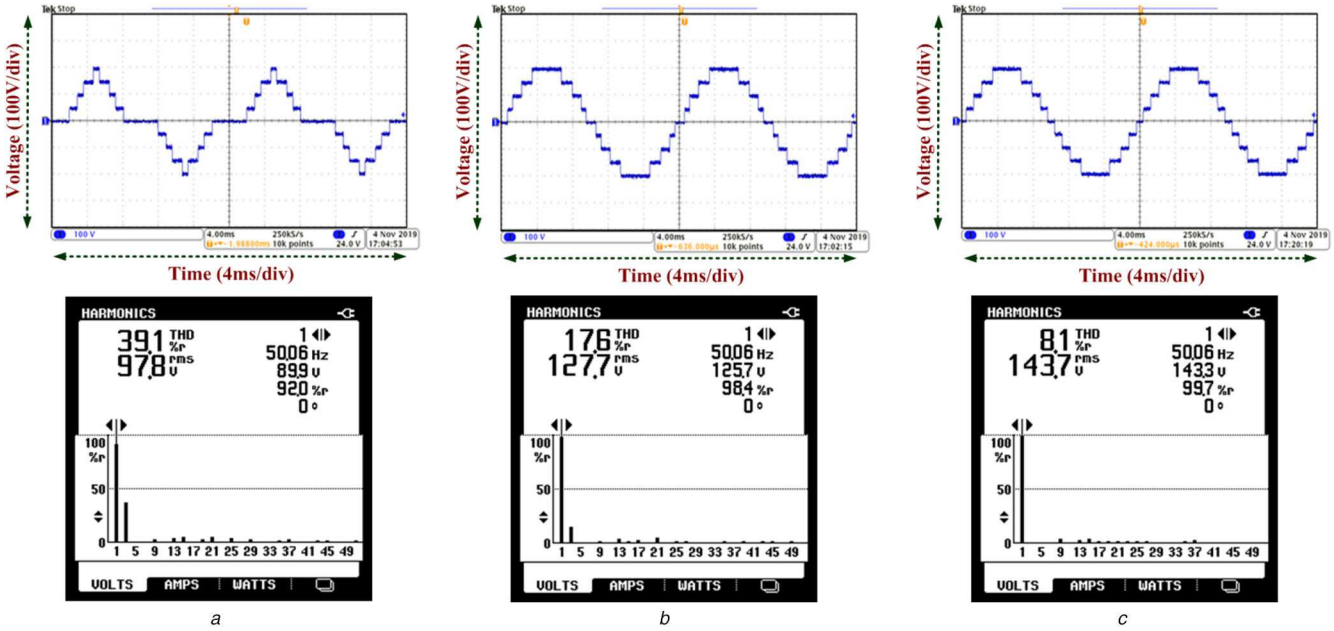

Fig. 12 *Hardware results of the proposed topology with different modulation index and their respective voltage harmonic spectrum (FFT)*
(a) $m_a = 0.50$ (set II), ***(b)*** $m_a = 0.70$ (set II), ***(c)*** $m_a = 0.80$ (set II)

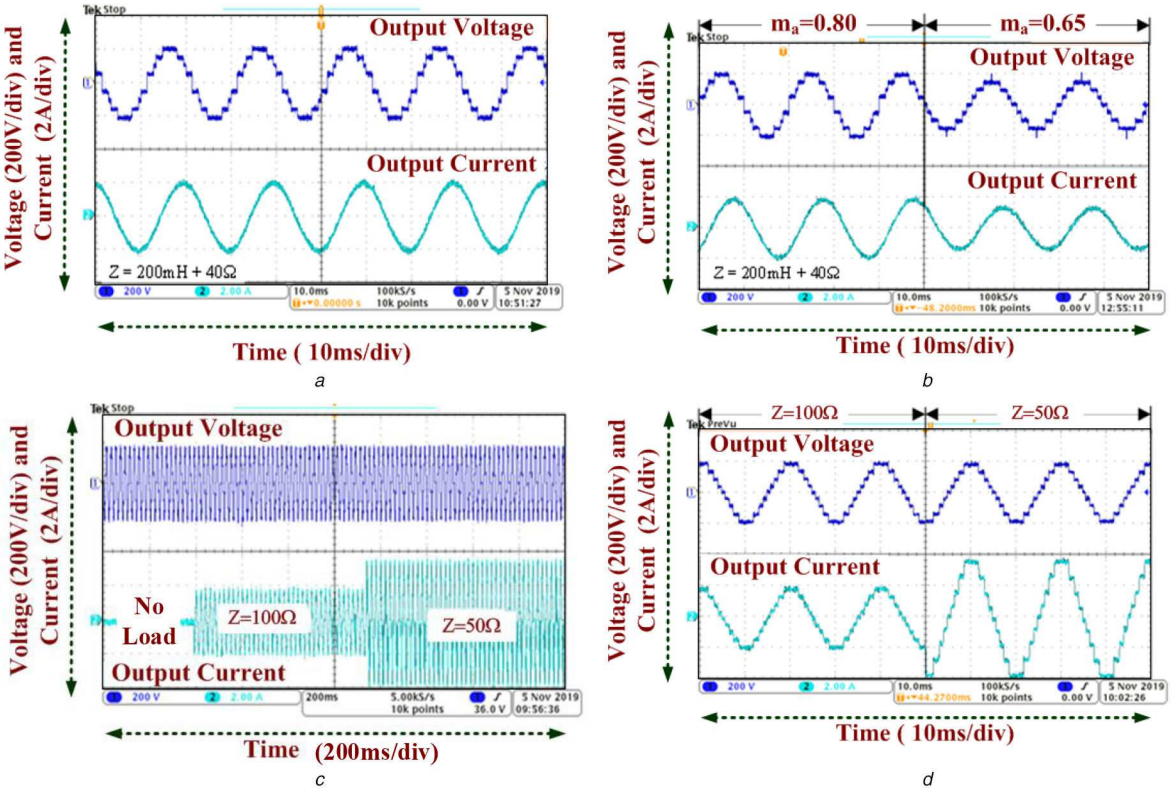

Fig. 13 *Experimental results of output voltage and current the proposed topology with*
(a) $Z = 200$ mH + 40 Ω at $m_a = 0.80$ (set I), ***(b)*** Change of m_a from 0.80 to 0.65 (set I), ***(c)*** Dynamic change of load with $m_a = 0.80$ (set II), ***(d)*** Change of load from no load to 100 to 50 Ω with $m_a = 0.80$ (set II)

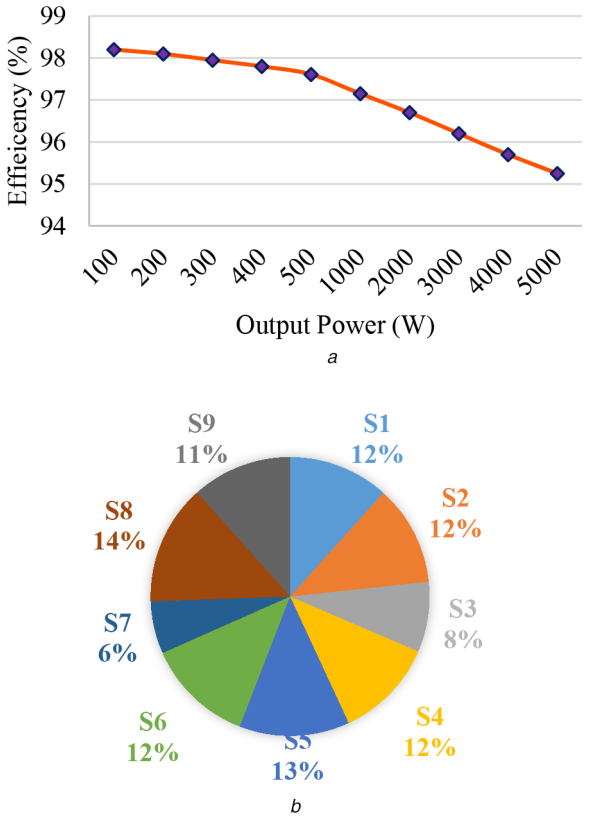

Fig. 14 *Power loss analysis with*
(a) Efficiency plot, ***(b)*** Loss distribution

sources, reduced power device and component count, low TSV, and able to produce both positive and negative voltages without using H-bridge. The proposed MLI also does not use any electrolytic capacitors or power diodes, hence it enhances its acceptability and reliability. The cascade connection of several modules is possible

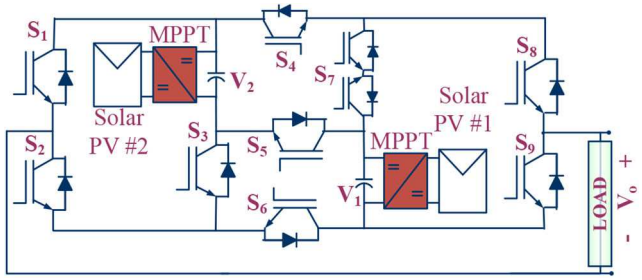

Fig. 15 *Solar PV application of the proposed topology*

to achieve more number of levels without increasing the voltage stresses of the power devices. Hence it is suitable for low, medium, and high power applications. SHEPWM and fundamental switching frequency PWM techniques have been used for the control of the proposed topology. Detailed information about these PWM techniques has been included in the paper. Finally, simulation and experimental results validated the performance of the proposed topology.

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