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Study The Effect of Classical And Raipd Thermal Annealing on The Electrical Characteristics of P-Ge/P-si Heterojunction

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دراسة التأثيرات العادية والسريعة للتلدين الحراري على الخصائص الكهربائية للمفرق الجيني المتماثل

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في هذا البحث تمت دراسة تأثير كل من التلدين الحراري التقليدي والتلدين الحراري السريع على الخصائص الكهربائية (تيار - جهد، سعة - جهد) للمفرق الهجيني المتماثل من نوع Ge/Si.

إن خصائص تيار جهد للمفرق الهجيني قد تحسنت بعد التلدين وأن التيار الأمامي يخضع لأنموذج ثنائي شوتكي، إن أفضل قيمة لعامل المثالية كان بحدود ١,٢ للعينات الملدنة بواسطة التلدين الحراري التقليدي (600 c/20 min) وكان ١,٣ للعينات الملدنة بالتلدين الحراري السريع (500 c/25 s).

إن خصائص سعة - جهد أوضحت أن المفرق الهجيني من النوع الحاد، وقد تمت دراسة تأثير كل من نوع وظروف التلدين على مقدار جهد البناء الداخلي Vbi.

Key Words: *Thermal Annealing – Electrical Characteristics.*

ABSTRACT

This paper describes the effect of classical thermal (CTA) and rapid thermal annealing (RTA) on the electrical characteristics (I-V, C-V) of isotype Ge/Si heterojunction.

The I-V characteristics were improved after annealing and they follow double-Schottky model, the optimum value of ideality factor was 1.2 for heterojunctions annealed by CTA (600 C/20 min), and was 1.3 for samples undergo to RTA (500 C/25 S). The C-V results suggest that the junctions are abrupt type. The effect of annealing type and annealing conditions on the built-in-voltage (V_{bi}) was investivated.

1. Introduction

It is well known that Si-Ge is a very promising system for producing junctions that can be used for photodetector and for modulation of doped field effect transistor which is significantly faster than silicon (1,2]. In order to fabricate high quanlity heterojunction (with minimum defects), firstly, the materials (semiconductor-semiconductor) should be lattice and thermal matched and secondly, the junction must be fabricated without internal diffusion [3]. There are several problems face the fabrication of Ge/Si heterojunction, the most important are the high lattice mismatch (4.1%) and high thermal mismatch of 50% [4,5], and consequently a large number of strained layers would be exist in the junction which affect the junction characteristics.

The target of the present work is the extensive study of different type of thermal annealing (CTA and RTA) to reduce the structural defects formed prior the fabrication process of Ge/Si heterojunction.

2. Experiment

Mirror-like single crystal p-type silicon wafers of (111) orientation having electrical resistivity of (3-5) Ω-cm were used. Prior to deposition of Ge films, the substrates were thoroughly cleaned to remove organic and inorganic contaminants from their surface using HF (1:10) chemical etchant. The substrates then washed in ultrapure running dionized waster and immediately transferred to vacuum chamber. High purity of Ge thin films of 200 mm thick were deposited on silicon using thermal resistive thechnique under vacuum pressure down 10^{-7} Torr. Classical thermal thermal annealing of Ge/Si heterojunction is carried out using vacuum tube furnace under different conditions 200-700°C/10-40 min).

Rapid thermal annealing of samples achieved with aid of high intensity incoherent halogen lamp for time (5-20 s) at temperatures (300-700°C) (one-sided illumination). The samples are positioned inside evacuated quartz tube. The temperature on the wafer was monitored by means of k-type thermocouple attached to the back of the wafer. The heating and cooling rates were estimated to be about (50-70)°C/s. The ohmic contacts were made on both Ge and Si sides using In and Au respectively. LCZ meter type (hp/4192 ALF) was used for C-V measurements at frequency of 100 kHz. The type of conductivity of deposited Ge before and after annealing was investigated using four points probe (FPP 5000), the results exhibited that the Ge layer was p-type.

3. Results and Discussion

Figs. (1 & 2) show the plots of forward I-V characteristics for Ge/Si heterojunctions before and after thermal annealing under different conditions. It is obvious that the I-V characterisstics are strongly dependent on annealing conditions (time and temperature). The I-V curves of annealed samples with optimum conditions (600°C/20 min for CTA and 500°C/20 S for RTA) are typically of near ideal isotype heterojunction, the ideality factor before annealing was about 1.95 and after annealing becomes 1.2 for samples annealed with CTA and 1.3 for those annealed by RTA. The I-V characteristic of annealed Ge/Si hetero-

junction followed the double-Schottky model [6]. Ideality factor was extracted from the slope of the semi-log (I-V) plot with aid of the following equation:

$$\beta = \frac{q}{kT} \frac{dV_{fj}}{dln\ (I_f\ /I_0)} \tag{1}$$

where

$\frac{q}{kT}$: reciprocal of volt equivalent of temperatu

V_f : forward

I_f : foward current, and

I_o : saturation current.

The obtained values of ideality factor for annealed Ge/Si are in fair agreement with those obtained by Pearsall et al [1]. The improvement in I-V characteristics after annealing could be attributed to the reduction in misfit dislocation which affect the junction characteristics [7]. Table (1) summarizes the values of ideality factor for different annealing conditions. Increasing the annealing time t_A and temperature T_A for CTA leads to poor I-V characteristics and hence higher values of ideality factor B, this effect may be probably due to gettering of diffusion of Ge atoms [8]. The Ge/Si annealed by RTA for tA < 25 S have higher value of ideality factor, this is because the short annealing time will be not sufficient to annealed the bulk structural defects (junction defects) [9]. Figs. (3 & 4) depict the C-V measurements of Ge/Si heterojunction before and after annealing (CTA & RTA), it is clear that the junction capacitance (C_i) is function to the reverse bias voltage (V_r) according to the following common equation

$$C_j = k\ V_r^{-n} \tag{2}$$

Where k is constant, on the other hand, the junction capacitance was strongly dependend onannealing conditions. In Fig. (5) the $1/C^2$ plotted against reverse bias voltage for Ge/Si HJ's annealed with optimum conditions.

The obtained results from Fig.(5) suggest that the junction was abrupt type, the extrapolation of the $1/C^2$ Vs. versus plot to the point $1/C^2 = 0$ gives the value of built-in-voltage (Vbi) and these results exhibit good agreement with those of Tamagawa et al [7]. The values of Vbi before and after annealing are listed in Table (2). The value of Vbi after annealing was higher than that before annealing by factor of 2 and 1.8 for CTA and RTA respectively. These results could be ascribed to the minimization of misfit dislocation and fully relaxation of the strain after thermal annealing [10].

4. Conclusions

We have demonstrated the feasibility of fabrication of high quality (near-ideal) isotype p-Ge/p-Si heterojunction with aid of twotypes of thermal annealing processes (CTA and RTA). Obtained values of ideality factor for annealed Ge/Si heterojunction were ranged from (1.2-1.3), which are not in contradiction with the existing experimental data. Investigation of Ge diffusion into Si after annealing with different condition using EDS technique under progress.

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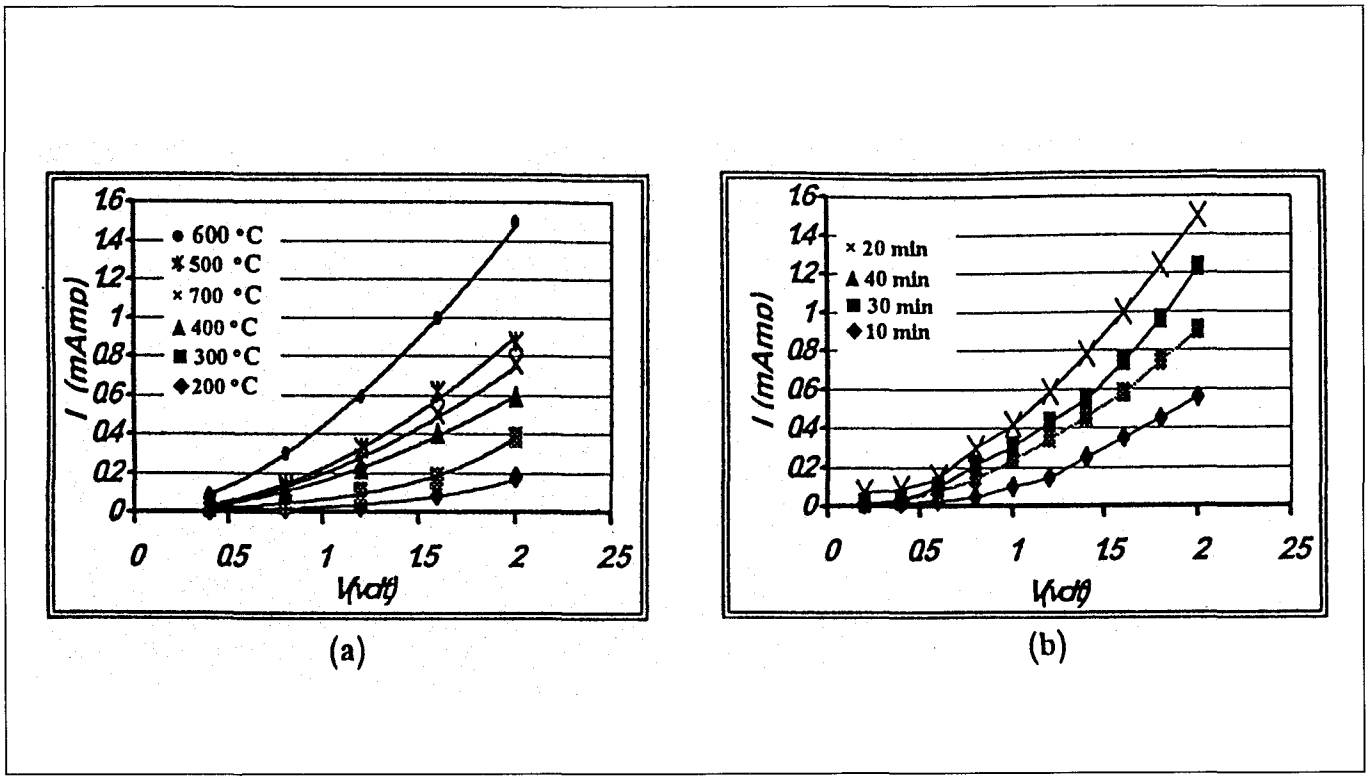


Fig. 1: I-V Characteristics of Ge/Si heterojunction before and after CTA annealing with different conditions.

(a) Different annealing temperatures.

(b) Different annealing times.

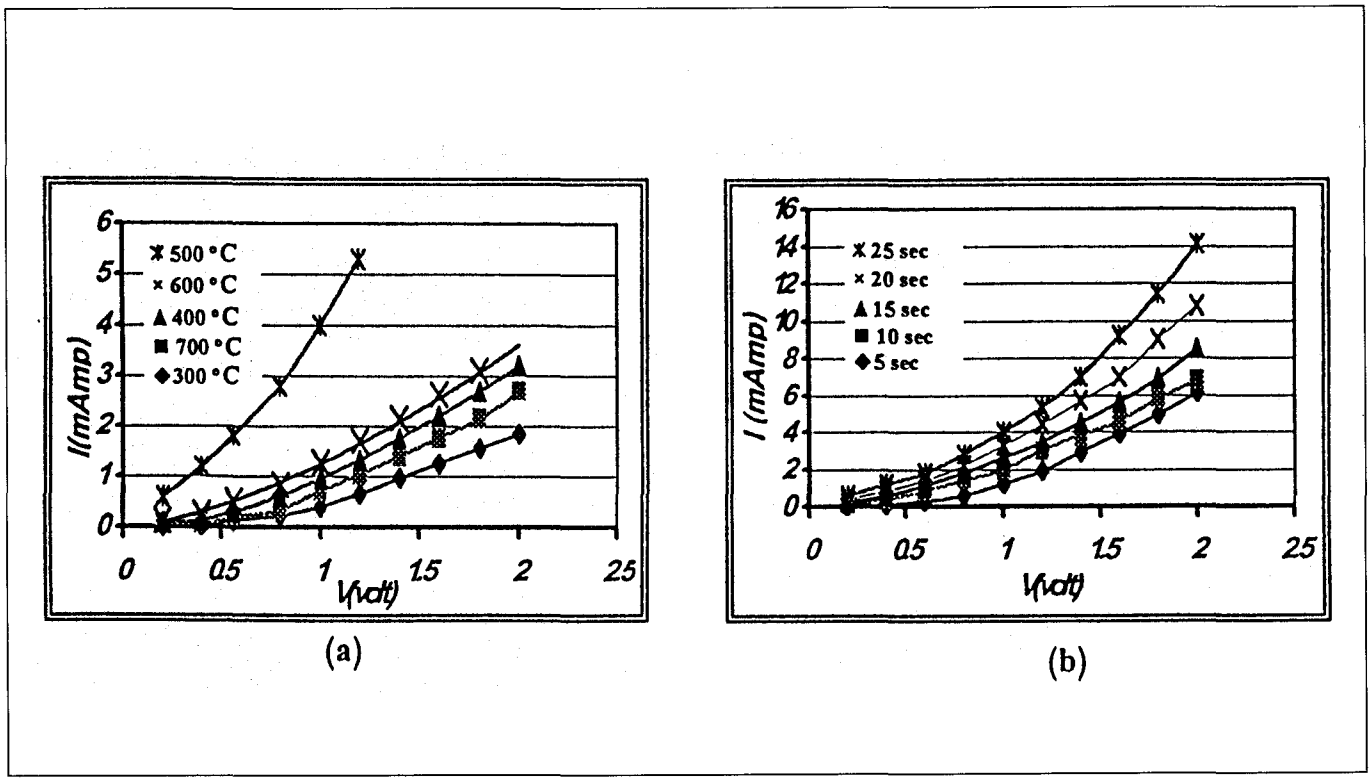


Fig. 2: I-V Plots of rapid thermal annealed Ge/Si sample for different annealing temperature and time

(a) Different annealing temperatures.

(b) Different annealing times.

Table (1)

Ideality factor as function of annealing conditions

p-type, 2000 °A, ann. (CTA)			
T°C	β	t (min)	β
200	1.92	10	1.93
300	1.64	20	1.20
400	1.31	30	1.90
500	1.25	40	2.10
600	1.20	-	-

p-type, 2000 °A, ann. (RTA)			
T°C	β	t (sec)	β
300	1.64	5	1.64
400	1.60	10	1.60
500	1.30	15	1.59
600	1.34	20	1.50
700	1.40	25	1.30

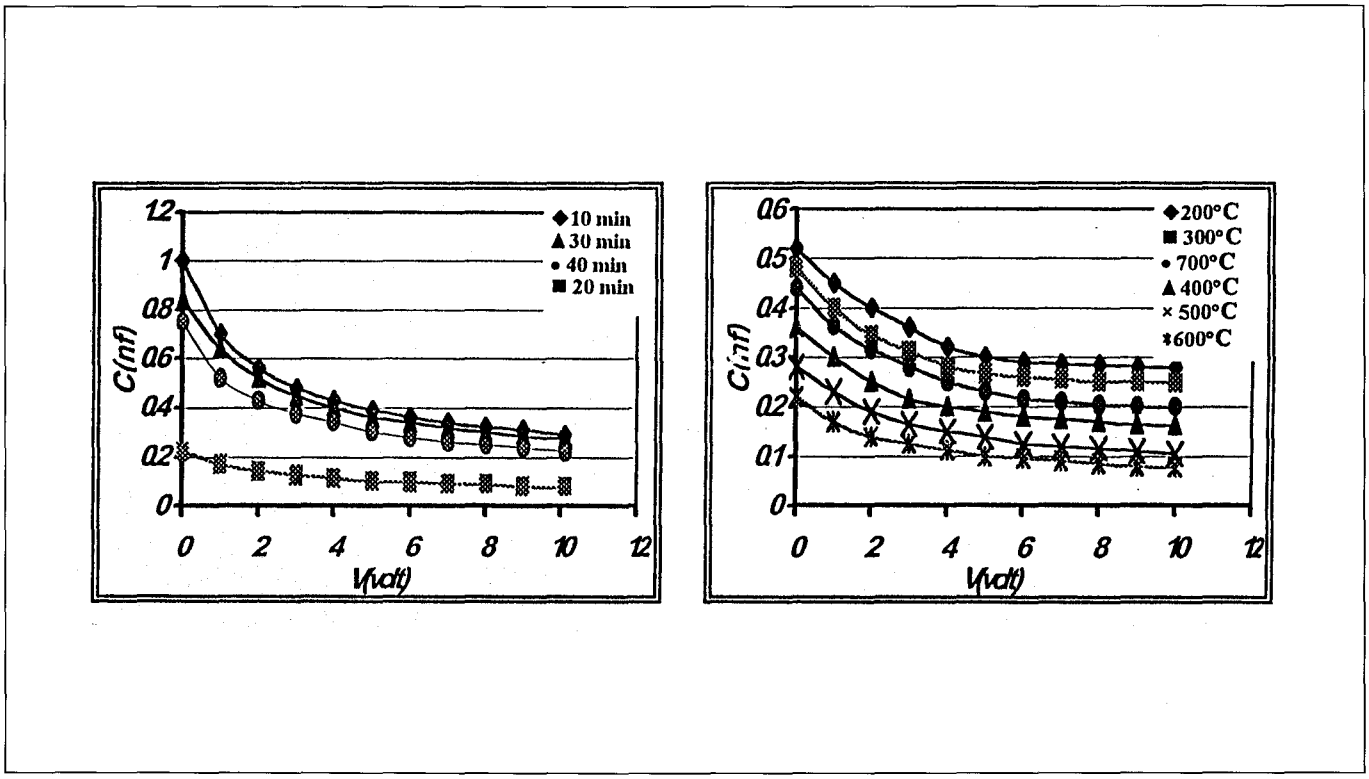


Fig. 3: C-V measurements of Ge/Si heterojunction after annealing with *CTA.*

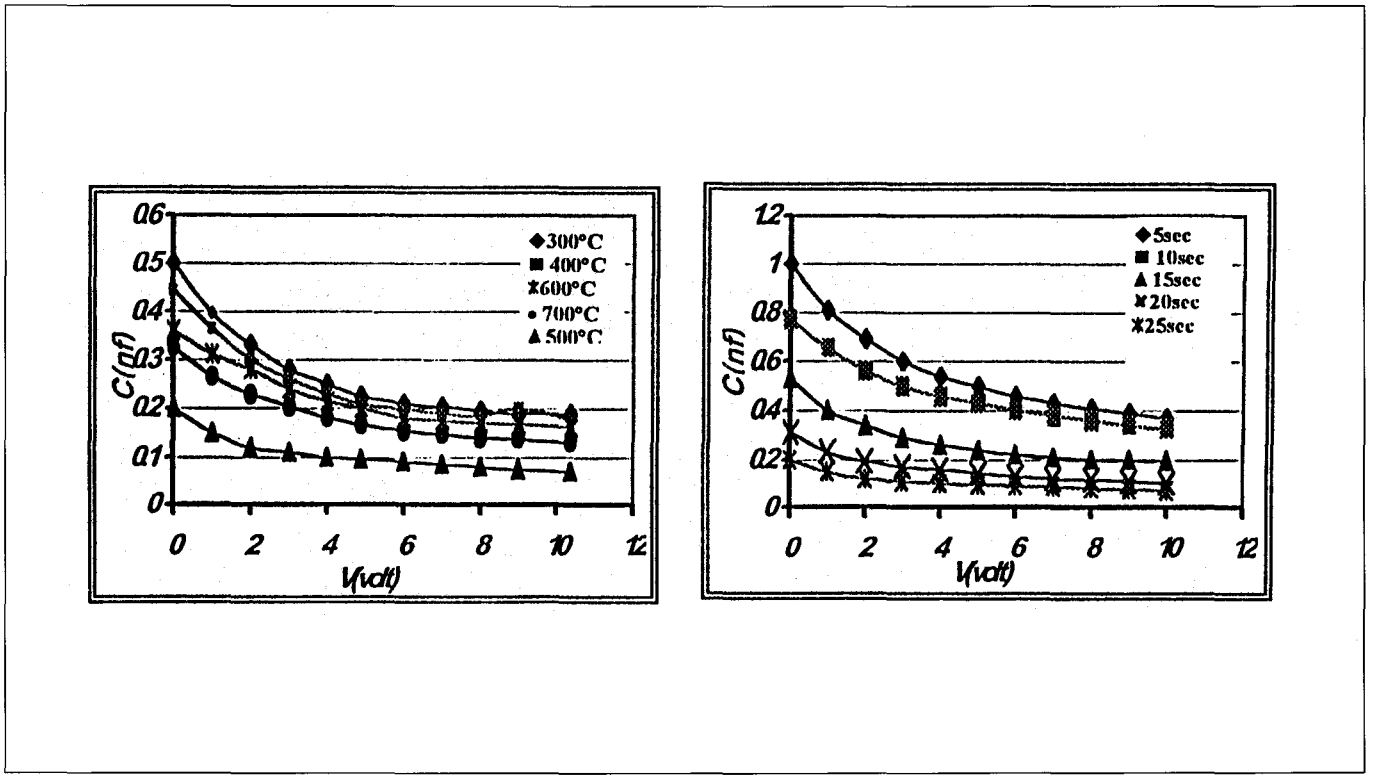
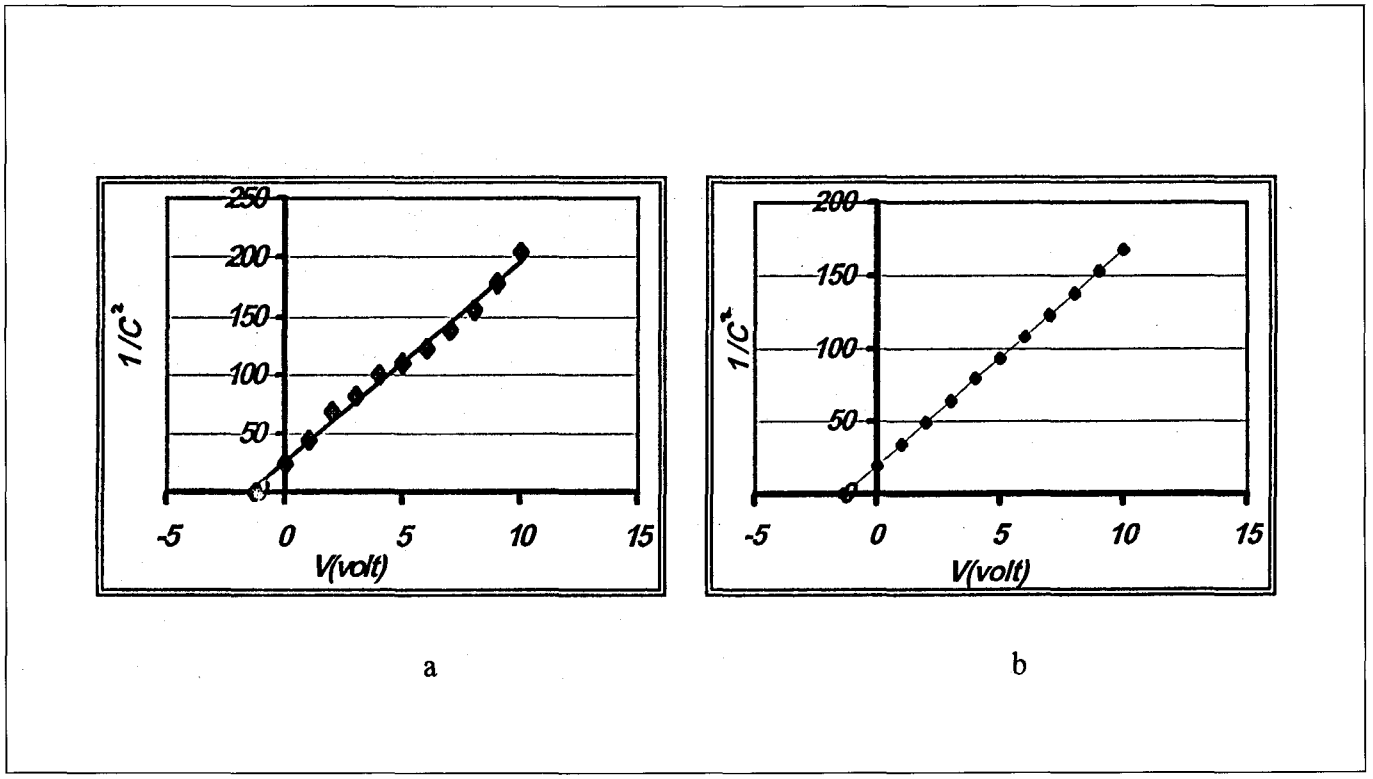


Fig. 4: C-V Plots as function to rapid annealing conditions.



a b

Fig. 5: $1/C^2$ Vs. Vr for Ge/Si samples after annealing

(a) CTA (600 C/20 min).

(b) RTA (500 C/25 s).

Table (2)

Built — in — voltage for hetrojunctions annealed with different conditions.

p-type, 2000 °A, ann. (CTA)			
T°C	V_{bi}	t (min)	V_{bi}
37	0.70	0	0.70
200	0.90	10	0.85
300	1.00	20	1.40
400	1.15	30	1.10
500	1.25	40	0.95
600	1.40	-	-

p-type, 2000 °A, ann. (CTA)			
t (sec)	V_{bi}	T°C	V_{bi}
0	0.70	37	0.7
5	0.80	300	0.9
10	0.90	400	1.1
15	1.00	500	1.3
20	1.15	600	1.1
25	1.30	700	0.95