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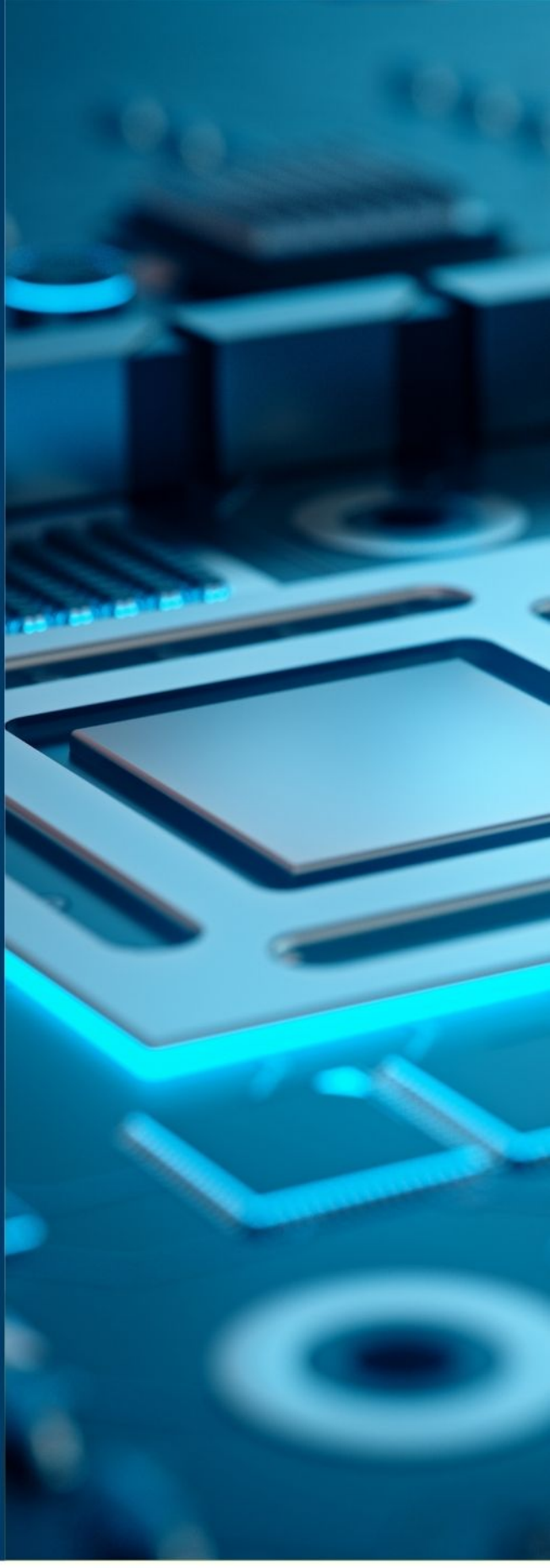

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RAPID COMMUNICATION

11 Level boost inverter topology with dual-source configuration

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Abstract

With the advancement of the application of power converters in the power industry, the research towards the prominent power converter namely multilevel inverter has gained a lot of attraction. Here, a dual-source configured 11 level inverter topology is being discussed, which uses nine power semiconductor devices and one capacitor. The proposed topology is able to charge the capacitor up to $2V_{dc}$ which provides the boosting feature with the voltage gain of 1.67. An extended comparison with several other topologies has been provided which highlights the major contribution of the work. A low-power laboratory prototype has been used for the validation of the proposed 11 level topology. Further, a thorough assessment of comparable topologies has been conferred in detail.

1 | INTRODUCTION

Multilevel inverters (MLIs) play a significant role in the development of EVs, HVDC, Fact devices renewable power plants, and microgrids. There are several prominent features of the MLIs inverter over two-level inverter, for example, low dv/dt characteristics, higher efficiency, superior EMC, modularity, and high fault tolerance abilities. However, the requirement of large number of dc sources, switches, diodes, capacitors, other components significantly rise the size and cost of the MLIs with higher voltage stress. A new approach toward the above-mentioned problem has been discussed in this article which is based on the combinations of the component that have been introduced in different topologies of the MLIs [1, 2].

Several single source boost inverter topologies have been proposed, however, the required number of components has been on the higher side. A developed switched-capacitor incorporated MLI with a string of dc sources is proposed in [3]. The main concern of the topology is to lower the stress at the backend H-bridge. The topology presented in [4] is based on switched capacitor producing seven-levels with self-voltage balancing at boosting factor of 3 without a backend H-bridge. In [5], an improved 7-level PUC inverter is investigated which uses a new voltage balancing method. The blocking voltage on the switches is low and the topology comes with boosting feature. The topology presented in [6] is a 19 level, three times voltage gain, hybrid switched-capacitor MLI which finds application in high-frequency ac distribution systems. This converter achieves self-voltage balancing by employing the series-parallel conversion method. MLI Topology suitable for high-frequency ac power distribution systems is developed in [7]. Under this, an asymmetric dc voltage source with a common ground is

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utilized to make it valuable for renewable energy farms and EVs. A 9-level PEC topology with reduced components count is presented in [8]. This topology enables multi-terminal operations and is suitable for both symmetrical and asymmetrical concoctions. In [9], a K-type modular multilevel inverter, in which capacitors are used as dc-link to produce 13-level staircase output waveform, is presented. A single-stage modified H-bridge SC-based seven-level multilevel inverter with triple voltage gain is presented in [10]. In [11], an improved sensor-less cascaded T-type 9-level multilevel converter with a reduced switched count is presented. Another 9-level SC-based topology with reduced count is presented in [12]. The topology uses phase disposition PWM to improve the quality of the output waveform. Another high-frequency ac power distribution system application-based topology is investigated in [13]. The results demonstrate low THD without the utilization of a high-frequency modulation scheme.

A cascaded 7-level switched-capacitor with a single input source is investigated in [14]. Where the phase-shifted sinusoidal pulse width modulation scheme is considered to control the capacitor voltage. Further, for high-frequency application, a cascaded MLI based on the switched capacitor is developed in [15]. In which, the H-bridge at the backend and switched capacitor at the frontend are used to generate the output. A similar approach has been adopted in the topologies of [16–22], however, the device count has been the limiting factor for these topologies. In this work, a dual-source dc to ac converter topology has been presented. The two sources are configured in asymmetrical magnitudes with the integration of a switched capacitor unit to provide the boosting feature. The lower device count with lower voltage stress is the other advantage of the proposed topology.

2 | TOPOLOGICAL DESCRIPTION AND ANALYSIS

2.1 | Proposed topology

The proposed 11-level Inverter with voltage gain is demonstrated in Figure 1. The major component of the proposed MLI are:

- Eight unidirectional switches
- Two dc sources in asymmetrical magnitude
- One diode
- One capacitor

The output voltage waveform is an 11-level across the load with the voltage level of $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$. The proposed topology has four pairs of complementary switches (S_1, S_2), (S_3, S_4), (S_6, S_7), (S_5, S_8). To prevent short-circuit conditions, the switches must not be turned ON simultaneously.

2.2 | Description of voltage states

The voltage levels produced by the proposed topology have been shown in Figure 2a–f for the positive half cycle and is discussed below:

2.2.1 | Zero voltage state ($V_o = 0$)

With zero output voltage level in this state, only three switches are conducting for producing this state as shown in Figure 2a. For this state, there is no cycle of charging and discharging happens for the capacitor C_1.

2.2.2 | First voltage state ($V_o = V_{dc}$)

The capacitor C starts charging from $2V_{dc}$ source in this state as shown in Figure 2b. The current flows through S_2, S_4, S_6, S_8. The output voltage level for this state is V_{dc}.

2.2.3 | Second voltage state ($V_o = 2V_{dc}$)

In this state, the capacitor C still charges from $2V_{dc}$ and the output voltage is obtained from the same source $2V_{dc}$ as shown in Figure 2c. The current flows from the path from S_1, load, S_3, S_8, $2V_{dc}$, diode D. The output voltage level generated in this state is $2V_{dc}$.

2.2.4 | Third voltage state ($V_o = 3V_{dc}$)

The state can be obtained by following the current path S_1, S_4, V_{dc}, S_8, $2V_{dc}$, Diode D and is shown in Figure 2d. The output voltage level achieved in this state is $3V_{DC}$. The capacitor is still charging from the source $2V_{dc}$ by following path $2V_{dc}$, D, capacitor C, S_6.

2.2.5 | Fourth voltage state ($V_o = 4V_{dc}$)

From this state as shown in Figure 2e, the capacitor C starts discharging. The current follows the path S_1, load, S_8, $2V_{dc}$, S_7, C. The output voltage level obtained from this state is $4V_{dc}$.

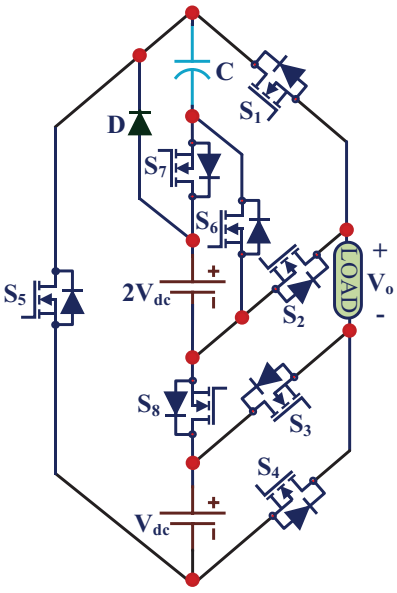

FIGURE 1 Proposed 11 level topology

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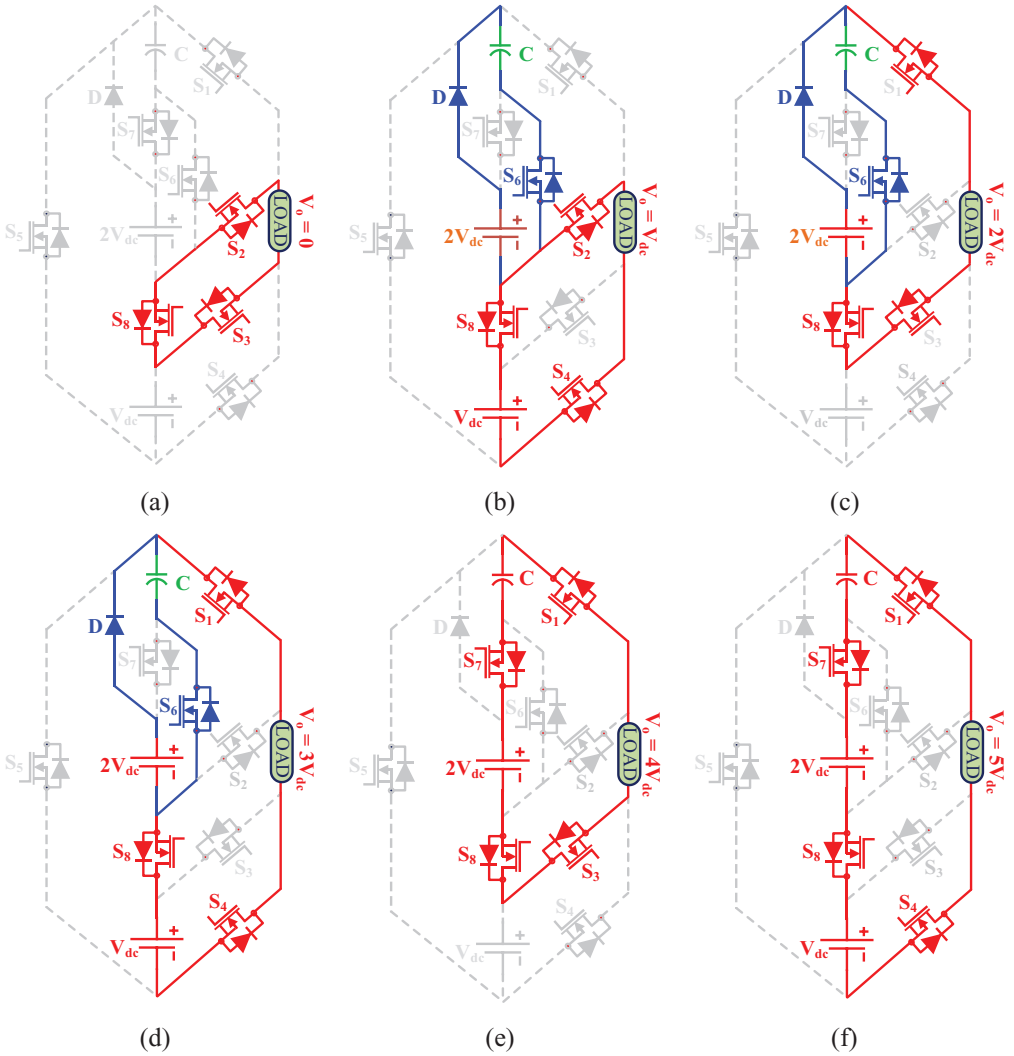

FIGURE 2 Positive voltage states of the proposed 11 level topology with (a) $V_o = 0$, (b) $V_o = V_{dc}$, (c) $V_o = 2V_{dc}$, (d) $V_o = 3V_{dc}$, (e) $V_o = 4V_{dc}$, (f) $V_o = 5V_{dc}$

2.2.6 | Fifth voltage state ($V_o = 5V_{dc}$)

This is the last state for the positive output staircase waveform and is as shown in Figure 2f. In this state, the output voltage level of $5V_{dc}$ can be obtained by following the path S_1, load, S_4, V_{dc}, S_8, $2V_{dc}$, S_7, C.

Similarly, the negative voltage levels can be obtained conferring to Table 1 which demonstrates the switching combinations for the proposed topology with both for the positive and negative voltage levels along with the voltage behaviour of the capacitor C.

2.3 | Capacitance value calculation

The role of the capacitance value of capacitor C is very crucial in order to satisfice the higher standards of performance. Figure 3 shows the arrangement of carrier signals with the reference along with the output voltage. The capacitor is charged

TABLE 1 Switching sequence of the proposed 11 level circuit

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o	V_C
0	1	1	0	0	0	0	1	Zero	–
0	1	0	1	0	1	0	1	V_{dc}	C_{ch}
1	0	1	0	0	1	0	1	$2V_{dc}$	C_{ch}
1	0	0	1	0	1	0	1	$3V_{dc}$	C_{ch}
1	0	1	0	0	0	1	1	$4V_{dc}$	D_{ch}
1	0	0	1	0	0	1	1	$5V_{dc}$	D_{ch}
1	0	0	1	1	0	0	0	Zero	–
1	0	1	0	1	1	0	0	V_{dc}	C_{ch}
0	1	0	1	1	1	0	0	$2V_{dc}$	C_{ch}
0	1	1	0	1	1	0	0	$3V_{dc}$	C_{ch}
0	1	0	1	1	0	1	0	$4V_{dc}$	D_{ch}
0	1	1	0	1	0	1	0	$5V_{dc}$	D_{ch}

Notation: 0 = Not conducting, 1 = Conducting, Capacitor voltage state with - = no change, C_{ch} = Charging, D_{ch} = Discharging.

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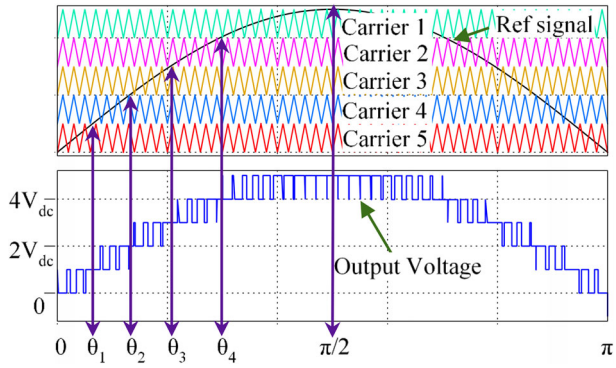

FIGURE 3 11 level waveform with the arrangement of carriers and references

during the $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ voltage levels and discharged at the voltage levels of $\pm 4V_{dc}$ and $\pm 5V_{dc}$. As the capacitors are discharged during the voltage states during $\pm 4V_{dc}$ and $\pm 5V_{dc}$, the maximum discharge time constitutes from $\pi - 2\theta_3$. As the charging and discharging of the capacitor is symmetrical, it shows the self-balancing behaviour of the voltage of the capacitor with some ripple content in its voltage which is dependent on various factors as given in (1).

$$C_{value} = \frac{5V_{dc}}{2\pi \times f_o \times R \times \Delta V_C} \times (\pi - 2\theta_3) \quad (1)$$

where C_{value}, f_o, R, and ΔV_C denotes the capacitance value, output voltage frequency, load resistance, ripple voltage, and maximum discharge time, respectively.

2.4 | Analysis of power loss

The analysis related to the power loss of the proposed 11-level MLI has been carried out using PLECS software. Two main losses in the switched capacitor based MLI are the losses linked with power devices and capacitors losses. The power semiconductor losses are mainly dependent on the voltage across the device, the current flowing through it, the operating frequency whereas the power loss of capacitor depends on its equivalent series resistance (ESR), current flow through it, the ripple content in its voltage. With PLECS, the thermal model of the proposed dual-source topology using the data from the manufacturer datasheet of switch IKW75N60T has been used. The magnitude of the voltage sources has been selected as 50 and 100 V which results in a peak output voltage of 250 V. The load parameters have changed to get the efficiency at different output power. The estimated efficiency has been depicted in Figure 4a. Further, the loss distribution among the components of the proposed topology has been provided in Figure 4b. As expected, the devices in the charging loop of capacitor C have a maximum percentage due to losses associated with the charging current.

3 | COMPARATIVE STUDY

To demonstrate the feature discussed in the previous section, a comparative analysis is performed in this section against some

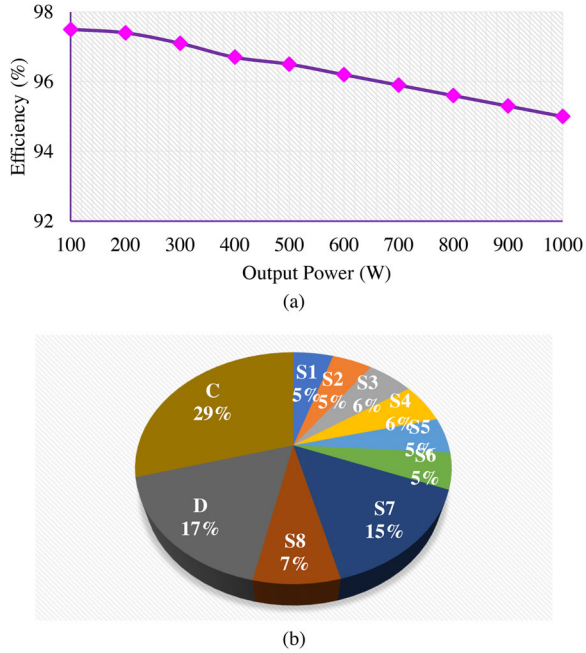

FIGURE 4 (a) Efficiency curve and (b) loss distribution

of the recent topologies [4, 5, 10, 16–22]. The comparison is done on the basis of the available number of switches, number of diodes, number of capacitors, voltage gain, TSV, and PIV. Table 2 gives the detail of the topologies in terms of comparative parameters. From Table 2, it is clear that the topologies [4, 5, 10] require less dc sources, but, to generate lower number of levels higher number of switches are needed. In case of [17, 18, 20], there is no need of a capacitor to produce the staircase output but they require higher number of dc sources as compared to the proposed topology. The topology presented in [16, 19] produces the same level of output but requires more and diode in comparison to the proposed topology. In case of MLIs elaborated in [21, 22], using less dc sources and requires no diode, however, to produce output voltage of 11-level the required switches as well as capacitance are much more than the proposed MLI.

In the topologies [4, 10, 19], the gain is higher with the same number of dc sources as compared to the proposed topology at the cost of higher number of capacitors and the number of switches. The topology presented in [5] has same gain, capacitances and dc sources but produces lower level with higher switch count. The rest of the topologies have lower voltage gain with higher number of components in comparison to the proposed topologies.

In comparison Table 2, a cost comparison is shown to analyze the cost of the topologies. The Cost Factor is calculated as:

$$CF = \left(N_s + N_D + N_{Cap} + N_{DC} + TSV_{PU} \times \sigma\right) / N_L \quad (2)$$

From Table 2, the cost factor is the lowest for the proposed topology. This also shows the merit of the proposed topology.

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TABLE 2 Comparison of SC based MLI topology

Top	N	N_S	N_D	N_{Cap}	N_{DC}	G	TSV_{PU}	N_S/N	$N_{CD(h)}$	Cost factor $\sigma = 0.5$	Cost factor $\sigma = 1.0$
[4]	7	12	0	2	1	3	5.3	1.71	10	2.52	2.9
[5]	7	9	0	1	1	1.5	1	1.28	4	1.64	1.71
[10]	7	16	0	2	1	3	1	2.28	4	2.78	2.85
[16]	11	20	18	10	1	1	NS	1.82	6	NS	NS
[17]	11	9	5	0	5	1	4	0.81	6	1.90	2.09
[18]	11	8	3	0	3	1	NS	0.72	2	NS	NS
[19]	11	14	0	4	1	5	2.29	1.27	6	1.83	1.93
[20]	11	12	0	0	6	1	2	1.09	5	1.72	1.81
[21]	11	12	0	5	1	1	3	1.09	5	1.77	1.90
[22]	11	11	0	2	1	1	3	1.00	5	1.40	1.54
[P]	**11**	**8**	**1**	**1**	**2**	**1.5**	**1.4**	**0.72**	**4**	**1.15**	**1.21**

N–Number of levels, N_S–Number of switches, N_D–Number of diodes, N_{cap}–Number of capacitors, N_{DC}–Number of dc source, G–voltage gain, TSV_{PU}–Per unit total standing voltage, NS – Not specified, $N_{CD(h)}$–Number of components conducted at the highest level.

TABLE 3 Parameters of the topology

Parameters	Values
Input DC voltage	50 V, 100 V
Output peak voltage	250 V
Fundamental frequency	50 Hz
Switching frequency	5 kHz
L load	50 mH
Capacitor	2200 μF
R-load	50 Ω, 75 Ω, 100 Ω

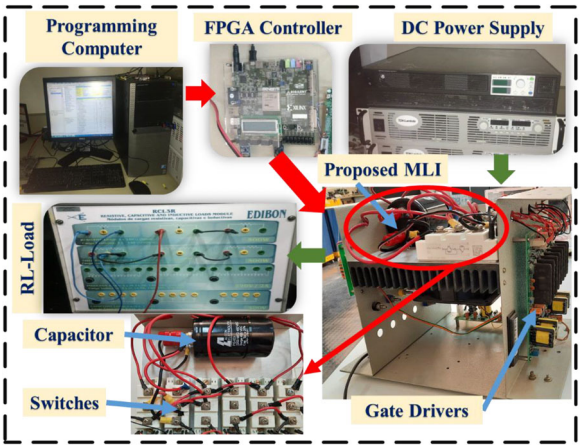

FIGURE 5 Hardware prototype of the proposed topology

4 | RESULTS AND DISCUSSION

The validation of the proposed converter is evaluated based on experiments conducted on the experimental setup. The MLI requires control signals to fire the gates of the switches. To achieve this, many modulation schemes have been used. One of them is SPWM, that is, sinusoidal pulse width modulation. There are two types of sinusoidal PWM multiple carrier arrangements that provide the necessary gate pulse to the switches in the MLI: sinusoidal pulse width modulation with Level-shifted carriers (SPWM-LS) and sinusoidal pulse width modulation with phase-shifted carriers (SPWM-PS). In this study, an SPWM- LS is employed for the proposed 11 level inverter and the carriers are arranged as displayed in Figure 3. The five triangular carrier signals with 5 kHz frequency are disposed and the gating pulses are produced. Table 3 gives the value of different used components. The experimental prototype setup is depicted in Figure 5.

The waveform presented in Figure 6 demonstrates the analysis of the proposed 11 level topology. Figure 6a presents the output voltage and output current for the 11 level topology. The variation in the nature of the load is shown in Figure 6b, where the load changes from R-load to RL-load, that is, from a unity power factor to a lagging power factor of 0.95. From Figure 6b, it can be observed that there is no variation in the voltage when the load changes from R-load to RL-load, however, the current smoothens. Figures 6c and d show the loading condition for different R-load and RL-load. In Figure 6c, the load power factor is unity in all the changes in load whereas in Figure 6d, the power factor changes from 0.99 to 0.95 and again to 0.95. As the overall load impedance increases, the current decreases, vice versa can also be observed.

Figure 7 shows the deviation of voltage level as the modulation index (MI) varies. The level decreases as the modulation index decrease, that is, five-level at MI = 0.40, seven-levels at MI = 0.60, nine-levels at MI = 0.80, 11 levels at MI = 1.0. From all these waveforms, the self-balancing of the capacitor voltage is confirmed. In addition, the proposed topology provides excellent performance in different loading conditions.

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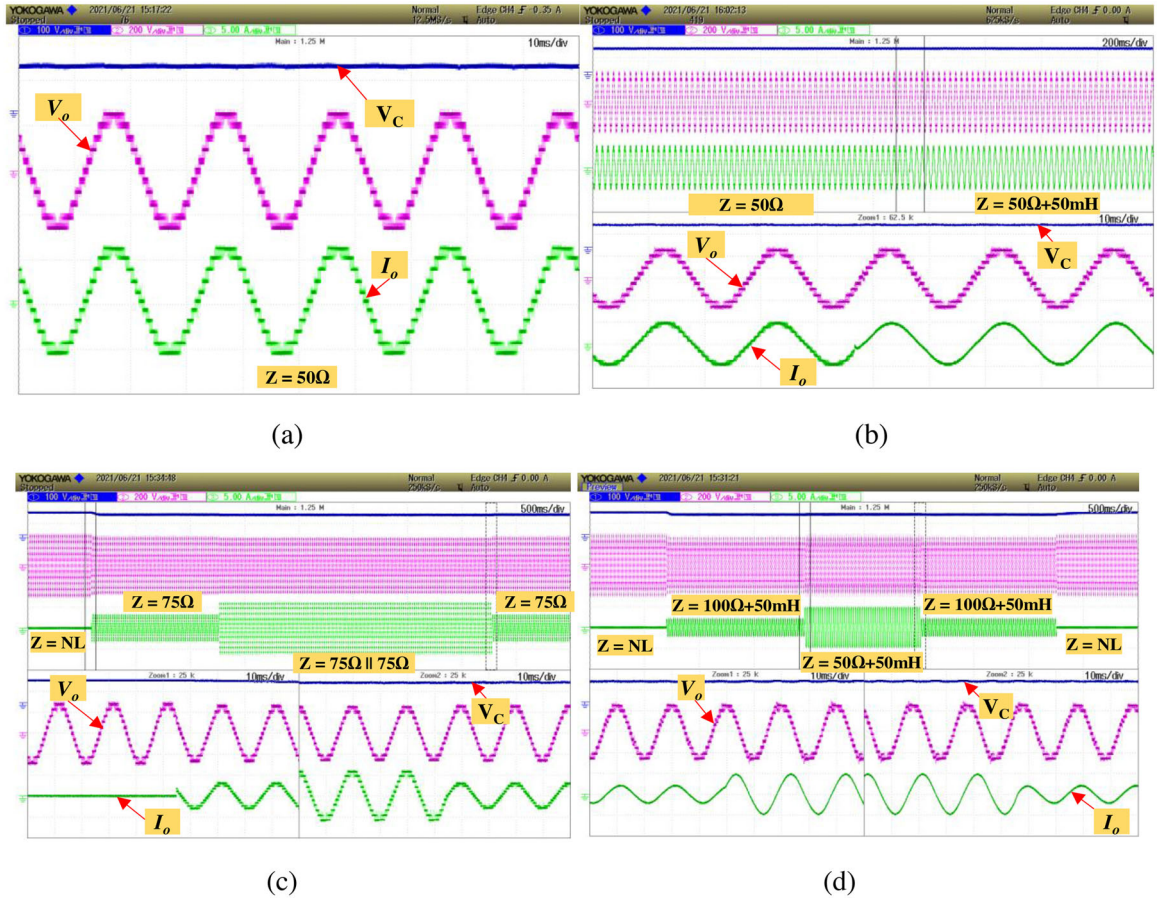

FIGURE 6 Waveform for output voltage (V_o), capacitor voltage (V_C) and output current (I_o). (a,b) Variation of load from R-load to RL-load, (c) variation of R-load, (d) variation of RL-load

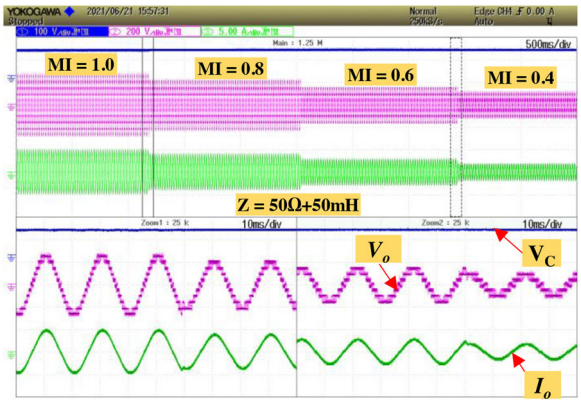

FIGURE 7 Experimental results with the change in MI

5 | CONCLUSION

This study presents an 11L MLI with the reduction in the switch count, with higher boosting capability having a dual-source configuration. It combines eight switches, one capacitor, one diode. A detailed comparative analysis is performed to prove the superiority of the proposed MLI in association with the recent converters. The major contribution of the proposed topology is a lower device count as compared to recent topologies. In addition, the proposed topology has the prominent feature of higher efficiency and sensorless balancing of the capacitor voltage. The validation of the proposed 11 levels MLI is performed under diverse operating environments with the help of a developed experimental prototype.

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CONFLICT OF INTEREST

There is no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable – no new data generated, or the article describes entirely theoretical research.

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