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REDUCED SNUBBER CIRCUIT ELEMENTS FOR PWM VOLTAGE SOURCE INVERTER

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ABSTRACT

This paper presents the description and simulation of a new proposed arrangement of RLD/RCD snubber circuit used with pulse width modulated voltage source inverter. The new arrangement allows minimizing the number of active elements of RCD with 50%. This will help the designer to reduce the size of the system. SPICE programming package is used as principal simulation tool. A detailed simulation given that includes the sever effects of snubber diode reverse recovery current, as well as, the effect of the stray inductance of D.C rails. Some results of a typical practical example are compared with their corresponding SPICE traces, in order to check the validity of the simulation results.

KEY WORDS: Snubber circuit, PWM inverter, SPICE simulation, Transistor switching.

1. INTRODUCTION

When a power semiconductor device is either on or off, its power dissipation is relatively small. On other hand, a high power is dissipated in it during the switching transition from one state to the other. This dissipated power increases with increasing switching frequency. The switching loss becomes the dominant consideration in achieving efficient operation, long life, and compact physical design [1]. Apart from heating the device, the instantaneous peak power dissipation during switching may cause internal crystal damage, and lead to secondary breakdown in the device such as power bipolar transistor [2,3]. It is well established in practice to use snubber circuits to relive the power semiconductor device during switching transients. However, the function of these circuits varies quite widely depending upon the type of power semiconductor device. These may be used to control di/dt, dv/dt, and to keep power semiconductor device within the safe operating area (S.O.A), as well as to control the effect of parasitic elements in the system under normal and abnormal conditions. The main function of using

snubber circuits with thyristor circuits is to control the rate of voltage rise dv/dt at the end of conduction cycle, otherwise this may lead thyristor to undesired turn-on condition. While the main function of these circuits with self turn-off devices such as bipolar transistor, power Darlingtons, MOSFET transistor, and GTO thyristor is to relive these devices, by reducing switching transition losses, control the stress of di/dt and dv/dt, keeping stable thermal condition, and fully utilizing the rating of the devices[4].

The design of these circuits differs in complexity from one power electronic circuit to another one. Previous works in references [5-9] had described how snubber circuits can be used to reduce the switching losses in choppers and switching regulators with different power semiconductor devices. In papers [4,10-13] these circuits are studied for pulse-width modulated inverters. Detailed analytical study of the turn-on and turn-off snubbers under idealized circuit conditions is given in references [4,13]. The goal of this paper is to analyze and simulate a new proposed arrangement, designed by the authors, of snubber circuit with transistorized PWM-VSI circuits, using PSPICE circuits simulations. Simulation results are Verified by comparing these with some experimental results, which were obtained from one leg of PWM- VSI circuit. Where PWM signals are generated using microcomputer. Another important effects of reverse recovery of snubber diodes, which causes sever transient oscillation in transistor current, are also investigated in the simulation and compared with the practical results.

2. REDUCED RLD/RCD SNUBBER CIRCUIT TOPOLOGY

The conventional snubber circuit for bipolar transistor of the single leg of PWM-VSI is shown in Fig.1(a). The top shunt snubber, consists of C_T, R_{CT} and D_{CT}, is used to control the turn-off conditions of top transistor (Q_T). The bottom shunt snubber consists of C_B, R_{CB} and D_{CB} and used for controlling bottom transistor (Q_B) turn-off conditions. While the separate pair of series snubber circuit L_T, RLT and $D_{LT;}$ and L_B, R_{LB} and D_{LB} are used to control the turn-on conditions of Q_T and Q_B respectively. The behavior and analysis of this type of the snubber is given in detail by [4]. In order to reduce the active element numbers of the shunt snubber a new arrangement of RLD/RCD snubber is designed and analyzed. The Reduced snubber circuit arrangement for a one compact leg of transistorized, Darlington, PWM-VSI is shown in Fig.1(b). The top shunt snubber, consists of capacitance, C_T, diode, D_{CT}, and common discharge resistance, R_{CTB} , with the bottom shunt snubber, which also consists of capacitance, C_B, and diode, D_{CB}. The top and bottom snubbers are used to control the turn-off conditions of the top transistor (Q_T), and the bottom transistor,(Q_B) respectively. Whereas each of the separate pair of series snubber circuit L_T, D_{LT} and $R_{LT;}$ and L_B, $D_{LB,}$ and R_{LB} are

used for controlling the turn-on conditions of Q_T and Q_B respectively. A stray inductances (L_{ST}&L_{SB}) of D.C rails also included in the analysis. The current in Q_B, due to the nature of inductive load, may not conduct when the top transistor is switched on and off, this is important in PWM. The load current, therefore, is transferred many times between Q_T and D_B. The load current is assumed constant during turn-on and turn-off because of snubber events for a few microseconds. More information about the practical circuit is included in Appendix 1.

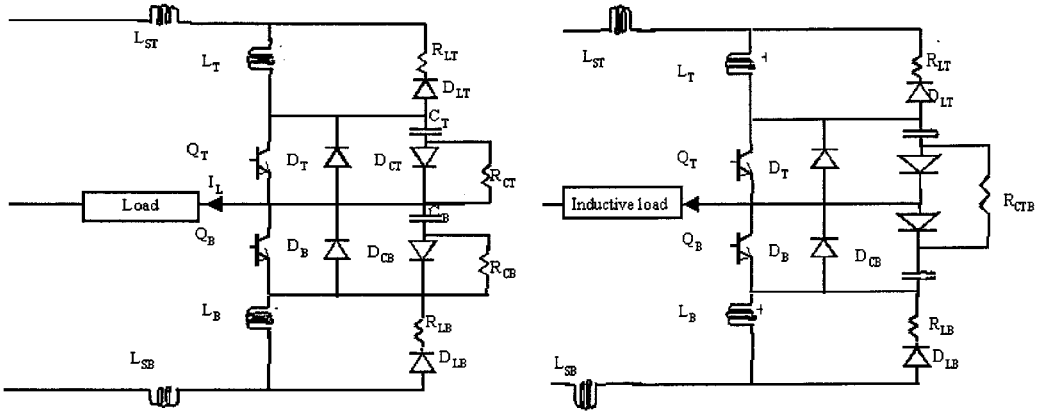


Fig.1 RLD/RCD snubber for one leg of PWM inverter
(a) **Conventional RLD/RCD snubber**
(b) **Reduced RLD/RCD snubber**

Turn-On Events

The equivalent circuits with current directions for turn-on stages of the top transistor for positive load current sense is shown in Fig.2. PSPICE simulation results, are shown in Fig.3 . Events of turn-on are explained bellow:

The first stage

Just before turning-on of Q_T, the positive load current is passing through L_B and D_B. The equivalent circuit of this stage becomes as shown in Fig.2(a).

The second stage

When Q_T is turned-on, its current is started to rise while the current in D_B is falling, the rate of rise and fall is same and equal to $(V_S/(L_T+L_B))$ and the load current starts to transfer from D_B to Q_T. The voltage across Q_T (V_{QT}), collapses and the source voltages V_{ST} and V_{SB} will appear across L_T and L_B respectively. During this stage C_T begins to discharge through QT and D_{CB} via R_{CTB}, see Fig.2(b) . The

peak value of discharging current is equal to (V_{ST}/R_{CTB}), and it is decaying with time constant ($R_{CTB}.C_T$). This stage ends when currents of D_B and L_B equal to zero.

The third stage

The freewheeling diode (D_B), reverses recovery during the third stage consequently, the current direction in it and in L_B is reversed, but the rate of current change is same as the previous stage (V_{SB}/L_B). Therefore the presence of snubber inductor is also essential in order to control the diode reverse recovery.Fig.2(c) shows the equivalent circuit of this stage.

The fourth stage

Before the reverse recovery of the D_B is completed, the voltage across C_B clamped by D_B to approximately zero value. When the reverse recovery is completed (the end of third stage), then D_B unclamps the voltage across C_B (V_{CB}). Therefore V_{CB} will be rise and charging current flows into C_B (I_{CB}), via Q_T, L_T, L_B and D_{CB}, see Fig.2(d), which may cause the over current condition in the transistor . The amplitude of this current, $\mathbf{i_{Cpeak}}$, is limited by L_T and L_B , as given approximately by:

$$i_{C\ peak} = V_S \cdot \sqrt{\frac{C}{L_T + L_B + L_S}} \qquad (1)$$

where $L_S = L_{S\,T} + L_{SB}$.

However, the worst-case turn-on current in the transistor can be represented by:

$$i_{Q\ peak} = \frac{V_S}{R_{CTB}} + i_{C\ peak} + I_{L\,\max} \qquad (2)$$

Where I_{Lmax} is the maximum load current , and I_{Qpeak} must be within S.O.A of the transistor, therefore attention should be given in selection of L_T,L_B and $R_{CTB.}$ On the other hand the voltages V_{LT} and V_{LB} would fall as V_{CB} rises, while rate of current change in L_T, L_B and Q_T reduces. The end of this stage when $V_{CB} = V_{ST} + V_{SB}$.

The fifth stage

At the beginning of this stage, the rate of current change in L_T and L_B will becomes negative. Therefore equal negative voltages will appear across L_T and L_B while V_{CB} rises over the total source voltage. These negative voltages across L_T and L_B are applied in the forward direction across D_{LT} and D_{LB} respectively .The current I_{CB} reduces and becomes zero, at the end of this stage, when the rate of change of V_{CB} becomes zero. The difference between I_{LB} and I_{CB} carried by R_{LB}, on the other hand

the current flowing in Q_T reduces from its maximum overshoot level towards the load current level. The equivalent circuit of this stage is illustrated in Fig.2 (e).

The sixth stage

During this stage the additional stored energy in L_T and L_B, owing to the capacitor charging current I_{CB}, discharging through R_{LT} and R_{LB} respectively . The snubber diode D_{CB} reverses recover via C_B and Q_T causes transient oscillation in the transistor current, and this snubber diode, therefore, must be fast recovery type to avoid transient oscillation. Fig.2 (f) shows the equivalent circuit of this stage.

The seventh stage

After the complete discharging of both C_B and L_B the load current is carried by the top transistor Q_T via L_T, as shown in Fig.2 (e). Now the voltage across the C_T is approximately zero. This is the last stage that represents the steady on- state. Experimental traces of some system voltages and currents are shown in Fig.4(a).

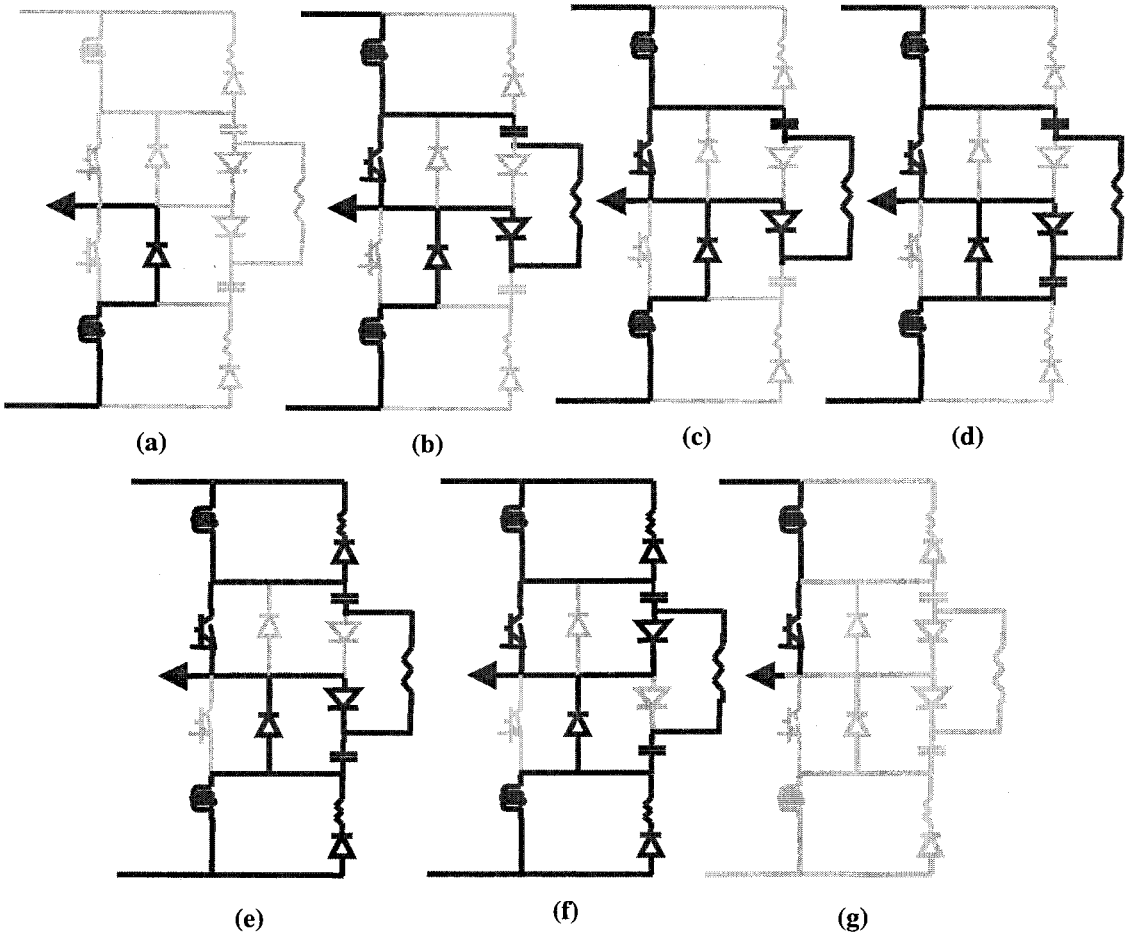


Fig.2 The equivalent circuits of turn-on events of the top transistor

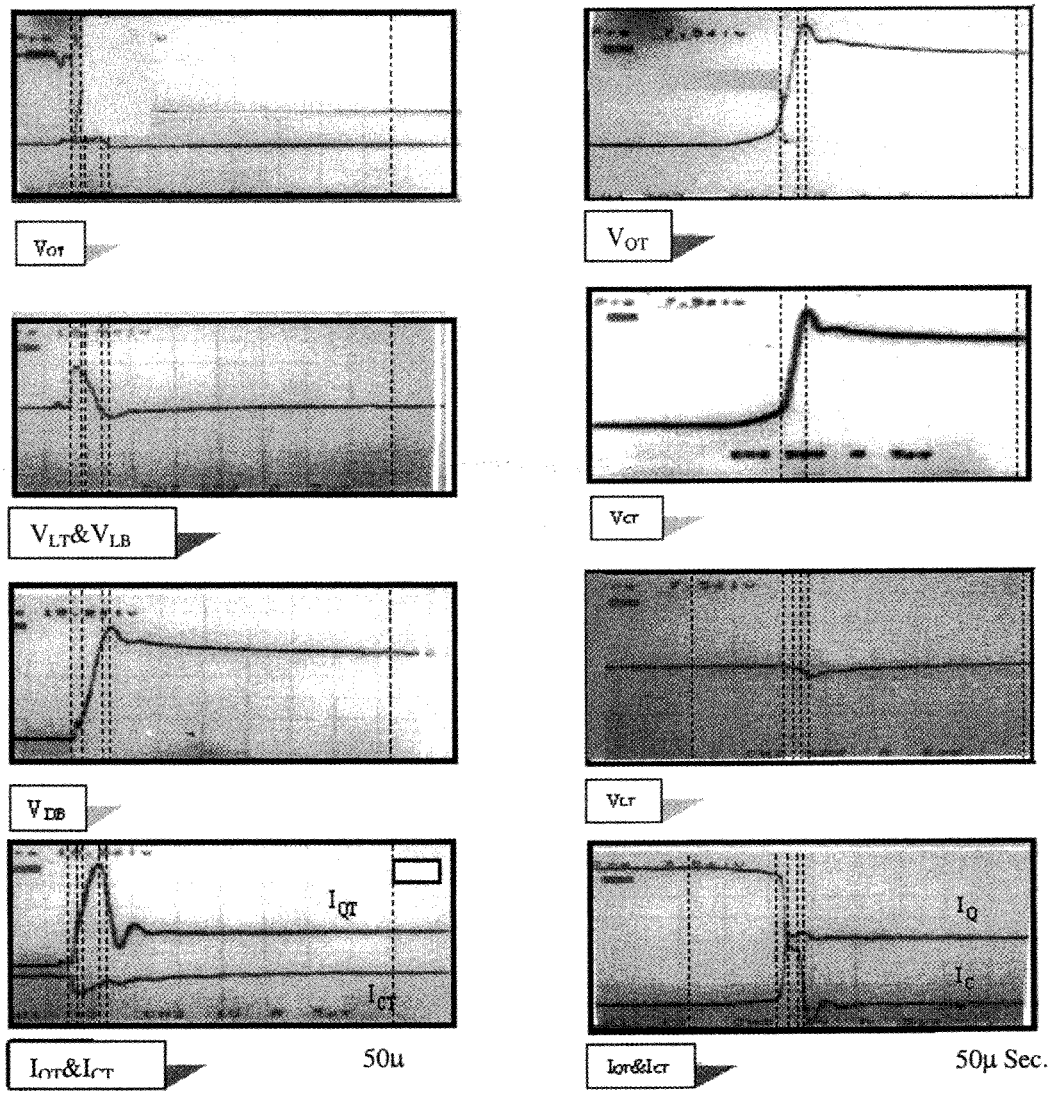


Fig.4 Experimental results for snubber stages (One) Turn-on stages, (b) Turn-off stages

Turn Off Events

Equivalent circuits of the system during turn-off the top transistor are shown in Fig.5.The voltage and current waveforms from the simulating results are shown in Fig.6. Some corresponding practical results are shown in Fig.4(b), and the major stages of operation are:

The first stage
Just before the turn-off of the top transistor (Q_T) , the positive load current passes within Q_T via L_T, as shown with the full black line in Fig.5(a). Whereas the voltage across the C_B is approximately equal to (V_{ST}+V_{SB}).

The second stage
The circuit condition remains as described above, when Q_T turns-off, until the storage time of Q_T is vanishes, which is the end of this stage. The equivalent circuit of this stage is shown in Fig.5(b).

The third stage
When the transistor storage time vanishes C_T starts to control the voltage rise across the transistor which is given as :

$$v_C = v_Q = \frac{1}{C}\int i_C .dt \qquad (3)$$

Where (i_{CT}) is the current through the capacitor, which rises as transistor current falls, so the load current remain constant. As V_{QT} increases the voltage V_{CB} falls. A small negative voltage across L_T and L_B appears due to a small change in I_{LT} and I_{LB}, causes a small current through R_{LT} and R_{LB}. When the current in Q_T ceases and capacitor current i_{CT} reaches to the load current level then the stage ends. Fig.5(c) shows the equivalent circuit of this stage.

The fourth stage
The interval of this stage is very short, in which the capacitor carries the full load current via $D_{CT,}$ see Fig.5(d), until the voltage across Q_T reaches the source voltage (V_{ST}+V_{SB}) then D_B comes into conduction and next stage begins.

The fifth stage
When the freewheeling diode D_B conducts, the load current begins to transfer to D_B through L_B and R_{LB} ,as illustrated in Fig.5(e) . The rate of current rise in D_B, and the rate of current fall in C_T is equal in magnitude and opposite in sense. The trapping energy in L_T during on state discharged through R_{LT} causes an over shoot voltage across the top transistor Q_T.

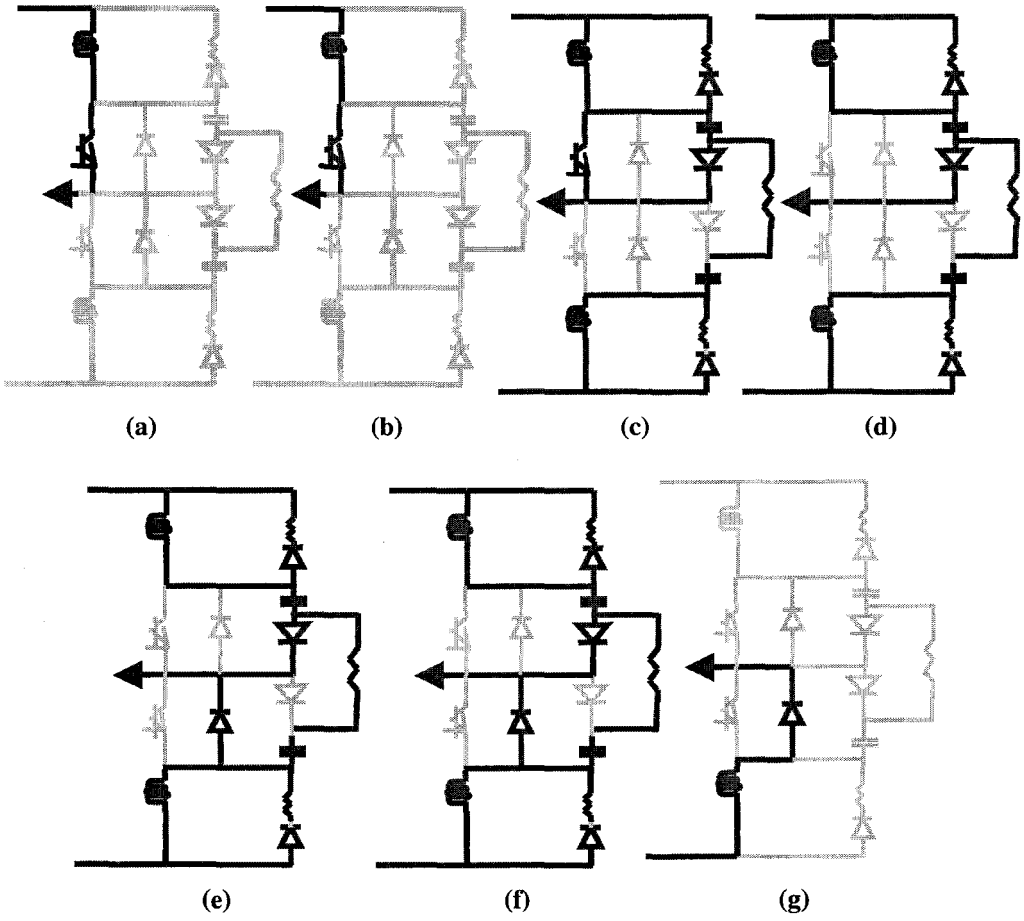


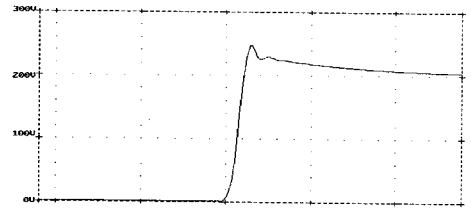
Fig.5 The equivalent circuits of turn-off events of the top transistor

The sixth stage

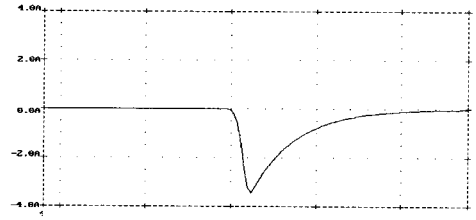
The current in D_{CT} diode reveres causes a transient oscillation in capacitor current. C_T begins to discharge through R_{CT} . L_T continues in discharging through R_{LT}. While the load current transfer from R_{LB} to L_B with time constant equal to (L_B/R_{LB}) .The equivalent circuit of the system for this stage is shown in Fig.5(f).

The seventh stage

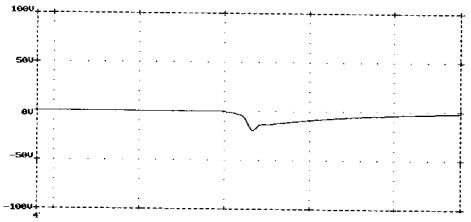
The present stage represents the steady off state, in which the positive load current completely passing through the bottom freewheeling diode D_B via L_B, as shown in fig.5(g). The top snubber inductance completely discharged through the R_{LT} . Now the voltage across the top transistor is completely fall back to the source voltage level $(V_{ST}+V_{SB})$ from its maximum overshoot level.



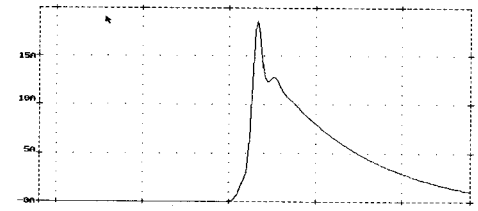
V_{CT}



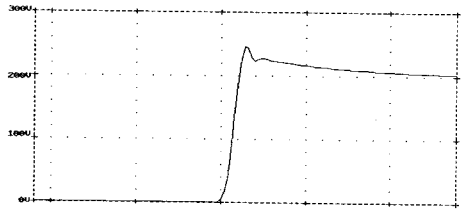
I_{RCTB}



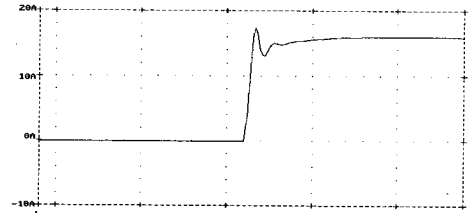
V_{LT}&V_{LB}



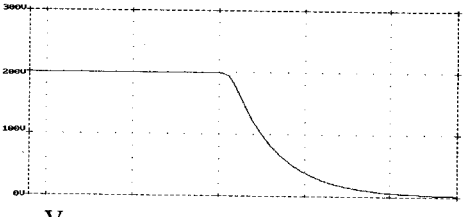
I_{RLT}&I_{RLB}



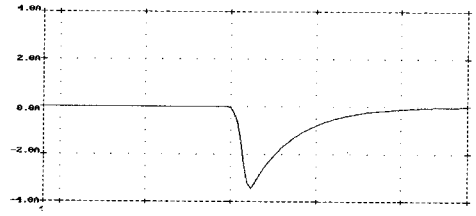
V_{CT}



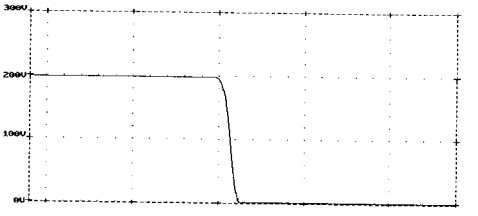
I_{DB}



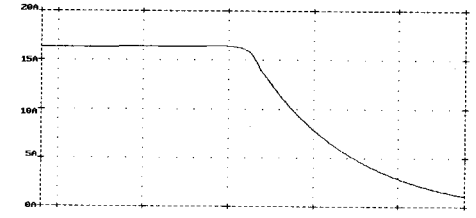
V_{CB}



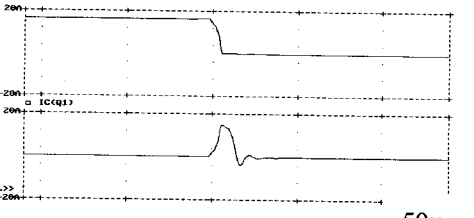
I_{CB}



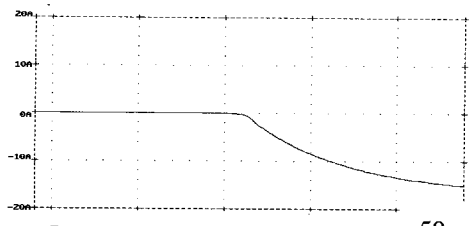
V_{DB}



I_{LT}



I_{OT}&I_{CT} 50µse



I_{LB} 50µse

Fig.6 SPICE simulation results for snubber turn-off stages

3. CONCLUSION

A new simple form of RLD/RCD snubber for single compact transistorized pulse –width modulated voltage source inverter leg has been presented. Stages of Turn on and off of the top transistor that occur during snubbing process for transient conditions are analyzed and simulated using PSPICE circuit simulation, to help the snubber designer to understand all snubber events. . Description of all snubbing events is, also, illustrated in terms of the equivalent circuit. The behavior of the new arrangement is approximately same as the behavior of the simple forms of RLD/RCD snubber that given by [4], with 50% reducing in the number of active elements of RCD snubber. The reduction in the number of the elements is helped the designer to minimize system size and cost. The reverse recovery of the shunt snubber diodes caused a transient oscillation in the transistor current, therefore these may be fast recovery type. Good agreements were obtained between the simulation results and the laboratory experimental results.

REFERENCES

1. **Gaur, S. P, and Lowe,G., 1977**.Power transistor crystal damage in inductive load switching. solid state Electron. , Vol. 20 pp. 1026-1027.
2. **Steyn, C. G., 1988**. Optimum size of dissipative non-linear turn-off snubber. IEE proc., pt. B, vol. 135,no.4, pp. 165-171.
3. **Calkin, E.T., and Hamilton, B. H., 1976**.Circuit Techniques for Improving the Switching loci of transistor Switches In switching Regulators. IEEE Trans. on industry applications, vol. IA-12, no. 4, pp. 364-369.
4. **Saied ,B. M., and Ameen, Y. M.Y., 1999.** Snubber circuit design for PWM voltage source inverter. AL-Rafidain Engineering, Vol.7, No.2,pp 1-17.
5. **Harada, K., 1979**.Optimum Design of RC snubbers for Switching Regulators. IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS, Vol. AES-15,No.2.
6. **Mcmurray, W., 1980.** Selection of snubbers and clamps to optimize the Design of Transistor switching Converters. IEEE Trans. Ind., Appli., Vol. 1A-16, No. 4, pp. 513-523.
7. **Ferraro, A., 1982**. An Overview of Low-Loss Snubber Technology for transistor Converters. In PESC Conf. Rec., PP.466-477.

8. **Willims, B.W., 1984.** High Voltage-frequency power-switching transistor module with switching-aid-circuit energy recovery. IEE Proc.,Vol. 131,pt.B,No.1,pp.7-12 .

9. **Fregien, G. and Jacobus, D., 1992.** Nonlinear Capacitors in snubber Circuits for GTO Thyristors. IEEE transaction ON Power Electronics Vol.7 No.2.,pp. 425-428.

10. **Evans, P.D., and Hill-Cottingham, R.J., 1979.** Some aspects of power transistor inverter design. IEE Elect. Power Appl. Vol.2, No.3, pp. 73-80.

11. **Brambilla, A., and Dallago, E., 1992.** Snubber Circuits and losses of Voltage-source GTO Inverters. IEEE transaction ON Power Electronics Vol.7 No.1.,pp. 231-238.

12. **Pong, M.H., and Jackson, R.D., 1987.**Computer–aided design of power transistor inverter snubber circuits. IEE Proc., Pt. B, Vol.134, No.2, pp 69-77.

13. **Evans, P. D., and Mestha, L. K., 1988**. Analysis of conventional snubber circuits for PWM inverter. IEE Proc. Vol.135,Pt. B,No.4, pp. 180-192

5-Appendix 1

The practical tests were carried out on one leg of bridge inverter type Fuji power transistor module 2D130 D-100 (30A, 1000v).
The practical values of snubber elements are given as follow: $C_T=C_B=0.11\mu$ F (400V).
$L_T=L_B=13\mu$H (air core inductor).Ω
$R_{CTB}=47\Omega$.
$R_{LT}=R_{LB}=1\Omega$.
DC supply voltage V_S =200v.
Load current at the begging of turn-on=7.5A.
Load current at the begging of turn-off=16.5A.μ
The switching frequency in the practical test was 500Hz.
The stray inductance in positive (L_{ST})and negative (L_{SB}) DC rail was equal to 0.75μH.