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A new family of boost active neutral point clamped inverter topology with reduced switch count

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Abstract

A new family of inverter topology for active neutral point clamped (ANPC) is proposed. The traditional ANPC gives the output voltage of half the input voltage which necessitates the use of higher input dc-link voltage. To fix this problem, a floating capacitor is used to increase the voltage of the output, which decreases the dc-link requirement. Moreover, no sensors are needed to stabilize the floating condenser for the proposed topology, which minimizes inverter complexities. The neutral point is connected directly to the load terminals, which decreases the leakage current and makes it suitable for solar PV integration. Two modes of operation of the proposed topology have been discussed while considering the voltage of the floating capacitor used in the topology. Furthermore, two extensions of the proposed topology with generalized structure have also been provided in the paper. A detailed comparison with similar topologies has been provided. The level-shifted pulse width modulation technique has been used for the control of the proposed active neutral point clamped topology. In order to illustrate the idea of the proposed active neutral point clamped inverter, the theory of operation and analysis is accompanied by simulation, and experimental waveforms obtained from a laboratory prototype are provided.

1 | INTRODUCTION

Multilevel inverters have some very important advantages over two-level VSI's, especially for higher-voltage power conversion, where the switch stress is lower with less harmonic content. Multilevel topologies are more prevalent for grid-connected applications such as photovoltaic and power generation inverters due to advantages in improved output performance, lower switching losses and decreased electromagnetic interference. For multilevel inverter topologies, low voltage switches can be used instead of the two-level inverter of high voltage switches. Low voltage switches are usually less costly and have low frequencies to accommodate. Furthermore, a low forward voltage drop will help minimize the conduction losses, as dv/dt is smaller in multilevel topologies. The switching loss also diminishes due to the smaller dv/dt. To achieve the same output quality in two-level topology, the switching frequency could be lowered in multi-topologies and the switching losses could be combined. Since the 1970s there have been studies in the literature regarding numerous multilevel converters of topologies [1–3]. Many multi-level converters with different features have since been proposed [4–6]. A better approximation of the sinusoidal waveform with many voltage levels can be obtained with a reduction of the passive filter and thus a lower THD. Yet, despite these benefits, the difficulty with regards to the structural and control systems is the key issue of multilevel inverters. In general, for solar PV and fuel cell applications, the power conversion will happen in two stages, that is, in the first stage higher magnitude of dc link voltage is obtained by high gain dc-dc converter or to raise the dc-link voltage with a string of PV linked series modules to allow the power transfer to the grid. In the second stage, the dc-ac power conversion will happen which can be obtained using the conventional MLIs or hybrid MLIs which enhances the power quality. The multistage power conversion nevertheless improves performance and reliability while increasing device size and expense. By connecting PV modules in series to create high dc connection stress, the further boost stage can be removed, while losses due to the difference between the modules and shading will relatively damage the voltage gain from the device. The A single-stage dc ac power converter with boost capabilities thus provides an interesting alternative to the two-stage approach. For addressing this, the switched boost MLI topologies have emerged as a competitive solution for replacing the conventional dc-dc converter and MLI topologies in PV and Fuel applications [7–12].

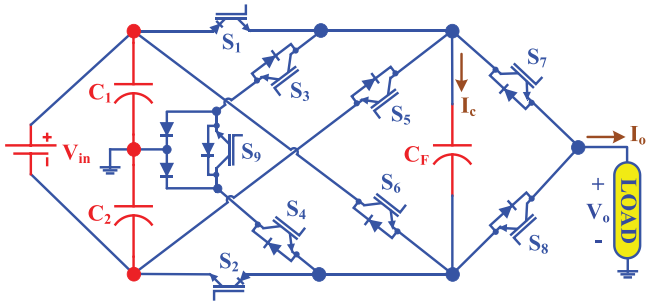

FIGURE 1 Proposed active neutral point clamped topology

The sensor less topology for the 5L-packed U cell inverter is being proposed in ref. [13]. In this topology, six switches and a capacitor are used for the processing of the 5L at load. The voltage of the floating capacitor is half the voltage and the input voltage of the converter is higher than the output voltage that restricts the high power applications for medium voltage. The 5L inverter for a transformer-free inverter with common ground topology is introduced in ref. [14]. Four switches, one diode, and three dc condensers are used for topology. V_{in} and $V_{in}/2$ are the voltage ratings of the floating capacitor. The voltage sensors are used to calculate the floating condenser voltage in order to control the five-level output voltage. In ref. [15], an E-type has been introduced for 5L inverters. Four capacitors and 10 switches for 5L output are used for the topology. To sustain the dc capacitor voltages, a more voltage equilibrium circuit is needed. The topology of the inverter 6S-5L and 7S-5L has been proposed in ref. [16] and ref. [17], respectively, which uses one floating capacitor. In both topologies, the output voltage is half of the input voltage

A new dc-ac power conversion system has recently been built with an advanced active neutral point clamped (ANPC) Topology, which removes the need for a front-end boost dc-dc converter [18]. The topology of this ANPC is based on the principle set out in ref. [19]. It increases the voltage gain by half with a unity voltage gain, thus reducing the dc-link voltage by half compared to conventional ANPC. Five voltage levels can be produced between $-V_{in}$ and V_{in}. Similarly, a new family of the boost ANPC topology has been proposed in refs. [20–27]. However, most of the topologies suffer from either lower voltage gain or with higher components counts with their voltage ratings. In this paper, a new family of ANPC topology has been proposed with reduced switch count. The proposed topology can be configured in different ways to control the voltage gain with the number of levels. Furthermore, the extension for the proposed topology with N-level output voltage has also been discussed.

2 | PROPOSED INVERTER TOPOLOGY

The circuit of the proposed ANPC topology has been depicted in Figure 1. It consists of two dc-link capacitors C_1 and C_2 which have been used to split the input voltage V_{in} into 0.5 V_{in}. The floating capacitor (C_F) has been used to provide the additional voltage level with an increase in the output voltage magnitude. The floating capacitor is charged up to the voltage magnitude equal to the input voltage by connecting them in parallel to the input voltage source. Apart from three capacitors, the proposed topology uses nine power semiconductor switches with two diodes. The switches S_1 and S_2 are configured as a reverse blocking switch in which only unidirectional current flow whereas the remaining switches, that is, from S_3 to S_9 supports the bidirectional current flow with its anti-parallel diode connected to the switch.

Based on the charging voltage of the floating capacitor, the proposed topology can be operated on two different modes which result in a different number of levels and voltage gain.

TABLE 1 Switching table of the proposed topology for 5L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o	C_F
0	0	0	0	0	1	1	0	0	V_{in}	▼
1	0	0	1	0	0	1	0	1	0.5 V_{in}	▲
0	0	1	0	0	0	1	0	1	Zero	—
0	0	0	1	0	0	0	1	1		
0	1	1	0	0	0	0	1	1	$-0.5\ V_{in}$	▲
0	0	0	0	1	0	0	1	0	$-V_{in}$	▼

TABLE 2 Current stress of the proposed topology for 5L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
0	0	0	0	0	I_o	I_o	0	0	V_{in}
$I_o + I_c$	0	0	I_c	0	0	I_o	0	I_c	0.5 V_{in}
0	0	I_o	0	0	0	I_o	0	I_o	Zero
0	0	0	I_o	0	0	0	I_o	I_o	
0	$I_o + I_c$	I_c	0	0	0	0	I_o	I_c	$-0.5\ V_{in}$
0	0	0	0	I_o	0	0	I_o	0	$-V_{in}$

2.1 | Mode I

In this mode of operation, the floating capacitor (C_F) is charged up to the half of the dc-link voltage, that is, 0.5 V_{in}. This voltage magnitude can be achieved by connecting the floating capacitor in parallel with either of the dc-link capacitors. Table 1 gives the different switching states of the proposed topology with Mode I. Here ▼ and ▲ gives the indication of discharging and charging of floating capacitor (C_F) respectively. In Mode I, 5 voltage levels are achieved with the unity voltage gain. The corresponding switching diagram for the proposed 5L topology is shown in Figure 2. The voltage and current stress of the switches are important factors which decide the overall cost of the topology. With this mode of operation. Tables 2 and 3 provide the information for the current and voltage stress of all switches with different voltage levels. Out of 9 switches, five switches need to have of the current rating of the addition of load current and capacitor charging current. Similarly, two switches need to block the voltage of 1.5 V_{in} and four switches need to block the input

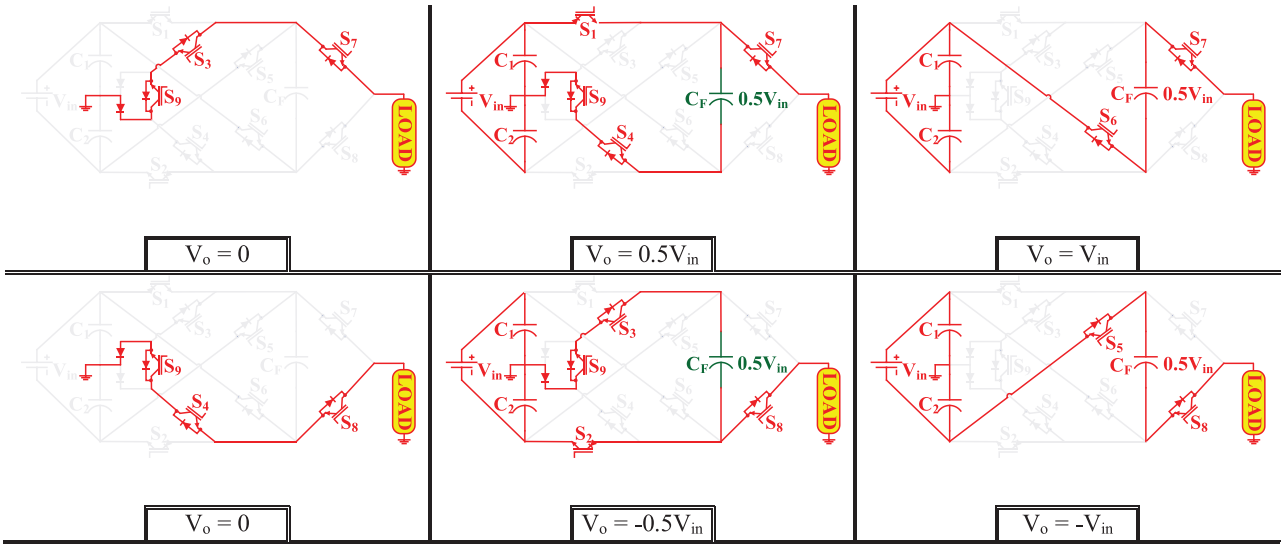

FIGURE 2 Different voltage levels of the proposed 5L topology

TABLE 3 Voltage stress of the proposed topology for 5L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
0.5 V_{in}	V_{in}	V_{in}	0	1.5 V_{in}	0	0	0.5 V_{in}	0.5 V_{in}	V_{in}
0	0.5 V_{in}	0.5 V_{in}	0	V_{in}	0.5 V_{in}	0	0.5 V_{in}	0	0.5 V_{in}
0.5 V_{in}	0	0	0.5 V_{in}	0.5 V_{in}	V_{in}	0	0.5 V_{in}	0	Zero
0	0.5 V_{in}	0.5 V_{in}	0	V_{in}	0.5 V_{in}	0.5 V_{in}	0	0	
0.5 V_{in}	0	0	0.5 V_{in}	0.5 V_{in}	V_{in}	0.5 V_{in}	0	0	−0.5 V_{in}
V_{in}	0.5 V_{in}	0	V_{in}	0	1.5 V_{in}	0.5 V_{in}	0	0.5 V_{in}	$-V_{in}$

voltage, the remaining switches block the voltage of half of the input voltage.

2.2 | Mode II

In this mode of operation, the floating capacitor is charged up to the voltage magnitude of input voltage, that is, V_{in} by connecting the floating capacitor in parallel to the input voltage. This results in the increase of the number of levels to seven compare to five in Mode I. Furthermore, the achieved voltage gain is 1.5 V_{in} compare to the unity voltage gain of Mode I. Table 4 gives the different switching combinations of the proposed topology with 7L output voltage. The different switching states for this mode of operation has been depicted in Figure 3. Furthermore, the current and voltage stress of the switches of the proposed 7L topology has been provided in Tables 5 and 6, respectively.

3 | EXTENSION OF THE PROPOSED TOPOLOGY

With the proposed topology given in Figure 1, in this paper a modified 9-level topology with an additional floating capacitor unit and a generalized N-level topology with the switched capacitor units has presented in the following subsections.

3.1 | Extension as 9L output voltage waveform

In this extension, an additional floating capacitor (mid-point capacitor clamped structure at the output side) has been added to the topology shown in Figure 1. With this extension, the two

TABLE 4 Switching table of the proposed topology for 7L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o	C_F
0	0	0	0	0	1	1	0	0	1.5 V_{in}	▼
0	0	0	1	0	0	1	0	1	V_{in}	▼
1	1	0	0	0	0	1	0	0	0.5 V_{in}	▲
0	0	1	0	0	0	1	0	1	Zero	—
0	0	0	1	0	0	0	1	1		
1	1	0	0	0	0	0	1	0	−0.5 V_{in}	▲
0	0	1	0	0	0	0	1	1	$-V_{in}$	▼
0	0	0	0	1	0	0	1	0	−1.5 V_{in}	▼

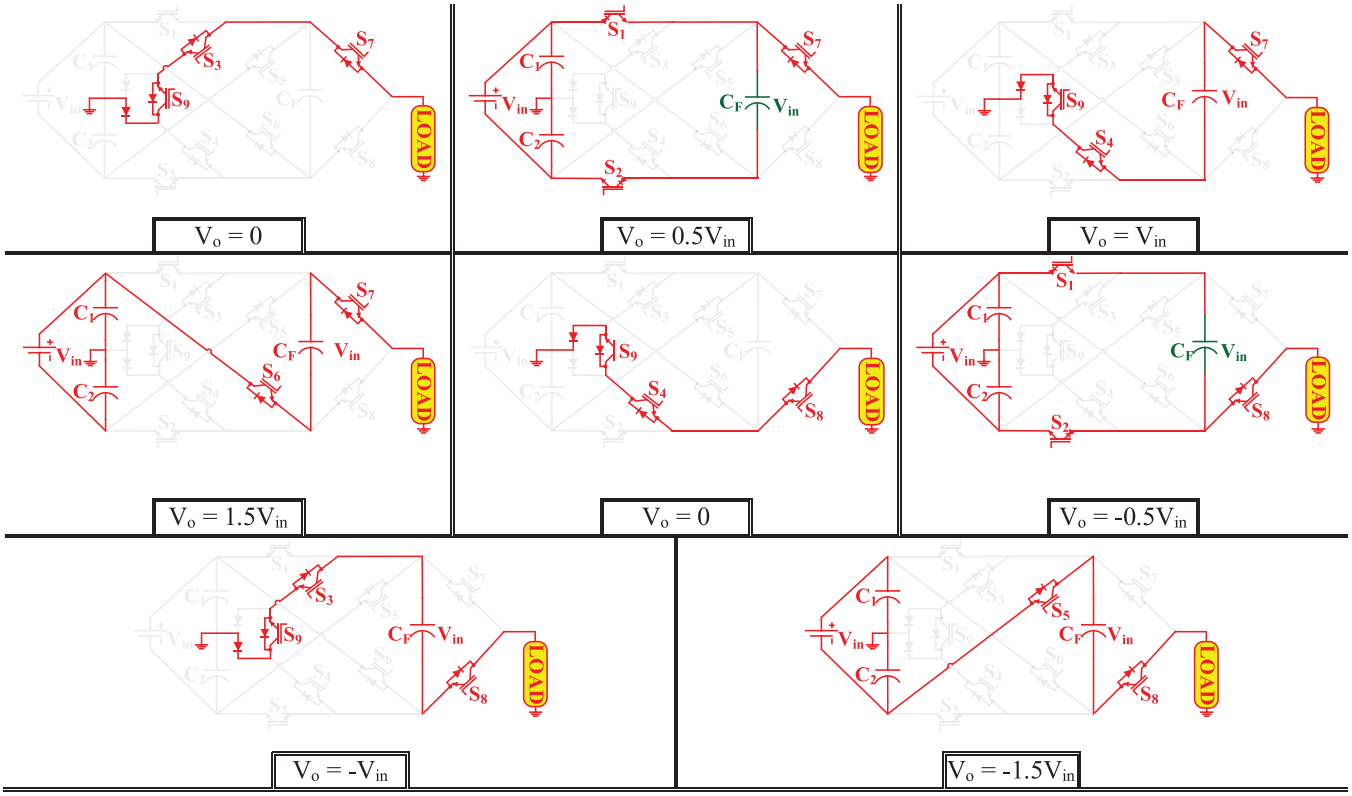

FIGURE 3 Different voltage levels of the proposed 7L topology

TABLE 5 Current stress of the proposed topology for 7L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
0	0	0	0	0	I_o	I_o	0	0	1.5 V_{in}
0	0	0	I_o	0	0	I_o	0	I_o	V_{in}
$I_o + I_c$	$I_o + I_c$	0	0	0	0	I_o	0	0	0.5 V_{in}
0	0	I_o	0	0	0	I_o	0	I_o	Zero
0	0	0	I_o	0	0	0	I_o	I_o	
$I_o + I_c$	$I_o + I_c$	0	0	0	0	0	I_o	0	−0.5 V_{in}
0	0	I_o	0	0	0	0	I_o	I_o	$-V_{in}$
0	0	0	0	I_o	0	0	I_o	0	−1.5 V_{in}

floating capacitors are charged up 0.25 V_{in} by connecting these two floating capacitors in parallel to either of the dc-link capacitor. The switching table for the topology shown in Figure 4 is given in Table 7.

3.2 | Generalized structure of the proposed topology

The higher number of levels and increased voltage gain can be achieved by including more number of switched-capacitor units in the proposed topology, that is, shown in Figure 1. The generalized proposed multilevel inverter structure for N-level voltage as well as for higher gain is shown in Figure 5. In this generalized

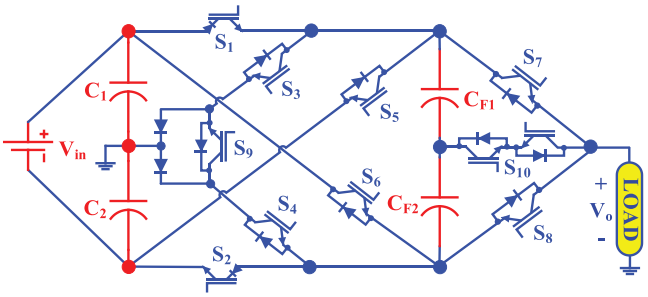

FIGURE 4 Proposed 9L topology

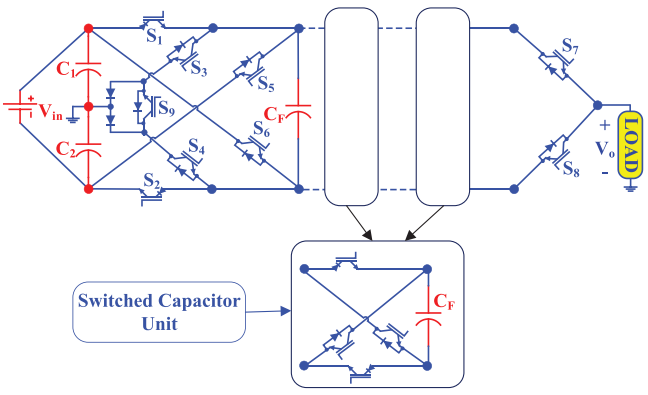

FIGURE 5 Generalized structure of the proposed topology

TABLE 6 Voltage stress of the proposed topology for 7L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
V_{in}	V_{in}	1.5 V_{in}	0	2 V_{in}	0	0	V_{in}	0.5 V_{in}	1.5 V_{in}
0.5 V_{in}	0.5 V_{in}	V_{in}	0	1.5 V_{in}	0.5 V_{in}	0	V_{in}	0	V_{in}
0	0	0.5 V_{in}	0.5 V_{in}	V_{in}	V_{in}	0	V_{in}	0.5 V_{in}	0.5 V_{in}
0.5 V_{in}	0.5 V_{in}	0	V_{in}	0.5 V_{in}	1.5 V_{in}	0	V_{in}	0	Zero
0.5 V_{in}	0.5 V_{in}	V_{in}	0	1.5 V_{in}	0.5 V_{in}	V_{in}	0	0	
0	0	0.5 V_{in}	0.5 V_{in}	V_{in}	V_{in}	V_{in}	0	0.5 V_{in}	−0.5 V_{in}
0.5 V_{in}	0.5 V_{in}	0	V_{in}	0.5 V_{in}	1.5 V_{in}	V_{in}	0	0	$-V_{in}$
V_{in}	V_{in}	0	1.5 V_{in}	0	2 V_{in}	V_{in}	0	0.5 V_{in}	−1.5 V_{in}

TABLE 7 Switching table of the proposed topology for 9L

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o	C_{F1}	C_{F2}
0	0	0	0	0	1	1	0	0	0	V_{in}	▼	▼
0	0	0	0	0	1	0	0	0	1	0.75 V_{in}	▼	—
1	0	0	1	0	0	1	0	1	0	0.5 V_{in}	▲	▲
0	0	0	1	0	0	0	0	1	1	0.25 V_{in}	▼	—
0	1	1	0	0	0	1	0	1	0	Zero	▲	▲
1	0	0	1	0	0	0	1	1	0			
0	0	1	0	0	0	0	0	1	1	−0.25 V_{in}	—	▼
0	1	1	0	0	0	0	1	1	0	−0.5 V_{in}	▲	▲
0	0	0	0	1	0	0	0	0	1	−0.75 V_{in}	—	▼
0	0	0	0	1	0	0	1	0	0	$-V_{in}$	▼	▼

topology, the switched capacitor unit consists of four switches and one floating capacitor. As the number of levels increases the harmonics in the output voltage will come down accordingly, which will results in reduction of filter requirement. According to the design of user requirement and application, the appropriate number of switched capacitor units has to be connected in the generalized multilevel inverter structure (given in Figure 5), that is, for a particular gain, number of levels and size of the filter requirement.

For the generalized structure, the equations for number of switches (N_{sw}), number of capacitors (N_C) and voltage gain (G) with respect to the number of levels (N) are given in Equations (1a) and (1b). If the floating capacitors are charged to half of the input dc source voltage, that is, $V_F = 0.5\ V_{in}$ (similar to the Mode I in the Section II), then the set of generalized equations are,

$$\begin{aligned} N_{sw} &= 2N - 1. \\ N_C &= \frac{1}{2}(N+1). \\ G &= \frac{1}{4}(N-1). \end{aligned} \tag{1a}$$

where $N = 5,7,9,11,13,15,\ldots\ldots$

If the floating capacitors are charged to input dc source voltage, that is, $V_F = V_{in}$ (similar to the Mode II in the Section II),

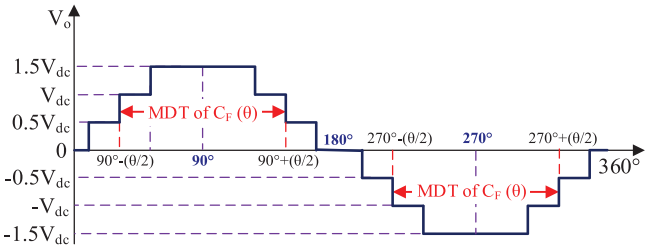

FIGURE 6 7L output voltage with maximum discharge time for C_F

then the set of generalized equations are,

$$\begin{aligned} N_{sw} &= N + 2. \\ N_C &= \frac{1}{4}(N+5). \\ G &= \frac{1}{4}(N-1). \end{aligned} \tag{1b}$$

where $N = 7,11,15,19\ldots\ldots$

4 | SELECTION OF CAPACITANCE

A major challenge with the switched capacitor based inverter topologies is the selection of the correct value of capacitors used in the topology. A proper value of the capacitor is required which decides the voltage ripple of the capacitor which directly affects the ripple losses of the capacitor. The load current through the dc-link capacitors is shared by both of them as the middle point is connected directly to the load. The selection of the capacitance value, C for the dc-link capacitors can be calculated as

$$C_1 = C_2 = C = \frac{I_{o,p}}{2\pi \times f \times \Delta V_c}. \tag{2}$$

where $I_{o,p}$, f and ΔV_c represent the peak load current, output frequency and ripple voltage.

The maximum discharge time for the floating capacitor used in the proposed topology with 7L output voltage has been shown in Figure 6. The floating capacitor is discharged during the voltage levels of $\pm V_{in}$ and $\pm 1.5 V_{in}$. These two voltage

levels are symmetrical around 90° during the positive half-cycle or 270° during the negative half-cycle, can be observed from Figure 6. From this figure, if maximum discharge period of the capacitor is an angle of θ degrees, then the capacitor discharges from the instant $90°-(\theta/2)$ to $90°+(\theta/2)$ during positive half cycle, and from the instant $270°-(\theta/2)$ to $270°+(\theta/2)$ during negative half cycle. Therefore, based on electric change supplied during this interval, the capacitance C_F is given as:

$$C_{F1} = C_{F2} = C_F = \frac{I_{o,p} \times \cos\left(90° - 0.5\theta\right) \times \cos\phi}{\pi \times f \times \Delta V_{C_F}}. \quad (3)$$

where ϕ, and ΔV_C represents the load power factor angle and voltage ripple voltage of the floating capacitor.

5 | POWER LOSS ANALYSIS

The power loss for a switched-capacitor based MLIs mainly comprises switching losses, conduction losses and capacitor ripple losses. The switching and conduction losses occur in the power semiconductor devices and the ripple losses are due to the capacitors. The overall power losses for the switched-capacitor based MLI is given as,

$$P_{losses} = P_{sw} + P_c + P_{ripple}. \quad (4)$$

5.1 | Switching losses (P_{sw})

The switching losses in the power semiconductor devices occur due to the non-ideal behaviour of a switch. During the transition of switching state, the voltage, and current overlap each other. The overlapping results in the switching loss of the device which can be calculated as,

$$P_{sw} = \left[\sum_{allswitches}\left(\sum_{\text{within } 1/f_0}\left(\frac{V_{on}I_{on}T_{on}}{6} + \frac{V_{off}I_{off}T_{off}}{6}\right)\right)\right] \times f_o. \quad (5)$$

Here, V_{on}, I_{on} and T_{on} represent the voltage, current and time duration, of a switch during turn ON state respectively. V_{off}, I_{off} and T_{off} represent the voltage, current and time duration during the turn OFF state of a device, respectively. f_o is the frequency of the output voltage waveform.

5.2 | Conduction losses (P_c)

The conduction losses of a device are caused because of the power loss associated with an internal resistance of the device. The conduction losses of the device are calculated as,

$$P_c = \sum_{\text{allswitches}} I^2_{o,switch} R_{on}. \quad (6)$$

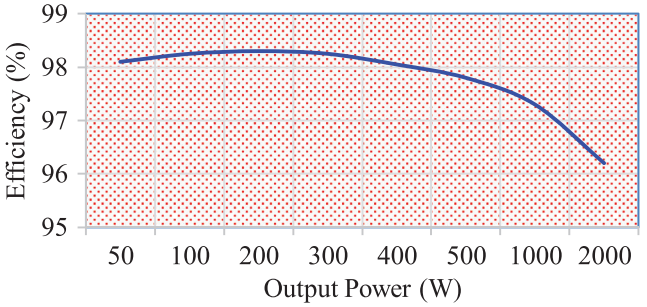

FIGURE 7 Efficiency curve of the proposed topology

where $I_{o,switch}$ and R_{on} represent the on-state current flow through the device having an internal resistance of R_{on}.

5.3 | Ripple losses (P_{ripple})

The voltage drop/power loss in the capacitor will occur mainly due to the internal resistance (known as equivalent series resistance) of the capacitor. This voltage drop gives the additional power loss in the converter losses with switched-capacitor units. The ripple voltage ΔV_c gives the power loss of a capacitor, which is given as,

$$P_{ripple} = \frac{f_{sw}}{2} \times C \times \Delta V_c^2. \quad (7)$$

With the Equations (5)–(7), the power loss of the proposed topology is estimated by using PLECS software with the thermal modelling of the different components. Figure 7 illustrates the efficiency curve of the proposed topology. The maximum efficiency of the proposed 7L topology comes out to be 98.3% at the output load range of (100–300) W. Moreover, the proposed topology will give an improved performance under the higher loading conditions. The efficiency of the 7L proposed topology is 96.2% at the output power of 2000 W.

6 | PULSE WIDTH MODULATION STRATEGY

The fundamental frequency pulse width modulation (PWM) control (FFC) techniques and high-frequency switching PWM control (HFC) strategies have been commonly used as MLI control strategies. In the light of significant output levels, selective harmonic elimination FFC is adopted for various topologies. In addition to maintaining the fundamental value, the magnitude of the voltage increases and switching losses are considerably reduced with FFC in contrast to the HFC. Within this respect, non-linear harmonic equations are resolved and the switching angles with different modulation index (mi) are stored in the form of a look-up table. The method based on the optimization algorithm is used to measure the switching angles, however, for a higher number of levels, the calculation of the

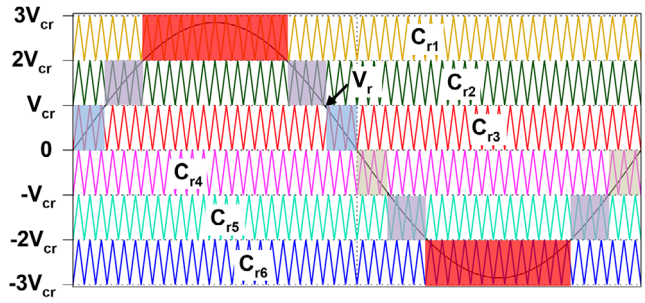

FIGURE 8 Level-shifted pulse width modulation strategy for the proposed topology with 7L output voltage

TABLE 8 Switching logic for 7L configuration

Switch	PWM logic
S_1 and S_2	$(C_{r3} < V_r < C_{r2})$ or $(C_{r5} < V_r < C_{r4})$
S_3	$(0 < V_r < C_{r3})$ or $(C_{r6} < V_r < C_{r5})$
S_4	$(C_{r2} < V_r < C_{r1})$ or $(C_{r4} < V_r < 0)$
S_5	$V_r < C_{r6}$
S_6	$V_r > C_{r1}$
S_7	$V_r > 0$
S_8	$V_r < 0$ or $\bar{S}_7$
S_9	$(C_{r2} < V_r < C_{r1})$ or $(C_{r4} < V_r < C_{r3})$ or $(C_{r6} < V_r < C_{r5})$

Abbreviations: $C_{rk} = k^{th}$ carrier wave; V_r = reference wave.

optimized angles become impractical due to higher computational burden.

A level-shifted sinusoidal pulse width modulation as shown in Figure 8 is used for the proposed topology. For switching state calculation, a sinusoidal reference (V_r) is compared with six level shifted triangular signals each having a magnitude of V_{cr}. The switching logic to generate the PWM pulses for each individual switch is given in Table 8, that is, realized from the Figure 3 (working states of each voltage level) and Figure 8 (LS-PWM reference and carriers). According to this switching logic, the generated gate pulse for the 7L topology has been illustrated in Figure 9. From this figure, it can be visualized that switching transitions from one voltage level to other voltage level.

7 | COMPARATIVE STUDY

A comparative study for the proposed topology has been carried out with Mode II, that is, with 7L with other similar topologies and is given in Table 9. The topologies proposed in ref. [20] generate the 9L output voltage however it lacks the voltage boosting of the input voltage with unity voltage gain. Similarly, the topology introduced in ref. [26] gives the peak of the output voltage half of the input voltage by using 12 switches. In addition, it uses five capacitors whereas the proposed topology uses only three capacitors for the same number of voltage levels

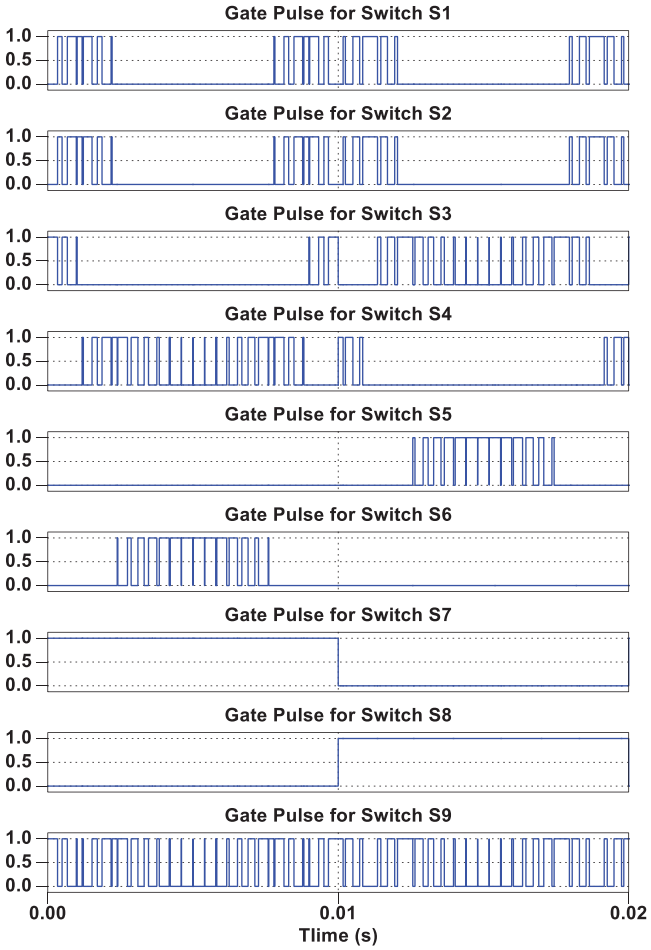

FIGURE 9 Gate pulses for the proposed topology with 7L output voltage

with a voltage gain of 1.5. The proposed topology has a lower number of switches with higher voltage gain makes it suitable for solar PV applications.

8 | RESULTS AND DISCUSSION

In this section, the proposed topology with 7L and 11L configuration has been discussed. For the 7L configuration, both simulation and experimental results have been provided and discussed in detail. For the extension of the proposed topology, two switched capacitor units have been used to generate 11L voltage and the simulation result for 11L has been provided.

8.1 | Simulation results

8.1.1 | 7L configuration

The simulation results for the proposed 7L topology has been carried out using PLECS software. For the simulation results, the input voltage has been selected as 200 V with a carrier

TABLE 9 Comparison between proposed 7L and topologies with single source configuration

Top	N	N_{sw}	N_d	N_c	N_{gd}	G	VB
[12]	7	10	0	3	8	1.5	Yes
[17]	5	7	2	3	7	0.5	No
[20]	9	12	0	3	12	1.0	No
[21]	7	10	0	4	8	1.5	Yes
[23]	7	10	0	3	10	0.5	No
[24]	7	10	0	4	10	0.5	No
[26]	7	12	0	5	11	0.5	No
[27]	7	10	0	4	8	1.5	Yes
[Proposed]	7	9	2	3	9	1.5	Yes

Abbreviations: $N_d/N_{sw}/N_{gd}/N_C$ = Number of diodes/switches/gate drives/capacitors; VB = voltage boosting ability of the topology; G = Voltage gain.

frequency of 5 kHz. Figure 10(a) shows the output current, voltage and floating capacitor voltage with a resistive load of 100 Ω. With 200 V input voltage, the peak of the output voltage has a value of 300 V which confirms the 1.5 times voltage gain. Similarly, the output quantity for the RL load has been illustrated in Figure 10(b) with a load value of $Z = 100\ \Omega + 200$ mH. From both simulation figures, the floating capacitor voltage remains balanced at the input voltage of 200 V. In addition, the proposed topology has been simulated with the dynamic operating conditions. Figure 11(a) shows the variation of the output quantity with the floating capacitor voltage with the dynamic change of modulation index with a load value of $Z = 75\ \Omega + 100$ mH. The modulation index (MI) is changed from 1.0 to 0.6 to 0.3 which results in a change of the number of levels from seven to five to three. Similarly, the change in load has also been shown in Figure 11(b) with the load changes from $Z = 75\ \Omega$ to $Z = 75\ \Omega + 100$ mH. From all these simulation results, the validity of the proposed topology has been established in the simulation environment with different operating conditions.

8.1.2 | 11L configuration

The extension of the proposed topology has also been validated using simulation results. Two switched capacitor units have been used. These two switched capacitor units have been changed up to the voltage of 200 V, that is, input voltage. Therefore, the peak of the output voltage has a magnitude of 500 V which gives the voltage gain of 2.5. Figure 12 shows the output current, voltage and both floating capacitor voltage with a load change from $Z = 75\ \Omega$ to $Z = 75\ \Omega + 100$ mH. Both capacitors voltage remains balanced for the extended topology with load changes.

8.2 | Experimental results

For the validation of the simulation results, a laboratory prototype has been developed with the IGBT switches, Gate drivers,

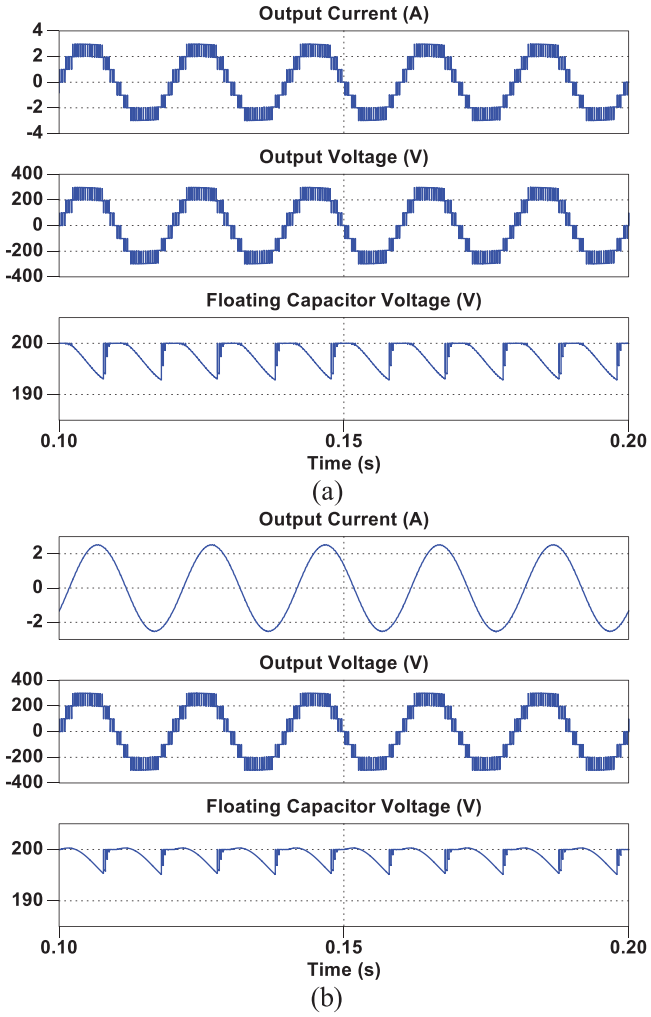

FIGURE 10 Simulation results of output current, voltage and floating capacitor voltage with (a) Z = 100 Ω, and (b) Z = 100 Ω + 200 mH

TABLE 10 Experimental parameters

Parameter	Value
Input voltage	100 V
Output frequency	50 Hz
Carrier frequency	5 kHz
Capacitor	2.2 mF, 200 V
Resistive load	150 Ω
Inductive load	80 mH

capacitors, FPGA Vertex-5 board, dc power supplies (15 V for gate drivers, 0–600 V for powering the proposed inverter) and RL load bank, as shown in Figure 13. The different parameters used for the experimental results have been given in Table 10.

Figure 14(a),(b) depicts the output voltage, current and floating capacitor voltage with the load values of 150 Ω and 150 Ω + 80 mH, respectively. The step voltage for the 7L output

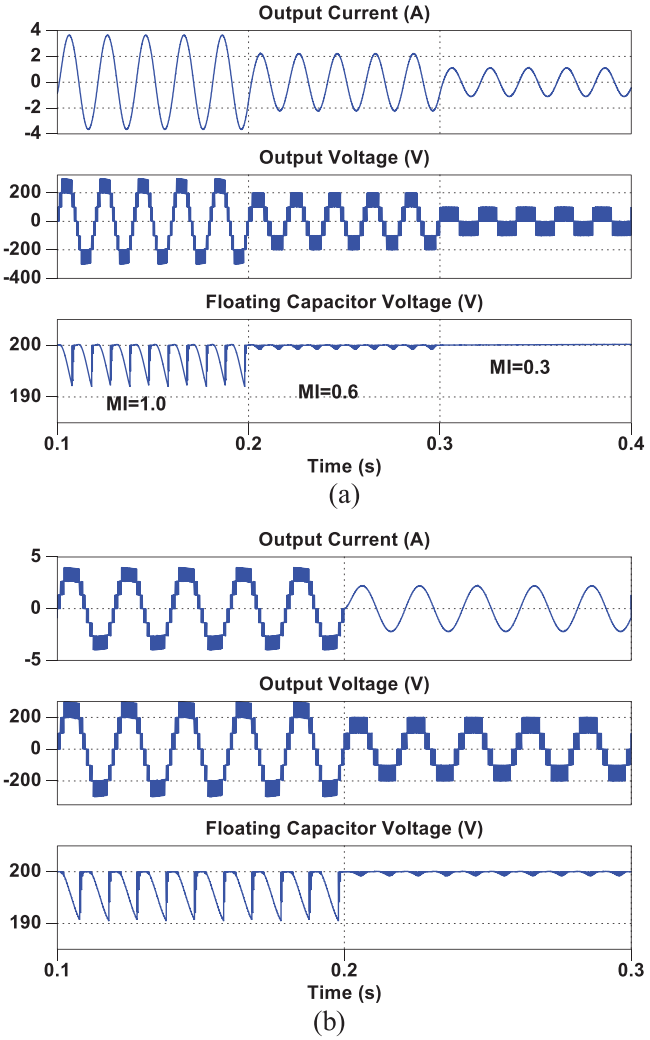

FIGURE 11 Simulation results of output current, voltage and floating capacitor voltage with (a) change of MI, and (b) change of load

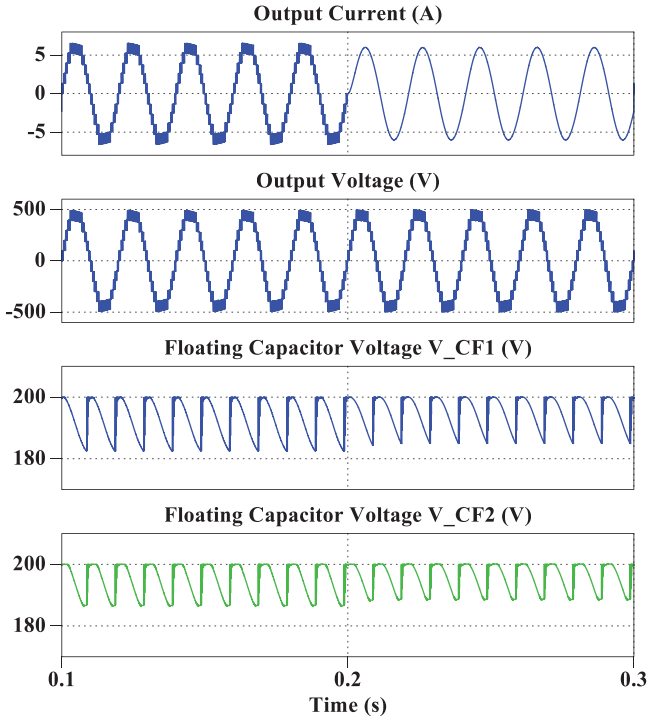

FIGURE 12 Simulation results of the extended topology showing output current, voltage and floating capacitors voltage with change of load

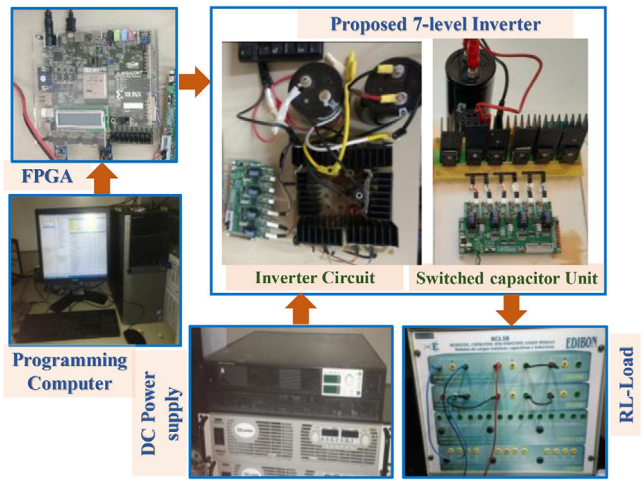

FIGURE 13 Experimental prototype of proposed multilevel inverter

is 50 V, which results in the peak output voltage as 150 V. The peak value of 150 V confirms the voltage gain of 1.5. Furthermore, the floating capacitor remains balanced at the input voltage of 100 V. Furthermore, the dynamic conditions of the proposed topology have also been tested with the change of load. Figure 14(c) shows the change of load with resistive load. First, the load is changed from a no-load condition to a load of 150 Ω. This change results in a change of current from zero to 1A peak. Further, a resistor of 150 Ω is connected in parallel to the existing load, makes the effective load of 75 Ω causing the doubling of the peak load current to 2 A. In addition, the change of load power factor has also been considered.

The change of pf from unity to 0.98 (lagging) has been illustrated in Figure 15(a). Furthermore, the transient condition with the starting condition has been depicted in Figure 15(b). At starting, the input voltage is zero and the floating capacitor voltage is fully discharged and at zero voltage level. As the input voltage is turned ON, the floating capacitor voltage reaches the steady voltage equal to the input voltage of 100 V. Figure 15(b) is evident that the floating capacitor is charged slowly from zero to 100 V in the first few cycles without any pre-charging and capacitor voltage balancing circuit and during that time transients in output current and voltage of the inverter are minimal. Further, Figure 15(c) depicts the waveforms with change of MI. The two change of MI, that is, from 1.0 to 0.66 and from 0.66 to 0.33 has been illustrated in Figure 15(c). With the change of MI, the number of levels reduces as evident from Figure 15(c). The reduction in the number of levels reduces

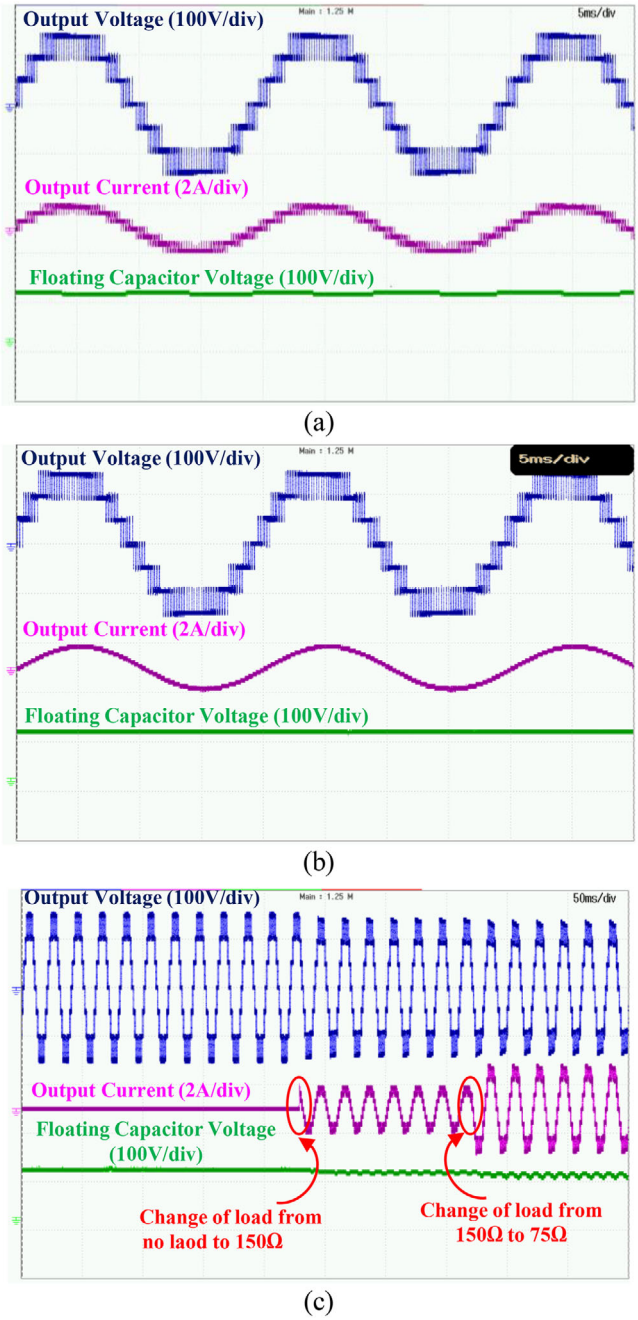

FIGURE 14 Experimental results of the output voltage, current and floating capacitor voltage with (a) $Z = 150\ \Omega$, (b) 150 Ω+80 mH and (c) dynamic change of resistive load

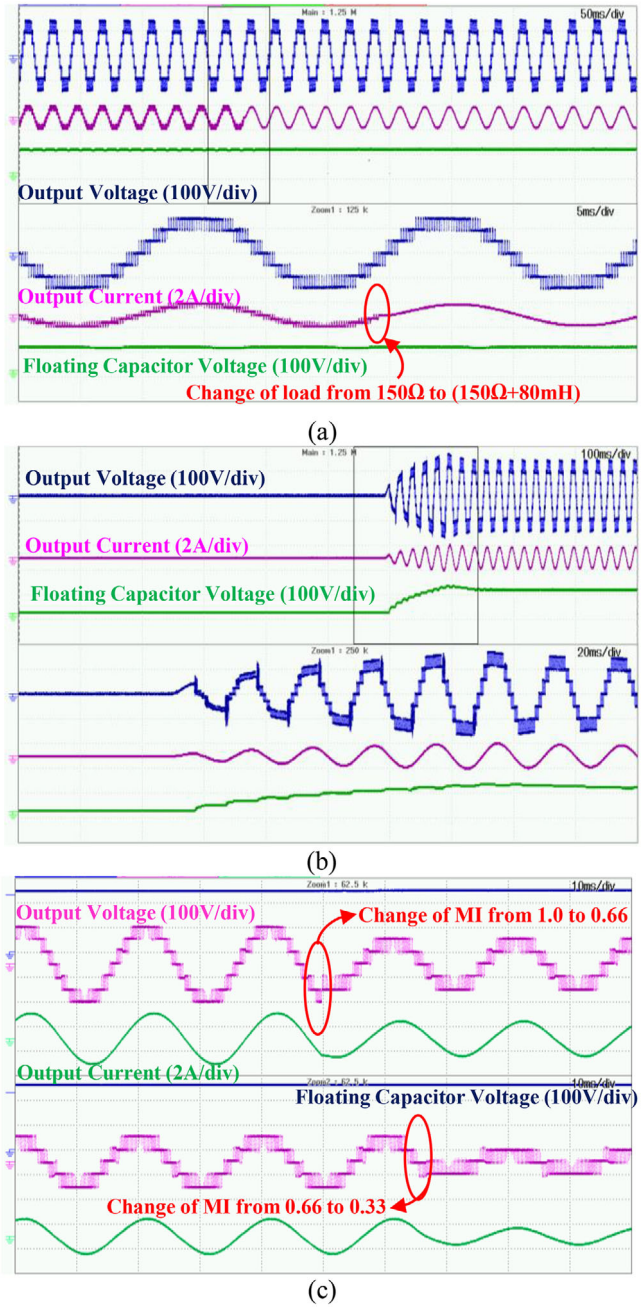

FIGURE 15 Experimental results of the output voltage, current and floating capacitor voltage with, (a) change of load from resistive to series connected resistive-inductive load, (b) starting of converter (from zero input voltage to 100 V) and (c) change of MI

the peak load voltage. At the MI of 0.66, the number of levels become five and at MI = 0.33, the number of levels become three. These reduction in MI results in the reduction in the peak output voltage from 150 V at MI = 1.0 to 100 V at MI = 0.66 to 50 V at MI = 0.33. From all these simulations and experimental results, it can be concluded that the proposed topology works satisfactorily with a different type of loading and operating condition with the self-balancing of the floating capacitor voltage.

9 | CONCLUSION

In this article, a family of boost ANPC topology has been introduced with reduced switch count. The proposed topology can be operated for different voltage gain and number of levels based on the requirement. Further, the proposed topology can be extended for higher voltage gain and number of levels by incorporation of just a few auxiliary devices. The proposed topology with 7L configuration has been thoroughly evaluated and tested. The different theoretical, simulation and

experimental findings have been established in this paper for the validation of the proposed topology. The suggested ANPC inverters topology with its extensions are interesting alternatives for the single-stage dc-ac conversion applications.

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REFERENCES

1. Akagi, H.: Multilevel converters: Fundamental circuits and systems. Proc. IEEE 105(11), 2048–2065 (2017)
2. Rawa, M., et al.: Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of components. IET Power Electron. 13(4), 881–891 (2020)
3. Siddique, M.D., et al.: Optimal design of a new cascaded multilevel inverter topology with reduced switch count. IEEE Access 7, 24498–24510 (2019)
4. Gupta, K.K., et al.: Multilevel inverter topologies with reduced device count: A review. IEEE Trans. Power Electron. 31(1), 135–151 (2016)
5. Siddique, M.D., et al.: A new multilevel inverter topology with reduce switch count. IEEE Access 7, 58584–58594 (2019)
6. Vijeh, M., et al.: A general review of multilevel inverters based on main submodules: Structural point of view. IEEE Trans. Power Electron. 34(10), 9479–9502 (2019)
7. Siddique, M.D., et al.: A new switched capacitor 7L inverter with triple voltage gain and low voltage stress. IEEE Trans. Circuits Syst. II: Express Briefs 67(7), 1294–1298 (2020)
8. Lee, S.S.: Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter. IEEE Trans. Power Electron. 33(10), 8204–8207 (2018)
9. Wang, L., et al.: Novel cascaded switched-diode multilevel inverter for renewable energy integration. IEEE Trans. Energy Convers. 32(4), 1574–1582 (2017)
10. Liu, J., et al.: A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system. IEEE Trans. Power Electron. 29(8), 4219–4230 (2014)
11. Liu, J., et al.: Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques. IEEE J. Emerg. Sel. Top. Power Electron. 6(3), 1616–1626 (2018)
12. Liu, J., Zhu, X., Zeng, J.: A seven-level inverter with self-balancing and low-voltage stress. IEEE J. Emerg. Sel. Top. Power Electron. 8(1), 685–696 (2020)
13. Sebaaly, F., et al.: Experimental design of fixed switching frequency model predictive control for sensorless five-level packed U-cell inverter. IEEE Trans. Ind. Electron. 66(5), 3427–3434 (2019)
14. Grigoletto, F.B.: Five-level transformerless inverter for single-phase solar photovoltaic applications. IEEE J. Emerg. Sel. Top. Power Electron. 8(4), 3411–3422 (2020)
15. Di Benedetto, M., et al.: Five-level E-type inverter for grid-connected applications. IEEE Trans. Ind. Appl. 54(5), 5536–5548 (2018)
16. Wang, H., et al.: A new six-switch five-level active neutral point clamped inverter for PV applications. IEEE Trans. Power Electron. 32(9), 6700–6715 (2017)
17. Wang, H., et al.: A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy. IEEE Trans. Power Electron. 32(7), 5146–5161 (2017)
18. Siwakoti, Y.P.: A new six-switch five-level boost-active neutral point clamped (5L-Boost-ANPC) inverter. Paper presented at the 2018 IEEE Applied Power Electronics Conference and Exposition, San Antonio, TX, USA, 4–8 March 2018
19. Siwakoti, Y.P., Blaabjerg, F.: Common-ground-type transformerless inverters for single-phase solar photovoltaic systems. IEEE Trans. Ind. Electron. 65(3), 2100–2111 (2018)
20. Sandeep, N., Yaragatti, U.R.: Operation and control of an Improved hybrid nine-level inverter. IEEE Trans. Ind. Appl. 53(6), 5676–5686 (2017)
21. Lee, S.S., Lee, K.B.: Dual-T-type seven-level boost active-neutral-point-clamped inverter. IEEE Trans. Power Electron. 34(7), 6031–6035 (2019)
22. Sandeep, N., Yaragatti, U.R.: Design and implementation of active neutral point-clamped nine-level reduced device count inverter: An application to grid integrated renewable energy sources. IET Power Electron. 11(1), 82–91 (2018)
23. Pulikanti, S.R., et al.: Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM. IEEE Trans. Ind. Electron. 60(11), 4794–4804 (2013)
24. Sheng, W., Ge, Q.: A novel seven-level ANPC converter topology and its commutating strategies. IEEE Trans. Power Electron. 33(9), 7496–7509 (2018)
25. Zeng, J., et al.: Switched-capacitor based active-neutral-point-clamped seven-level inverter with natural balance and boost ability. IEEE Access 7, 1 (2019)
26. Yadav, A.K., et al.: A hybrid 7-level inverter using low-voltage devices and operation with single DC-link. IEEE Trans. Power Electron. 34(10), 9844–9853 (2019)
27. Lee, S.S., et al.: New family of boost switched-capacitor 7-level inverters (BSC7LI). IEEE Trans. Power Electron. 34(11), 10471–10479 (2019)

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