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A New Transformer-Less Single-Phase Photovoltaic Inverter to Improve the Performance of Grid-Connected Solar Photovoltaic Systems

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Mohua Biswas [1], **Shuvra Prokash Biswas** [1], **Md. Rabiul Islam** [2], **Md. Ashib Rahman** [2], **Kashem M. Muttaqi** [2] **and S. M. Muyeen** [3,*]

1 Department of Electronics & Telecommunication Engineering, Rajshahi University of Engineering & Technology, Rajshahi 6204, Bangladesh
2 School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, NSW 2522, Australia
3 Department of Electrical Engineering, Qatar University, Doha 2713, Qatar
* Correspondence: sm.muyeen@qu.edu.qa; Tel.: +974-4403-4205

Abstract: Photovoltaic (PV) energy systems have found diverse applications in fulfilling the increasing energy demand worldwide. Transformer-less PV inverters convert the DC energy from PV systems to AC energy and deliver it to the grid through a non-isolated connection. This paper proposes a new transformer-less grid-connected PV inverter. A closed-loop control scheme is presented for the proposed transformer-less inverter to connect it with the power grid. The proposed transformer-less inverter reduces extra leakage current and holds the common-mode voltage at a constant point. To eliminate extra leakage current, as well as achieve constant common-mode voltage, a midpoint clamping method is utilized to operate the inverter. The proposed transformer-less inverter is formed of seven insulated gate bipolar transistors (IGBTs) employing a unipolar sinusoidal pulse width modulation (SPWM) technique for switching purposes. An LCL filter is employed to reshape the two-level inverter output voltage and current to obtain closer sinusoidal waveforms. The output voltage and current total harmonic distortion (THD) of the proposed transformer-less inverter were found to be 1.25% and 0.94%, respectively, in the grid-connected mode. The leakage current elimination mechanism with the proposed transformer-less inverter is deeply analyzed in this paper. The performances of the proposed transformer-less inverter were evaluated with MATLAB/Simulink simulation and validated in a laboratory scale experiment.

Keywords: photovoltaic energy; transformer-less inverter; grid-connected inverter; leakage current; common-mode voltage; unipolar sinusoidal pulse width modulation

1. Introduction

Photovoltaic (PV) energy is one of the promising future renewable energy routes for meeting the rising energy demand as fossil fuel-based energy extraction increases the carbon footprint. Due to the scientific improvements in material and manufacturing techniques, the cost of operating a PV system is decreasing, making it the most cost-effective energy source for future mass deployment. The cumulative power of installed PV systems amounted to 900 GW in 2021 globally [1]. However, more research is required to develop more efficient, reliable, and grid-friendly renewable energy systems.

In the past, line frequency transformers were connected to PV inverters to boost the DC link voltage for grid integration purposes. However, the use of line frequency transformers makes the system bulky and costly [2]. A grid-connected transformer-less PV inverter does not employ any transformer and can be connected directly to the power grid [3]. This type of inverter is highly efficient, offers lower switching losses, is lighter in weight, and is cost effective. However, these inverters suffer from some drawbacks. Voltage

fluctuations in stray capacitors of the PV cell cause fluctuations in common-mode voltage, which results in extra leakage current flow [4]. This extra leakage current through the parasitic capacitors to the converter ground may lead to unexpected conduction paths and can cause serious electric shock. The leakage current can be reduced if the common-mode voltage remains constant. Using a conventional H-bridge inverter, the leakage current would be higher than 500 mA. High leakage current can cause serious electric shocks in conventional H-bridge inverter-based PV systems. Furthermore, excessive leakage current drives electromagnetic interference (EMI), which increases ripples, as well as harmonics, in the grid current [5]. Leakage current can be eliminated and reactive power support for PV inverters can be provided via traditional bipolar pulse width modulation (BPPWM) technology [6]. However, employing bipolar PWM to manage reactive power results in substantial switching loss, which reduces the system's efficiency. As a result, a number of transformer-less PV inverter topologies employ the unipolar pulse width modulation (UPPWM) technique to regulate the system's reactive power [7,8]. The PWM mechanism in the H5 inverter topology switches from UPPWM to BPPWM during the negative power area [9]. Although reactive power can be controlled, doing so in practice is difficult. Significant current ripple and high switching loss further contribute to the poor efficiency. Although a switching technique has been put forth in [10], it suffers from some extra switching losses in the positive power zone. The direction of leakage current flow is demonstrated in Figure 1.
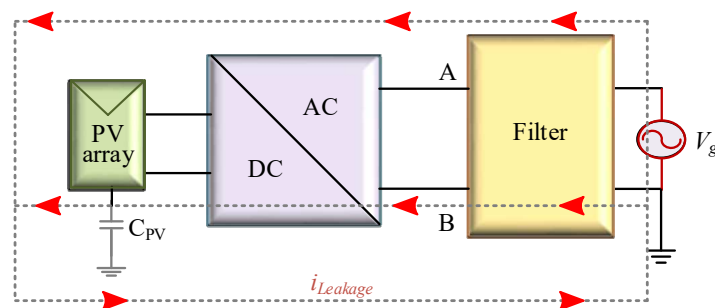
Figure 1. Direction of leakage current in a grid-tied single-phase transformer-less PV inverter.

To alleviate these problems, numerous studies have been carried out or are in progress. Several transformer-less PV inverter topologies, such as H5 [11], oH5 [12], HERIC [13], and H6 [14], have been reported and applied to improve efficiency and reduce leakage current. In these topologies, the galvanic isolation method is used, in which the ground of the photovoltaic source is separated from the inverter ground. The efficiency of these topologies is in the range from 96 to 97%. However, the leakage current suppression of these topologies is not pleasant, around 45–80 mA. An H5-D topology was proposed in [15], where, by utilizing an extra clamping diode, the common-mode voltage fluctuations were suppressed. However, an efficiency analysis of this proposed inverter is missing. An improved H6 topology was investigated in [16] to suppress the resonance. The topology applied a snubber circuit to reduce power losses and extra common-mode current. However, a power loss analysis of this topology was not considered there. Furthermore, the effect of the strong ripples on the snubber voltage can increase the harmonics of the output voltage. A symmetric Z-source HERIC inverter was proposed in [17], but power loss analysis was not taken into consideration. A dual-buck and boost-type inverter was proposed in [18]. This was a dual-buck and boost inverter with a single input DC source (DBBI-SIDS) and two extra MOSFETs. However, the switching losses can be high with that method. The approach in [19] avoids neutral-point voltage unbalancing but uses three-level inverters. In this approach, the ripples in the neutral-point voltage not only reduce the lifetime of the DC link capacitors but also increase the harmonics in the output voltage. In [20], a separate MPPT is used to suppress neutral-point voltage ripples. However, in this method, to interact with the separate MPPT, the voltages of up and down capacitors are controlled

asymmetrically. The bipolar carrier-based pulse width modulation (CB-PWM) method was applied in [21] to balance the neutral-point voltage offset, as well as reduce the ripples in the neutral-point voltage. However, the separate MPPT is cancelled because of the dipolar CB-PWM procedure. In [22], a single-phase grid-connected non-isolated H7 inverter was proposed with less leakage current flow and constant common-mode current, as well as less power losses. However, only simulation results were considered there and experimental analysis was not performed.

This paper proposes a new single-phase transformer-less PV inverter topology. This proposed topology utilizes unipolar sinusoidal pulse width modulation (SPWM) technique. Seven insulate gate bipolar transistor (IGBT) switches with antiparallel diodes are utilized as control switches. Moreover, six independent diodes are utilized in the freewheeling branch to compress the leakage current flow from the ground line. The freewheeling branch is connected between the DC link midpoint and LCL filter. A voltage controller is presented to control the inverter output voltage while operating in grid-connected mode. The proposed inverter:

- Mitigates the ripples in the stray capacitor voltage;
- Eliminates the extra leakage current;
- Keeps the common-mode voltage constant;
- Reduces the harmonics in the grid voltage and current, as well as the losses;
- Increases the inverter performance, even if the solar energy intensity is scarce.

The performances of the proposed transformer-less inverter are compared with other existing inverters to prove the superiority of the proposed inverter.

The rest of the manuscript is organized as follows: Section 2 contains the topology description, common-mode voltage analysis, and conduction mode analysis for the proposed transformer-less inverter. The modulation strategy and the control scheme for the proposed transformer-less inverter are detailed in Section 3. Simulation results are presented in Section 4. Experimental results are included in Section 5. Comparisons between the proposed and existing transformer-less inverters are discussed in Section 6. Finally, Section 7 concludes the paper.

2. Proposed Single-Phase Transformer-Less Inverter

2.1. Structure of the Proposed Transformerless PV Inverter

The proposed transformer-less inverter contains seven IGBT switches to form the bridge connection, as well as six diodes in the freewheeling branch in total, as depicted in Figure 2. The common-mode current is clamped to the DC link midpoint through the freewheeling branch. The branch contains six diodes (D_1–D_6) and an IGBT switch (S_7). The diodes D_1–D_4 form another bridge circuit along with two diodes D_5 and D_6, which form the freewheeling branch. These diodes are forward biased in the freewheeling modes for both positive power region operation and negative power region operation. In the positive half cycle, switches S_1 and S_4 have the same switching sequence. Likewise, in the negative half cycle, switches S_2 and S_3 have the same switching sequences. Switches S_5 and S_6 conduct in both conduction modes and are disconnected in both of the freewheeling modes. The common-mode voltage is constant and clamps half of the input DC voltage. As a result, voltage in the stray capacitor does not fluctuate and the leakage current flow is reduced.

There are two power flow regions if phase shift occurs between the grid voltage and current. If voltage and current both remain in the same quadrant (positive or negative), then the power flows through the PV array to the grid. This situation is known as the positive power region. Likewise, it is called the negative power region if the power flows from the grid to the PV array. In that period, voltage and current stay in different quadrants. However, if the power factor is 1, then only the positive power region will form. Two capacitors are used for the DC link connection and an LCL filter is used at the grid side for harmonic suppression.
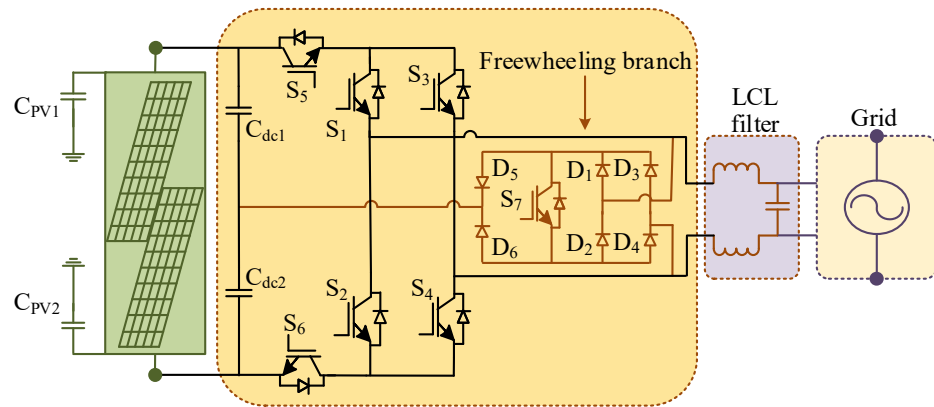
Figure 2. Schematic diagram of proposed inverter topology.

2.2. Modulation Technique

Seven gate pulses are required to operate the proposed transformer-less inverter. The gate pulse generation technique and obtained gate pulses for firing the IGBTs are illustrated in Figures 3 and 4, respectively. The unipolar SPWM technique is utilized here. Compared to the bipolar SPWM method, the unipolar PWM provides improved efficiency. Furthermore, switching losses can be reduced with the unipolar SPWM method. Figure 4 shows that the switches S_1 and S_4 have the same switching sequences. Similarly, switches S_2 and S_3 have the same switching sequences. The switches S_1 and S_4 are activated in the positive half cycle, whereas the switches S_2 and S_3 are activated in the negative half cycle. During the positive half cycle, the switching pulses of the switches S_5 and S_6 are as similar as the gate pulses of the switches S_1 and S_4. Similarly in the negative half cycle, the switching pulses of S_5 and S_6 are as similar as the gate pulses of the switches S_2 and S_3. The switch S_7 has the opposite pulses compared to S_5 and S_6; i.e., when S_7 is ON, S_5 and S_6 are OFF and vice versa.
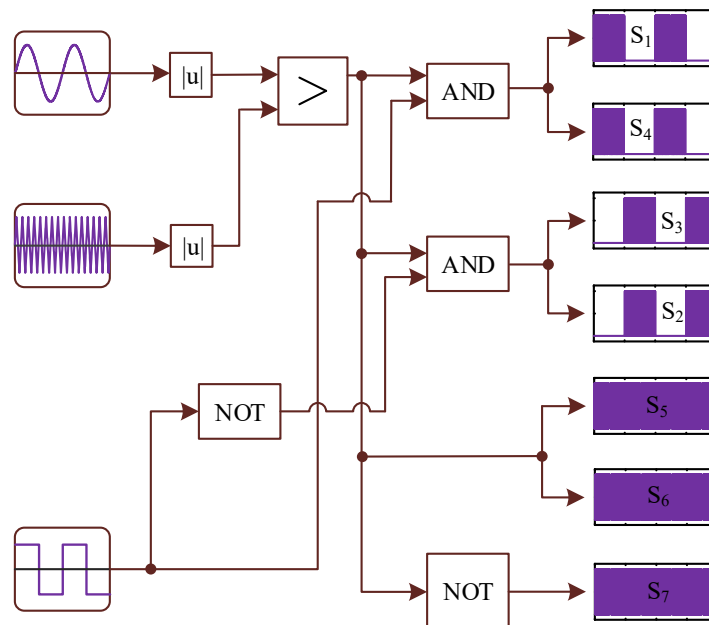
Figure 3. Gate pulse generation technique for the proposed transformer-less inverter.
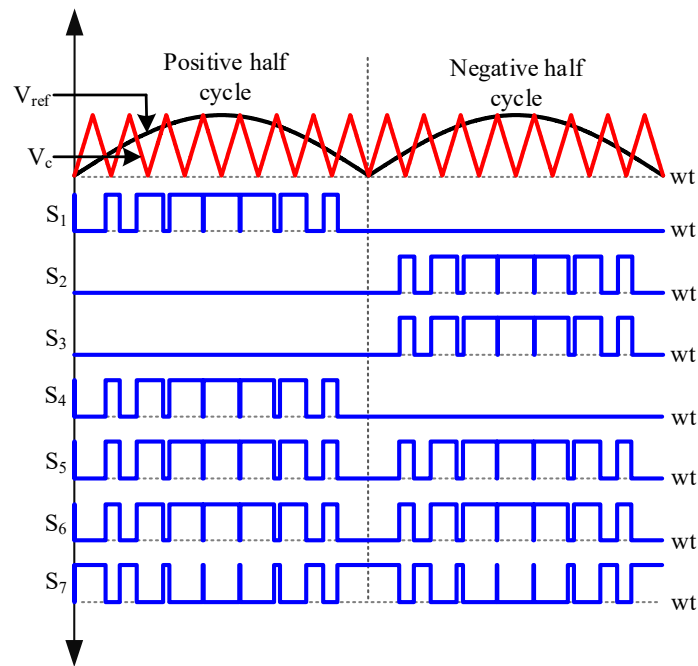
Figure 4. Gate-driving pulses for the proposed transformer-less inverter.

2.3. Control Scheme

A maximum power point tracking (MPPT) controller is used on the DC side to control the PV array power. On the inverter side, two PI controllers are used as a feedback controller. One PI controller is used as a voltage controller and another one is used in the inner current controller loop. The control loop control strategy is depicted in Figure 5. The proportional end of the controller reduces the error, while the integrator minimizes the offset value. The value of the proportional gain is determined by the current error. To improve system response, the proportional and integrator gain must be tuned [23]. Here the proportional gain and integrator gain can be defined as K_p and K_I.
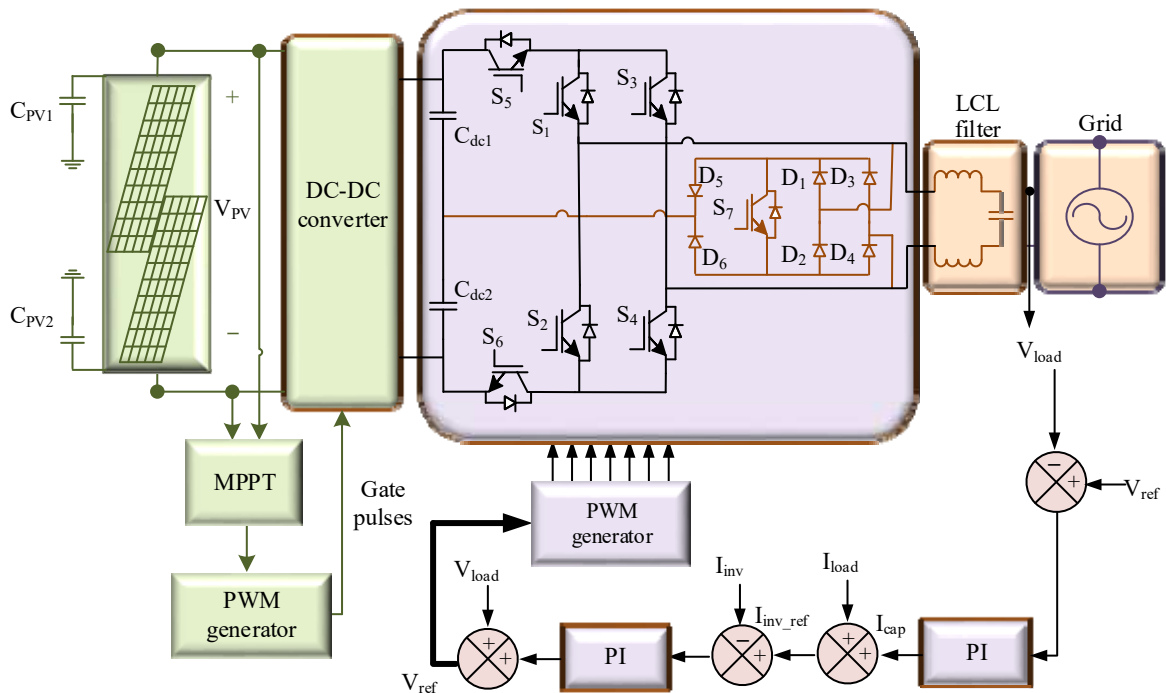

Figure 5. Control strategy for the proposed transformer-less inverter.

The proportional and integrator terms for the voltage controller are expressed in Equations (1) and (2), respectively.

$$K_P = \frac{C_{Filter}}{T_v} \tag{1}$$

$$K_I = \frac{r_{Capacitor}}{T_v} \tag{2}$$

where C_{Filter} is the filter capacitance, $r_{capacitor}$ is the series resistance of the filter capacitor, and T_v is the time constant of the voltage controller. The proportional and integrator terms for the current controller are shown below:

$$K_P = \frac{L_{Filter}}{T_c} \tag{3}$$

$$K_I = \frac{r_{Inductor}}{T_c} \tag{4}$$

where L_{Filter} is the filter inductance, $r_{inductor}$ is the series resistance of the filter inductance, and T_c is the time constant of the current controller.

A block diagram representation of the control mechanism of the proposed inverter is depicted in Figure 6. The parameters of the block diagram are expressed as follows:

$$G_{filter} = \frac{1}{s(L_1 + L_2) + s^3(C_o L_1 L_2)} \tag{5}$$

$$G_{PI} = K_P + \frac{K_I}{s} \tag{6}$$

$$G_{PWM} = \frac{1}{1 + 1.5Ts} \tag{7}$$

where G_{inv}, G_{filter}, G_{PI}, and G_{PWM} represent the gains of the inverter, the filter, the PI controller, and the pulse width modulator.
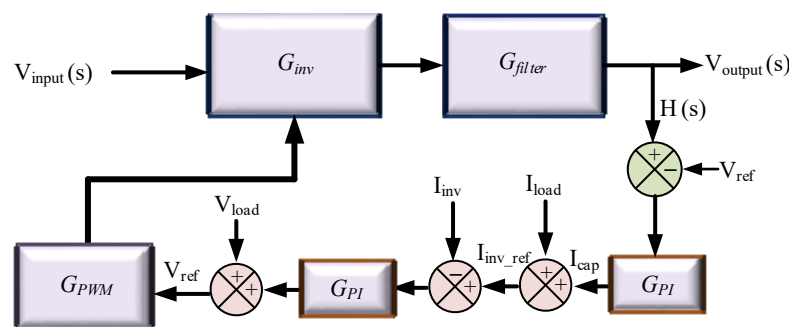

Figure 6. Block diagram representation of the proposed inverter system.

The transfer functions for determining the stability yield:

$$L.T = \frac{G_{inv}G_{filter}}{1 + (G_{inv}G_{filter})G_{pi}G_{gain}G_{PWM}H(s)} \tag{8}$$

## 3. Conduction Modes of the Proposed Transformer-Less Inverter

3.1. Conduction Modes in Unity Power Factor Operation

There are four conduction modes in unity power factor operation. These modes are: the active mode and freewheeling mode of the positive half cycle (modes 1 and 2) and the active mode and freewheeling mode of the negative half cycle (modes 3 and 4). All the conduction modes are described below.

Positive half-cycle active mode (mode 1): As shown in Figure 7a, four power switches are shorted in this mode. The load current flows in the switches S_5, S_1, S_4, and S_6. In this situation, inverter output voltage (V_{AB}) becomes equal to the input DC voltage (V_{DC}), where $V_{AN} = +V_{DC}$ and $V_{BN} = 0$. Therefore, the common-mode voltage becomes:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{dc} + 0) = \frac{V_{dc}}{2} \tag{9}$$
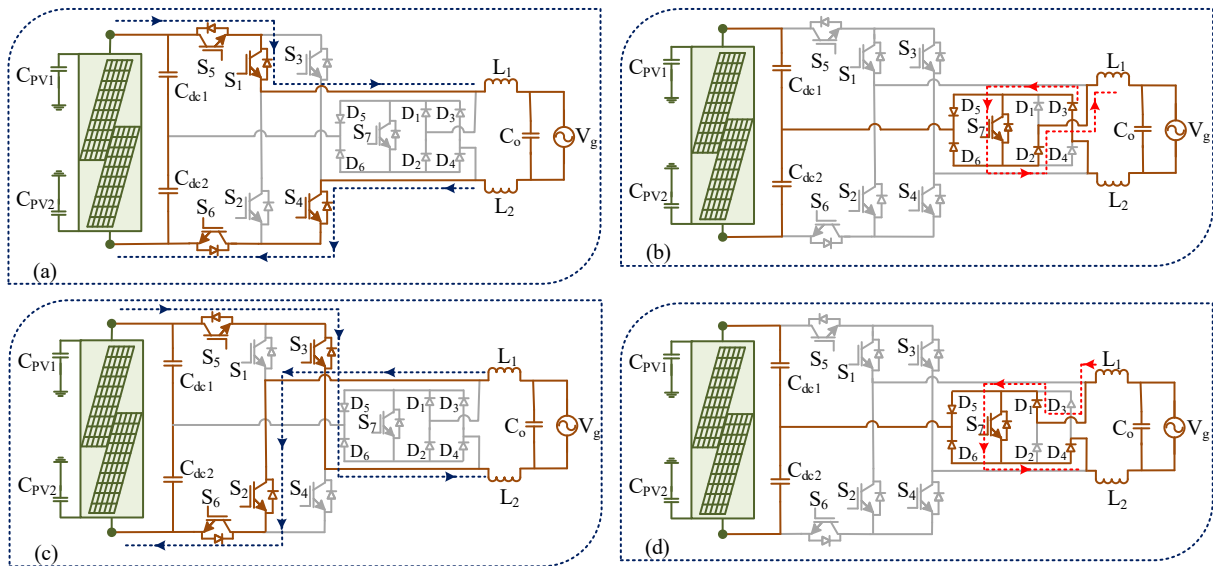
Figure 7. Conduction modes under unity power factor: (**a**) positive half-cycle active mode, (**b**) positive half-cycle freewheeling mode, (**c**) negative half-cycle active mode, and (**d**) negative half-cycle freewheeling mode.

In addition to the load current:

$$i_L(t) = \frac{V_{dc} - V_g}{L}(t) \tag{10}$$

where V_g is the grid voltage.

Positive half-cycle freewheeling mode (mode 2): As represented in Figure 7b, the freewheeling branch is conducted in this mode and all the IGBTs of the bridge circuit are open circuited. Along with the switch S_7, four diodes (D_2, D_3, D_5, and D_6) are forward biased. Circulating freewheeling current flows via the path shown in Figure 7b. In this mode, inverter output voltage (V_{AB}) becomes zero, decreasing V_{AN} to half of the DC input voltage ($V_{DC}/2$) and increasing V_{BN} to half of the DC input voltage ($V_{DC}/2$). Thus, the common-mode voltage in freewheeling mode remains the same as that of the active mode, and stray capacitor voltage fluctuations are avoided. As a result, the leakage current is reduced. The common-mode voltage yields:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} \tag{11}$$

and the load current:

$$i_L(t) = \frac{-V_g}{L}(t) \tag{12}$$

Negative half-cycle active mode (mode 3): As in mode 1, four IGBTs conduct in this mode, as shown in Figure 7c. In this mode, the inverter output voltage (V_{AB}) becomes equal to the input DC voltage again, but the polarity is negative ($-V_{DC}$). This is because V_{AN} decreases to 0 and V_{BN} increases to the DC input voltage ($+V_{DC}$). Meanwhile, the common-mode voltage stays the same as the previous modes, $V_{DC}/2$. The load current

flows through the switches S_5, S_3, S_2, and S_6. It was observed that the switches S_5 and S_6 conduct in both the active modes. Thus, finally, the common-mode voltage yields:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(0 + V_{dc}) = \frac{V_{dc}}{2} \tag{13}$$

and the load current:

$$i_L(t) = \frac{V_{dc} - V_g}{L}(t) \tag{14}$$

Negative half-cycle freewheeling mode (mode 4): Similarly, to the previous freewheeling mode, inverter output voltage (V_{AB}) becomes zero in this mode too. This is because V_{AN} increases to $V_{DC}/2$ and V_{BN} decreases to $V_{DC}/2$. Along with the switch S_7, four diodes (D_1, D_4, D_5, and D_6) are forward biased. Circulating freewheeling current flows via the path shown in Figure 7d. It can be observed that the switches S_5 and S_6 are open circuited in both freewheeling modes. Common-mode voltage stays constant in this mode too, which yields:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} \tag{15}$$

where the load current:

$$i_L(t) = \frac{-V_g}{L}(t) \tag{16}$$

3.2. Conduction Modes under Non-Unity Power Factor

The power factor becomes less than 1 if the phases of the grid voltage and current do not match. There are eight conduction modes in total under the non-unity power factor, which are included in two periods known as the positive power region and the negative power region [24], as represented in Figure 8. In the positive power regions 1 and 2, power flows from the PV system to the grid. During the negative power regions 1 and 2, the inverter absorbs power from the grid.
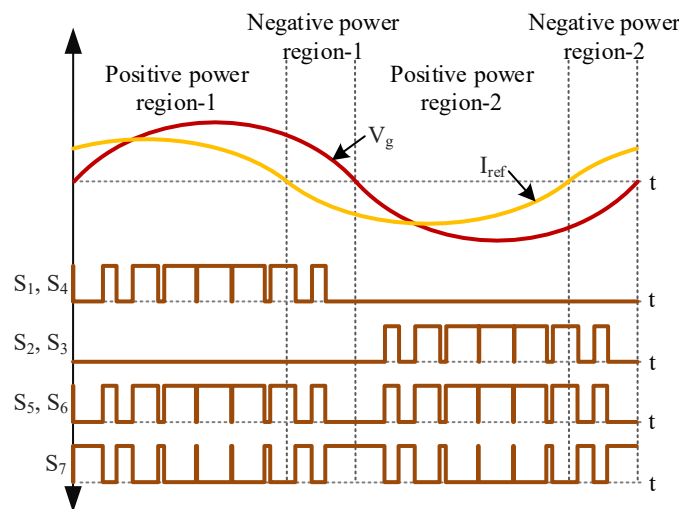

Figure 8. Different power regions and corresponding switching pulses.

Positive power region: This period contains four conduction modes, as represented in Figure 9a–d. In the positive power region 1, modes 1 and 2 simultaneously generate $+V_{DC}$ and 0. Likewise, in positive power region 2, modes 3 and 4 simultaneously generate $-V_{DC}$ and 0 again. Modes 2 and 4 are freewheeling modes and act to remove overflow of the leakage current. Here, modes 1 and 2 are the active modes.
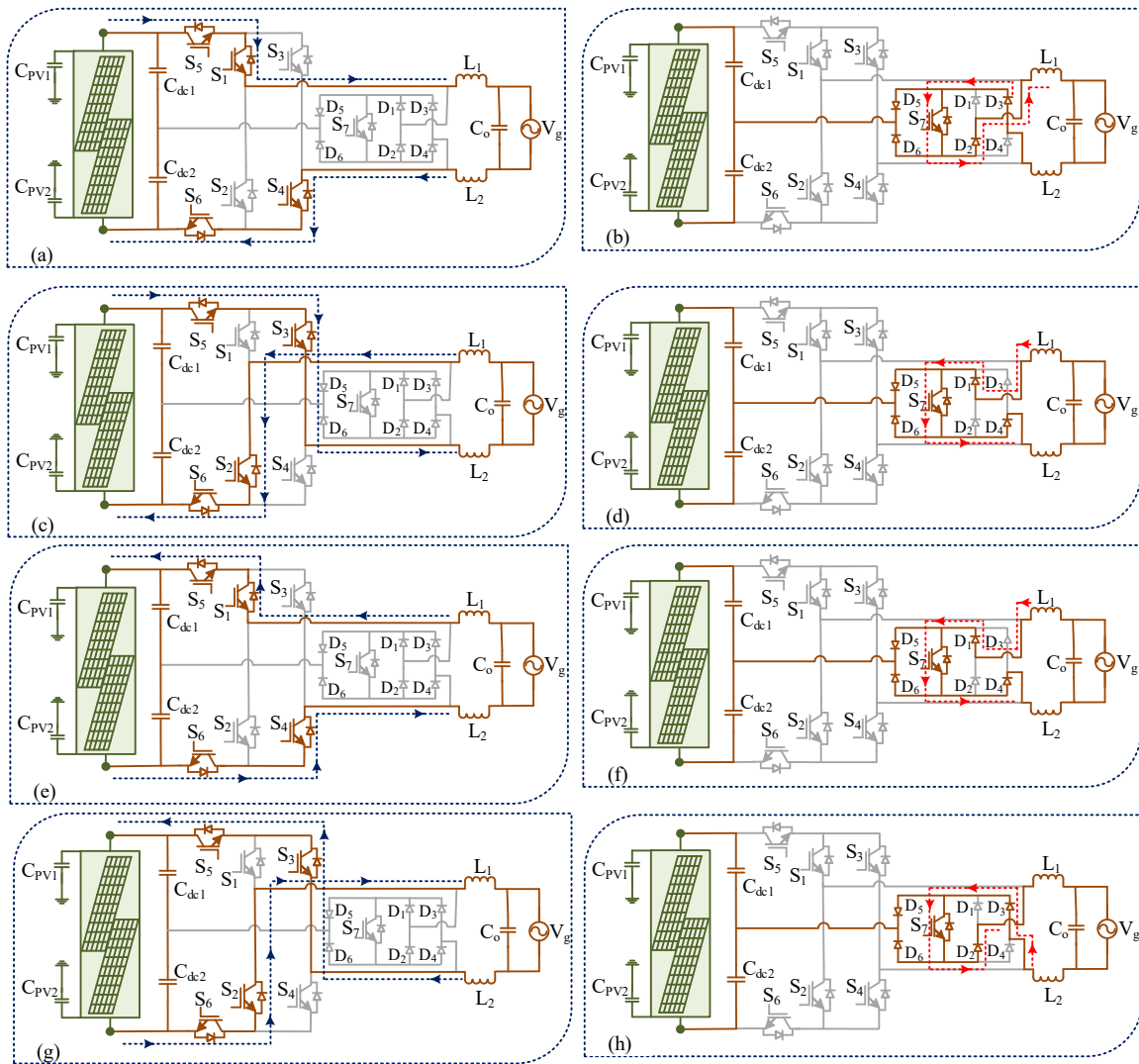
Figure 9. Conduction modes under non-unity power factor: (**a**) mode 1 ($V_{AB} = +V_{DC}$), (**b**) mode 2 ($V_{AB} = 0$), (**c**) mode 3 ($V_{AB} = -V_{DC}$), (**d**) mode 4 ($V_{AB} = 0$), (**e**) mode 5 ($V_{AB} = +V_{DC}$), (**f**) mode 6 ($V_{AB} = 0$), (**g**) mode 7($V_{AB} = -V_{DC}$), (**h**) mode 8 ($V_{AB} = 0$).

Negative power region: This period also contains four conduction modes, as depicted in Figure 9e–h. In negative power region 1, modes 5 and 6 simultaneously generate $+V_{DC}$ and 0. Likewise, in negative power region 2, modes 7 and 8 simultaneously generate $-V_{DC}$ and zero again. In the negative power region, power flows from the grid to PV system, which means the inverter consumes power in this mode.

4. Simulation Results

A simulation was conducted in the MATLAB/Simulink environment. The simulation parameters are listed in Table 1.

The MPPT controller was employed on the DC side to control the PV array voltage. Two 75 nF capacitors, connected to the DC side and ground, generated the parasitic capacitance (C_{PV}). Two 3 mH series inductors and a 2.2 uF capacitor were utilized as the LCL filter.

The output characteristics of the proposed transformer-less inverter are shown in Figure 10. The waveforms of V_{AN} and V_{BN} are depicted in Figure 10a,b, respectively. Figure 10c,d depict the waveforms of the common-mode voltage V_{CM} and differential-mode voltage V_{AB}, respectively. Figure 10c also provides a closer look of the V_{CM}. The oscillation of the common-mode voltage is not excessively high, which inhibits unnecessary

leakage current flow. Even at 0 output voltage, it remains constant. The grid voltage waveform is depicted in Figure 10e, where a THD of 1.25% was measured. As illustrated in Figure 10f, the grid current THD was recorded as 0.94%. The common-mode voltage was maintained at half of the DC input voltage in a steady manner. As a result, an 8.03 mA leakage current was measured, which is illustrated in Figure 10g.

Table 1. Simulation parameters.

Parameter Name	Symbol	Value
Input DC voltage	V_{DC}	400 V
Grid voltage	V_g	230 V/50 Hz
Maximum output power	P_{out}	2 kW
Switching frequency	f_s	20 kHz
DC link capacitor	C_{DC1} and C_{DC2}	940 uF
Parasitic capacitor	C_{pv1} and C_{pv2}	75 nF
Output filter inductor	L_1 and L_2	3 mH
Output filter capacitor	C_0	2.2 uF
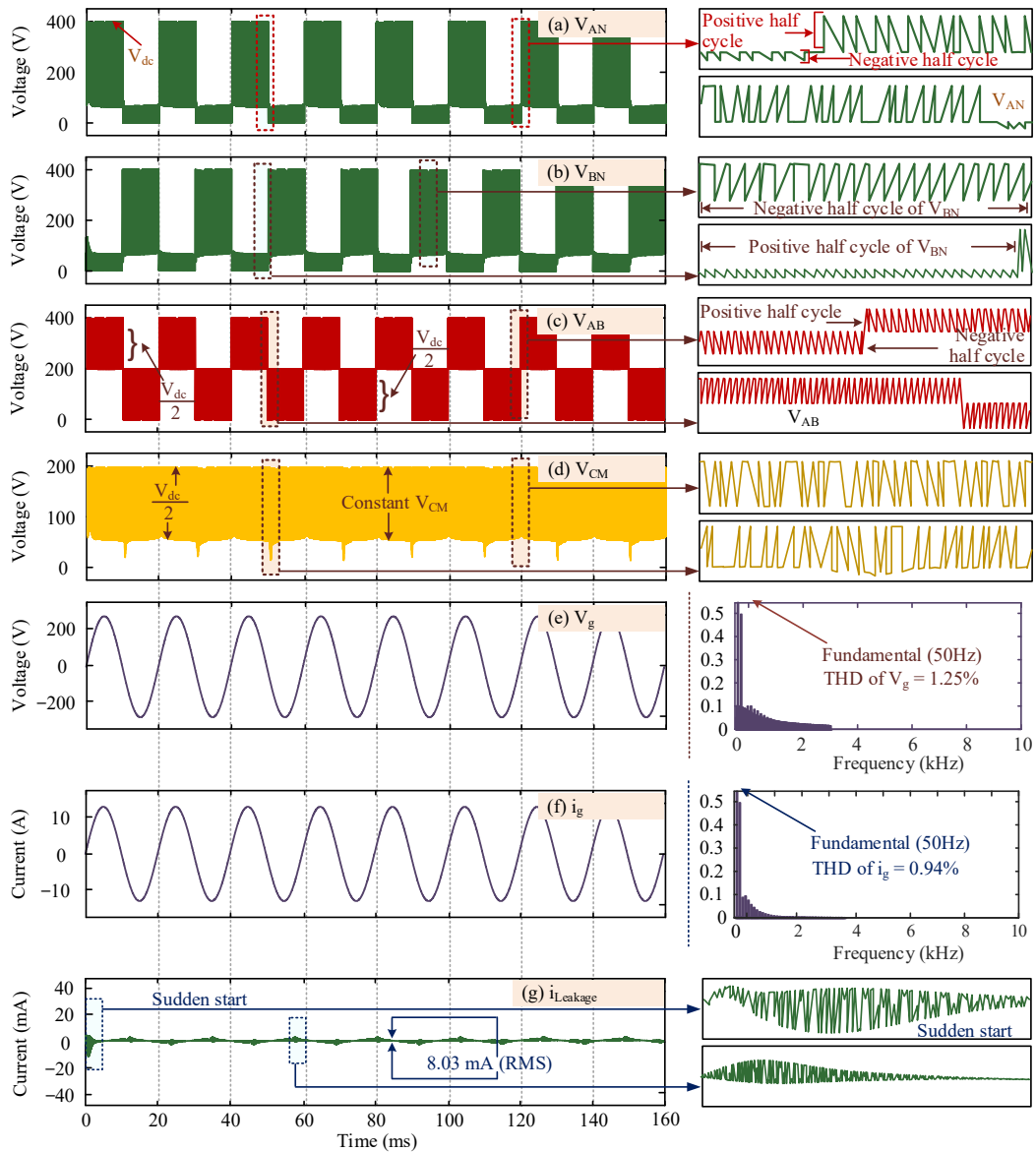
Figure 10. Simulation results for the proposed transformer-less inverter: (**a**) V_{AN}, (**b**) V_{BN}, (**c**) V_{CM}, (**d**) V_{AB}, (**e**) grid voltage V_g and its THD, (**f**) grid current ig and its THD, and (**g**) leakage current $i_{Leakage}$.

The grid voltage and current waveforms when changing the current reference in the current controller are depicted in Figure 11. As can be seen from Figure 11a, the grid voltage remained constant. In addition, the harmonics orders of the grid voltage were counted and 1.30% THD was found, which is very low. Figure 11b represents the grid current waveform, which was also constant. The harmonics orders of the grid current were also counted and 0.95% THD was found. Therefore, it can be said that the proposed transformer-less inverter offers promising performance in terms of leakage current, constant common-mode voltage, and THD for the grid voltage and grid current.
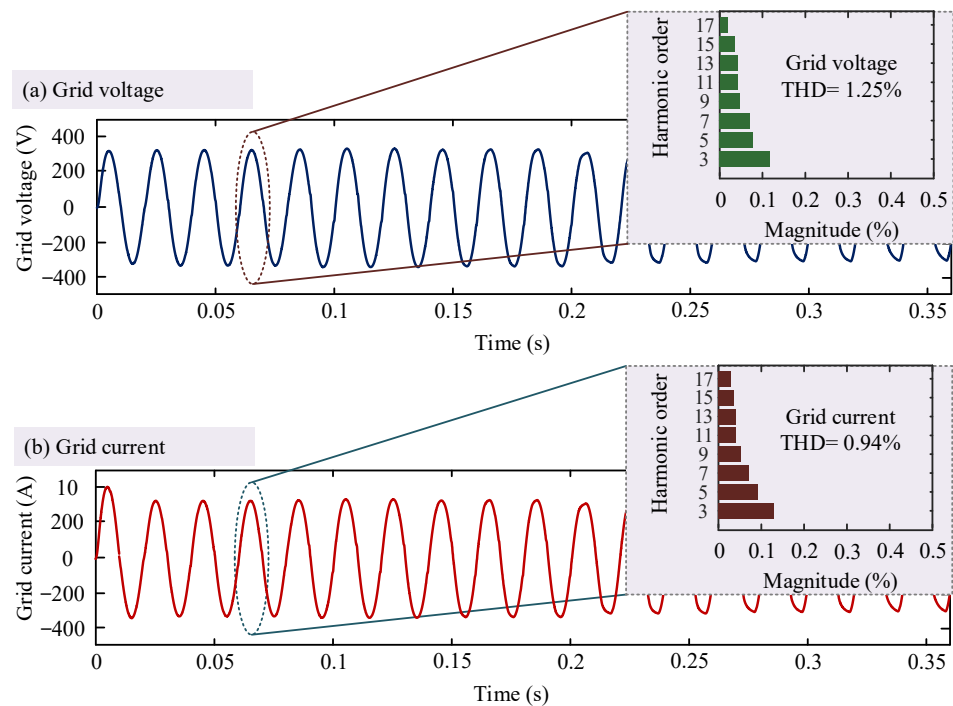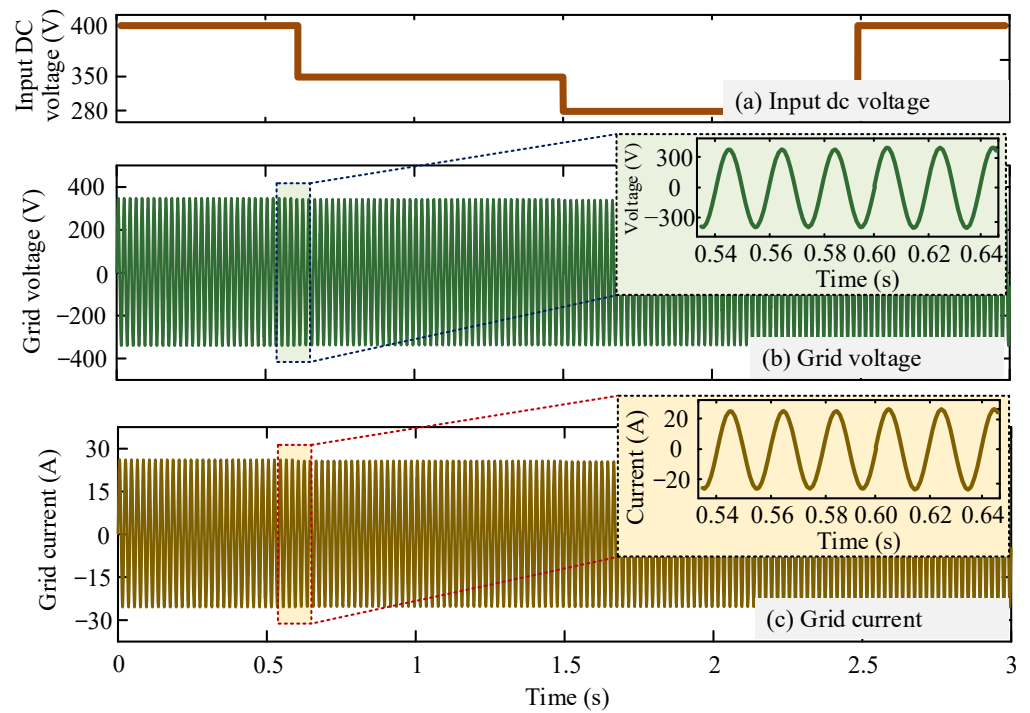

Figure 11. Grid voltage and current waveforms with the proposed transformer-less inverter and its harmonic counting after varying the current reference in the current controller: (**a**) grid voltage and its harmonic counting, (**b**) grid current and its harmonic counting.

Another test was performed to verify the inverter performance by varying the input DC voltage in the grid-connected mode. The test outcome is shown in Figure 12. The range of the input voltage variation should be around the voltage reference of the voltage controller. The grid voltage remained unchanged after applying dynamic input DC voltage, as seen in Figure 12a. Likewise, the grid current remained constant after applying dynamic input DC voltage, as seen in Figure 12b. Both waveforms are shown after zooming out.

The average voltage stresses over the switches were calculated according to Equation (17):

$$V_{IGBT} = \frac{1}{1 - \alpha} \times V_{dc} \tag{17}$$

where α is the firing angle of the gate pulse and V_{IGBT} is the voltage of the IGBT switch in conduction mode. The individual average voltage waveforms of the IGBTs, as well as the diodes used in the inverter topology, are depicted in Figure 13. Figure 13a–g represent the stress voltages of the IGBTs. Figure 13h–m illustrate the individual voltage waveforms of the diodes that are used in the proposed topology.

Figure 12. Grid voltage and current waveforms with step change of DC input voltage in grid-connected mode: (**a**) input DC voltage variation, (**b**) grid voltage V_g, (**c**) grid current i_g.
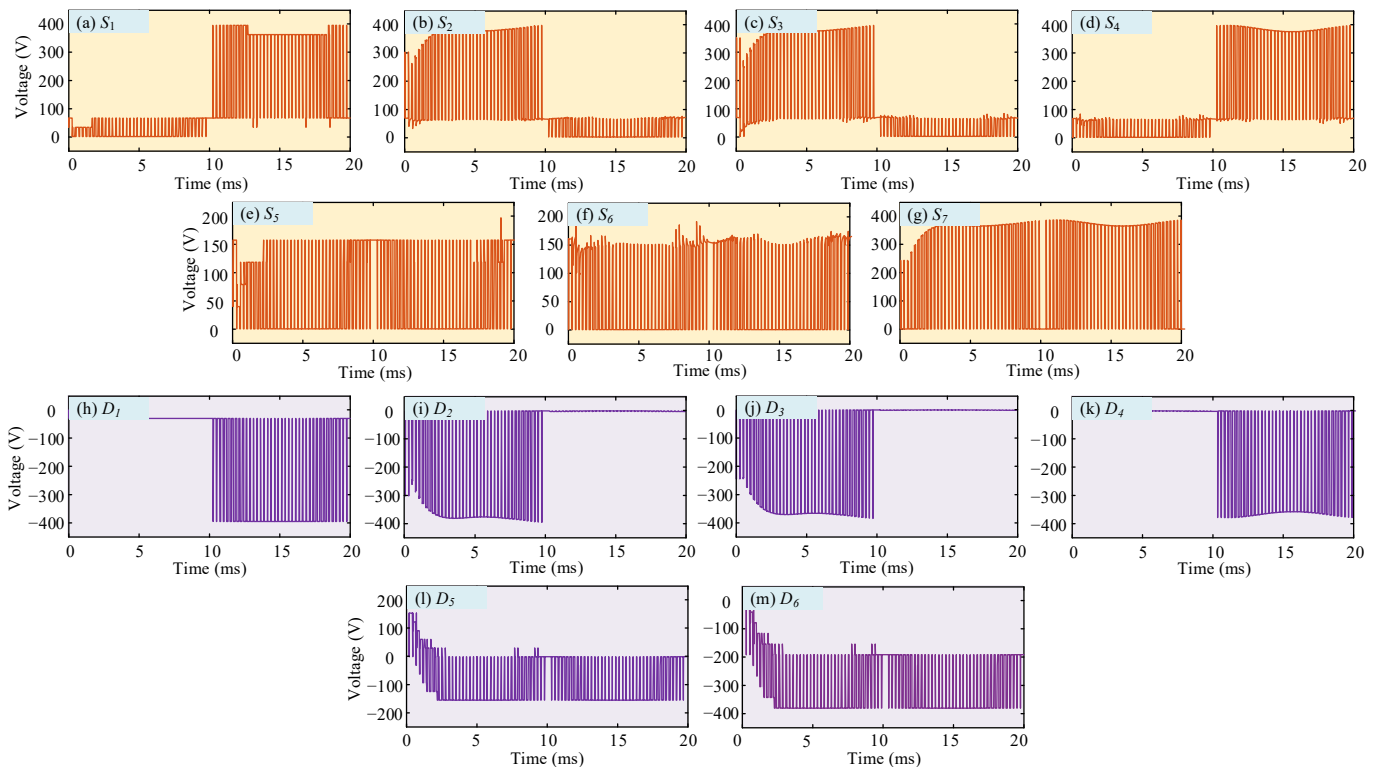
Figure 13. Stress voltage waveforms of the IGBTs and diodes used in the proposed transformer-less inverter: (**a**) S_1, (**b**) S_2, (**c**) S_3, (**d**) S_4, (**e**) S_5, (**f**) S_6, (**g**) S_7, (**h**) D_1, (**i**) D_2, (**j**) D_3, (**k**) D_4, (**l**) D_5, and (**m**) D_6.

To understand the weak signal behavior of the inverter control, a Bode plot analysis is presented. Figure 14 illustrates the Bode diagram of the control scheme of the proposed inverter topology. Figure 14a depicts the magnitude plot and Figure 14b represents the phase plot. The positive gain margin and positive phase margin indicate that the system is stable, as seen from Figure 14.
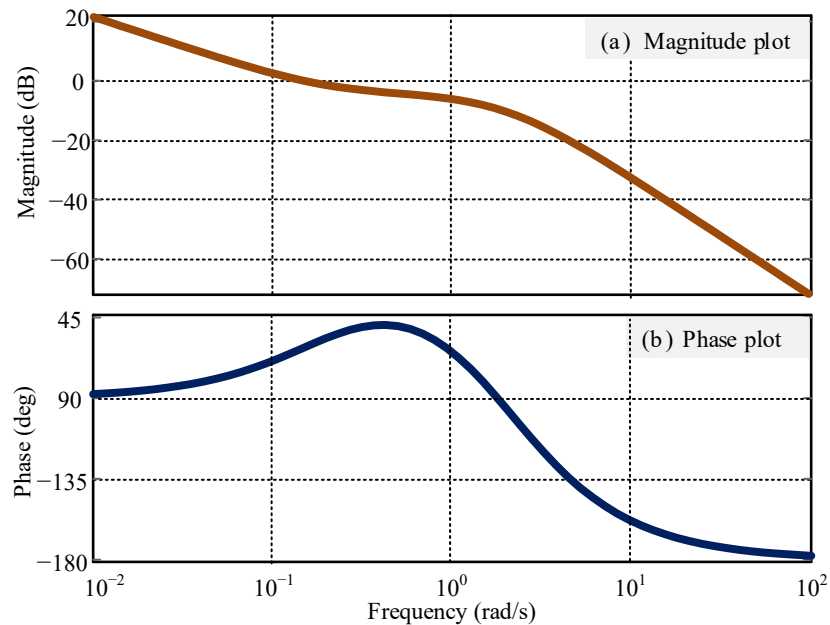
Figure 14. Bode diagram of the inverter controller: (**a**) Magnitude plot, (**b**) Phase plot.

The inverter efficiency was calculated using Equation (18) as follows:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{18}$$

The input and output power were calculated as follows [25]:

$$P_{in} = \frac{1}{T} \int_0^T V_{DC} I_{DC} dt \tag{19}$$

$$Pout = \frac{1}{T} \int_0^T Vg I_g dt \tag{20}$$

5. Experimental Results

An experiment was carried out using the parameters mentioned in Table 1. For this proposed inverter, 1.2 kV, 43 A HGTG11N120CND N-channel IGBTs with antiparallel hyper-fast diodes were utilized. The IGBTs used were the development type TA49291 and the antiparallel diodes used were the development type TA49189. An IXYS DSEE15-12CC superfast recovery (25 ns) dual diode module was considered for the diodes D_1, D_2, D_3, and D_4. For diodes D_5 and D_6, RHRP15120 hyper-fast diodes with soft recovery characteristics were utilized. The input DC voltage was generated by programming an AMETEK TerraSAS PV Simulator ETS 1000/10 at 1000 W/m² irradiance and 30 °C. A parasitic capacitor was employed to emulate the capacitance between the PV module and ground. An LEM CT 0.2-P current sensor was utilized for the leakage current measurement, which usually works on the flux gate principle. The presented controller was designed using the dSPACE MicroLabBox-based embedded platform. The onboard FPGA in the MicroLabBox was programmed with the real-time interface FPGA programming block sets.

KEYSIGHT N2791A differential voltage probes and Agilent N2781A differential current probes were utilized to collect the voltage and the current signals, respectively. To observe the voltage and current signals, a KEYSIGHT InfiniiVision DSOX4024A digital oscilloscope was employed.

Figure 15 represents the experimental waveforms of the steady-state response of the proposed H7 inverter. The waveforms of V_{AN}, V_{BN}, and V_{AB} are depicted in Figure 15a, and the waveforms of the grid voltage (V_g), grid current (i_g), common-mode voltage (V_{CM}), and leakage current ($i_{Leakage}$) are depicted in Figure 15b. Here, the grid voltage and grid current are in the same phase.
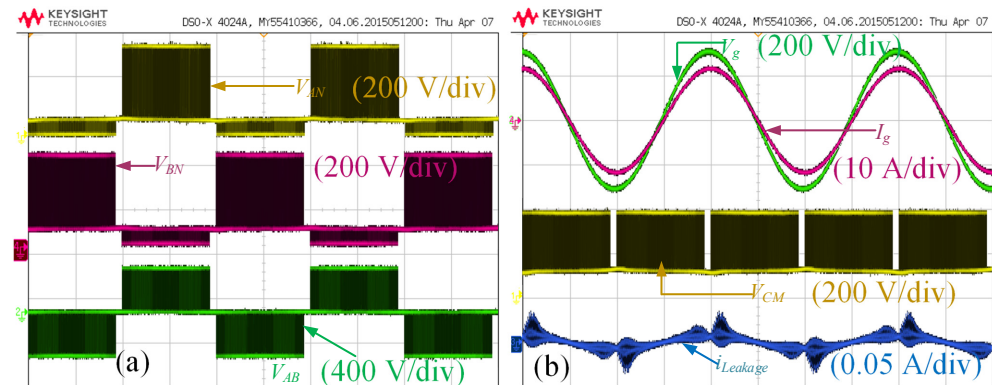
Figure 15. Steady-state response of the proposed inverter: (**a**) V_{AN}, V_{BN}, and V_{AB}; (**b**) grid voltage (V_g), grid current (i_g), common-mode voltage (V_{CM}), and leakage current ($i_{Leakage}$).

Figure 16 represents the experimental waveforms of the dynamic response of the proposed transformer-less inverter. Here, the DC input voltage was varied to observe the dynamic response of the inverter in grid-connected mode. As can be seen, the inverter output voltage V_{AB} was constant because of the voltage controller. Furthermore, the current controller also held the grid current (i_g) flow at a constant point. As a result, it is clear that the changes in input voltage did not affect the grid voltage or current as the inverter output voltage remained constant.
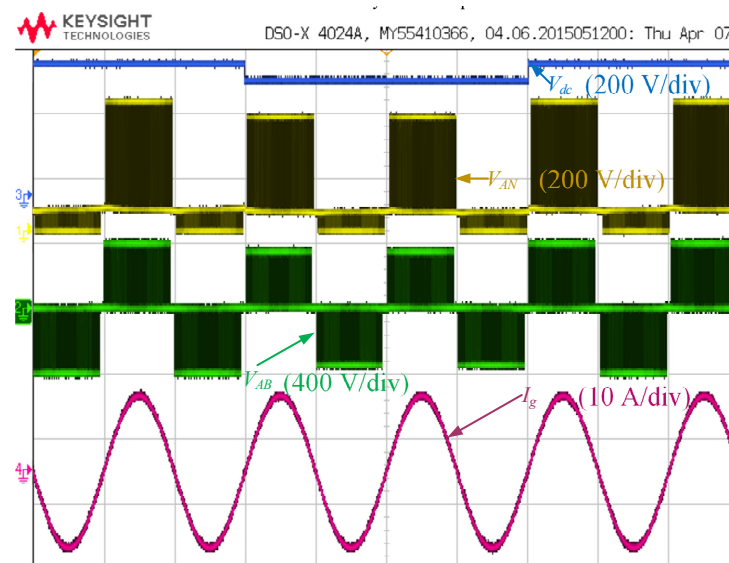
Figure 16. Dynamic response of the proposed transformer-less inverter with the step change in the DC input voltage.

6. Comparison with Other Existing Topologies

Table 2 shows a comparison of the proposed topology with various existing topologies in terms of common-mode voltage, switch counts, diode counts, leakage current, PWM pattern, grid current THD, and efficiency. The proposed transformer-less inverter provides constant common-mode voltage, which is highly important for reducing extensive leakage current flow. Constant common-mode voltage reduces stray capacitor voltage ripples and, therefore, leakage current is reduced. However, in the H5 and HERIC topologies, a floating-type CMV was noticed. The HBZVR topology provides a semi-floating type CMV. The proposed transformer-less inverter topology utilizes a unipolar SPWM technique to control the power switches, as in the other conventional topologies shown in Table 2. As can be seen from the table, the proposed transformer-less inverter had a leakage current of 8.03 mA (RMS), which is the lowest, whereas some of the topologies shown in Table 2 contain leakage currents greater than 50 mA. The HBZVR topology provides 74.4 mA leakage current; accordingly, HERIC, H5, and HBZVR-D topologies produce nearly 49 mA, 45 mA, and nearly 43 mA leakage currents. The oH5 topology provides 18 mA and the H6 topology provides 15.5 mA leakage currents. All these conventional topologies shown in Table 2 are established using the unipolar SPWM technique, which is efficient for lowering harmonics. The proposed transformer-less inverter also used unipolar SPWM technology to generate the gate pulses. Thus, this inverter injects fewer harmonics into the grid current and voltage. A 0.94% grid current THD was recorded, which is the lowest, whereas the other topologies have THDs greater than 1.5%. Both the HBZVR and HBZVR-D topologies have 1.9% THDs in the grid current. Likewise, the H5, oH5, HERIC, and H6 topologies provide 1.5% grid current THDs. The grid-connected inverter topologies mentioned in Table 2, as well as the proposed topology, are implemented for 50 or 60 Hz frequency systems. In addition, their switching frequencies are fixed at 20 kHz, which was also used in the proposed inverter to ensure a fair comparison. The filter configuration used in the inverter output side is the same for all topologies mentioned in Table 2, as well as the proposed one. Two inductors of 3 mH, as well as one capacitor of 2.2 uF, are used for the filter. Therefore, after ensuring all these test conditions, the lowest grid current THD is obtained with the proposed inverter, which indicates that the proposed topology is undoubtedly efficient for mitigating the harmonics. Now, in terms of the inverter losses, the proposed inverter topology is more efficient than any other topology, with an efficiency of 97.93%, as depicted in Table 2. Finally, it can be said that, in terms of leakage current flow and grid current THD, the proposed transformer-less inverter is more efficient and superior compared to the other existing topologies.

Table 2. Comparison of the proposed transformer-less inverter with existing topologies.

Topology Name	H5 [11]	oH5 [12]	HERIC [13]	H6 [14]	HBZVR [14]	HBZVR-D [14]	Proposed
Number of IGBTs	5	6	6	6	5	5	7
Number of diodes	0	0	0	2	5	6	6
PWM pattern	Unipolar SPWM	Unipolar SPWM	Unipolar SPWM	Unipolar SPWM	Unipolar SPWM	Unipolar SPWM	Unipolar SPWM
CMV	Floating (~200 V)	Constant	Floating (~200 V)	Constant	Semi-floating (~200 V)	Constant	Constant
Leakage RMS current (mA)	45	18	48.8	15.5	74.4	42.7	8.03
Grid current THD (%)	1.5	1.5	1.5	1.5	1.9	1.9	0.94
Efficiency (%)	97.59	97.55	98.16	97.24	97.65	97.88	97.93

7. Conclusions

This paper proposes a new single-phase transformer-less PV inverter that can achieve better performance in terms of common-mode voltage, leakage current, THD, and efficiency. The proposed transformer-less inverter produces a constant common-mode voltage, which is required for leakage current suppression. The leakage current was measured as 8.03 mA,

which is lower than those of existing transformer-less inverter topologies. Smooth dynamic behavior was achieved for the proposed transformer-less inverter, as shown by both the simulation and experimental results, which is a very important feature for a grid-tied inverter. The harmonic orders of the grid voltage and current were also counted. The magnitudes of the lower-order odd harmonic components were very low, which led to less distortion. The grid voltage and current THD for the proposed transformer-less inverter were recorded as 1.25% and 0.94%, which are lower than those of existing transformer-less inverter-based PV systems. As well as these, the proposed transformer-less inverter offers 97.93% efficiency, which is also lower than that of existing counterparts. Therefore, it can be concluded that the proposed inverter is highly suitable for single-phase grid-tied PV applications.

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