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Five-level F-type inverter with buck-boost converter-based equalization channels



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Abstract Multilevel inverters have been widely used in various applications, as they provide output voltage with better quality, lower dv/dt , and lower Total Harmonic Distortion (THD). Multilevel inverter such as Neutral Point Clamped (NPC) inverter uses a large number of semiconductor devices (IGBTs and diodes) which negatively affects the inverter cost and efficiency. Recently, a three-level (3L) F-type inverter has been proposed with lower switch voltage stresses, cost, and losses compared to 3L T-type and NPC inverters. This paper proposes a five-level (5L) F-type inverter as an extension for the 3L F-type inverter. Like a 5L NPC inverter, the voltages of the involved dc-link capacitors should be kept at a certain voltage level. To achieve that, buck-boost converter-based Equalization Channels (ECs) are employed. To show the pros and cons of the 5L F-type inverter, a comparison between the proposed inverter and other existing multilevel inverters has been held. The numerical assessment also shows that the proposed architecture has a lower kVA rating and losses than the conventional 5L NPC inverter. Finally, different Simulation and experimental results of the proposed 5L F-type inverter are presented. The presented results show the viability of the proposed converter.

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1. Introduction

Voltage source converters (VSCs) are crucial in various applications such as motor drives, renewable energy, electric transportation, HVDC and Flexible AC transmission and active power filters ... etc. [1–13]. Two-level VSC [14] is the most

common type of VSCs in different industrial applications, but it has high dv/dt at its output terminals, and its semiconductor devices are rated at the full dc voltage. As voltage-level/power-level increases, the multi-level inverter is recommended as it has reduced voltage derivatives (dv/dt), lower harmonic content, and higher efficiency [15–22].

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Generally, the multilevel VSC (3L, 5L, .. etc.) has a staircase output voltage wave with several levels, which can be generated with the help of the involved dc capacitors. One of the multilevel VSC challenges is the voltage unbalance between different levels (i.e., voltage unbalance between the involved dc capacitors). As a solution, some types use extra hardware equalization circuits/channels [23] to ensure operating with balanced capacitors voltages.

Different types of multilevel VSCs have been highlighted in literature. The main conventional types are neutral point clamped multilevel VSC, flying capacitor multilevel VSC, and cascaded H-bridge multilevel VSC [24]. The neutral point clamped multilevel inverter needs excessive clamping diodes when the number of levels is high [24]. Flying capacitor multilevel converter also needs an excessive number of dc capacitors when the number levels are high [24]. In addition, the converter with a high number of levels will have complicated control, and it will be difficult to package and be more expensive [24]. The main drawback of the cascaded H-bridge multilevel VSC is that it has no common dc-link and needs separate dc sources for real power conversions, making it suitable for limited applications. Three-level T-type inverter [25] is an extension of conventional two-level VSC, where an additional bidirectional switch is connected between the mid-point of the inverter leg and the mid-point of dc-link capacitors to add the possibility of having a zero-voltage state at the output terminals, i.e., the 3L output voltage can be generated successfully.

On the other hand, the modular multilevel converter (MMC) [26] is a promising converter for medium-/high-voltage high-power applications, but it has a lot of current and voltage measurements. MMC needs a higher number of semiconductor devices, and its control is complex, especially at a high number of levels.

In [27], a 5L E-type inverter has been proposed for grid-connected applications. The proposed architecture consists of four dc capacitors and eight IGBTs per leg. The voltages of involved dc capacitors are balanced and bounded in a certain voltage window with the help of series resonant balancing circuits (SRBCs).

Recently 3L F-type has been proposed [28], where it provides dc-ac conversion with reduced losses, higher efficiency, and lower cost compared to the conventional T-type converter [25] in low-/medium-voltage systems. This paper presents an extension to the recently published 3L F-type inverter, where a 5L converter is proposed along with buck-boost converter-based equalization channels [23] to ensure voltage balancing of the involved dc capacitor.

The main limitation of the proposed 5L F-type inverter is that the highest possible operating voltage of the proposed converter depends on the highest available voltage rating of semiconductor devices in the market. This makes the proposed converter suitable for low-voltage to medium-voltage applications (rated at few kVs). The proposed concept can be employed with higher voltages, however, series-connected devices should be employed to implement high-voltage switches. Nevertheless, proper active gate control should be applied to ensure operating with successful dynamic voltage sharing among the involved series-connected devices, increasing the system's complexity.

In the presented work, single-phase and three-phase of the proposed 5L F-type inverters are presented, along with the

detailed operational concept and sinusoidal pulse width modulation (SPWM) of both versions. The proposed 5L inverter is compared with the conventional 5L neutral-point clamped (NPC) inverter for assessment. Like the proposed 5L F-type inverter, the 5L NPC inverter needs equalization channels to ensure operating with balanced capacitors voltages. The assessment shows the superiority of the proposed 5L F-type inverter over the conventional 5L NPC inverter, where it has lower losses and a lower kVA rating for the involved semiconductor devices. Simulation results for single-phase and three-phase versions are presented. The results are promising and show the viability of the suggested approach. Finally, an estimation of proposed converter losses is presented compared to the conventional 5L NPC to show the advantages of the proposed approach.

The main contributions and novelty of the presented work are summarized as follows:

- 5L F-type inverter is proposed as an extension to the recently published 3L F-type inverter, where the proposed 5L F-type inverter has a lower kVA rating and lower losses compared to the conventional 5L inverters such as the NPC.
- A multilevel modulation technique is presented for the proposed 5L F-type inverter.
- Single-phase and three-phase versions for the proposed 5L F-type inverter are presented.
- Buck-boost converter-based equalization channels are suggested to ensure operating with balanced dc-link capacitor voltages, i.e., to avoid energy drift between the involved DC capacitors during the dc-ac conversion process.

2. Three-level F-type inverter

Fig. 1 shows the recently proposed single-phase 3L F-type inverter [28], consisting of two dc capacitors rated at $V_{dc}/2$

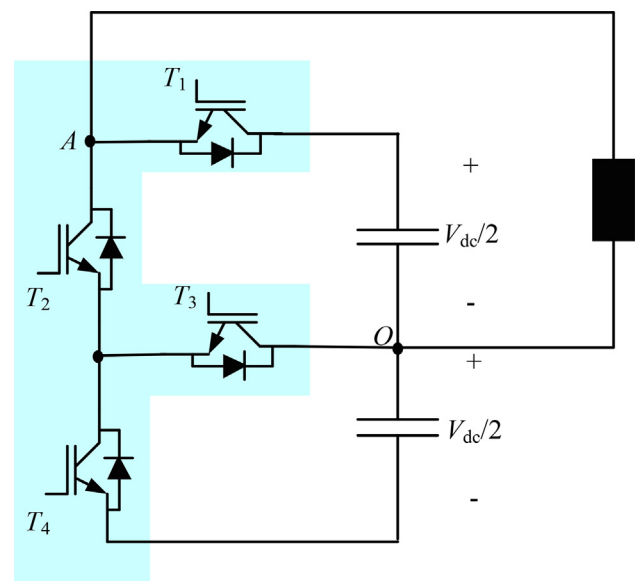


Fig. 1 3L F-type inverter [28].

and four IGBTs. The transistor T_1 is rated at V_{dc} , while T_2 , T_3 , and T_4 are rated at $V_{dc}/2$, where V_{dc} is the input dc voltage. Three voltage levels can be generated successfully across the load from the 3L F-type inverter, which are $+V_{dc}/2$, 0, and $-V_{dc}/2$, where the load is connected between points A and O , as shown in Fig. 1. Table 1 shows the switching states of the shown single-phase 3L F-type inverter and its corresponding output voltage, v_o . While Fig. 2 shows the equivalent circuit of each switching state.

Multilevel pulse-width modulation techniques such as the phase disposition (PD) technique can be employed to identify which of the aforementioned switching states to be activated with the variation of ac output voltage reference, as by comparing the carriers with the reference, three signals (p , z , and n) can be generated as shown in Fig. 3.

The signal p will be high when a positive output voltage is generated, while signal n will be high when a negative output voltage is generated. Finally, signal z will be high when zero

Table 1 Switching states of single-phase 3L F-type inverter.

Switching state	IGBTs				v_o
	T_1	T_2	T_3	T_4	
Positive state	1	0	1	0	$+V_{dc}/2$
Zero state	0	1	1	0	0
Negative state	0	1	0	1	$-V_{dc}/2$

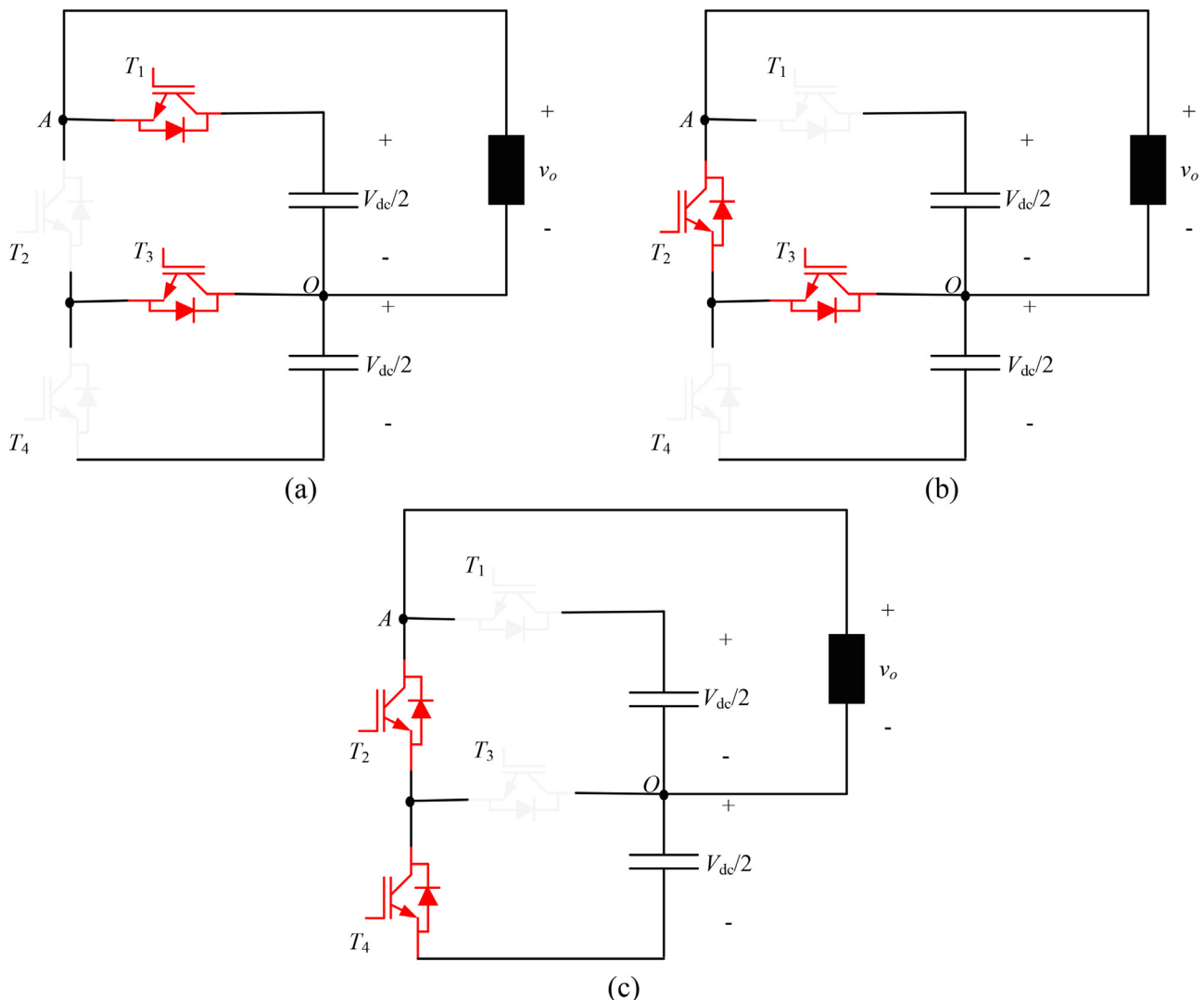


Fig. 2 switching states of single-phase 3L F-type Inverter. (a) positive state, (b) zero state, and (c) negative state.

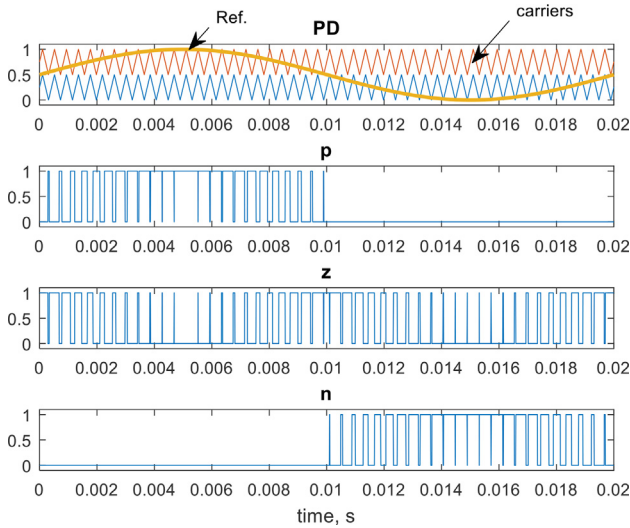


Fig. 3 Phase Disposition (PD) modulation for gate pulses generation of 3L F-type inverter at amplitude modulation index $m_a = 1$ and frequency modulation index $m_f = 48$.

output voltage is generated across the load. These signals (p , n , and z), shown in Fig. 3, are employed to generate the gate pulses of the involved switches. As with the help of Table 1, the gate pulses of the involved IGBTs are given by (1), and the corresponding normalized AC output voltage is shown in Fig. 4, where 3L AC output voltage is generated successfully.

$$T_1 = p, T_2 = z + n, T_3 = p + z, T_4 = n \quad (1)$$

3. The proposed Five-level F-type inverter

In this section, a single-phase 5L F-type inverter is proposed as an extension of the aforementioned single-phase 3L F-type inverter. The proposed single-phase 5L F-type inverter is shown in Fig. 5. The AC load is connected between points A and O . The proposed inverter has five voltage levels that can be applied across the load (v_o). It has two positive states, p_1 and p_2 , where a voltage of $+V_{dc}/2$ and $+V_{dc}/4$ are applied across the load, respectively. The zero state, z , where zero volt-

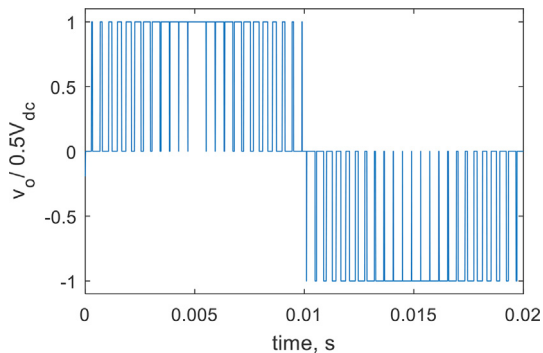


Fig. 4 The corresponding normalized AC output voltage of the 3L F-type inverter.

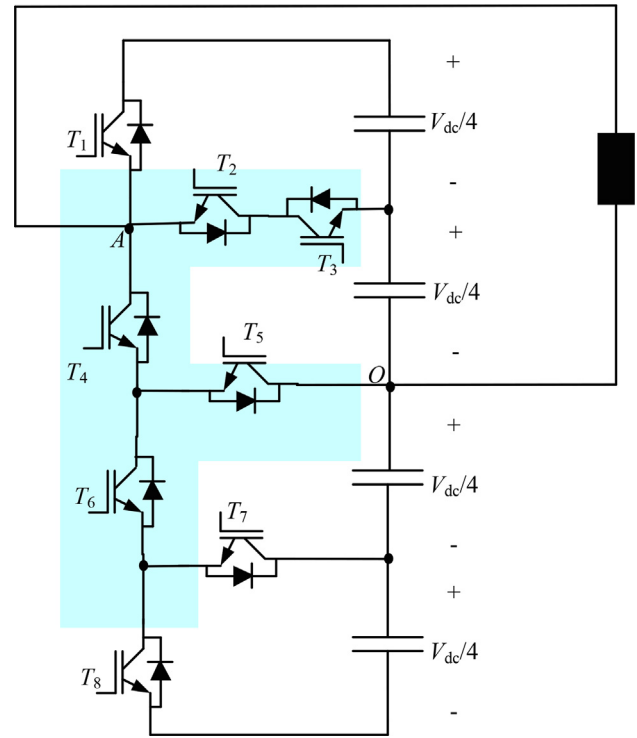


Fig. 5 The Proposed single-phase 5L F-type Inverter.

age is applied across the load. Finally, the two negative states, namely, n_1 and n_2 , where $-V_{dc}/4$ and $-V_{dc}/2$ are applied across the load, respectively. Table 2 shows the switching states and the corresponding output voltage (v_o) of the single-phase 5L F-type inverter shown in Fig. 5, while Fig. 6 shows the equivalent circuit of each switching state. It has to be noted that, like conventional NPC inverters, equalization circuits should be employed to ensure operating with balanced capacitor voltages. These equalization circuits are not shown in Fig. 5 and will be covered in detail in the later sections.

The proposed single-phase 5L F-type inverter, shown in Fig. 5, consists of four dc capacitors rated at $V_{dc}/4$ and eight IGBTs where the voltage ratings of the involved IGBTs are listed in Table 3. Five voltage levels can be generated successfully across the load from the proposed 5L F-type inverter, $+V_{dc}/2$, $+V_{dc}/4$, 0 , $-V_{dc}/2$, and $-V_{dc}/2$, which represent the p_1 state, p_2 state, z state, n_1 state, and n_2 state respectively as shown in Fig. 6. It has to be noted that some IGBTs are turned-on during the different aforementioned switching

Table 2 Switching states of single-phase 5L F-type inverter.

Switching state	IGBTs								v_o
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	
Positive state 1	1	0	0	0	1	0	1	0	$+V_{dc}/2$
Positive state 2	0	1	1	0	1	0	1	0	$+V_{dc}/4$
Zero state	0	0	0	1	1	0	1	0	0
Negative state 1	0	0	0	1	0	1	1	0	$-V_{dc}/4$
Negative state 2	0	0	0	1	0	1	0	1	$-V_{dc}/2$

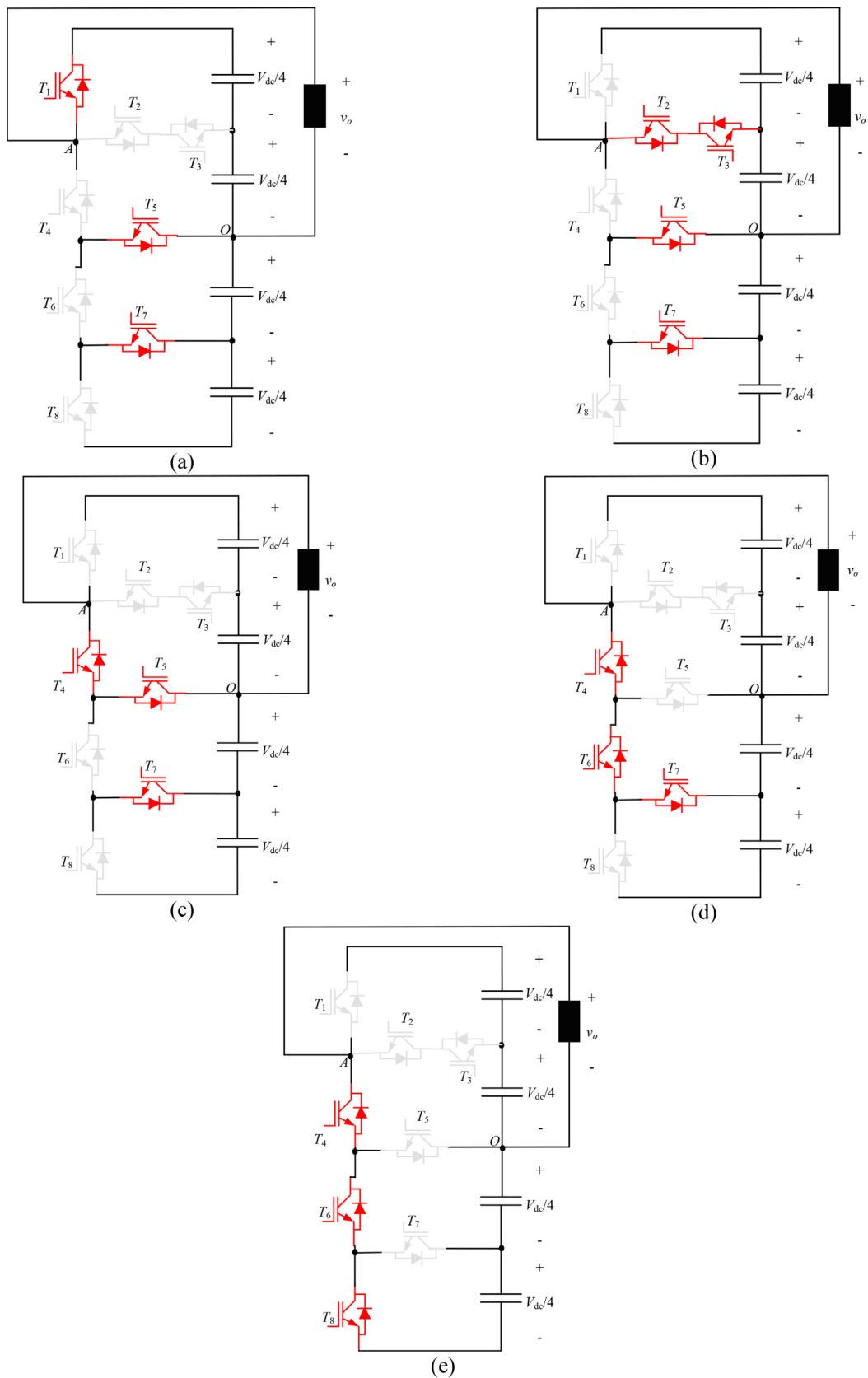


Fig. 6 Switching states of the proposed single-phase 5L F-type inverter. (a) p_1 state, (b) p_2 state, (c) z state, (d) n_1 state and (e) n_2 state.

Table 3 IGBTs voltage rating of the proposed single-phase 5L F-type inverter.

IGBT	Voltage rating
T_1	V_{dc}
T_2	$3V_{dc}/4$
T_4, T_5	$V_{dc}/2$
T_3, T_6, T_7, T_8	$V_{dc}/4$

states, shown in Table 2, to clamp the capacitor voltages at certain voltage levels.

PD modulation technique is employed to identify which of the aforementioned switching states to be activated with the variation of ac output voltage reference, as by comparing the carriers with the reference, five signals ($p_1, p_2, z, n_1,$ and n_2) can be generated as shown in Fig. 7. The signals p_1 and p_2 will be high when $+V_{dc}/2$ and $+V_{dc}/4$ output voltages are generated, respectively, while signals n_1 and n_2 will be high when $-V_{dc}/4$ and $-V_{dc}/2$ output voltages are generated, respectively. Finally, the signal z will be high when zero output voltage is generated across the load.

These signals ($p_1, p_2, z, n_1,$ and n_2), shown in Fig. 7, are employed to generate the gate pulses of the involved switches. As with the help of Table 2, the gate pulses of the involved IGBTs are given by (2), and the corresponding normalized AC output voltage is shown in Fig. 8, where 5L AC output voltage is generated successfully.

$$\begin{aligned} T_1 &= p_1, T_2 = p_2, T_3 = p_2, T_4 = z + n_1 + n_2, \\ T_5 &= p_1 + p_2 + z, T_6 = n_1 + n_2, \\ T_7 &= p_1 + p_2 + z + n_1, T_8 = n_2 \end{aligned}$$

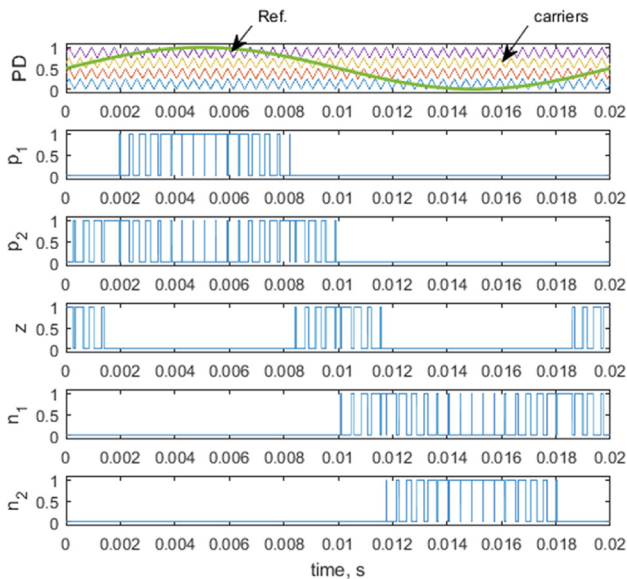


Fig. 7 Phase Disposition (PD) modulation for gate pulses generation of single-phase 5L F-type inverter at amplitude modulation index $m_a = 1$ and frequency modulation index $m_f = 48$.

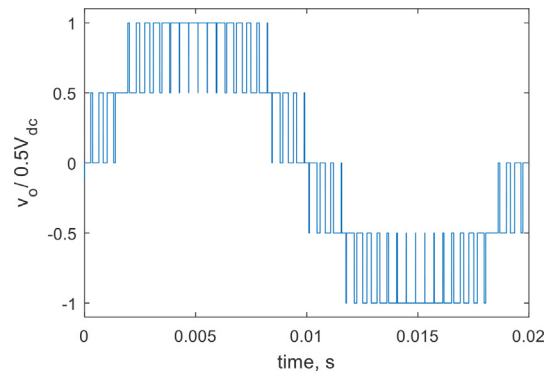


Fig. 8 The normalized AC output voltage of the proposed single-phase 5L F-type inverter.

4. Three-phase five-level F-type inverter

The three-phase version of the proposed configuration is shown in Fig. 9, where three identical legs are employed, and the three-phase load is connected to the converter legs at points $A, B,$ and C assuming a star-connected load. In the three-phase version, the same modulation technique presented in section 3 is applied but with shifted references, as shown in Fig. 10, where each voltage reference is compared with the carrier signals to extract (p_1, p_2, z, n_1, n_2) signals of each phase as presented in Fig. 7. Then with the help of equation (2), these signals are used to generate the gate pulses for semiconductor devices of each phase. It has to be noted that, like conventional 5L NPC inverter, to ensure operating with balanced capacitor voltages, buck-boost converter-based equalization circuits should be employed [23]. This part will be covered in detail in the following section. The equalization circuits/channels are not shown in Fig. 9 for simplicity. Fig. 11 shows the corresponding normalized generated phase voltages.

5. Buck-boost converter-based equalization circuits

To ensure operating with balanced capacitors voltages, equalization circuits should be employed with the proposed 5L F-type inverter. Buck-boost converter-based equalization circuits [23] are used in the presented work, where two equalization circuits are used, one for the upper capacitors and one for the lower capacitors, as shown in Fig. 12. Each converter operates as an energy channel to transfer the energy between their capacitor, where the energy is transferred from the higher voltage capacitor to the lower voltage capacitor through this equalization circuit/channel. This can be done by operating the switches of the buck-boost converter with a 50 % duty cycle under continuous conduction mode to keep operating with equal voltages at the upper or lower capacitors.

The relation between the buck-boost converter's input and output voltages under continuous conduction mode is given by (3).

$$V_o = DV_i / (1 - D) \quad (3)$$

Where D is the duty cycle, V_i and V_o are the input and output voltages of the buck-boost converter, respectively. Based on Eq. (3), for a 50 % duty cycle, the input and output voltages

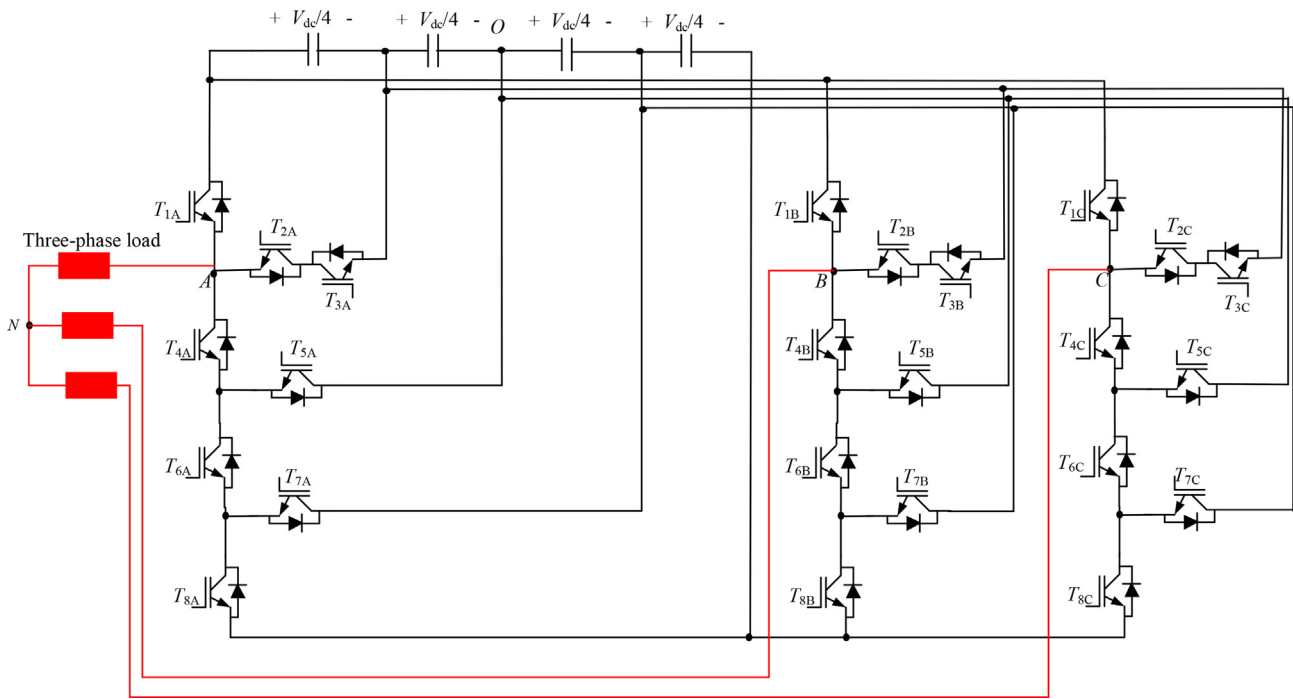


Fig. 9 The proposed three-phase 5L F-type inverter.

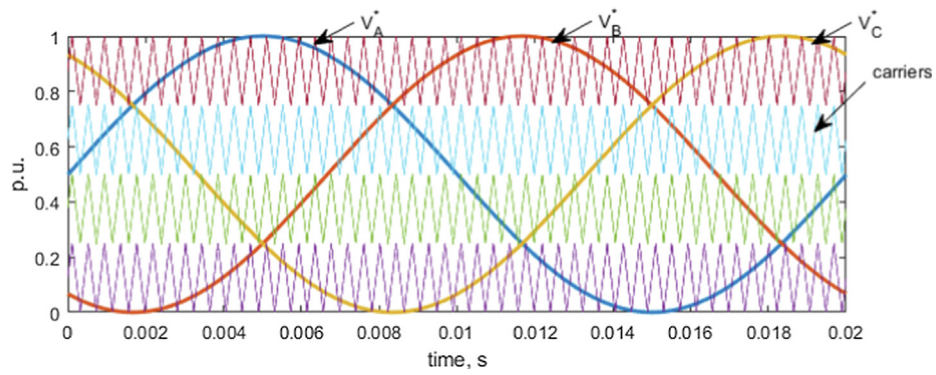


Fig. 10 PD modulation technique for three-phase 5L F-type inverter.

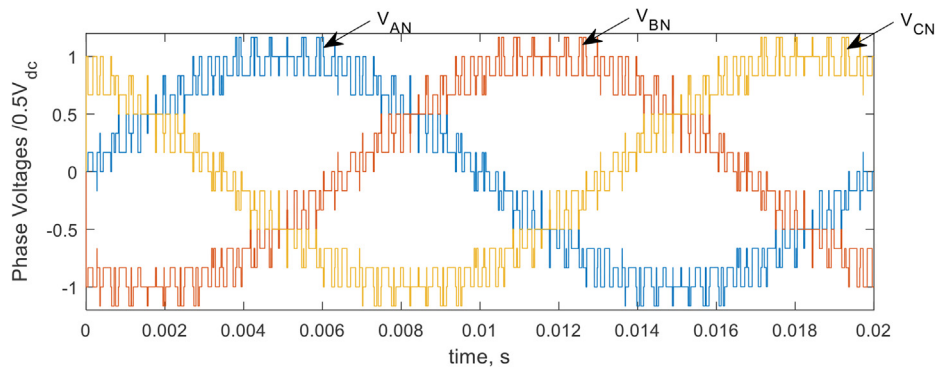


Fig. 11 The normalized three-phase phase voltages of the proposed three-phase 5L F-type inverter.

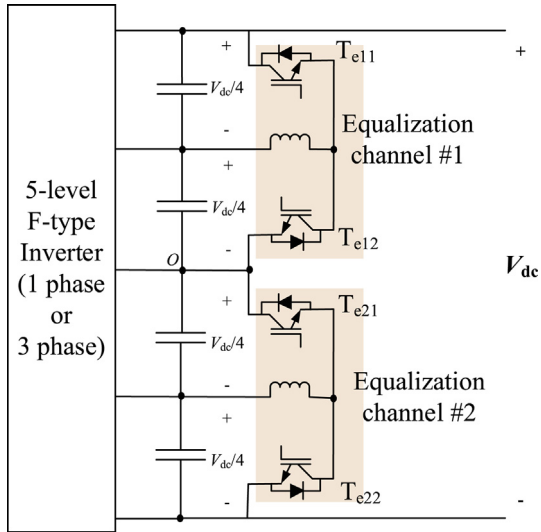


Fig. 12 Equalization channels of the proposed single-/three-phase 5L F-type inverter.

Table 4 Simulation parameters of the Proposed 5L F-type inverter.

Parameters	Value
Inverter leg	
DC input voltage	200 V
DC-link capacitances	10 mF
AC load impedance	$10 \sqrt{2} \angle 45^\circ \Omega$ (inductive load)
Amplitude modulation index, m_a	1
Frequency modulation index, m_f	48
AC output fundamental frequency	50 Hz
Modulation technique	Phase disposition (PD)
Equalization channel (Buck-boost converter)	
Inductance	10 mH
Switching frequency	5 kHz
Duty cycle	50 %

of the buck-boost converter can be kept at the same voltage level, i.e., the upper two dc capacitors are kept equal at the same voltage level. Similarly, for the lower two dc capacitors, they are kept equal by employing another equalization channel for them, as shown in Fig. 12.

6. Simulation

Two simulation models have been built to check the performance of the proposed architecture. One model for the one-leg single-phase inverter and the other for the three-legs three-phase version. The simulation parameters are given in Table 4. The aforementioned modulation techniques for

single-phase and three-phase versions, shown in Figs. 7 and 10, are employed to generate the gate pulses of the involved semiconductor devices with the help of Eq. (2). It has to be noted that in both models, the voltages of the involved dc capacitors are kept balanced at the same voltage level by employing the aforementioned buck-boost converter-based equalization channels. Figs. 13-18 show the corresponding simulation results for the single-phase version, while Fig. 19 shows the simulation results of the three-phase version.

Fig. 13a shows the AC output voltage, where 5L voltage is generated successfully with a magnitude of $V_{dc}/2$ at $m_a = 1$. This voltage is applied across the inductive load, and the corresponding AC output current is shown in Fig. 13b, where the sinusoidal output current passes through the load. Fig. 13c shows the voltages of the involved dc capacitors, where they are kept at the same voltage level at $V_{dc}/4$ (50 V), thanks to the employed buck-boost converter-based equalization channels. The corresponding inductors currents of the involved buck-boost converters are shown in Fig. 13f, while the currents of dc capacitors are shown in Fig. 13e. The input dc current is shown in Fig. 13d, where oscillatory current with double the grid frequency (100 Hz) is drawn from the dc source due to the oscillatory power in case of single-phase systems.

Fig. 14 shows the currents of involved switches in the inverter leg during one complete cycle. The leg contains eight switches (sw_1 to sw_8). Each switch consists of IGBT and an anti-parallel diode where the positive switch current passes through IGBT while the negative switch current passes through the anti-parallel diode. Based on 14, it is clear that the proposed operation is safe, and no switch suffers from current stresses. On the other hand, Fig. 15 shows the voltage across the involved IGBTs (T_1 to T_8) during one complete cycle. It is clear that the transistors' voltages are well-clamped, where one IGBT is rated at V_{dc} , one at $3V_{dc}/4$, two at $V_{dc}/2$, and four at $V_{dc}/4$.

The variation of output voltage THD (THD_v) and output current THD (THD_i) versus the variation of amplitude modulation index (m_a) for the proposed 5L F-type inverter, and the conventional 5L NPC are shown in Fig. 16. The results show the superiority of the proposed converter. On the other hand, for the same load impedance magnitude at unity amplitude modulation index ($m_a = 1$), the variation of output current THD (THD_i) of the proposed 5L F-type inverter versus the load power factor is shown in Fig. 17.

To check the effect of load power factor on the equalization process, different tests are examined, where different power factors are assumed, namely, 0.1, 0.5, and 0.9 lagging power factors. The corresponding capacitors voltages variations for these three scenarios are shown in Fig. 18, where the results show that thanks to the employed equalization channels, the capacitors' voltages are kept balanced at the different defined power factors.

For the three-phase 5L F-type inverter assuming a three-wire star-connected load, Fig. 19a shows the output phase voltages (V_{AN} , V_{BN} , and V_{CN}), where N is the neutral point of the star-connected load. Three-phase voltages are generated

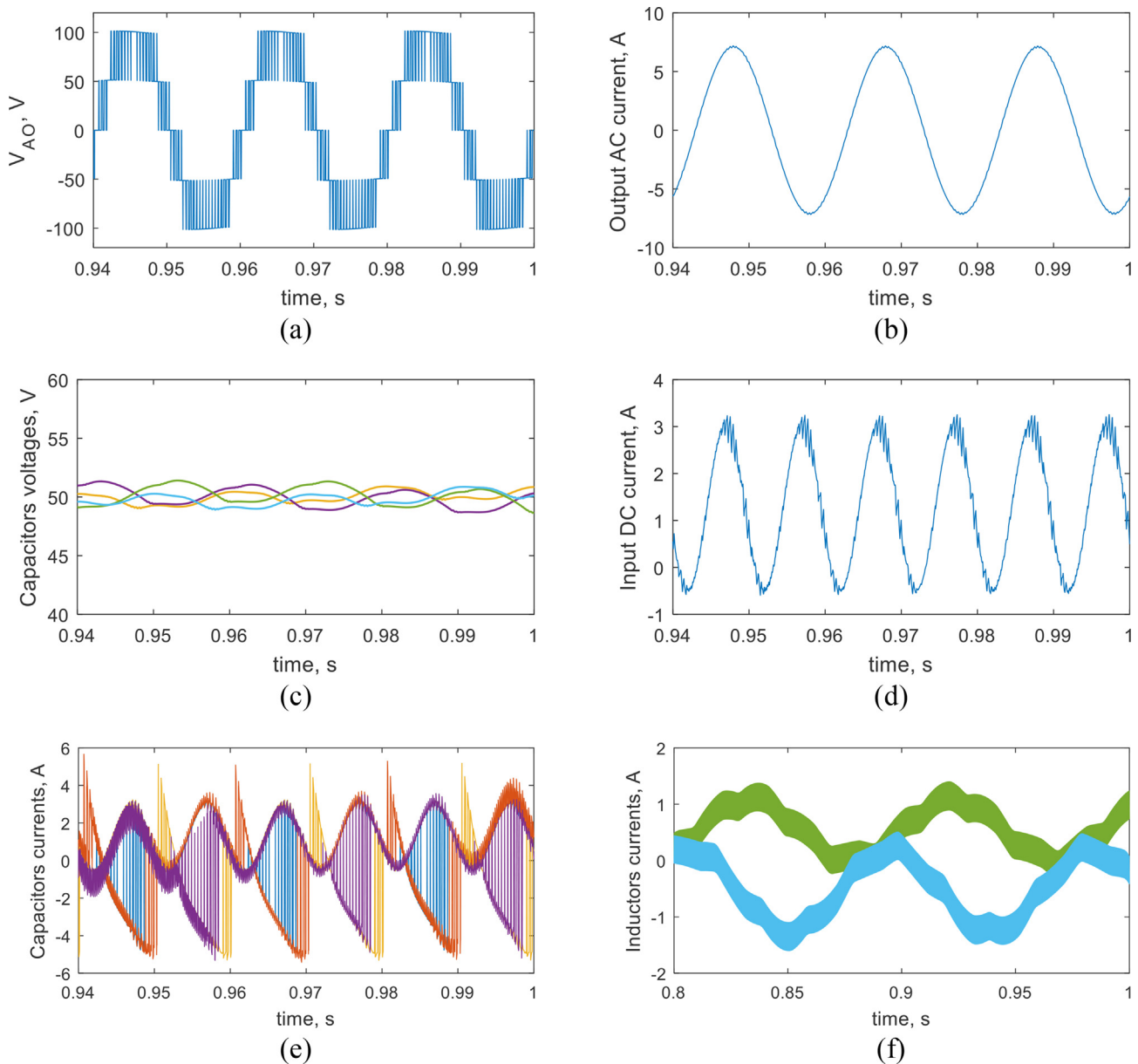


Fig. 13 Simulation results of single-phase 5L F-type inverter (a) output AC voltage, (b) output AC current, (c) voltages of dc capacitors, (d) input dc current, (e) currents of dc capacitors, and (f) inductors currents of the employed equalization channels.

successfully with a magnitude of $V_{dc}/2$ at a unity modulation index. Fig. 19b shows the three-phase output currents where the currents are sinusoidal with good quality. Fig. 19c shows the voltages of the dc capacitors where they are kept at the same voltage level thanks to the employed equalization channels.

Fig. 19d shows the input dc current where it is not oscillatory as presented in the single-phase case as the power is constant in the balanced three-phase condition. Fig. 19e shows the currents of the involved dc capacitors. Finally, Fig. 19f shows the inductors currents of the employed buck-boost converter-based equalization channels to ensure operating with balanced

capacitors voltages via providing upper and lower energy channels to transfer the energy between the upper capacitors and lower capacitors, respectively.

To show the effect of buck-boost converter-based energy equalization channels on balancing capacitors voltages, the system is firstly run while enabling the energy equalization channels. Then channels are disabled. The corresponding capacitors voltages variation is shown in Fig. 20. It is clear that the capacitors voltages are balanced and bounded when the equalization channels are enabled. Nevertheless, when equalization channels are disabled, the capacitors' voltages diverge, and energy drift starts.

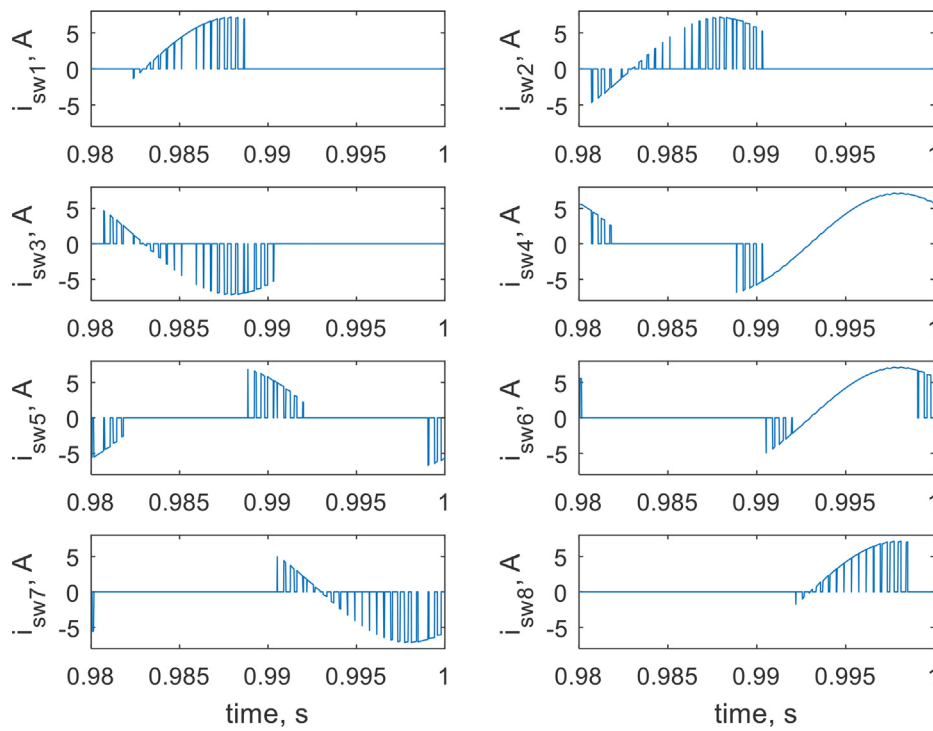


Fig. 14 Currents of the switches in the proposed architecture (switch = IGBT + antiparallel diode).

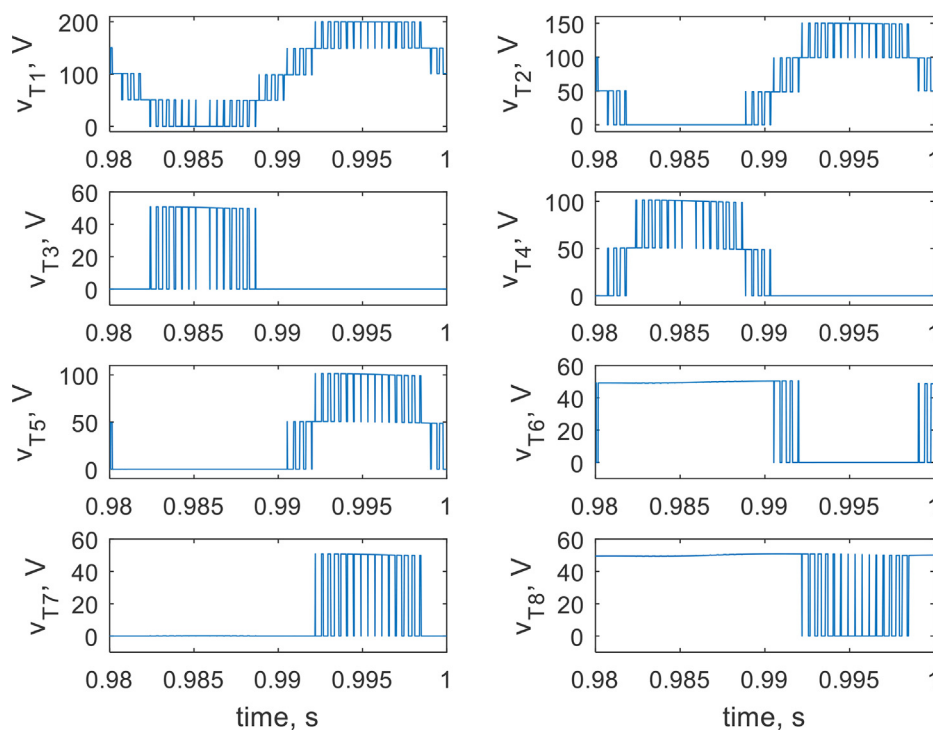


Fig. 15 Voltages of the IGBTs in the proposed architecture.

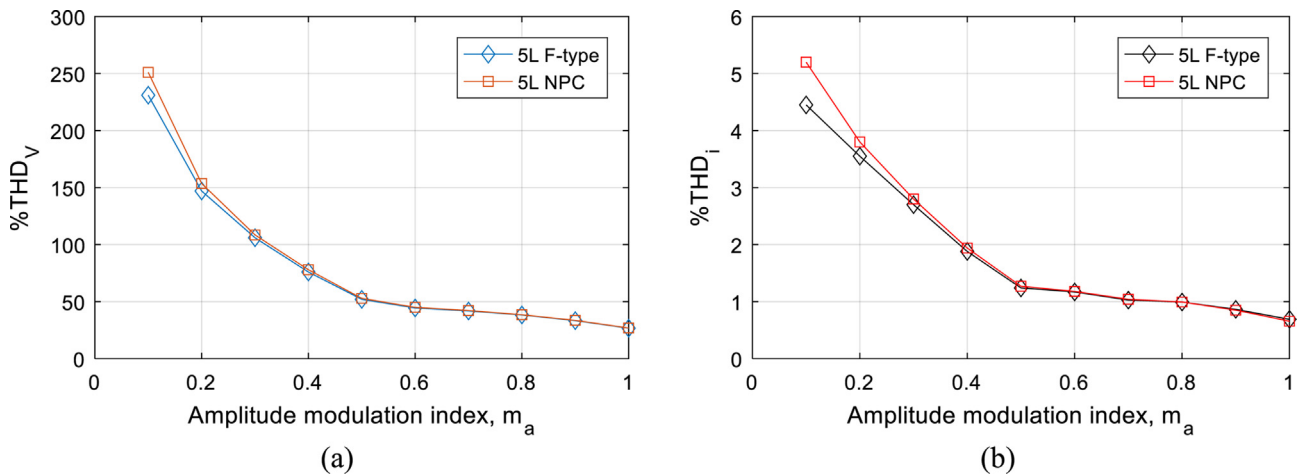


Fig.16 Variation of voltage THD and current THD versus amplitude modulation index (m_a). (a)%THD_V and (b) %THD_I.

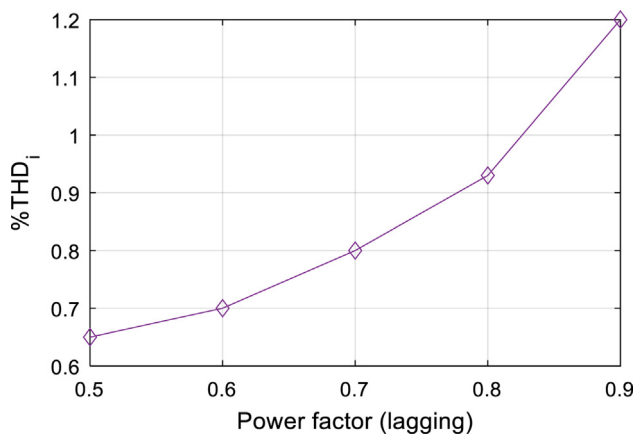


Fig. 17 Variation of %THDi versus load power factor (5L F-type).

7. Assessment of the proposed five-level F-type inverter

7.1. Comparison

In this section, an assessment of the one-leg single-phase version of the proposed 5L F-type Inverter (shown in Fig. 5) com-

pared to other existing 5L inverters such as 5L NPC inverter, 5L Flying Capacitor (FC) inverter, 5L Modular Multilevel Converter (MMC) and 5L E-type Inverter presented in [27], are presented to show the pros and cons of the suggested 5L F-type inverter. The comparison is shown in Table 5. It is clear that 5L MMC and 5L FC use a higher number of dc capacitors than the others. In addition, 5L MMC needs extra dc-link capacitances and a higher number of semiconductor devices, i.e., a higher number of gate drive circuits, but neither 5L MMC nor 5L FC inverter needs energy equalization circuits. The 5L NPC needs extra six diodes, which negatively affects the system cost and losses. Finally, the 5L E-type inverter needs a higher number of semiconductor devices rated at the full dc input voltage compared to the proposed 5L F-type inverter.

7.2. The proposed 5L F-type inverter versus 5L NPC inverter (numerical example)

This subsection presents a numerical case study to show the voltage stresses, current stresses, and losses of the proposed 5L F-type inverter (shown in Fig. 21a) versus 5L NPC (shown in Fig. 21b) for the same operating conditions.

For dc input voltage of 800 V, amplitude modulation index (m_a) of 1, frequency modulation index (m_f) of 48, and AC load

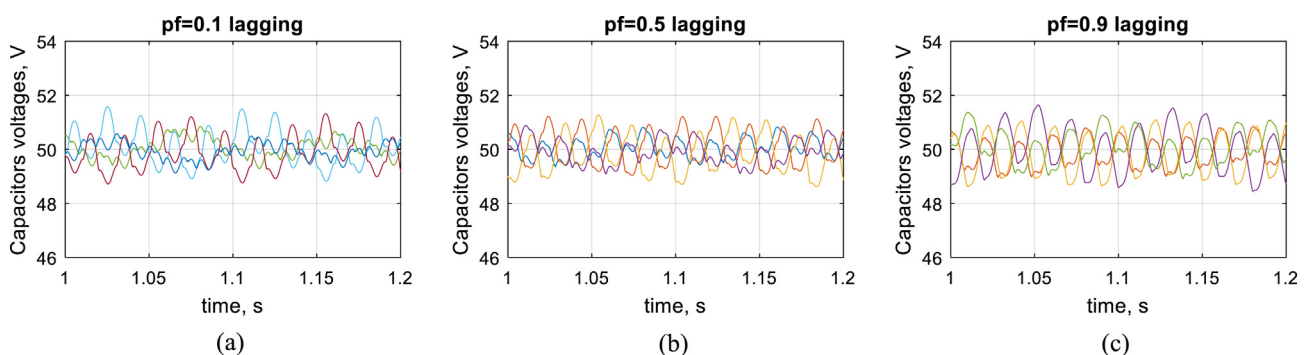


Fig. 18 Capacitors voltages variations at different load power factors.

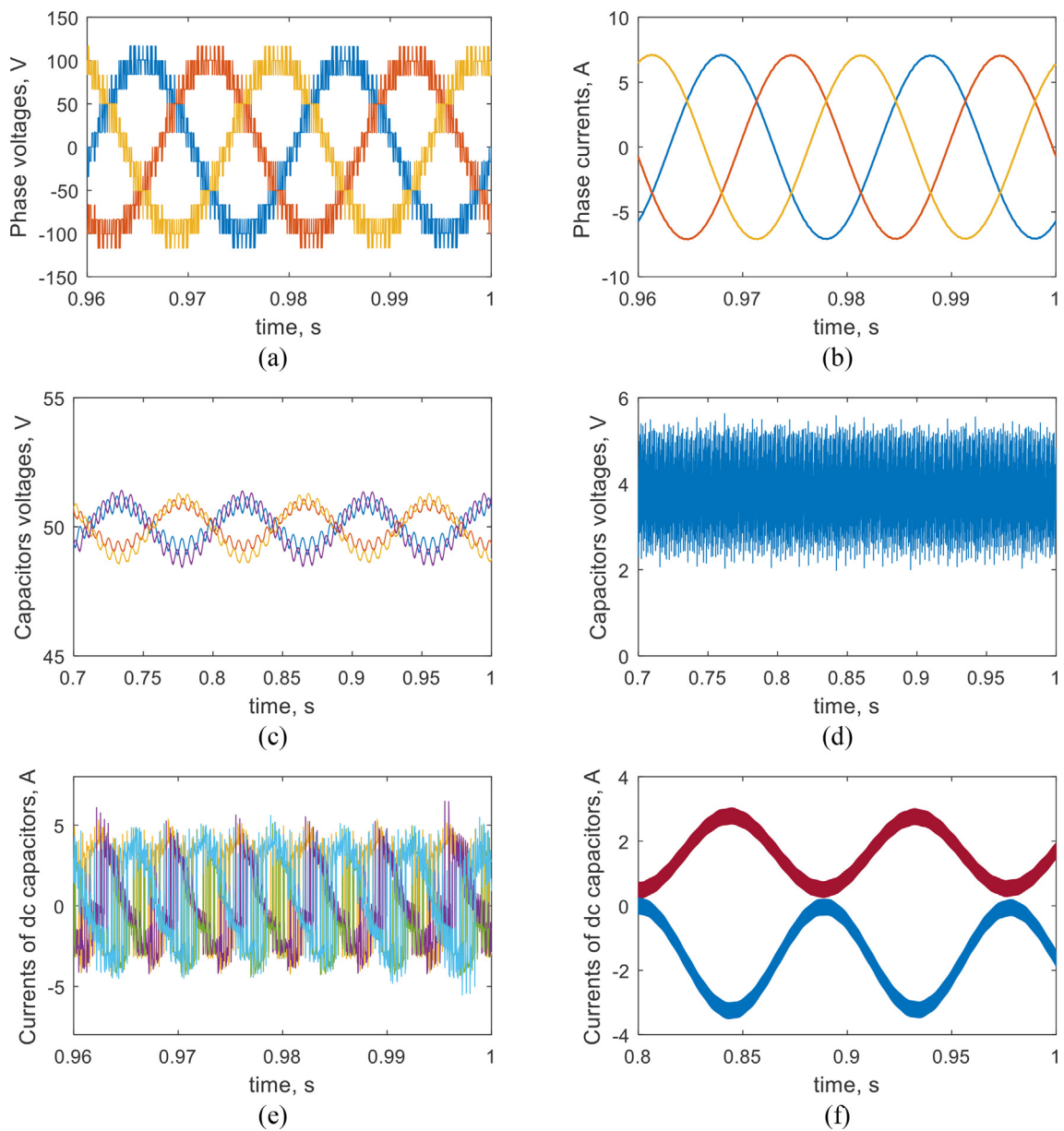


Fig. 19 Simulation results of the three-phase version. (a) output phase voltages, (b) output phase currents, (c) voltages of dc capacitors, (d) input dc current, (e) currents of dc capacitors, and (f) inductors currents of the employed equalization channels.

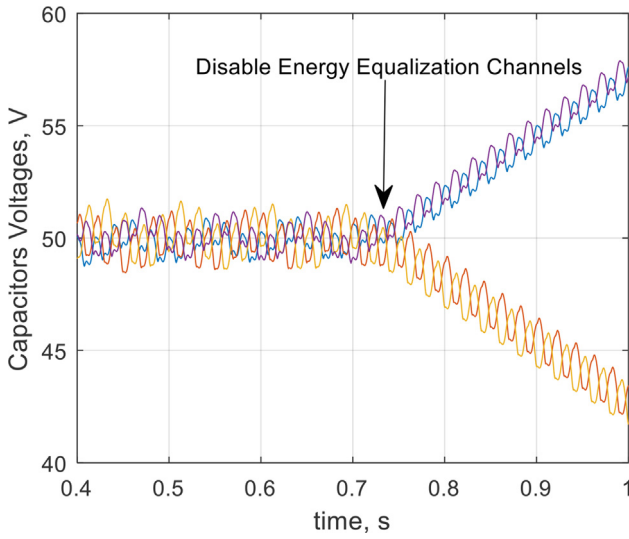


Fig. 20 The effect of buck-boost converter-based energy equalization channels on balancing capacitors' voltages.

impedance of $40 \angle 45^\circ \Omega$ at 50 Hz at rated condition, the corresponding current stresses (highest instantaneous current), voltage stresses (highest instantaneous voltage), total kVA of the involved semiconductor devices, conduction and switching losses of both inverters without considering the equalization channels are summarized in Table 6, where approximate conduction losses and switching losses are estimated using Eq. (4) and Eq. (5) respectively.

$$P_c = I_{rms}^2 R_{on} + I_{ave} V_{on} \quad (4)$$

$$P_s = 0.5 f_s (I_1 V_1 t_{on} + I_2 V_2 t_{off}) \quad (5)$$

Where $P_{c\ sw}$ is the conduction losses per switch, I_{rms} and I_{ave} are the root mean square and mean value of the switch current, respectively, V_{on} and R_{on} are the switch on-state voltage and on-state resistance, respectively. In the presented analysis, V_{on} of 1 V and R_{on} of 5 m Ω are used. On the other hand, P_s is the switching losses, f_s is the switching frequency, I_1 and V_1 are the current and voltage of the switch during turn-on state, while I_2 and V_2 are the current and voltage of the switch during turn-off state. Finally, t_{on} and t_{off} are the turn-on and turn-off times of the switch, respectively. In the presented analysis t_{on} of 1 μ s and t_{off} of 1.3 μ s are assumed.

Based on Table 6, it is clear that the proposed 5L F-type inverter has a lower total kVA rating assuming that the voltage/current rating of the device equals its highest instantaneous voltage/current. The proposed 5L F-type inverter also has lower conduction losses. Unlike 5L-NPC, it has no clamping diodes. Finally, the switching losses of both inverters are almost the same. Fig. 22 shows both inverters' conduction and switching losses at the rated condition. Finally, Fig. 23 shows the variation of conduction in both types with loading (from no-load condition to full-load condition). Based on Fig. 23, it is clear that the conduction losses of the proposed 5L F-type inverter are always less than the conduction losses of the 5L-NPC inverter in the whole operating range.

8. Experimental validation

A scaled-down prototype of the proposed single-phase 5L F-type inverter, shown in Fig. 24, has been implemented for experimental validation. The parameters of the experimental setup are given in Table 7. The corresponding experimental results are shown in Fig. 25.

Fig. 25a shows the output AC voltage and output current, where 5L output voltage has been generated successfully from

Table 5 The proposed 5L F-type inverter versus Other Existing 5L-Inverters (One-leg single-phase Inverters).

	Proposed 5L F-type inverter	5L-NPC inverter	5L-FC Inverter	5L MMC	5L E-type Inverter [27]
No. of IGBTs	8	8	8	16	8
IGBT Voltage	$1x(V_{dc}), 1x(3V_{dc}/4), 2x(V_{dc}/2), 4x(V_{dc}/4)$	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$	$2x(V_{dc}), 2x(3V_{dc}/4), 2x(V_{dc}/2), 2x(V_{dc}/4)$
No. of Discrete Diodes	—	6	—	—	—
Diodes Voltages	—	$2x(V_{dc}/4), 2x(V_{dc}/2), 2x(3V_{dc}/4)$	—	—	—
No. of dc Cap.	4	4	10	10	4
Cap. Voltage	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$	$8x(V_{dc}/4) + 2x(V_{dc}/2)$	$V_{dc}/4$
Need for Equalization Channels (ECs)	Yes	Yes	No	No	Yes
No. of ECs	2	2	—	—	2
No of IGBTs in EC	$2x(V_{dc}/2)$	$2x(V_{dc}/2)$	—	—	$4x(V_{dc}/4)$
EC passive elements	Buck-boost based L	Buck-boost based L	—	—	SRBC-based $L + C$

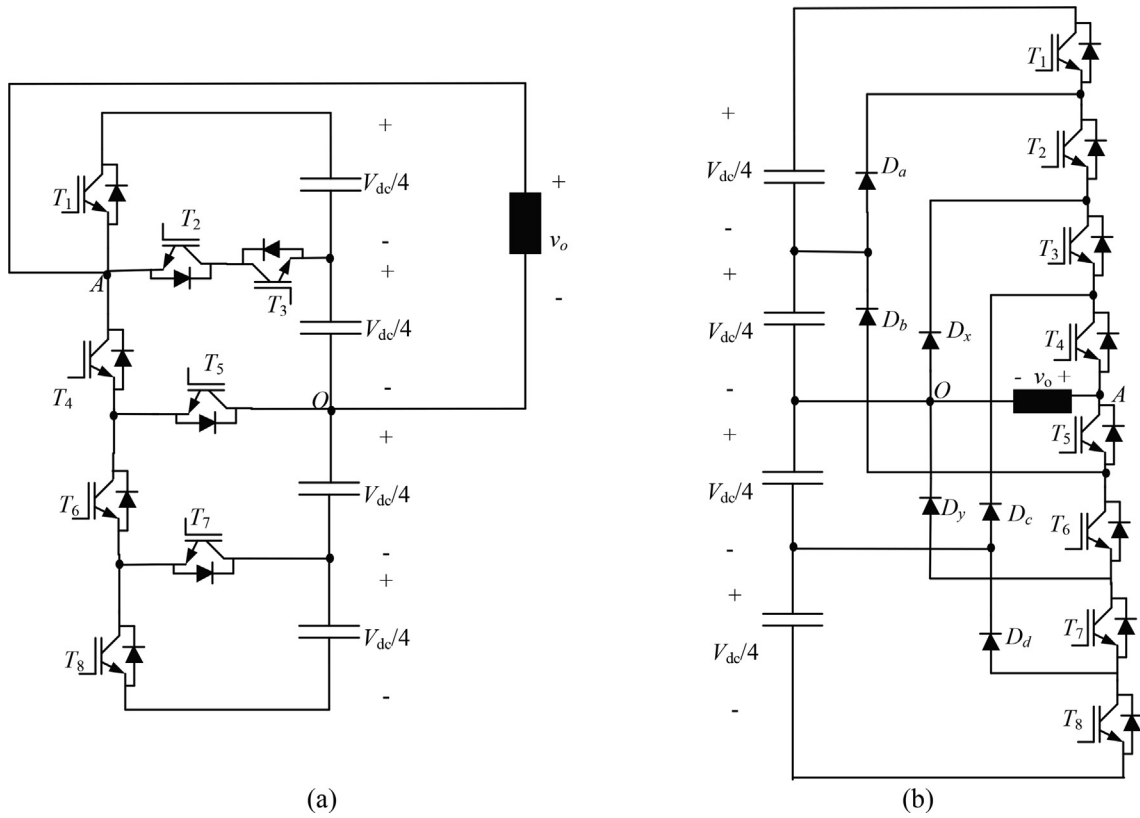


Fig. 21 Converters under assessment. (a) the proposed 5L F-type inverter and (b) the conventional 5L-NPC inverter.

Table 6 The proposed single-phase 5L F-type inverter versus 5L-NPC inverter for the given case study.

	The proposed 5L F-type inverter				5L-NPC			
IGBTs current stresses	T_1	10 A	T_2	10 A	T_1	11 A	T_2	11 A
	T_3	10 A	T_4	10 A	T_3	10 A	T_4	10 A
	T_5	10 A	T_6	10 A	T_5	10 A	T_6	10 A
	T_7	10 A	T_8	10 A	T_7	11 A	T_8	11 A
	—	—	—	—	—	—	—	—
Diodes current stresses	—	—	—	—	D_a	10 A	D_b	5.5 A
	—	—	—	—	D_x	8.5 A	D_y	8.5 A
	—	—	—	—	D_c	5.5 A	D_d	10 A
	—	—	—	—	—	—	—	—
IGBTs voltage stresses	T_1	800 V	T_2	600 V	T_1	200 V	T_2	200 V
	T_3	200 V	T_4	400 V	T_3	200 V	T_4	200 V
	T_5	400 V	T_6	200 V	T_5	200 V	T_6	200 V
	T_7	200 V	T_8	200 V	T_7	200 V	T_8	200 V
	—	—	—	—	—	—	—	—
Diodes voltage stresses	—	—	—	—	D_a	-200 V	D_b	-600 V
	—	—	—	—	D_x	-400 V	D_y	-400 V
	—	—	—	—	D_c	-600 V	D_d	-200 V
	—	—	—	—	—	—	—	—
Total kVA rating of devices	28.66				33.3			
Conduction losses	21.61 W				34.6 W			
Switching losses	3.43 W				3.52 W			

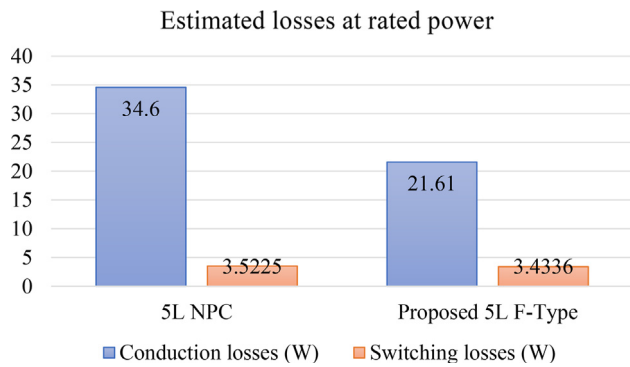


Fig. 22 Conduction and switching losses of the proposed single-phase 5L F-type inverter and 5L-NPC inverter.

Table 7 Experimental Setup Parameters.

Parameter	Value
Input dc voltage	100 V
Number of dc link capacitors	4
DC link capacitance	2.2 mF
SPWM carrier frequency	5 kHz
AC Load	Inductive (series RL load with R = 10 Ω and L = 11 mH)
Equalization channel inductance	1.77 mH
Equalization channel switching frequency	10 kHz
Modulation index	0.85

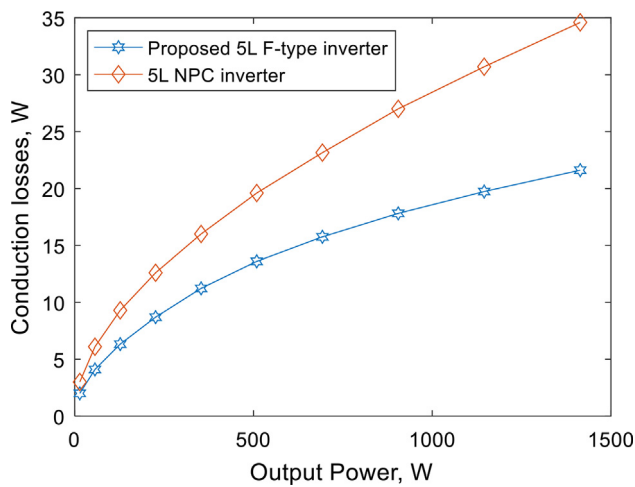


Fig. 23 Variation of the conduction losses with loading for the proposed single-phase 5L F-type inverter and 5L-NPC inverter for the given case study.

the proposed 5L F-type topology. The load current is sinusoidal with a peak of approximately 4A at 0.85 modulation index. Fig. 25b shows the voltages of the involved dc-link capacitors, where the voltages are well balanced and kept bounded in certain voltage window with an average of 25 V ($V_{dc}/4$) thanks to the employed equalization channels, where they are operated with 50 % duty cycle to ensure balanced capacitors' voltages. The corresponding inductors' currents of the involved buck-boost converter-based equalization channels are shown in Fig. 25c. Fig. 25d shows the input dc link current, where it oscillates with 100 Hz, i.e., the double of load frequency, due to the nature of the single-phase AC instantaneous power.

Finally, to show the importance and effectiveness of the employed equalization channels, the proposed topology has been run while enabling the equalization channels, then they are disabled, then they are enabled again after a while, the corresponding dc-link capacitors' voltages are shown in Fig. 26. It is clear that the capacitors' voltages are balanced when the equalization channels are enabled, which ensures successful conversion process. On the other hand, when the equalization

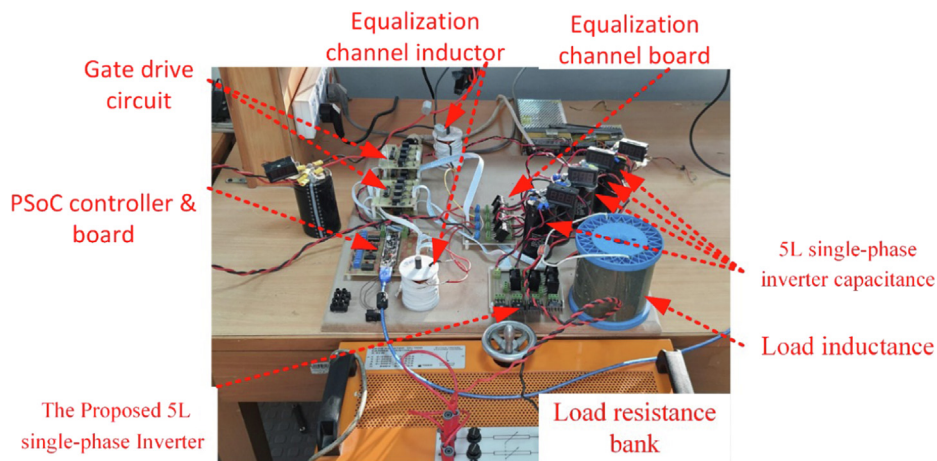
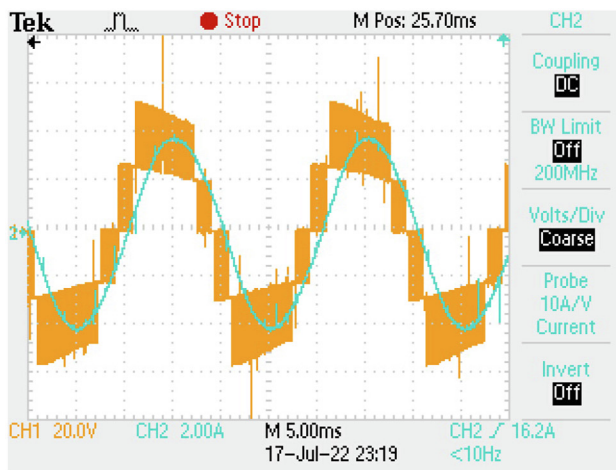
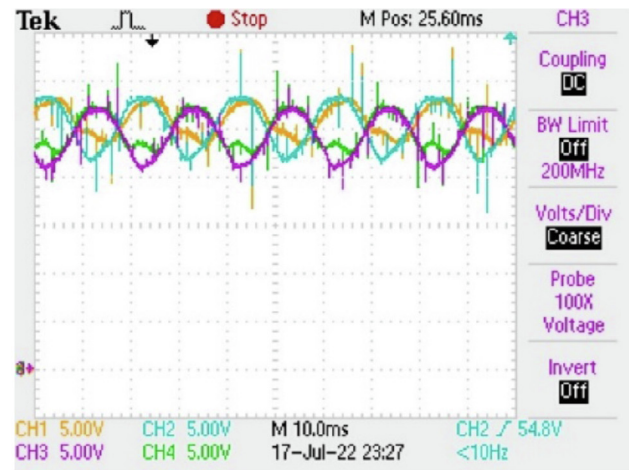


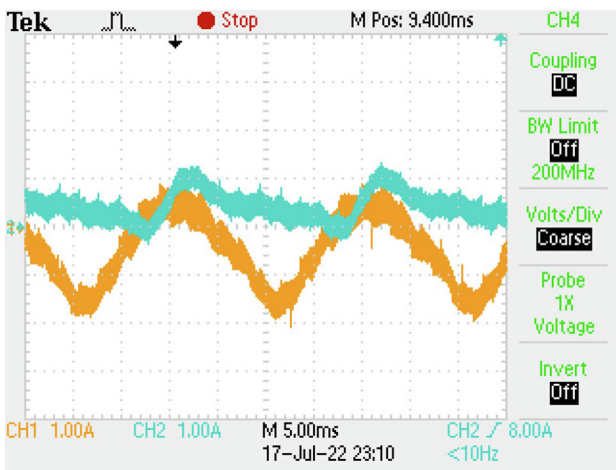
Fig. 24 A scaled-down prototype of the proposed single-phase 5L F-type inverter.



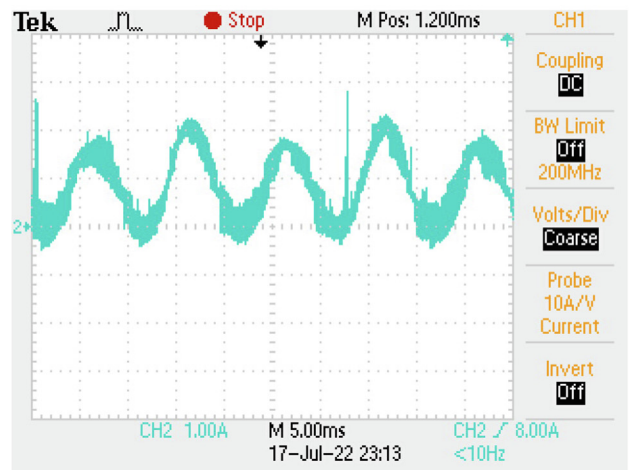
(a)



(b)



(c)



(d)

Fig. 25 Experimental results of the proposed single-phase 5L F-type inverter. (a) CH1: output voltage and CH2: output current, (b) voltages of the involved dc-link capacitors, (c) currents of equalization circuits inductors and (d) input dc current.

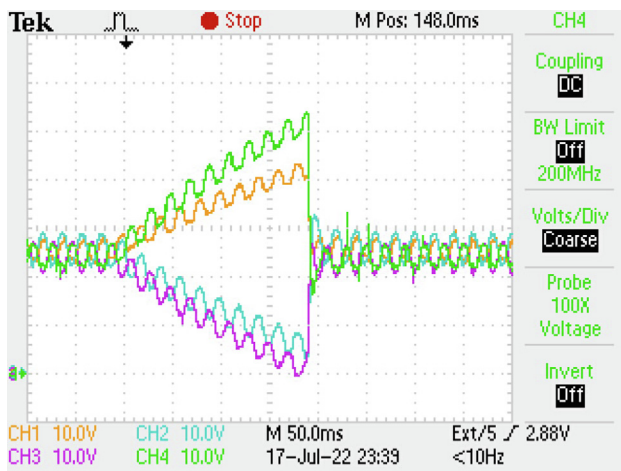


Fig. 26 Effect of enabling and disabling the employed equalization channels on the dc-link capacitors' voltages.

channels are disabled, the capacitors' voltages start in diversion, which leads to unsuccessful conversion process.

9. Conclusion

In this paper, a new 5L F-type inverter has been proposed for low-/medium-voltage applications. Single-phase and three-phase versions are presented along with their modulation technique. Buck-boost converter-based equalization circuits/channels are employed to ensure operating with balanced dc-link capacitors via transferring the energy from higher voltage capacitors to lower voltage capacitors through these equalization channels. A comparison between the proposed 5L F-type inverter and other 5L existing multilevel inverters has been held. Numerical comparison between the proposed 5L F-type inverter and 5L NPC in terms of voltage stresses, current stresses, and losses has been presented. The comparison shows that the proposed 5L F-type inverter has a lower kVA rating and losses, positively affecting the system cost and size. Simulation results for single-phase and three-phase versions are pre-

sented to show the performance and viability of the suggested converter. Finally, experimental validation for the proposed single-phase five-level F-type has been presented.

Acknowledgment

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