QATAR UNIVERSITY

COLLEGE OF ENGINEERING

MODEL PREDICTIVE CONTROL STRATEGY FOR LEAKAGE CURRENT REDUCTION IN PHOTOVOLTAIC SYSTEMS: A STUDY ON PUC AND CSC INVERTER TOPOLOGIES

BY

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ABSTRACT

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Title: Model Predictive Control Strategy for Leakage Current Reduction In Photovoltaic Systems: A Study On PUC and CSC Inverter Topologies

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Solar energy is one of the most commonly used sources of renewable energy. It is a clean and noiseless energy source that does not emit greenhouse gases. This thesis focuses on studying a double-stage transformerless photovoltaic (PV) microinverter grid-connected system. The main concern when using a transformerless PV setup is the need to take safety measures, as this configuration can result in PV panel leakage current issues. This thesis studies this issue in two inverter topologies: the packed U-cell (PUC) and the crossover switches cell (CSC) inverters. A Finite-Control-Set model Predictive Control is proposed to mitigate the PV panel leakage current. The proposed controller was simulated using Matlab/Simulink, and the results show that the controller effectively mitigates the leakage current. In the case of a PUC inverter, the RMS leakage current decreases from 336 mA to 155 mA. In the case of a CSC inverter, it decreases from 360 mA to 140 mA, which is below 300 mA as per the DIN VDE 0126-1-1 standard. These results were achieved while maintaining a gird current total harmonic distortion (THD) of less than 5% and maintaining the voltage across the inverter capacitors constant with less than 0.5% variation. Furthermore, a hardware-in-the-loop implementation was utilized to test and validate a proposed control algorithm for the PUC inverter. Through this testing, it was found that the PV panel leakage current has been successfully mitigated from 1.1 A to 0.5 A while maintaining the PUC

capacitor fixed with minor variations and the THD remaining below 5.6%.

DEDICATION

To my parents and siblings,

whose endless support and guidance have been my strength and inspiration.

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I humbly extend my sincerest gratitude to the Most Gracious and Merciful Allah for bestowing upon me innumerable blessings and for illuminating my path with unwavering wisdom and perseverance. I am deeply appreciative of the strength and patience that Allah has granted me throughout this journey.

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CHAPTER 1: INTRODUCTION

1.1 Background

In today's world, electricity is an essential requirement, and renewable energies (RE) play a crucial role in meeting the increasing demand. Integrating RE technologies into electricity networks and enhancing their efficiency are vital steps in reducing CO_2 emissions. As populations continue to grow and develop, the demand for electrical energy is on the rise globally [1]. Non-renewable energy sources like fossil fuels are not a feasible future option. because they are not renewable and pollute the environment. Hence, it is imperative to curtail the usage of non-renewable resources and focus more on RE, which will play a pivotal role in shaping the future [1]. Solar energy is currently the world's most widely used energy source. It is a clean and noiseless form of energy, which makes it highly desirable. This is why photovoltaic (PV) technology has become one of the most popular forms of RE. By the conclusion of 2015, solar energy systems had been installed worldwide to produce an estimated 230 gigawatts of power [2]. The installation of PV solar plants has increased significantly in the past few years, leading to a substantial increase in power generation.

Two types of PV system configurations, string and central, were initially available [3]. These systems utilize lengthy DC cables with high voltage to transmit power from PV arrays to inverters and eventually to the utility grid. The lengthy cables result in increased power loss. Furthermore, utilizing these configurations necessitates implementing a singular maximum power point tracking (MPPT) for the whole PV setup. Consequently, the overall efficiency of the system decreases due to mismatch losses [4]. Moreover, the aforementioned configurations require high-level power inverters that limit and constrain the system's ability to expand. A new development in solar panel technology is the integration of the inverter on the panel's back sheet. This

panel type is called an integrated AC module and is sold as a complete system to the user. This approach offers several benefits, such as removing the need for DC cables, and decreasing maximum power point (MPP) mismatch losses. Consequently, it enhances the entire system's efficiency and significantly reduces installation costs [5].

Considering that the AC integrated module will be installed behind the solar panel, having a weighty, cumbersome transformer becomes unnecessary and challenging to set up. However, eliminating the transformer results in certain disadvantages, mainly caused by the galvanic connection between the PV system and the power grid. Achieving galvanic isolation in PV systems can be accomplished by utilizing a low-frequency AC transformer or a high-frequency DC-DC transformer on the grid and PV system sides, respectively. Using a low-frequency AC transformer for isolation on the grid side of PV inverters, however, results in a larger overall system size and a complex installation procedure. In DC-DC converter topologies that involve high-frequency transformers, overall efficiency is compromised due to additional losses incurred by the transformer [6], [7], [8]. Eliminating the transformer can improve efficiency by 1-2% [9]. Transformerless inverters, on the other hand, create a common-mode (CM) resonant circuit composed of the grid impedance, inverter, filter, and DC source-ground parasitic capacitances (PC). In this scenario, a CM current is produced by both the grid and the PV system, leading to a rise in the harmonics content of the grid [10], [11]. As a result, electromagnetic interference is created between the two systems. Furthermore, the PC permits leakage current (LC) to flow, which can attain high levels, thereby posing a safety hazard to individuals who come into contact with the PV system.

The use of multilevel inverters (MLIs) in power systems has increased due to their ability to produce a desired output voltage rating demand and meet power quality

while minimizing electromagnetic interference and harmonic distortion [12]. MLIs have gained popularity in industrial applications because they provide high power quality and dynamic performance for systems that require a power range between 1 and 30 MW [13]. Thus, MLIs are well-suited for high-voltage applications because they generate higher voltages despite limited device ratings while producing low total harmonic distortion (THD) output voltage waveforms [14]. MLIs can effectively interface with RE sources including the wind turbines [15], fuel cells and PV cells. In addition, the efficient operation, optimal power ratings, and appropriate application of MLIs depend heavily on the control algorithm used in their pulse-width modulation (PWM) mechanism [16]. In industries, the commonly employed topologies for MLIs are cascaded H-bridge (CHB), flying capacitor, and diode clamped , or neutral point clamped (NPC) [17], [18], [19].

Packed U Cell (PUC) and Crossover Switches Cell (CSC) MLIs are among the topologies mentioned that require the least number of DC sources and switches, generating 7 and 9 voltage levels, respectively [20], [21], [22]. However, these types of inverters require complicated controllers to balance flying capacitor voltage, resulting in fewer isolated DC sources. Accordingly, to regulate the capacitor voltage at the required level in the PUC and CSC inverter, the hysteresis current control has been implemented. This approach, however, has led to concerns including high and variable switching frequency, which many industries consider undesired. [23], [24].

The use of predictive control for regulating power converters holds great promise due to its many advantages, such as eliminating the requirement for linear controllers and modulators, incorporating nonlinearities and constraints, and providing fast dynamic response [25], [26]. Although various methods for predictive control have been presented, Finite Control Set Model-based Predictive Control (FCS-MPC) is a

viable option for power converter regulation [27]. FCS-MPC utilizes the system's discrete model to predict its future behavior, and then determines the optimal switching state that minimizes a specific cost function, then applies it to the converter. A model-based predictive controller should ideally regulate the inverter output current and the DC-link capacitor voltages simultaneously.

1.2 Thesis Objectives

This research aims to study two multi-level inverters, the packed U-cell (PUC) and the crossover switches cell (CSC) inverters, within a transformerless PV grid-connected system. Specifically, it aims to explore the effectiveness of an advanced control technique designed to achieve unity power factor and maintain low total harmonic distortion (THD) while regulating the capacitor voltage at the reference level. A critical aspect of this investigation will focus on mitigating PV panel leakage current (LC) by minimizing the voltage variation across the parasitic capacitances (PC).

To achieve these aims, the following objectives will be accomplished:

1. Modeling of the PUC and CSC multilevel inverters.
2. A new multi-tasking control technique using a suitable cost function will be developed to control the PUC and CSC inverters. The cost function will include the capacitor voltages balancing, the output current control and the common-mode voltage (CMV) reduction.
3. Simulation of PUC and CSC inverters and the designed controllers.
4. Hardware-in-the-loop (HIL) implementation of PUC and CSC inverters and the designed controllers.

1.3 Thesis Contribution

A noteworthy breakthrough has been made in the field of renewable energy (RE) by successfully reducing the leakage current (LC) in PV arrays for grid-connected systems. The method employed was FCS-MPC. The LC has been significantly reduced by utilizing the PV system's PUC and CSC inverters, which has greatly improved the system's overall performance. This achievement can pave the way for further research in this field and make a valuable contribution to the RE industry.

1.4 Thesis Outline

The thesis is structured into seven chapters. Chapter 1 introduces the topic and emphasizes the objective and contribution of the thesis. Chapter 2 presents a comprehensive literature review. Chapter 3 presents the main system design, including an overview of all systems, the design of the PV array and quadratic boost converter (QBC), and the mathematical model of the PUC and CSC inverters. The cost function design procedure also stated the weighting factor determination technique. Chapters 4 and 5 present the results and discussion of Simulink simulation and HIL implementation, respectively. Finally, Chapter 6 summarizes the thesis work and proposes avenues for future research.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter presents a comprehensive literature review of a double-stage PV grid-connected system, as illustrated in Figure 2-1. The system consists of a PV panel, DC-DC converter, DC-AC inverter, AC grid, and two control parts (the MPPT and inverter controller). The review covers all system elements and begins by explaining and comparing different PV grid-connected system inverter-based configurations. It then delves into the power processing stages and transformer-based and transformerless PV systems. The review also focuses on the issues related to utilizing transformerless systems, highlighting the PV panel LC and different mitigation techniques.

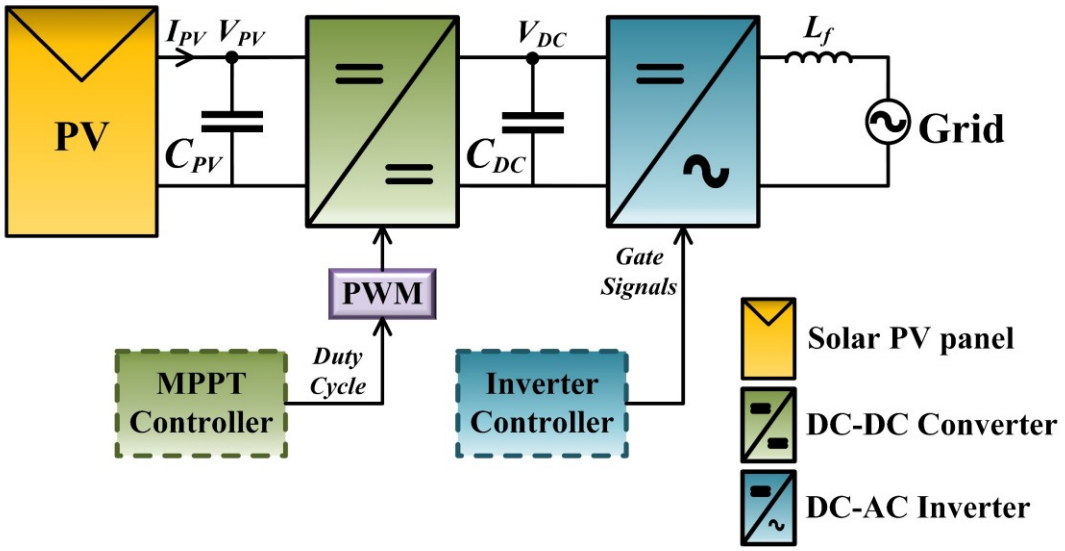

Figure 2-1. Double-stage PV grid-connected system

The review encompasses twenty-seven different non-isolated boost DC-DC converters, which are categorized into seven topologies. One of these topologies is a cascaded technique, including a QBC. The topology of this converter is introduced, and a comparison is made between it and the conventional boost converter. Additionally, the review compares different MPPT techniques based on their robustness, convergence speed, complexity, and whether they require tuning.

The review also covers MLIs and compares them with two-level inverters. Different non-isolated MLI topologies for grid-connected PV applications are compared based on LC, number of switches, and efficiency. The review provides a detailed explanation of the PUC and CSC inverter topologies and compares them with other MLIs. Furthermore, the review concludes by presenting control strategies for MLI topologies for grid-connected PV systems. It also focuses on FCS-MPC and reviews the papers that utilized FCS-MPC to control PUC and CSC inverters. Finally, the review summarizes the gaps in the literature.

2.2 PV grid-connected system inverter based configurations

The most frequently utilized PV configurations involve series and parallel connections. When PV panels are linked in series, it creates a string, and when the strings are then connected in parallel, they form an array. Essentially, there are four main types of grid-connected inverters for PV systems: centralized, string, multi-string, and microinverters [28]. These configurations have similar energy extraction and power capture abilities under consistent sunlight. Nevertheless, the energy extraction performance of the PV systems is considerably impacted by the converter structure in situations when shading circumstances are not uniform [29]. These inverters-based configurations will be thoroughly described in the following sections.

2.2.1 Central Inverter

The central inverter configuration was presented in the seventies due to the direct coupling technology, allowing the direct connection of solar cell arrays to the electric power grid [30]. In this configuration, a single inverter connects the solar panels to the AC grid. Consequently, a string is formed by connecting several PV panels in series to amplify the inverter input voltage [31]. Moreover, a PV array is formed to increase the power output by connecting multiple strings in parallel, as Figure 2-2 illustrates.

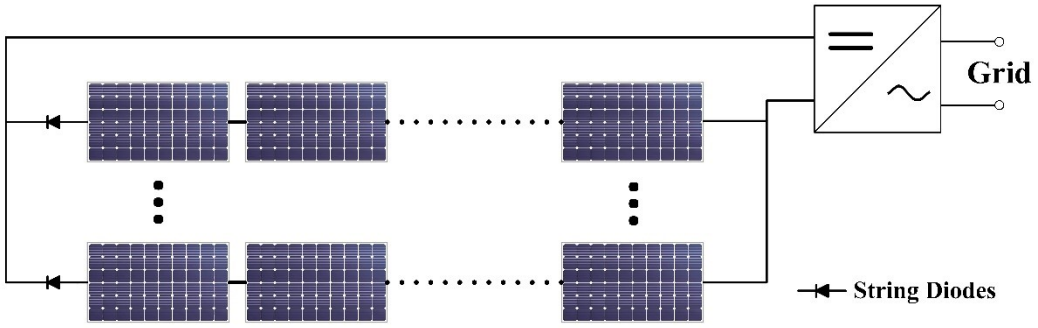

Figure 2-2. Grid connected centralized inverter system

During cloudy weather, a DC-DC boost converter steps up the PV array's output voltage, enabling it to be fed into a grid-connected inverter and ensuring a continuous power supply. This approach presents a notable drawback: it relies on a single MPPT for the entire system, which results in panel mismatches and diminishes the system's overall effectiveness [32]. One of the significant concerns in the central configuration is that if the main inverter of a PV system stops working, the whole system will be affected and unable to function properly [33]. This configuration is the most cost-effective option compared to other configurations. It is commonly used for power ratings ranging from 1 MW to 50 MW. Furthermore, it is highly robust, reduces AC power losses, and necessitates low maintenance [34], [35].

2.2.2 String Inverter

This configuration is a widely utilized technology that provides a partial solution to the limitations of central inverters [36]. The string configuration in a PV system involves connecting strings in parallel to the inverter as shown in Figure 2-3. This design allows for greater adaptability and flexibility, as each string can be monitored and controlled individually for maximum power output [37]. As a result, each string is controlled independently using an MPPT, which enhances overall efficiency compared to the central inverter [38]. This configuration is used for power rating up to 5 kW per string, and its modular design allows for easy expansion to higher ratings. In the central

configuration, a malfunctioning inverter can affect the entire PV system. However, in this configuration, a malfunctioning string inverter will only impact the corresponding string. The string inverter configuration is both reliable and flexible, with low losses in switching and DC power. Additionally, the use of string inverters will reduce cable costs. Nonetheless, the installation cost of this setup is considerably higher in comparison to the central configuration, resulting in a more expensive overall cost [34], [35].

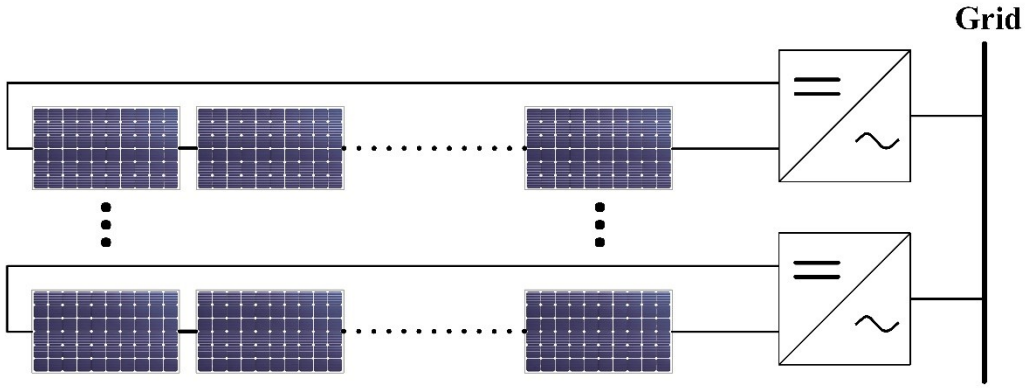

Figure 2-3. Grid connected string inverter system

2.2.3 Multi-String Inverter

This configuration is a combination of the benefits and advantages of both string and central inverter configurations. The multi-string configuration consists of a single inverter connected to multiple strings through DC-DC boost converters controlled separately via the MPPT controller [39], as demonstrated in Figure 2-4. As reported in [40], the utilization of an independent MPPT system led to increased accuracy and flexibility. This configuration is suitable for different power plant sizes - low, medium, and large. Its flexible design allows for future expansion of up to 50k [41]. While this technology is more expensive than the microinverter configuration, it is less costly than the central configuration. However, its ability to integrate different PV string ratings may cause a significant voltage fluctuation at the inverter input side [34], [35].

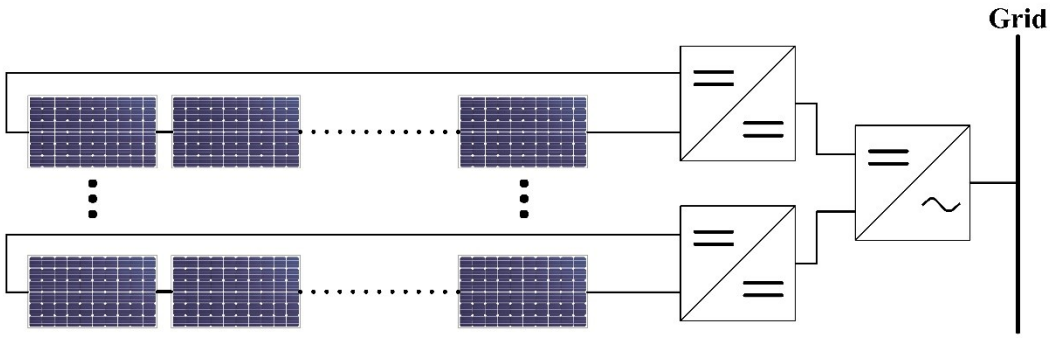

Figure 2-4. Grid connected multi-string inverter system

2.2.4 Microinverter

The microinverter configuration is highly suitable for residential use due to its modular design. Each solar panel is equipped with its inverter instead of relying on a high-power centralized inverter. Figure 2-5 depicts microinverter system structure.

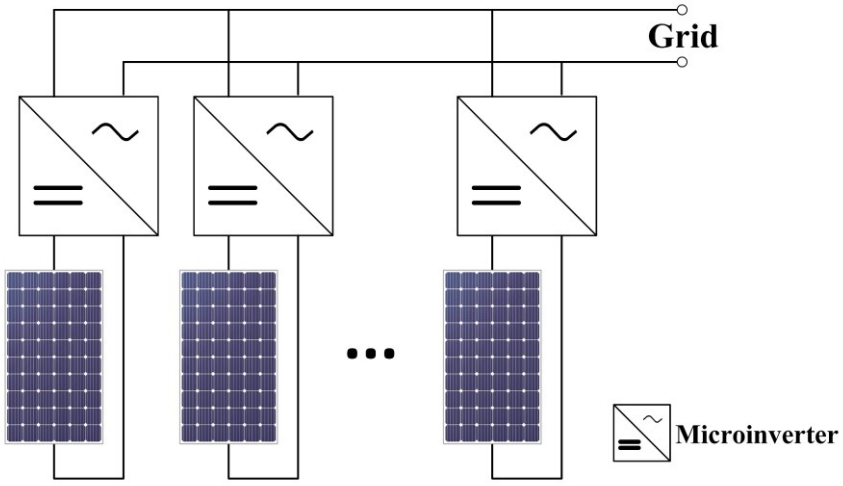

Figure 2-5. Grid connected microinverter system

The advantages of this approach include reduced power loss due to shading, as the power reduction is limited to the microinverter connected to the shaded panel, implementing MPPT for each panel enhances the system's efficiency, easy to maintain individual panels separately without completely disconnecting the system, the cost for installation can be adapted to fit specific needs and requirements, the ability to expand the system panel by panel [42]. However, there remain numerous challenges that must

be addressed in order to attain reduced production expenses, enhanced conversion efficiencies, and longer lifespan. Microinverters are usually positioned behind or incorporated into the back skin of the PV panel. As a result, it is critical to consider inverter longevity that matches that of the PV panel during the design process [28].

Table 2-1 presents a comparison of the inverter configurations for solar power systems: centralized, string, multi-string, and microinverter. It provides a comprehensive overview of the key benefits and main limitations of each topology, power capacity, and cost [43].

Table 2-1. Comparison between different inverter configurations

Inverter Configuration	Characteristics	Details
Central	Key Benefits	1. Cost-efficient because of the central inverter
	Main limitations	1. Non-flexible design. 2. Low reliability. 3. In case of inverter failure, it is not possible to provide power to the grid. 4. The functionality of the solar panel is affected when some parts of it are shaded. 5. The power loss is caused by issues such as single MPPT, string diodes, and mismatches in the PV modules. 6. Losses in high-voltage DC cables
	Cost & Capacity	• The cost is lower compared to string inverters. Power rating 1-50 MW
String	Key Benefits	1. Flexible design 2. Moderate reliability 3. The AC signal from each string is directed to a common AC bus, providing improved stability and safety measures against potential failures. 4. The power losses that occur in string diodes have been eliminated. 5. Minimizing the power loss caused by partial shading
	Main limitations	1. Utilized for lower power levels applications.
	Cost & Capacity	• Compared to centralized inverters, the cost is relatively higher. Power rating 1-50 MW / string.

Inverter Configuration	Characteristics	Details
Multi-String	Key Benefits	1. Voltage-boosting capability due to the use of DC-DC converters . 2. MPPT and current control function separately. 3. Losses in string diodes are eliminated. 4. Minimizing the power loss caused by partial shading.
	Main limitations	1. Integrating DC-DC converters leads to extra power losses. 2. The reliability of the system has decreased due to the use of a single inverter.
	Cost & Capacity	• Compared to centralized inverters, the cost is relatively higher. Power rating 50 MW.
Microinverter	Key Benefits	1. Elimination of bulk electrolytic capacitors increases the average life to 25 years. 2. Modularization makes it suitable for mass production. 3. Easy failure detection of the modules 4. Expandable and flexible design 5. No mismatch losses between modules 6. Suitable for residential use cases where partial shading is a significant concern.
	Main limitations	1. Difficulty of inverter replacement in case of any fault
	Cost & Capacity	• The cost is higher compared to string inverters, Power rating up to 600 W..

2.3 Classification of inverter topologies

The configurations of inverters in PV grid-connected system are categorized according to various factors including the number of power processing stages, and the types of transformers used (line-frequency or high-frequency).

2.3.1 Number of power processing stages

In PV grid-connected applications, there are two main inverter configurations based on power processing stages: single-stage and double-stage power processing. The single-stage configuration, shown in Figure 2-6 (a), consists of a DC-AC inverter that excludes the DC-DC converter stage. In contrast, the double-stage configuration includes a DC-DC converter, shown in Figure 2-6 (b). In the single-stage configuration, the inverter is responsible for carrying out various tasks such as MPPT, regulating the

grid current, and amplifying the voltage. In the double-stage configuration, the DC-DC converter performs voltage amplification and MPPT [43].

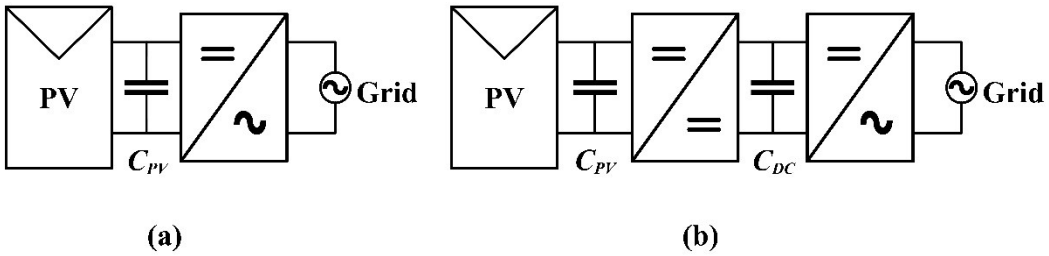

Figure 2-6. Two types of PV inverter (a) Single stage inverter, (b) Two stage inverter.

In the comparison presented in Table 2-2 between single-stage and double-stage grid-connected PV systems [44], it is interesting to note that the single-stage system is slightly more efficient overall, which makes it a more cost-effective option for lower rooftop solar capacities. However, its efficiency is impacted by higher DC bus voltage variations, requiring a larger capacitor. This leads to a slight increase in THD and a decrease in stability.

On the other hand, the double-stage system has lower efficiency because of the additional losses in the DC-DC converter stage. However, the double-stage system offers superior MPPT efficiency and stability due to minimal voltage variations. This makes it more suitable for larger solar farms and microgrid applications.

Table 2-2. Comparison between single and double power stages system

Aspect	Single-Stage System	Double-Stage System
Efficiency	Slightly more efficient overall.	Less efficient because of the power loss in the DC-DC converter stage.
MPP Tracking Efficiency	Lower due to higher DC bus voltage variations.	Higher due to minimal DC bus voltage variations.
Power Transformer Need	Required at low PV output voltage.	Not necessarily due to the ability to boost DC voltage or use isolated boost converters for galvanic isolation along with boost mechanism.
Cost	lower initial costs.	Higher initial costs.

Aspect	Single-Stage System	Double-Stage System
DC Bus Voltage Variations	Higher, requiring a bigger capacitor to minimize variations.	Lower, offering better stability.
DC Bus Voltage Stability	Lower stability; needs a bigger capacitor for stability.	Higher stability.
THD	Slightly higher.	Lower.
Suitability	More suitable for low rooftop solar capacity due to cost-efficiency and overall efficiency.	Recommended for large solar farms and microgrids to improve system stability.
Power Output Variations	Higher injected power variations.	Lower injected power variations.
Maximum Power Extraction	Lower than actual maximum power due to affected MPPT from DC bus voltage variations.	Closer to actual maximum power due to stable MPPT.

2.3.2 Transformer based and Transformerless inverters

Grid-connected PV inverters fall into two categories: isolated and non-isolated. The distinction is based on whether or not galvanic isolation exists between the power grid and the PV module [31]. Three different types of transformer-based inverters are used to isolate the PV grid-connected system. Each of these types has a unique configuration. The first type is the line frequency transformer. The second type is the high-frequency transformer embedded in a DC-DC converter. The third type is the high-frequency transformer that is embedded in an inverter. The different configurations of these types are in Figure 2-7 [31].

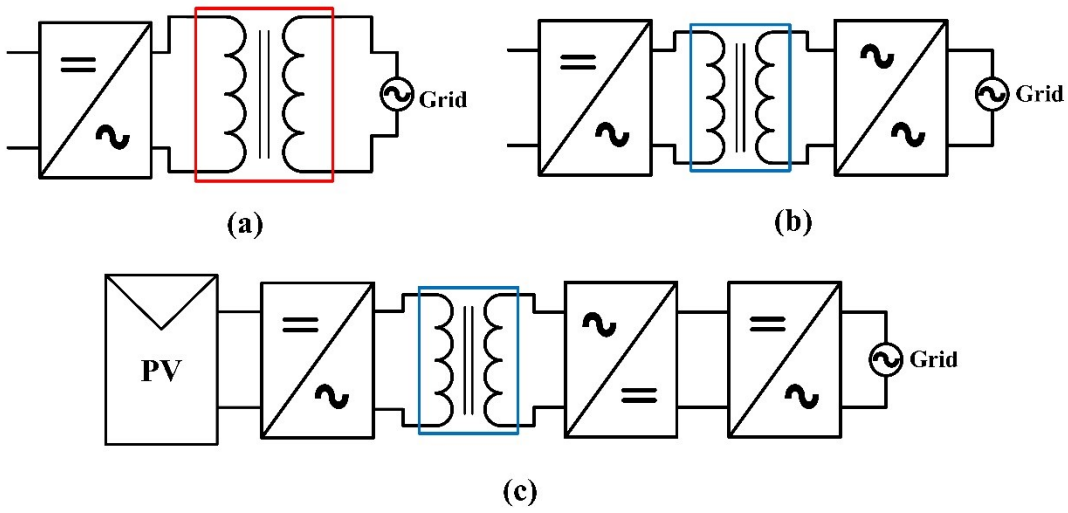

Figure 2-7. Transformer-based inverters. (a) Line-frequency transformer. (b) High-frequency transformer is embedded in ac/ac inverter. (c) High-frequency transformer is embedded in DC–DC converter

To monitor the galvanic isolation and regulate the DC voltage of the converter, a high-frequency transformer or a line-frequency transformer can be used . However, it is important to note that detecting galvanic isolation through a transformer can significantly impact the efficiency of the DC-to-AC conversion in grid-connected PV systems. Each country sets its own standards for galvanic isolation in a grid-connected PV system. In some countries, such as Italy and the United Kingdom, galvanic isolation is required [45], which can be achieved by using a low-frequency step-up transformer on the grid side or a high-frequency transformer on the DC side.

When designing a new converter, avoiding the line and frequency transformers is preferable due to their weight, size, and cost. Incorporating a high-frequency transformer requires multiple power stages, posing efficiency and cost challenges.

In certain countries like Spain and Germany, it is optional to incorporate galvanic isolation when other technological alternatives are available to keep the electrical grid and PV array separate [45]. A transformerless PV system is a typical

example of such an alternative, which simplifies installation and reduces the system's weight, cost, and size. However, the absence of a line frequency transformer may result in the production of DC current by the inverter, which can lead to overheating and failure. On the other hand, transformerless PV systems significantly improve total efficiency by 2%. A comprehensive summary of the comparison between different inverter transformer based and transformerless topologies is presented in Table 2-3 [46].

Table 2-3. Comparison between transformer-based and transformer-less inverter

Inverter Type	Advantages	Disadvantages
Transformer Based (Line-Frequency)	1. The design is simple. 2. It is highly reliable. 3. It is safe because of galvanic isolation.	1. The efficiency is low. 2. The weight and volume are high.
Transformer Based (High-Frequency)	1. The design is simple. 2. The efficiency is high. 3. The weight and volume are low. 4. It is safe because of galvanic isolation.	1. The technology is complex and expensive.
Transformerless	1. The efficiency is high. 2. The weight and volume are low.	1. The design is complex. 2. Safety measures are necessary

2.3.2.1 Transformerless inverters

The size of PV inverters with an isolation transformer on the grid side is quite large, making installation difficult and the system bulky. Topologies incorporating high-frequency transformers in the DC-DC converter experience decreased overall efficiency due to transformer leakage. Eliminating the transformer can result in a smaller, lighter, and more cost-effective inverter [47]. However, transformerless options present safety concerns related to the parasitic capacitances (PC) of the solar panel. The PV panels in these systems are directly connected to the power grid through the PV-to-ground PC, creating a conduction loop with the PV inverter and the utility

grid. The conduction loop allows the flow of LC induced by high-frequency CMV [47].

2.3.2.2 PV Panel Leakage Current (LC)

LC can have a negative impact on the system's performance and may result in various issues, such as current harmonics, safety concerns, higher power losses, and electromagnetic interference issues [48]. Various techniques are available to reduce LC, such as modifying the converter topology, incorporating filters, adjusting modulation schemes, and changing control schemes [49].

Due to their design, PV panels consistently demonstrate capacitance towards their surroundings, as shown in Figure 2-8 [47].

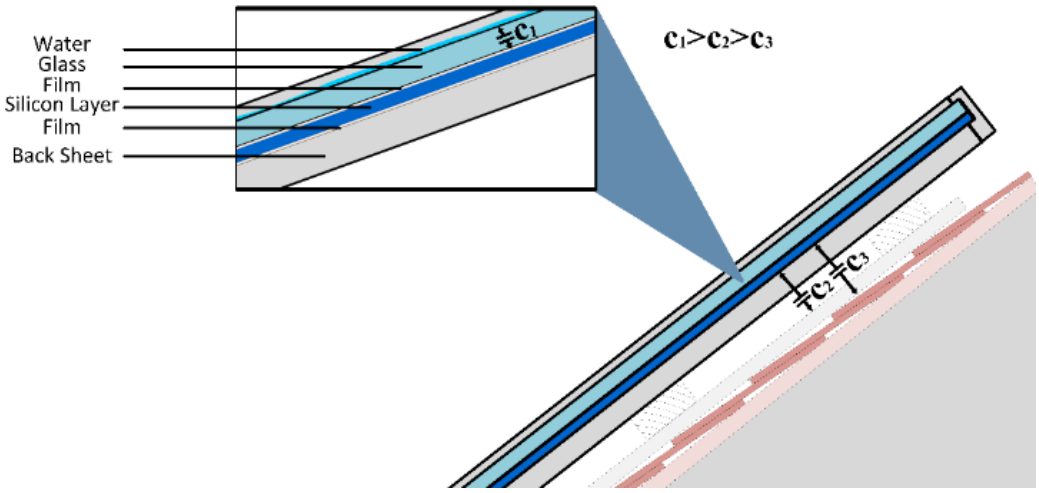

Figure 2-8. PC in the PV Panel Assembly.

The PC is caused by the installation process and the panel's mechanical structure. Isolated materials like films, glass, and back sheets act as dielectric layers between the cell terminals and the panel's metal frame, creating this capacitance. Hence, a PV system with high power output demonstrates a proportionately substantial PC, which will be further amplified in the presence of moisture on surfaces, such as rain or condensation.

C_1 dominates the total capacitance (C_{cm}) in rainy and damp conditions, while C_2 and C_3 are ignored. However, all PC must be considered in dry situations. As per [50],

the overall PC (C_{cm}) value can be approximated by considering a constant layer of water on the glass surface, resulting in high capacitance values. For Crystalline Silicon panels, the estimated value is 17 nF/m^2 or 110 nF/kW; for Thin Film Silicon, it is 16 nF/m^2 or 160 nF/kW .

Figure 2-9 shows the PV grid-connected system with the PC. Proper safety protocols require the PV panels' grounding and the grid's connection to the ground via the neutral conductor, which forms a conduction loop. Consequently, the produced LC will flow through the formed loop [47].

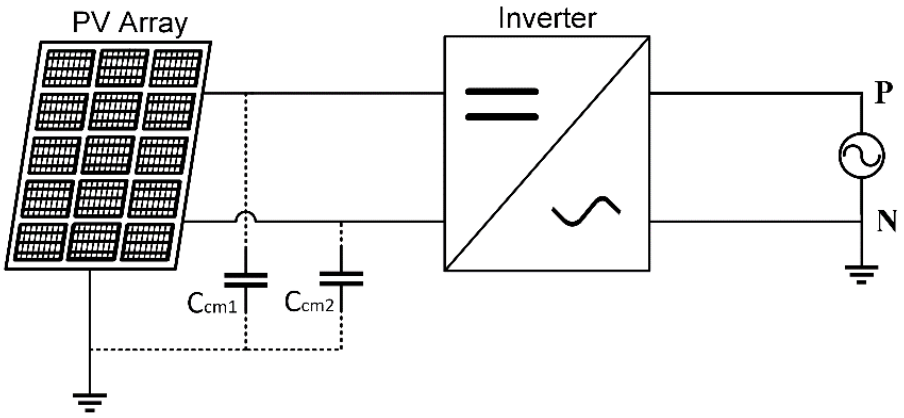

Figure 2-9. PV Grid-Connected System with PC.

2.3.2.3 PV Panel LC Mitigation

There are various approaches to reducing LC, as documented in the literature. Figure 2-10 illustrates some of these approaches. The first method involves modifying the conventional H-bridge inverter by incorporating additional IGBTs to create the H5 and H6 inverters [51], [52], [53]. By using proper modulation schemes, it is possible to maintain a constant switched CMV [54] or only with low-frequency components. Another method to mitigate LC is by adding an additional output filter stage, as reported in previous studies [55], [48], [56]. The third technique involves adjusting the modulation scheme of traditional inverters [57], [58], [59]. Lastly, changing the control scheme is an alternative option for addressing current leakage concerns [60].

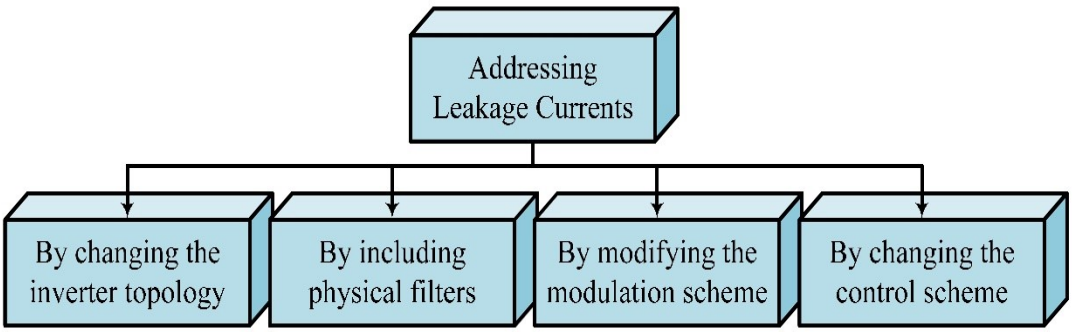

Figure 2-10. Strategies for reducing LC in transformerless inverters.

2.4 Non-isolated Boost DC-DC converters for PV applications

In a double-stage PV system configuration, a DC-DC converter is the first stage. Its purpose is to convert the variable and low input voltage to a fixed and high output voltage. The input voltage in a PV microinverter configuration can range from 12 to 60V. While the output voltage of the DC-DC converter depends on the application, it can reach as high as 760V for power system line transmission or as low as 24V for low-voltage applications like lighting and batteries [61]. Therefore, DC-DC converters play a significant role in boosting the limited and variable input voltage to the required high and fixed output voltage.

When connecting a PV system to the grid, one of the main challenges is to amplify the voltage to meet the voltage level requirement of the grid [62]. However, conventional boost converters cannot boost the voltage to a high level. To overcome this limitation, researchers have modified the existing DC-DC converters to step up the voltage while maintaining high levels of efficiency and reliability [62]. Based on the power and gain level, four different boost DC-DC converter topologies have been categorized as follows:

A. high-power high-gain (HPHG)

B. high-power low-gain (HPLG)

C. low-power high-gain (LPHG)

D. low-power low-gain (LPLG)

The LPHG topology group is widely used in PV systems among the four power and gain ranges of the modified topologies. The review paper [62] comprehensively compares 27 different LPHG DC-DC converters (with a conversion ratio of >15). These converters are categorized into seven different topology voltage-multiplier cells (VMCs) [63], [64], [65], [66], [67], voltage doublers [68], [69], [70], coupled inductor (CI) [71], [72], [73], [74], [75], coupled inductor and switched clamp (CI and SC) [76], [77], [75], [78], switched clamp and switched-inductor (SC and SI) [77], [79], [80], [81], Cascaded techniques [82], [83], [84], [85], and voltage-lift (VL) techniques [86], [87].

The VMC-based DC-DC converters are distinguished by their simpler design, modularity, and the ability to reduce the switch's voltage stress. Nevertheless, it has some limitations. For instance, it is incapable of maintaining a consistent and stable output voltage, and its high number of components (NOC) restricts the voltage gain as it depends on the NOC used. Compared to VMC, The DC-DC converter topology based on voltage-doubler has a simple design with fewer NOC, resulting in higher efficiency. Nevertheless, the voltage gain ratio is limited. The CI-based DC-DC converter topology is complex due to the requirement for complicated CI manufacturing. Compared to other converter topologies, it shows the highest level of efficiency, and it can handle relatively higher power. The topology based on CI and SC utilizes the highest number of switches and other components, making it more complex, but it provides low voltage stress and high efficiency. Similar to topology based on the CI and SC, the converter topology based on the SI and SC also has low switch voltage stress and high efficiency. However, it requires relatively more switches, making the system more complex. There are several variations of the DC-DC converter topology based on the cascade technique.

This technique is easy to apply because of its modular and simple structure. Nevertheless, this simplicity results in a higher number of required components. Besides, adding more active and passive components will reduce the efficiency of the converter. The VL technique-based DC-DC converter topology has a simple structure, presenting high efficiency, high voltage gain, and low switch voltage stress. Additionally, compared to other topologies, it has fewer NOC.

Figure 2-11 presents a detailed comparison of the seven converters based on several performance parameters, including the NOC, voltage stress on the switch (VSS), power-handling capability, complexity, maximum efficiency, and voltage gain. It is important to note that some parameter values are inversed: NOC, VSS, and complexity, where the high values on the graph correspond to smaller values. Therefore, the overall performance of each converter can be evaluated by calculating the total area of the rating parameter values of each converter.

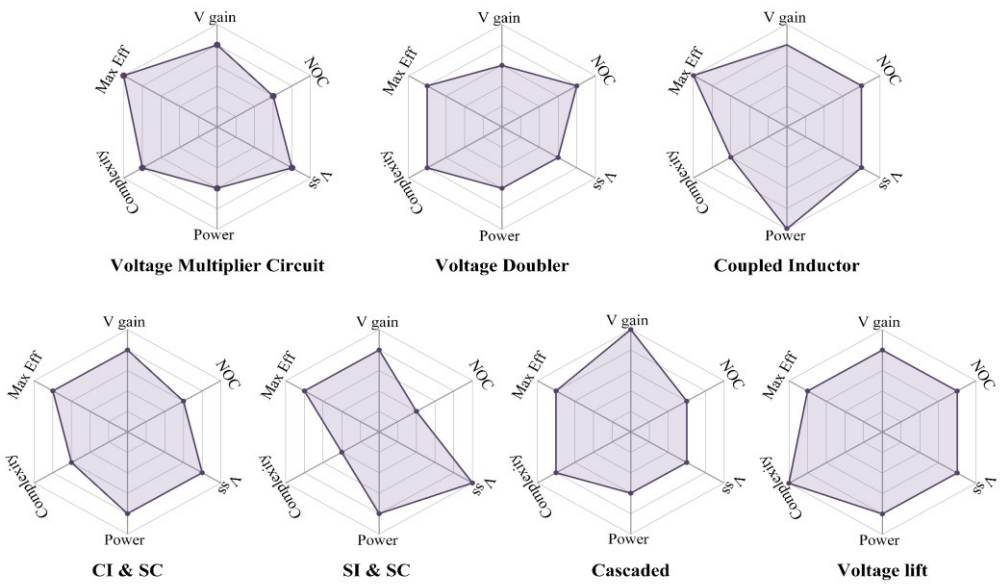

Figure 2-11. Performance comparison between non-isolated DC-DC boost converter topologies

2.4.1 Quadratic Boost Converter (QBC)

Power electronics converters play a crucial role in diverse applications, particularly in RE generation systems encompassing fuel cells, solar panels, and DC sources such as batteries. Due to the output voltage of these systems being lower than the nominal requisites of grid-connected inverters, it becomes crucial to employ DC-DC converters with high-voltage gain [88].

The Conventional buck-boost and boost can theoretically achieve high voltage gain by utilizing extreme duty cycles. Nevertheless, there are certain limitations that prevent voltage gain from reaching its maximum potential, such as switch speed, parasitic components, and power losses [89]. As a result, there are ongoing efforts to develop converters with high voltage gain and many have already been proposed. One example is the QBC topology introduced in [90].The model for the single-switch QBC is shown in Figure 2-12.

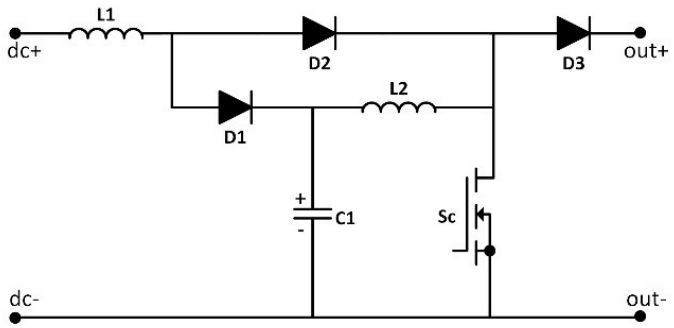

Figure 2-12. QBC Topology.

The QBC generates a steady and consistent DC voltage on the load side with no pulsation while having a high voltage gain [91]. Formula (2-1) presents the equation for QBC voltage gain.

$$\frac{V_{out}}{V_{dc}} = \frac{1}{(1-D)^2} \tag{2-1}$$

When compared to a conventional boost converter with equivalent input voltage

and duty ratio, QBC can achieve a higher voltage gain, as demonstrated in Figure 2-13.

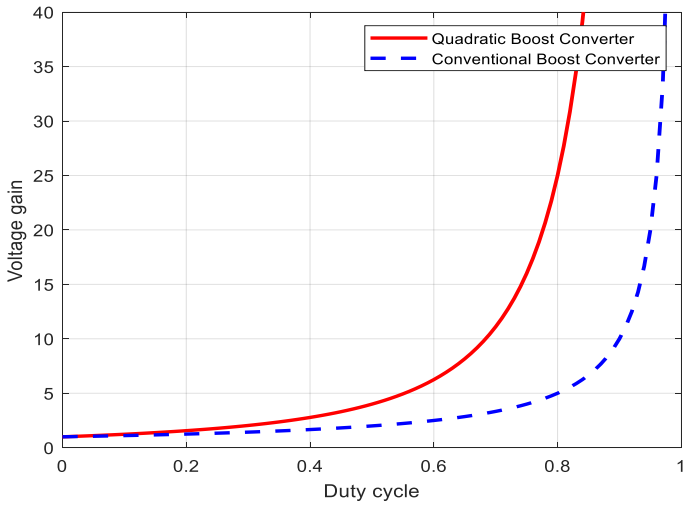

Figure 2-13. Input to Output Voltage Gain Ratio of QBC vs Boost Converter.

2.5 MPPT Controllers

The DC-DC converters in the PV systems are responsible for applying the MPPT control signal to extract the maximum power from the PV arrays [92]. These controllers track the MPP of the PV power and voltage characteristic curve—the P-V curve shown in Figure 2-14. However, the MPP can vary based on environmental factors like temperature and irradiation. So, to keep track of the MPP, the controllers must measure the PV voltage, current, or temperature. This information is then used to calculate the MPP, allowing the controller to calculate the duty cycle (D) optimally. The duty cycle is then applied to the DC-DC converter to ensure the system works at maximum power [92].

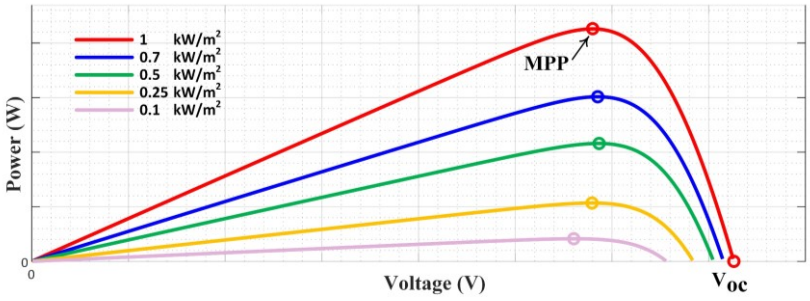

Figure 2-14. PV characteristic power–voltage curve under constant temperature.

Different MPPT methods have been proposed in the literature, each with advantages and disadvantages. Choosing a specific method can be challenging and depends on the intended application. Table 2-4 shows the characteristics of different MPPT techniques, including robustness, convergence speed, tuning, and complexity [92].

Table 2-4. MPPT techniques comparisons

MPPT Technique	Robustness	Convergence speed	Tuning	Complexity
Perturb and observe (P&O)	Yes	Varies	No	Low
Open-circuit voltage (V_{OC})	No	Medium	Yes	Low
Short-circuit current (I_{SC})	No	Medium	Yes	Medium
Pilot cell (Pilot-Cell)	No	Medium	Yes	Medium
Temperature algorithm (Temp)	No	Medium	Yes	High
Incremental Conductance (IC)	Yes	Fast	No	High
State space based (state-space)	No	Slow	Yes	High
Linear reoriented coordinate (LRC)	No	Slow	No	High
Sliding mode control (SMC)	Yes	Fast	No	Medium
Fuzzy logic control (FL)	Yes	Fast	Yes	High
Neural network (NN)	Yes	Fast	Yes	High
Particle swarm optimization (PSO)	Yes	Fast	Yes	High

The P&O, IC, SMC, FL, and NN techniques are marked as robust. This means that these techniques can perform well under varying conditions and maintain performance despite disturbances or changes in irradiation and temperature. Convergence speed is a critical parameter for MPPT techniques as it indicates how quickly the system can adapt to find the MPP when environmental conditions change. Techniques such as IC, SMC, FL, NN, and PSO are noted for their fast convergence speed. This is advantageous in dynamic environments where light intensity and other

factors affecting solar panel output can change rapidly. Techniques like P&O, IC, SMC, and LRC do not require tuning, which could make them easier to implement. Lastly, lower complexity techniques are easy to design and implement, as seen with P&O, Voc, and Isc.

One of the most commonly used methods by researchers in industry and laboratories is the P&O technique. This technique falls under the measurement and comparison techniques and is utilized to track the MPP [92]. Several models have been suggested for this algorithm—the P&O flowchart depicted in Figure 2-15 [93]. The system measures PV voltage (V) and current (I). Using these measured values, the system computes the power (P(j)) at the current iteration (i) by multiplying the voltage and current (V(i) * I(i)). The next step is a decision-making point where the system evaluates if the change in power (P(i) - P(i-1)) between the current and previous iterations is zero, greater than zero, or less than zero. If the change in power is exactly zero, the system does not alter the voltage. However, if the change in power is greater than zero, indicating an increase in power, the system checks the change in voltage (V(i) - V(i-1)). Depending on whether the voltage has increased or not, the system either decreases or increases the voltage by a small increment, represented as Δ.

Conversely, if the change in power is less than zero, the system again checks the change in voltage. If the voltage has not increased, it reduces the voltage by Δ. If the voltage has increased, it raises the voltage by Δ. Finally, the technique will return the reference PV voltage.

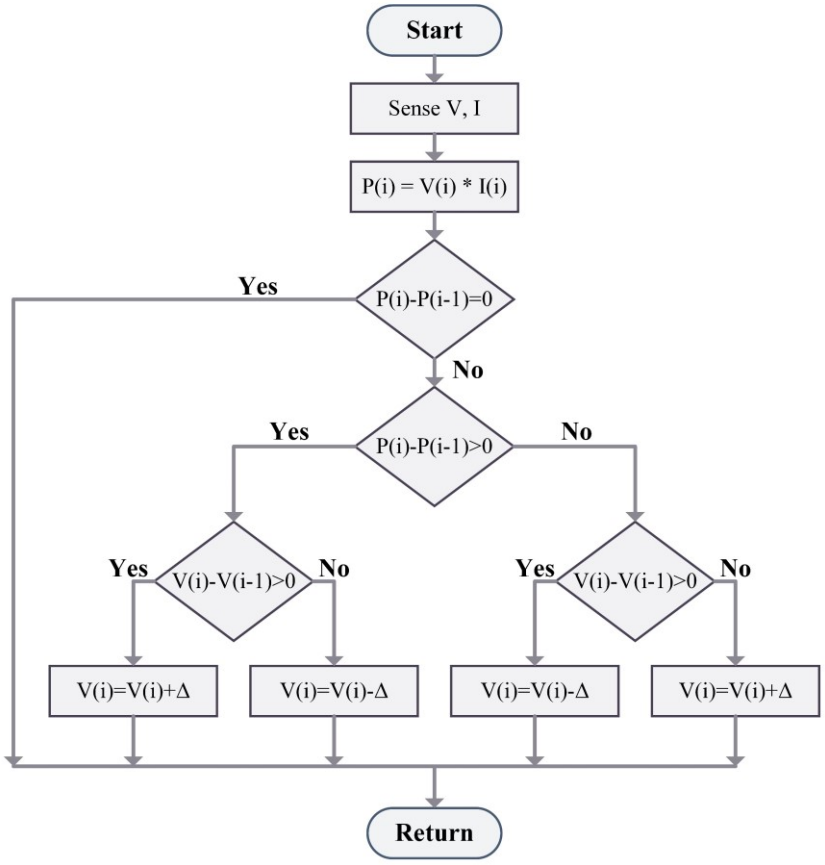

Figure 2-15. P&O algorithm fowchart

2.6 MLIs

An inverter is a device that has the ability to transform DC power to AC power. At first, inverters were primarily utilized to power lighting loads during grid outages [94]. However, in the present era, rapid developments in technology have significantly expanded the range of uses for inverters. In the past, the utilization of two-level inverters was prevalent. These inverters generated output with two different voltage levels [94]. However, they result in significant switching losses, and high harmonic voltage resulted in a flow of harmonic current in the circuit, leading to further losses. In order to address the limitations associated with existing inverters, certain advancements have been made to enhance their performance. One such improvement involves increasing the number of levels in the inverter, allowing for the generation of a pure sinusoidal waveform at the output voltage. This modification also enables the

suppression of harmonics in the output voltage and reduces the percentage of losses [94]. This enhanced inverter topology is commonly referred to as a MLI topology. As stated by reference [95], a MLI provides several benefits in comparison to the two-level inverter. The advantages encompass a reduction in the adverse impact of distortion caused by harmonics, the generation of a pure sine waveform through the utilization of multiple voltage levels, the capability to function at both fundamental and high switching frequency PWM, diminished losses incurred during switching, improved power quality, and a low rate of voltage variation. MLIs do exhibit several limitations. One such negative is their reliance on a considerable number of switches despite their relatively lower individual ratings. The complexity and cost of the entire system are increased due to the interrelation between each switch and its corresponding gate-driving circuit.

The use of the NPC-MLI is common in industrial and commercial drive applications, especially for three levels [96]. Its advantage is that it only needs a single DC source for all three legs. However, when it comes to more than three levels, balancing the capacitor voltage becomes a significant issue, which makes the inverter more complicated due to the need for a larger number of devices [97]. The Flying Capacitor MLI has a similar structure to the NPC inverter, but it replaces the clamping diode with a flying capacitor. This inverter does not pose any issues for three levels, but at output voltage levels above three, regulating the capacitor's voltage can be problematic [98]. The CHB-MLI has a modular design advantage, but its application is limited due to the requirement for isolated DC sources [99]. In 2008, the PUC-MLI was created as a modification of the CHB-MLI. This involved removing two lower switches and directly connecting two U-cells by adjusting the upper two switches. The PUC inverter has the fewest devices needed for specific output levels among all MLIs [100].

Table 2-5 compares different inverter topologies used in PV grid-connected applications based on LC, input voltage, number of switches, and efficiency [101].

Table 2-5. Non-isolated MLI topologies for grid-connected PV applications comparison.

Topologies	Leakage Current	Input Voltage	Switches		Efficiency (%)
			Transistors	Diodes	
Half Bridge	Moderate	700	2	-	*
Conergy NPC	Very Low	800	3	4	**
Full Bridge	Moderate	400	4	-	*
Dual-Buck	Low	400	4	2	****
NOC	Very Low	400	4	2	**
Three-Level NPC	Very Low	800	4	2	***
H5	Low	400	5	-	***
Single-Buck	Moderate	400	5	1	**
HB-ZVR	Low	400	5	5	*
Virtual DC Bus	Low	400	5	-	**
HERIC	Low	400	6	2	***
H6	Low	400	6	2	***
HRE	Low	400	6	6	****
oH5	Very Low	400	6	-	***
Cascaded	Moderate	400	8	-	-

The Half Bridge and Full Bridge topologies have a moderate LC, which indicates a balanced approach but may not be the most suitable for applications requiring minimal LC. On the other hand, the Conergy NPC, NPC, and Three-Level NPC topologies have very low LC, making them an excellent choice for systems where LC must be minimized to prevent power loss and potential safety hazards. The Dual-Buck, H5, HB-ZVR, Virtual DC Bus, HERIC, and H6 topologies have low LC but may not be as effective as those with very low LC.

2.6.1 PUC

The PUC inverter is classified as a multilevel topology, with cells that consist of two switching devices and one capacitor per cell. The inverter's total number of switches is determined by the quantity of cells, denoted as n. Specifically, there will be $2n$ switches, with each cell containing two switches that function in a complimentary

fashion. Additionally, the inverter will include *n*-2 capacitors. An instance of a PUC inverter of three cells would include six switching devices, a single DC source, and a flying capacitor. This results in a reduced NOC needed for the same number of output voltage levels when compared to other seven-level MLIs, as shown in Table 2-6 [102].

Table 2-6 Comparion between different seven-level inverter topologies.

Topologies	Power Semiconductor Switches	Clamping Diodes	Capacitors	Control Complexity
Diode Clamped	12	10	6	Very High
CHB	12	0	3	Low
Flying Capacitor	12	0	6	Very High
Hybrid CHB	8	0	2	High
PUC 7-level	6	0	1	Very High

The PUC inverter has the potential to be designed at many levels, including five-levels [103], seven-levels [104], nine-levels [105], fifteen levels [106], or thirty-one levels [21]. Figure 2-16 presents the topology of five and seven levels PUC. It is composed of three sets of two active switches each, with each set of switches (S_1 and S_4, S_2 and S_5, and S_3 and S_6) operating in a complementary manner. The capacitor serves as the secondary DC source, and it must be maintained at a certain value by careful regulation in order to get the levels on the output waveform that are needed. In the case of five-level the flying capacitor should be regulated at one-half of the DC source while in the seven level at one-third of DC source.

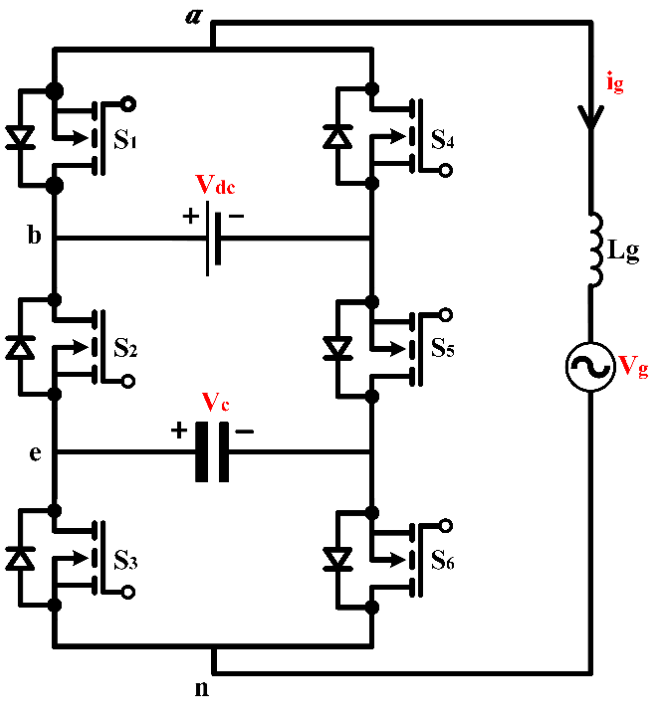

Figure 2-16. Grid-tied PUC topology

Table 2-7 presents a switching table for five-level and seven-level PUC inverters. In the five-level output PUC, the eight states generate five different output levels 0, ±E, and ±2E, where E equals the flying capacitor voltage. In seven-level output PUC, the eight states generate seven different output levels 0, ±E,±2E, and ±3E.

Table 2-7. Five-Level and Seven-Level PUC Switching States.

State	[S_1,S_2,S_3]	Output Voltage	Five-Level PUC (V_{an})	Seven-Level PUC (V_{an})
1	[0,1,1]	$-V_{dc}$	-2E	-3E
2	[0,1,0]	V_c-V_{dc}	-E	-2E
3	[0,0,1]	$-V_c$	-E	-E
4	[0,0,0]	0	0	0
5	[1,1,1]	0	0	0
6	[1,1,0]	V_c	E	E
7	[1,0,1]	V_{dc}-V_c	E	2E
8	[1,0,0]	V_{dc}	2E	3E

The PUC topology is unsuitable in high-power applications that need an output voltage higher than the input DC source, as the PUC's maximum output voltage level is restricted to the DC source voltage. Additionally, the capacitor can only charge

through one path in this topology, leading to problems when there is an energy shortage and a lengthy interval between the charging and discharging phases [22].

2.6.1.1 Modelling of PUC inverter

The status of the PUC inverter is determined by a switching function, S_i. The function equals 0 when switch S_i is inactive and 1 when switch S_i is active. The inverter has three switches, numbered 1 through 3; this binary status indication applies to all of them.

The inverter output voltage can be expressed as (2-2), based on the circuit diagram shown in Figure 2-16.

$$V_{an} = V_{ab} + V_{be} + V_{en} \tag{2-2}$$

The switching function (S_i) can be used to compute the voltages V_{ab}, V_{be}, and V_{en}, (2-3).

$$\left.\begin{array}{c} V_{ab} = (S_1 - 1)\, V_{dc} \\ V_{be} = (1 - S_2)\, (V_{dc} - V_c) \\ V_{en} = (1 - S_3)\, V_c \end{array}\right\} \tag{2-3}$$

The output voltage (V_{an}) of the inverter can be calculated using (2-3) as shown in (2-4).

$$V_{an} = (S_1 - S_2)\, V_{dc} + (S_2 - S_3)\, V_c \tag{2-4}$$

2.6.1.2 PUC Control Techniques

Extensive research has been conducted on using PWM techniques to control PUC inverters. One approach involves sensor-less voltage balancing techniques, which use proportional-integral (PI) linear controllers to ensure balanced voltage levels and minimize steady-state error. These controllers employ feedback loops that incorporate phase-locked loops (PLL) for power factor control, which is crucial for reactive power exchange with the grid. Overall, this research aims to improve the efficiency and effectiveness of PUC inverters [103].

In a research paper [107], the authors analyzed two different PWM techniques: level-shifted (LS-PWM) and phase-shifted (PS-PWM). These techniques were used in PUC inverter. The authors used both triangular and sawtooth carriers and examined the effect of each technique on system distortion, as well as how the controllers should be designed to work with them. They found that using triangular carriers is better than sawtooth carriers because it reduces distortion and is more suitable for solar panels and connection to the power grid.

A six-band hysteresis control scheme has been used for controlling a seven-level PUC inverter. This method aims to generate near-sinusoidal current and meet international standards. It achieves this by implementing PI control schemes for DC bus voltages and producing line current references for unity power factor operation [23]. A fourteen-band hysteresis controller has also been proposed for a fifteen-level PUC inverter. This controller reduces harmonic distortion and improves energetic efficiency [108].

Researchers have developed Artificial Neural Networks (ANN) based on the Levenberg-Marquardt algorithm to control the PUC inverter. These networks offer robustness against disturbances, self-tuning capabilities, and high performance in handling system dynamics [109]. The Adaptive Neural Fuzzy Inference Systems (ANFIS) controller has also been developed to regulate the PUC inverter. This controller incorporates NN and FL and has been shown to be effective in regulating capacitor voltage and load current, especially under nonlinear load conditions [110].

2.6.2 CSC

The CSC is a modification of the PUC that adds two crossover switches between the capacitor and the DC source, hence overcoming the limitations of PUC [22]. With this upgrade, there are now nine possible charging states, up from seven in the previous

topology (PUC). CSC has a voltage-boosting capability to boost voltage to the sum of DC source and capacitor voltages. The inclusion of two more switches enables the capacitor to be charged through several pathways. This ensures the flying capacitor's voltage remains stable, regardless of any alterations to the DC voltage source or load.

Table 2-8 presents a comparison among various nine-level topologies, such as Classic and hybrid CHB, flying capacitor, PUC and CSC [111]. The CSC is unique in its ability to generate nine-level output voltage while using the least number of power semiconductor switches and capacitors.

Table 2-8 Comparion between different nine-level inverter topologies.

Topologies	Power Semiconductor Switches	Capacitors
CHB	16	3
Flying Capacitor	16	8
Hybrid CHB	12	2
PUC 9-level	8	2
CSC	8	1

As presented in Figure 2-17. The CSC topology utilizes S_7 and S_8, two cross-section switches, and two bidirectional switches, S_2 and S_5, to generate two additional higher output levels. These levels are the combined values of the DC input source and the voltages across the capacitors. Table 2-9 comprehensively represents the various potential switching states of the CSC inverter. Assuming a DC input source voltage of 3E and a flying capacitor voltage of E, it also presents the output voltage V_{an}. As shown in the table, the CSC has 16 switching states, producing nine output voltage levels ranging from 0 to ±4E. This shows that the inverter can increase the output voltage and provide the load more power than the conventional PUC inverter.

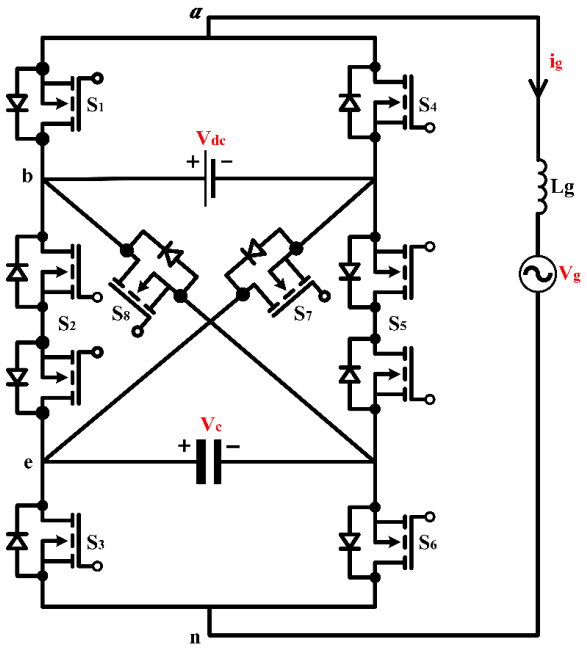

Figure 2-17. Grid-tied Crossover Switches Cell topology.

Table 2-9. Crossover Switches Cell (CSC) Switching States.

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output Voltage	V_{an}
1	1	0	0	0	0	1	1	0	$+V_{dc}+V_c$	+4E
2	1	0	0	0	1	1	0	0	$+V_{dc}$	+3E
3	1	0	1	0	0	0	1	0	$+V_{dc}$	+3E
4	1	0	1	0	1	0	0	0	$+V_{dc}$ $-V_c$	+2E
5	0	0	0	1	0	1	1	0	$+V_c$	+E
6	1	1	0	0	0	1	0	0	$+V_c$	+E
7	0	0	1	1	0	0	1	0	0	0
8	1	1	1	0	0	0	0	0	0	0
9	0	0	0	1	1	1	0	0	0	0
10	1	0	0	0	0	1	0	1	0	0
11	0	0	1	1	1	0	0	0	$-V_c$	-E
12	1	0	1	0	0	0	0	1	$-V_c$	-E
13	0	1	0	1	0	1	0	0	$-V_{dc}$ $+V_c$	-2E
14	0	0	0	1	0	1	0	1	$-V_{dc}$	-3E
15	0	1	1	1	0	0	0	0	$-V_{dc}$	-3E
16	0	0	1	1	0	0	0	1	$-V_{dc}$ $-V_c$	-4E

2.6.2.1 Modelling of CSC inverter

The CSC inverter operates using eight switches, numbered 1 through 8. The inverter's status is determined by a switching function, S_i. When a switch S_i is inactive, its function value is 0. Conversely, when the switch S_i is active, its function value is 1.

This binary status indication applies to all the inverter's switches.

The inverter output voltage (V_{an}) can be expressed as (2-5), based on the circuit diagram shown in Figure 2-12.

$$V_{an} = V_{ab} + V_{be} + V_{en} \tag{2-5}$$

The switching function (S_i) can be used to compute the voltages V_{ab}, V_{be}, and V_{en}, (2-6).

$$\left.\begin{array}{c} V_{ab} = (S_1 - 1)\, V_{dc} \\ V_{be} = (1 - S_2 - S_8)\, V_{dc} - (1 - S_2 - S_7)\, V_c \\ V_{en} = (1 - S_3)\, V_c \end{array}\right\} \tag{2-6}$$

The inverter output voltage (V_{an}) can be calculated using (2-6) as shown in (2-7).

$$V_{an} = (S_1 - S_2 - S_8)\, V_{dc} + (S_2 - S_3 + S_7)\, V_c \tag{2-7}$$

2.6.2.2 CSC Control Techniques

In order to control CSC in [22], a control strategy is employed that focuses on achieving a zero power factor and balancing the voltage of the flying capacitor. This is achieved through the use of a dual PI controller approach. The voltage of the capacitor is initially compared with a reference value, which is set at one-third of the DC source voltage. The difference between the two values is then fed into the first PI controller, which calculates the reference current that is aligned with a sinusoidal wave. The reference current is then compared to the actual load current, and any deviations are addressed by a second PI controller. The final output from this controller is a modulation reference wave that guides the logic comparator block in the inverter, ensuring that the desired output voltage levels are maintained with stability and precision.

2.7 Control Strategies for MLI topologies for Grid-Connected PV Systems

Different types of controllers are used for PV grid-connected systems. These controllers are categorized into linear, predictive, robust, non-linear, adaptive, and intelligent. This categorization is based on grid behavior and operating conditions [112], [36]. Figure 2-18 illustrates this categorization.

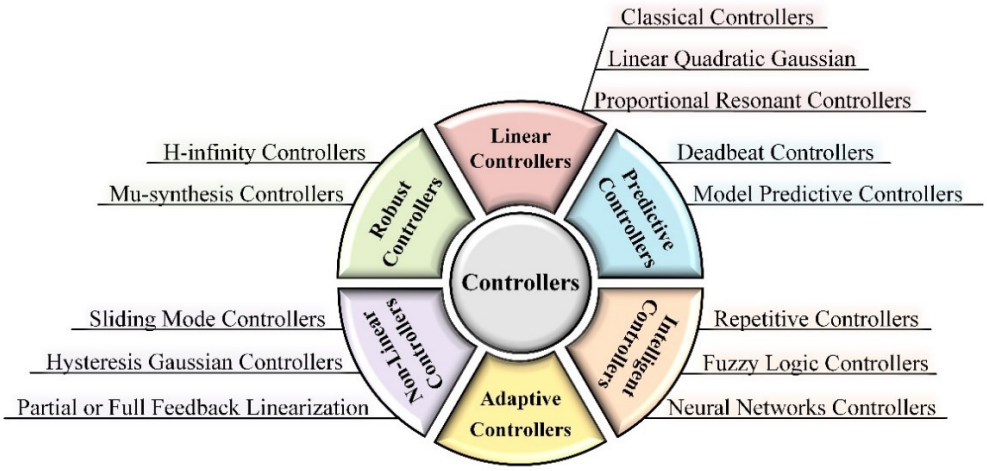

Figure 2-18 Different types of inverter control strategies

Table 2-10 presents a comparison of six different control techniques [113]. Predictive techniques use models to forecast future system behavior and optimize control actions to enhance efficiency under varying conditions. Its ability to anticipate and mitigate power quality issues is a significant advantage, contributing to more stable and reliable system performance. However, this technique has challenges, as it requires accurate system models and a higher investment in computational resources and additional sensors. These requirements can lead to increased costs and implementation complexity. Moreover, the scalability and responsiveness of the predictive control method are directly influenced by the sophistication and accuracy of the predictive models employed. Despite these challenges, the predictive approach is a compelling choice for applications where dynamic control is critical for system performance and efficiency.

Table 2-10. Comparison between different inverter control strategies

Control Technique	Advantages	Disadvantages
Linear	1. Simple to implement. 2. good steady-state performance and stability. 3. widely used. 4. lower initial implementation costs.	1. Cannot handle nonlinearities effectively. 2. Cannot handle disturbances effectively. 3. Potential power quality issues (e.g., harmonic distortion). 4. Less efficient under dynamic conditions. 5. Not highly scalable.
Non-Linear	1. Effectively handles nonlinear characteristics. 2. Potentially optimizes efficiency. 3. Mitigates power quality problems. 4. Adaptable to system changes for better stability.	1. Complex implementation 2. Requires accurate system modeling. 3. Scalability and response time vary with algorithm complexity.
Predictive	1. Optimizes control actions based on the system's future behavior. 2. Improved efficiency. 3. Anticipates and mitigates power quality issues. 4. Stable as it considers future behavior.	1. Requires accurate models. 2. Higher computational resources and additional sensors. 3. Increased costs and complexity. 4. Scalability and response time depend on the predictive model.
Adaptive	1. Good performance under varying conditions. 2. Handles uncertainties/parameter variations. 3. Maximizes efficiency. 4. Adapt for power quality and stability. 5. Responsive to changes.	1. Needs online parameter estimation. 2. Sensitive to modeling errors/noise. 3. Complexity increases with adaptability.
Intelligent	1. Robust performance under varying conditions. 2. Uses AI to adjust actions adaptively. 3. Higher overall efficiency. 4. Adaptable to dynamic environments.	1. The cost is high since advanced hardware, sensors, and computational resources are required. 2. Design and tuning complexity can be challenging. 3. Scalability depends on the chosen architecture.

Control Technique	Advantages	Disadvantages
Robust	1. Stable and reliable performance, even amid uncertainties and disturbances. 2. Maintains high efficiency, power quality, and stability. 3. Fast response and scalable. 4. Reasonable implementation costs.	1. Requires accurate modeling. 2. Potentially higher implementation complexity, 3. Compared with non-linear and intelligent techniques in optimal conditions, it is less efficient

2.8 Model Predictive Control (MPC)

The utilization of MPC in power electronics and drives research has increased due to its ability to handle multivariate cases, system constraints, and nonlinearities, despite its significant computational demands [114]. The MPC is widely used for its precise mathematical model's ability to predict controlled variable behavior in mechanical and electrical systems [114].

The MPC concept involves using a precise model to forecast controlled variable behavior over a prediction horizon (N) and optimizing the cost function to produce the system's control action sequence [115]. In each sampling period, the algorithm executed and always uses the optimal sequence's first value in the system at instant *k*. There are various forms of cost function, and the general form is as (2-8):

$$g = \sum_{i} \lambda_i \left(x_i^* - x_i^p\right)^2 \tag{2-8}$$

The variables x_i^* and x_i^p denote the reference and predicted values, respectively, of variable x_i, The index i represents the number of controlled variables, while λ_i is the weighting factor. This basic approach enables control systems to manage multiple objectives, nonlinearities , and constraints. The predicted values, x_i^p , are derived from the controlled model.

2.8.1 MPC in Power Converters

The growing utilization of MPC in power converters is a result of advancements

in digital microcontrollers [25], [27]. Controlling power converters and drives requires high computational power within a short sampling time. To solve this issue, the following methods are suggested:

1) The optimization problem can be effectively addressed through multiparametric programming, which enables offline solution. The implementation of this approach is relatively straightforward, requiring only basic calculations and referencing a look-up table [116].
2) The Generalized Predictive Control (GPC) technique is utilized as an online optimization approach. GPC allows longer prediction horizons without significantly raising computational costs. When GPC is utilized for power electronics and drives, it does not consider the switching of power semiconductors [115], [117].
3) One viable technique for implementing MPC strategies in power converters is using a discrete methodology. This methodology involves applying the cost function to forecast the controlled variables behavior based solely on the switching states of the power converters. Known as Finite-Control-Set Model Predictive Control (FCS-MPC), this approach exclusively considers a limited set of control actions [118].

2.8.2 FCS-MPC Principle

The FCS-MPC refers to a type of MPC controller that utilizes the discrete properties of power converters to decrease the computational burden associated with MPC strategies. This is feasible because the system response only requires evaluating the specified switching states these devices can provide [114]. The FCS-MPC fundamental control diagram is depicted in Figure 2-19, illustrating the utilization of a generic converter to deliver power to a generic load, with the ability to operate in n

distinct switching states. The main purpose of control is to ensure that the variable x accurately follows the desired reference value x^*. The FCS-MPC method consists of several fundamental steps [119] . 1) The initial step involves measuring and/or estimating the controlled variables. 2) Apply the optimum switching state that was determined during the preceding sample interval. 3) Using the mathematical model, forecast the behavior of variable x in the following sample period for each switching state of the converter. 4) The cost function, or error, evaluated for each prediction by calculating the absolute difference between the predicted value (x_{pi}) and the actual value (x^*), denoted as $g = |x^* - x_{pi}|$. 5) The optimal switching state that minimizes the cost function denoted as S, is selected and stored to be applied to the converter during the next sampling period.

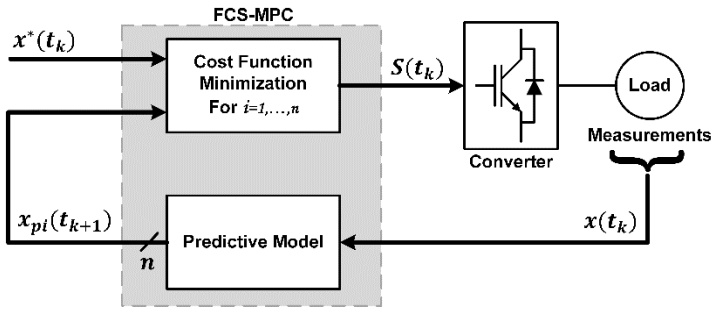

Figure 2-19. Fundamental FCS-MPC Control Diagram

The FCS-MPC algorithm depicted in Figure 2-20 [120], The algorithm starts by measuring a parameter during each sampling period. A predictive model is used to calculate a future value based on the measured value, which is then compared to a reference value. The converter is switched to the state that reduces the cost function. This process is repeated for each sampling interval.

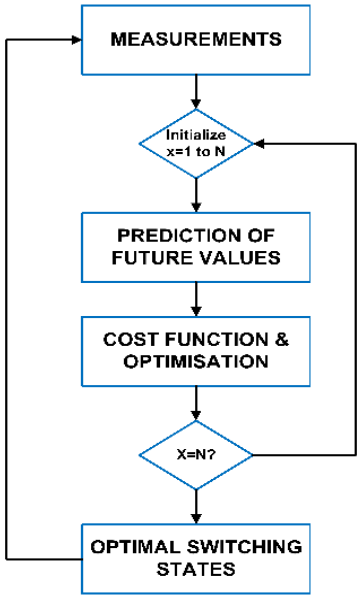

Figure 2-20. MPC Algorithm

2.8.3 FCS-MPC for PUC and CSC

FCS-MPC has been used to control PUC in various grid-connected systems, including the DC-source grid-connected system, shown in Figure 2-16. In [121], the researcher presents a real-time implementation of FCS-MPC controlling a 7-level PUC inverter. [111] and [122] presents a simulation (Simulink/Matlab) for FCS-MPC controlling 9-level and 15-level PUC inverters. In [123] and [124], the researchers added a PV array to the system. In [123] the researchers added the PV in parallel with the flying capacitor, achieved the MPP, and balanced the flying capacitor voltage using cost function optimization. In [124], the DC source was replaced with a capacitor, and the PV array was added in parallel with the replaced capacitor. The researcher applied a P&O to get the voltage reference value and used this value in the cost function to achieve PV MPP.

Authors in [125], [126] , and [127] present the FCS-MPC, controlling seven, nine, and fifteen-level PUC inverters in the PV grid-connected system and adding a DC-DC boost converter. The DC-DC converter boosts the PV input voltage and tracks the PV

voltage MPP. In [126], the current oriented IC MPPT algorithm is used. The main objective of all FCS-MPCs is to achieve grid-connected current injection with unity power factor and minimal THD while keeping the capacitor voltage balanced, regardless of the operating conditions.

The [128] has implemented FCS-MPC for a nine-level CSC in a DC source grid-connected system, as shown in Figure 2-17. The designed controller guarantees low grid current THD and unity power factor while maintaining the flying capacitor voltage around its reference.

2.8.4 LC Control in PV Systems using FCS-MPC

The researchers in [60] employed FCS-MPC to regulate the H-bridge neutral-point-clamped (H-NPC) inverter in a grid-connected PV system to attain minimized neutral-point voltage, effective DC-link voltage control, and unity power factor. In addition, the predictive controller's performance has been improved by incorporating a constraint on the average device switching frequency to mitigate the rate of change of voltage (dv/dt). The primary contribution of this study is implementing a predictive model-based control strategy to mitigate the LC resulting from PC in solar modules.

To reduce the LC, it is crucial to minimize the voltage across the PC. The topology in [60] shows that there are five different PC voltages in eight switching states and five output voltages, namely ($\pm V_{dc}/2$, $\pm V_{dc}$, 0). Therefore, the inverter can generate five different voltage levels, but the researcher decided to eliminate two of them ($\pm V_{dc}$ /2) to reduce the PC voltage range. This decision was made because the other levels ($\pm V_{dc}$, 0) share the same PC, V_{dc} and 0. To mitigate the LC, the researcher used a fixed reference value at V_{dc} as it repeatedly more than 0.

2.9 Summary

The selection of a microinverter PV grid-connected system configuration is preferred due to its ability to eliminate the mismatch losses between the models effectively and to eliminate the bulk capacitors. However, this configuration has a maximum input power of 600W, which results in a low input voltage that needs to be boosted. To address this, a double-stage system can be employed. Furthermore, using a transformerless system is necessary to reduce the system's cost, volume, and weight while maintaining a high level of reliability. Nevertheless, the transformerless grid-connected PV system raises significant safety concerns, particularly due to the potential for PV panel LC caused by the PV panel structure.

In this study, a non-isolated QBC will be employed as a part of cascaded techniques to boost the PV input voltage. This type of converter has a high efficiency and high voltage gain, and to regulate its operation, a P&O MPPT technique will be implemented due to its low complexity. Previous research has explored various non-isolated inverters in transformerless systems and has been extensively studied, with some papers highlighting mitigating LC using different techniques. However, it has been observed that the PUC and CSC inverters are not covered and studied in a transformerless systems. Besides, the controller that will be used is FCS-MPC because it has been used to mitigate LC and because it is a multi-objective controller, which will be a good choice to reduce the LC, control the grid output current, and control the flying capacitor of the inverters.

Figure 2-21 illustrates a double-stage transformerless microinverter PV grid-connected system that will be designed and simulated in the following chapters.

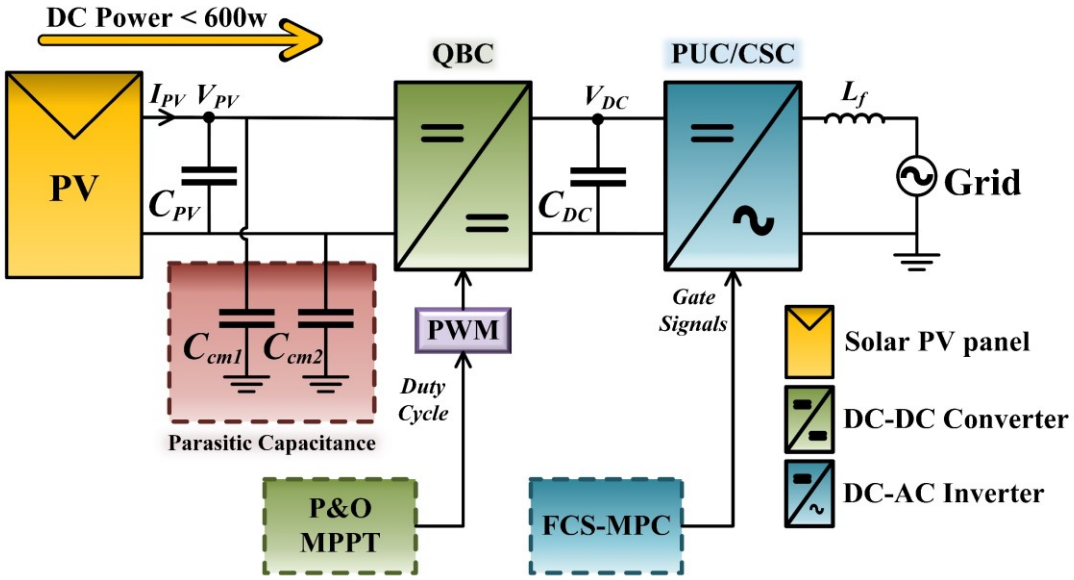

Figure 2-21. double-stage transformerless microinverter PV grid-connected system

CHAPTER 3: SYSTEM DESIGN

3.1 Introduction

In this chapter, a comprehensive design of the system depicted in Figure 2.21 will be presented. This system will be divided into six different systems, each employing different configurations of inverters and integrating PV panel PC to address specific design challenges. The focus will be on the PUC inverter and the CSC inverter, with the first three systems utilizing the PUC inverter and the remaining three utilizing the CSC inverter. The thesis's main contribution concerns Systems 3 and 6. On the other hand, Systems 1, 2, 4, and 5 will be utilized to examine the impact of PC on the systems and compare them with the proposed Systems 3 and 6.

PUC Inverter Systems

System 1: Basic PUC Inverter Configuration

This system employs a PUC inverter without incorporating components of PV panel PC. This configuration serves as a foundational model, allowing an understanding of the PUC inverter's baseline performance and characteristics in PV applications, the system depicted in Figure 3-1. The design of transformerless microinverter using a high gain DC-DC Converter and PUC Inverter proposed in [129].

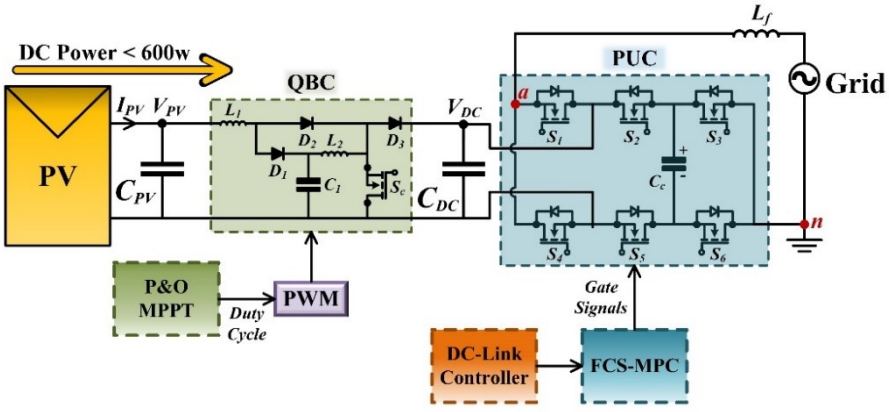

Figure 3-1. System 1: Double-stage transformerless microinverter PV grid-connected system uses a PUC inverter.

System 2: PUC Inverter with PC Consideration

This system integrates PV panel PC components. However, it does not address the control of PV panel LC; this system allows for the study of the PV panel LC in the system and emphasizes the need to mitigate it or not.

System 3: PUC Inverter with PC Consideration and LC Mitigation Control

This system and system 2 have the same circuit configuration where the PV panel PC is added, as Figure 3-2 presents. However, the proposed FCS-MPC will mitigate the PV panel LC in this system.

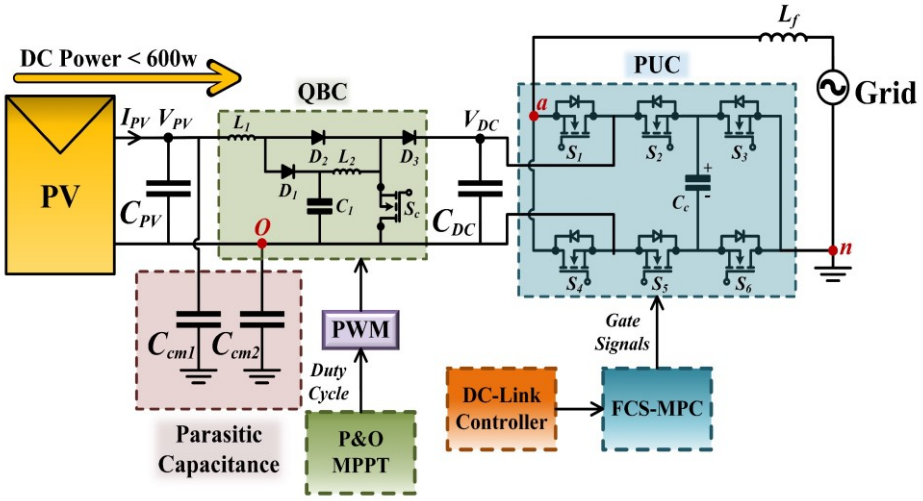

Figure 3-2. System 2 and 3: Double-stage transformerless microinverter PV grid-connected system uses a PUC inverter and added PC.

CSC Inverter Systems

System 4: Basic CSC Inverter Configuration

Mirroring the System 1 approach taken with the PUC inverter, this system utilizes a CSC inverter without PV panel PC components. This configuration serves as a foundational model and allows an understanding of the baseline performance and characteristics of the CSC inverter in PV applications, the system depicted in Figure 3-3.

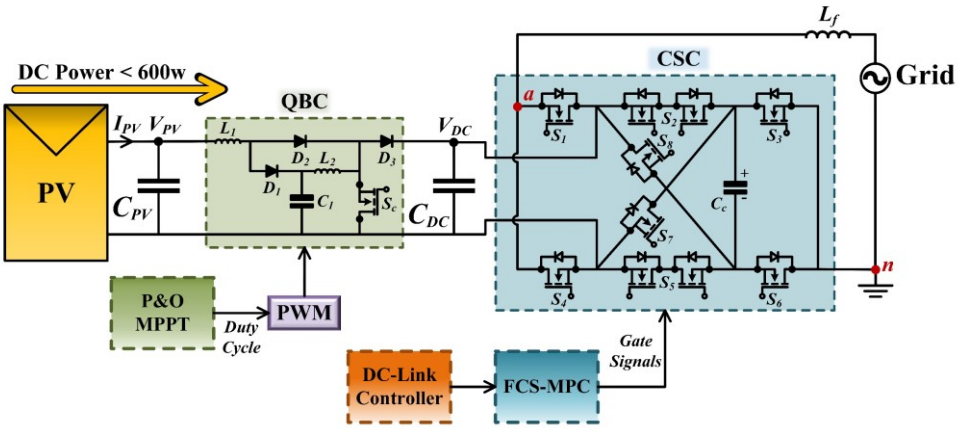

Figure 3-3. System 4: Double-stage transformerless microinverter PV grid-connected system uses a CSC inverter.

System 5: CSC Inverter with PC Components Consideration

This system integrates PV panel PC components, as Figure 3-4 presents. However, it does not address the control of PV panel LC; this system allows for the study of the LC in the system and emphasizes the need to mitigate it or not.

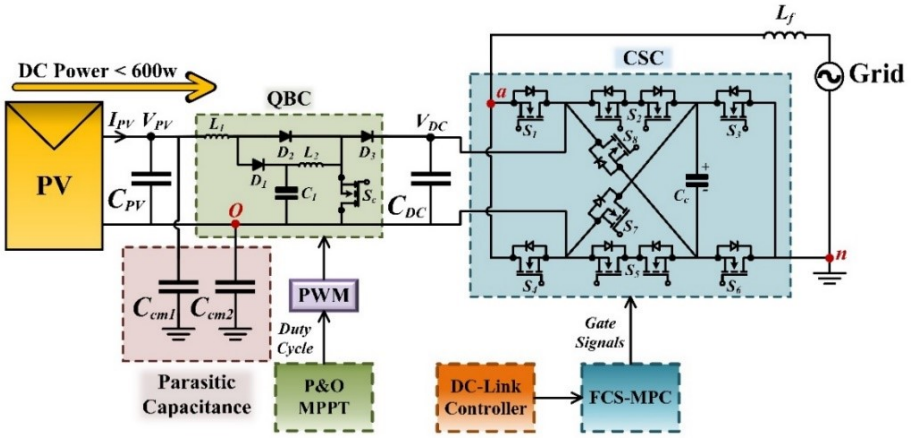

Figure 3-4. System 5 and 6: Double-stage transformerless microinverter PV grid-connected system uses a CSC inverter and added PC.

System 6: CSC Inverter with PC Consideration and LC Mitigation Control

This system and system 5 have the same circuit configuration where the PV panel PC is added, as Figure 3-4 presents. However, the proposed FCS-MPC will mitigate the PV panel LC in this system.

3.2 Chapter Structure

The chapter is comprised of three main sections. The first section pertains to the design of common components in all systems, such as PV array , PC, QBC, MPPT, and DC-Link controller. The second section discusses the PUC topology and mathematical model, and an FCS-MPC design for Systems 1 and 2 will be presented, as they share the same inverter controller. This will be followed by an FCS-MPC for System 3. The third section covers the CSC topology and mathematical model and includes the FCS-MPC design for Systems 4 and 5 and the FCS-MPC design for System 6.

3.3 Common Components Design

3.3.1 PV Modules' Selection

The design for the microinverter requires a maximum power of 600 W from the PV array at optimum operating conditions of 1000 W/m^2 and 25^{o}C. This power requirement has been chosen based on the information in [43]. To meet this requirement, the Trina Solar TSM-300PDG14 module, with a voltage of 36.9V, has been selected. The module specifications presented in Table 3-1 were found to be suitable, and only one PV panel will be used.

Table 3-1. TRINA SOLAR TSM-300PDG14 Spesifications

Parameters	Value
Maximum power P_{mpp} (W)	300
Cells per module (N_{cell})	72
Short-circuit current I_{sc} (A)	8.6
Open circuit voltage V_{oc} (V)	45.3
Maximum current I_{mpp} (A)	8.13
Maximum voltage V_{mpp} (V)	36.9

3.3.2 PV Panel PC Estimation

The maximum PC that can be found in a thin film silicon PV panel is 16nF per square meter or 160nF per kW. The Trina solar panel has dimensions of 1.956m in length and 0.992m in width. Therefore, the total PC is estimated to be around 31nF, which is the product of the estimated PC per meter square and the area of the panel.

3.3.3 QBC Design

The QBC is designed to operate in continuous conduction mode (CCM) based on (3-1) – (3-4) and using the parameter values specified in Table 3-2.

$$i_{L1,(Min,Max)} = i_{L2,(Min,Max)} = \frac{I_{o,(Min,Max)}}{(1-D)^2} \tag{3-1}$$

$$L_{1,(Min,Max)} = \frac{V_{DC} \times D}{\Delta i_{L1,(Max,Min)} \times f_s} \tag{3-2}$$

$$L_{2(Min,Max)} = \frac{V_{DC\times} D}{\Delta i_{L2,(Max,Min)} \times (1-D) \times f_s} \tag{3-3}$$

$$C_{1,(Min,Max)} = \frac{I_{o,(Min,Max)} \times D}{\Delta V_{C1} \times (1-D) \times f_s} \tag{3-4}$$

The values calculated for inductors L_1 and L_2 are 16 mH and 45 mH respectively, and the capacitor C_1 is 150 µF.

Table 3-2. parameters' values used to design QBC

Parameters	Value
Duty Cycle D	0.65-0.7
Voltage source (V)	36.9,33.6
Minimum output current (A)	0.076
Maximum output current (A)	0.813
Current Ripple L_1,L_2 (%)	10
Voltage Ripple C_1 (%)	2.5
Switching frequency f_s (kHz)	25

3.3.4 P&O MPPT

The P&O MPPT controller is designed to track the MPP of the PV P-V characteristic curve. The controller takes the PV voltage and current as input and follows the logic in the flowchart in Figure 2-15. The output reference voltage is subtracted from the PV voltage to determine the error, which is input into the PWM generator block. The output signal from this block is sent to the QBC. The block diagram of the controller is shown in Figure 3-5.

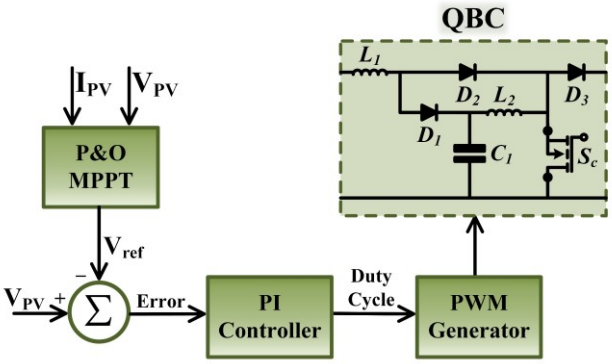

Figure 3-5. MPPT controller block diagram

3.3.5 DC-Link Controller

The primary purpose of the DC-Link controller is to ensure that power is transmitted from the PV to the grid sides. Additionally, it regulates the DC-Link voltage around three times the PUC/CSC flying capacitor voltage. To achieve this, the DC-Link PI controller receives the input of the difference between the DC-Link voltage measured and reference values. It generates the amplitude of the reference grid current ($|I_g^*|$), which will be multiplied by a sine wave in phase with the grid voltage. The sine wave is obtained by calculating the phase angle of the grid voltgae using a PLL. The block diagram of the controller is shown in Figure 3-6.

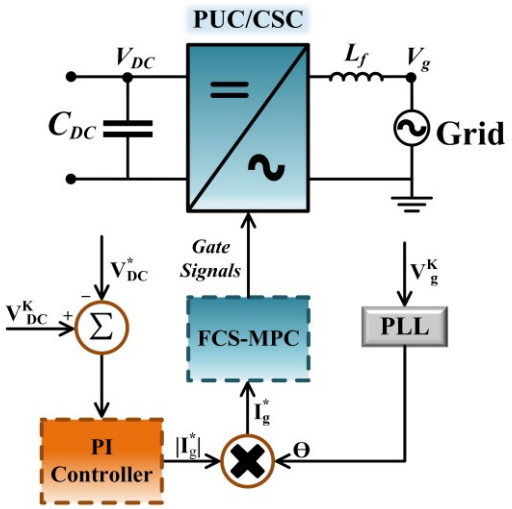

Figure 3-6. DC-Link controller block diagram

3.4 PUC Systems Design

3.4.1 PUC inverter mathematical model

Equations (3-5) to (3-7) for the PUC mathematical model are derived using Kirchhoff's laws for the circuit in Figure 3-1.

$$(1-D)^2\, i_{PV}(t) - C_{DC}\frac{dV_{DC}(t)}{dt} = (s_2 - s_1) i_g(t) \tag{3-5}$$

$$C_c \frac{dV_c(t)}{dt} = (s_3 - s_2) i_g(t) \tag{3-6}$$

$$L_g \frac{di_g(t)}{dt} = (s_1 - s_2) V_{DC}(t) + (s_2 - s_3) V_c(t) - V_g(t) \tag{3-7}$$

3.4.2 Design FCS-MPC for Systems 1 and 2

The main objective of the FCS-MPC is to maintain a balanced voltage of the inverter flying capacitor V_c while ensuring a unity power factor on the grid side and maintain the grid current THD under 5%. The instantaneous grid current $i_g(k)$ and inverter capacitor voltage V_c (k) serve as the state variables for this process. In order to obtain the predicted values $i_g(k+1)$ and V_c $(k+1)$, the Euler forward approximation is utilized for (3-6) and (3-7), with T_S being the sampling period. The predicted values of $i_g(k+1)$ and V_c $(k+1)$ can be calculated by applying (3-8) - (3-9) to the seven switching states [125].

$$i_g(k+1) = i_g(k) + \frac{T_s}{L_g}\left[(s_1 - s_2) V_{DC}(k) + (s_2 - s_3) V_c(k) - V_g(k)\right] \tag{3-8}$$

$$V_c(k+1) = V_c(k) + \frac{T_s}{C_c}(s_3 - s_2)\, i_g(k) \tag{3-9}$$

The cost function **A** is calculated using the values of (3-8) - (3-9). From (3-10), the value of $\boldsymbol{A}$ is obtained [125].

$$\boldsymbol{A} = \sqrt{\lambda\left(\frac{V_c^* - V_c(k+1)}{\Delta V_{c,max}(k)}\right)^2 + \left(\frac{i_g^*(k) - i_g(k+1)}{\Delta i_{g,max}(k)}\right)^2} \tag{3-10}$$

Where $\Delta V_{c,max}(k)$, and $\Delta i_{g,max}(k)$ are represent the maximum variations in the

capacitor voltage and grid current, respectively, and can be obtained from (3-11) and (3-12) [125].

$$\Delta V_{c,max}(k) = \frac{2i_g(k)}{C_c}\, T_s \tag{3-11}$$

$$\Delta i_{g,max}(k) = \frac{2V_{DC}(k)}{L_g}\, T_s \tag{3-12}$$

The $\Delta V_{c,max}(k)$, and $\Delta i_{g,max}(k)$ calculated using the (3-11)-(3-12) ; these values normalize the state variables due to the differing magnitudes of the two variables' values. Voltages are typically recorded in hundreds of volts, while currents only amount to several amperes.

In equation (3-10), λ serves as a weighting factor that prioritizes either capacitor voltage or grid current regulation. The selection of this factor is generally guided by the objective to maintain the grid current's THD at 5% or less.

The PUC capacitor voltage reference value is one-third DC-link voltage, and the grid current amplitude reference value will be calculated from the DC-link PI controller, and the phase from PLL controller.

The flowchart presented in Figure 3-7 , illustrates the step-by-step process for a FCS-MPC algorithm for System 1 and 2.

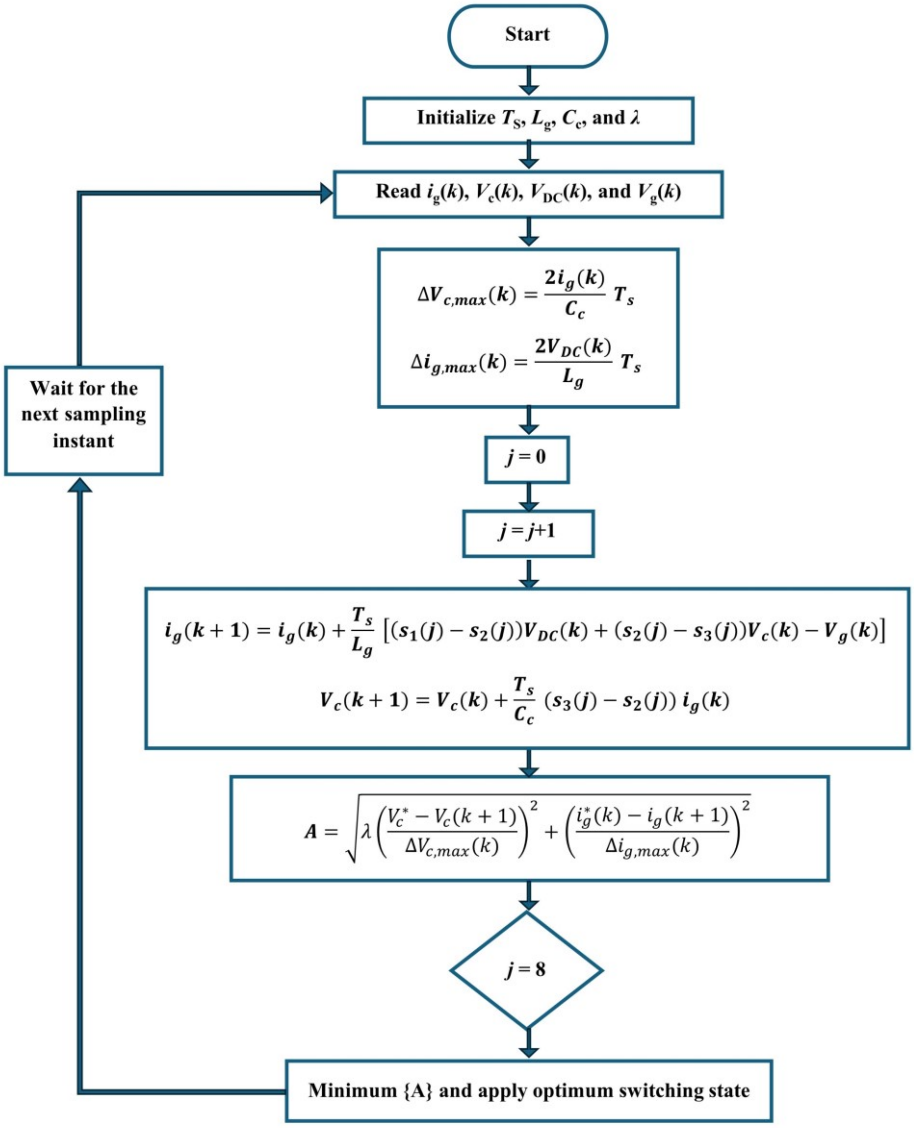

Figure 3-7. FCS-MPC Algorithm of System 1 and 2

The process begins by initializing the sampling time, grid filter inductance, flying capacitor capacitance, and weighting factor. Next, the algorithm reads the grid current and voltage, flying capacitor voltage, and DC-link voltage. It then calculates the maximum variations in the flying capacitor voltage and in grid current. An iteration counter is set to zero and incremented with each cycle. The algorithm then computes the predicted grid current and flying capacitor voltage values using the initialized and read values. Additionally, the calculations involve the switching status corresponding

to the iteration counter, as per Table 2-7. After computing these values, the cost function is calculated. This loop continues until the iteration counter reaches eight. At this point, the algorithm applies the optimum switching state. The process is repeated cyclically, waiting for the next sample to iterate again.

3.4.2.1 Weighting Factor Selection

The value of the weighting factor λ for the cost function (3-10) can be determined by minimizing the THD of the grid current (less than or equal to 5%) and the variation in the voltage across the PUC capacitor (less than 0.5%) [125]. The graph in Figure 3-8 shows the relationship between THD, ΔV_c, and λ. A weighting factor of 0.1 was chosen, resulting in a THD of 2.67% and a capacitor voltage variation of 0.25%.

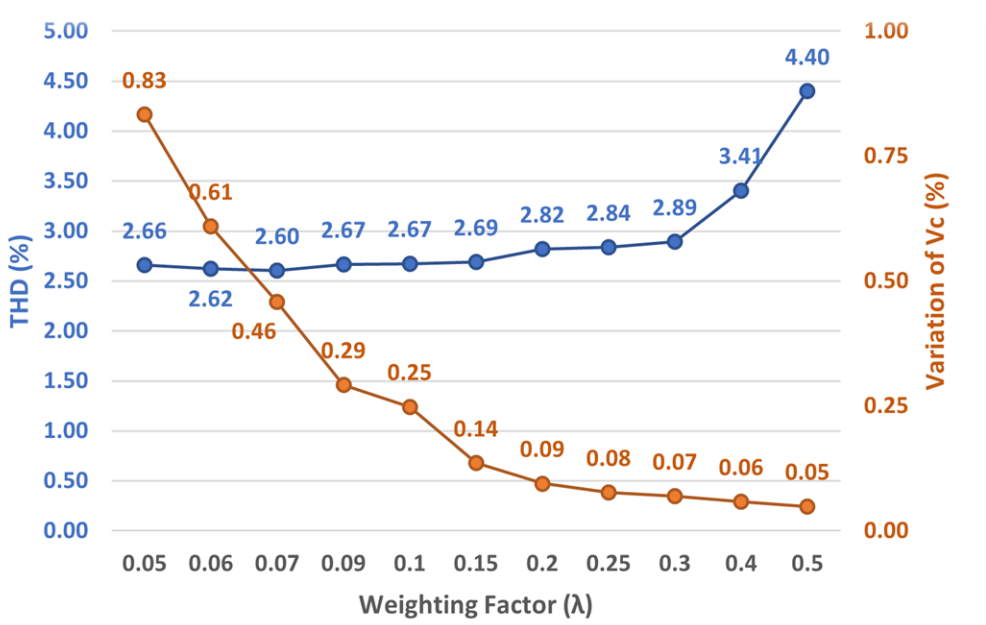

Figure 3-8. THD (%) and ΔVc (%) vs Weighting Factor (λ)

3.4.3 Design FCS-MPC for System 3

The FCS-MPC in System 3 has the same objectives as FCS-MPC in System 1 but with extra PV LC mitigation aim which will be done by controlling the CMV across the PV panel PC (V_{cm2}), so a new state variable will be added V_{cm2}. The $V_{cm2}(k)$ can be calculated using the (3-13) - (3-16) that derived from Figure 3-2.

$$V_{an}(k) = V_{ao}(k) + V_{on}(k) \quad (3\text{-}13)$$

$$V_{an}(k) = (s_1 - s_2)V_{DC}(k) + (s_2 - s_3)V_c(k) \quad (3\text{-}14)$$

$$V_{on}(k) = V_{cm2}(k) \quad (3\text{-}15)$$

$$V_{ao}(k) = V_{DC}(k) \times s_1 \quad (3\text{-}16)$$

Substitute (3-13) - (3-15) in (3-16) to get the CMV equation (3-17).

$$V_{cm2}(k) = (-s_2)V_{DC}(k) + (s_2 - s_3)V_c(k) \quad (3\text{-}17)$$

From equation (3-17) the predictive value for CMV obtained (3-18)

$$V_{cm2}(k+1) = (-s_2)V_{DC}(k+1) + (s_2 - s_3)V_c(k+1) \quad (3\text{-}18)$$

According to Equation (3-17) the $V_{DC}(k+1)$ has to be calculated, so by applying Euler forward approximation for Equation (3-5), the predicted value $V_{DC}(k+1)$ obtained as depicted in Equation (3-19).

$$V_{DC}(k+1) = V_{DC}(k) + \frac{T_s}{C_{DC}}\left[(1-D)^2 \times i_{PV}(k) - (s_2 - s_1)i_g(k)\right] \quad (3\text{-}19)$$

The cost function **B** is calculated using the values of (3-8), (3-9), and (3-17). The value of **B** is obtained from equation (3-20),.

$$\boldsymbol{B} = \sqrt{\lambda_1\left(\frac{V^*_{cm2}(k) - V_{cm2}(k+1)}{\Delta V_{cm2,max}(k)}\right)^2 + \lambda_2\left(\frac{V^*_c - V_c(k+1)}{\Delta V_{c,max}(k)}\right)^2 + \left(\frac{i^*_g(k) - i_g(k+1)}{\Delta i_{g,max}(k)}\right)^2} \quad (3\text{-}20)$$

To reduce the LC, the voltage variation across the CM capacitor must be minimized so the reference value (V^*_{cm2}(k)) chosen to be $V_{cm2}(k)$, and the V_{cm2} maximum variation ($\Delta V_{cm2,max}$) is $V_{DC}(k)$, besides, λ_1 *and* λ_2 are the weighting factors. The FCS-MPC System 3 algorithm presented in Figure 3-9.

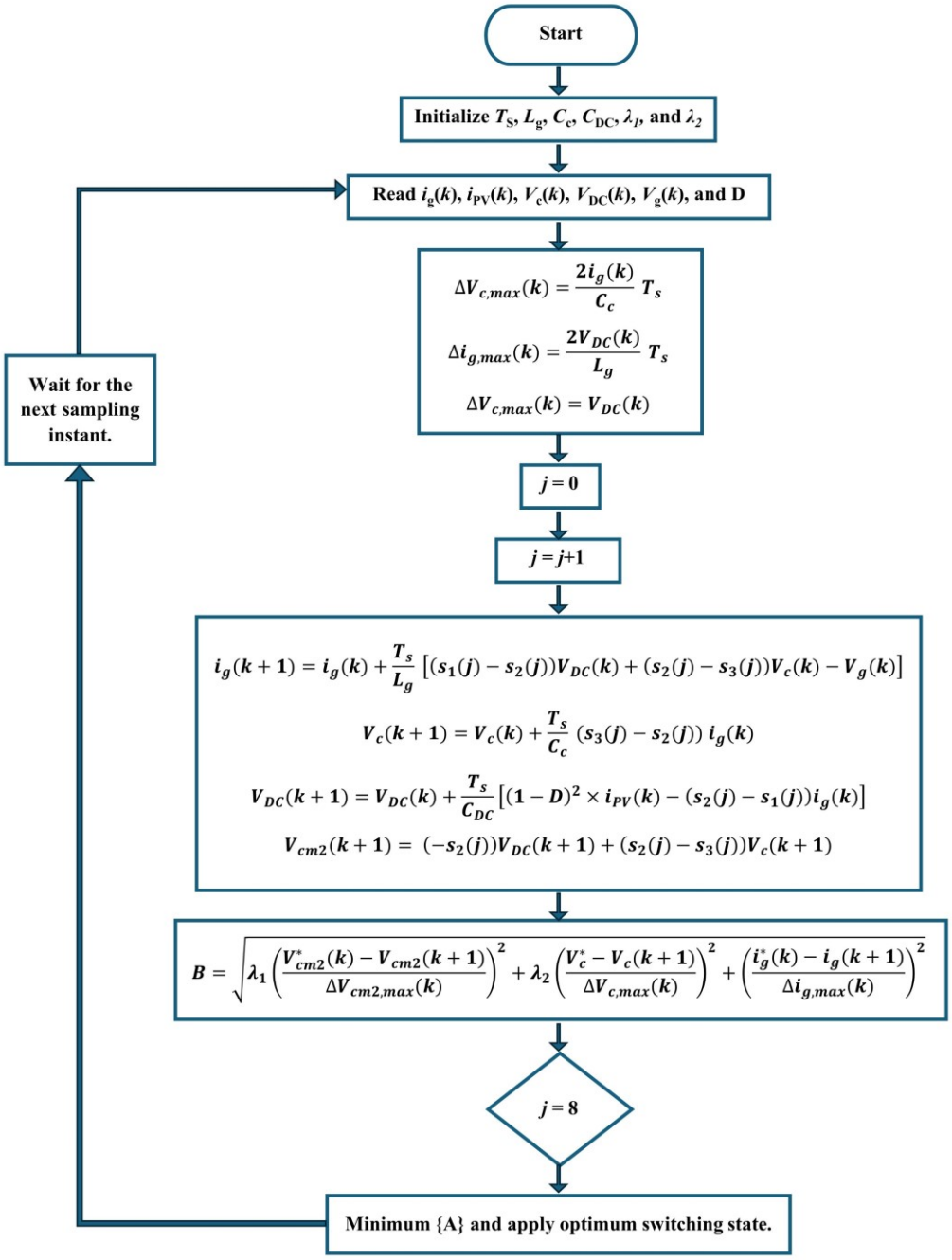

Figure 3-9. FCS-MPC Algorithm of System 3

3.4.3.1 Weighting Factor Selection

To ensure the optimal functioning of the FCS-MPC, precise tuning of the parameters λ_1 and λ_2 is crucial in Equation (3-20). The goal of the FCS-MPC is to keep the grid current THD below 5% following the IEEE-519-2014 Standard, the RMS PV panel LC below 300 mA as per the DIN VDE 0126-1-1 Standard, and the PUC

capacitor voltage variation below 0.5%. The weighting factors are adjusted based on these constraints. The variance is then calculated using Equation (3-21).

$$Variance = Var\left(\left(\frac{THD\%}{5}\right), \left(\frac{I_{cm2}(RMS)}{0.3}\right), \left(\frac{\Delta V_c}{0.5}\right)\right) \quad (3\text{-}21)$$

The results of the simulations performed using varying weighting factors are shown in Figure 3-10. The simulation range for λ_1 is from 0.3 to 0.6, while for λ_2, it is between 0.05 and 0.2 . The optimal values for λ_1 and λ_2 are 0.4 and 0.1, respectively. These values lead to the lowest overall variance.

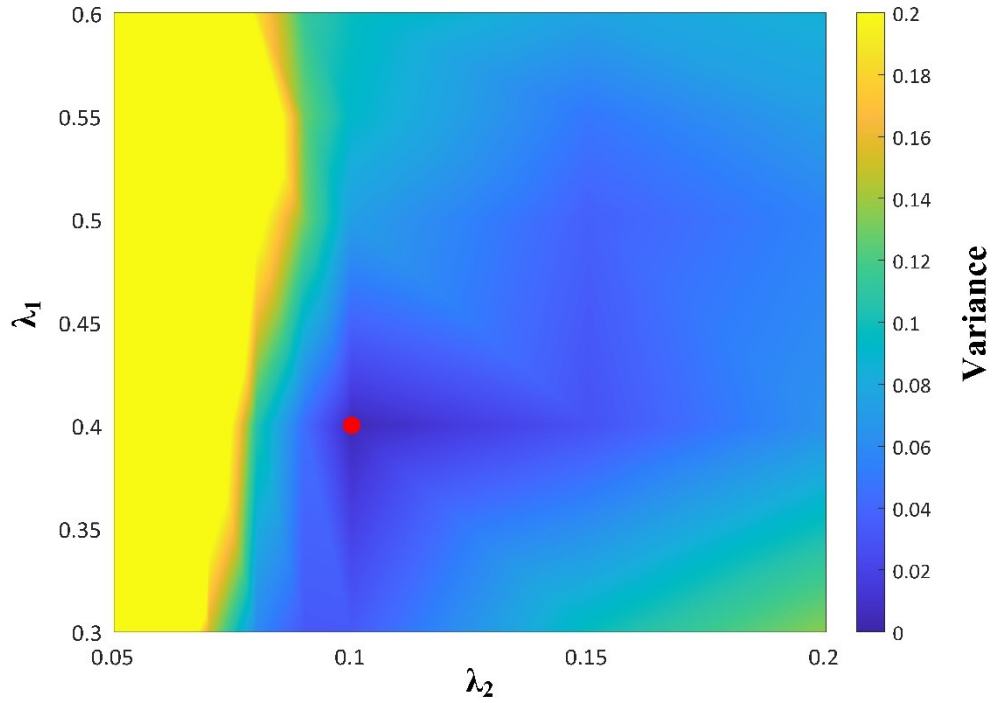

Figure 3-10. Heatmap plot for different λ_1 and λ_2 Vs. the variance

3.5 CSC Systems Design

3.5.1 CSC inverter mathematical model

Equations (3-22) to (3-24) for the CSC mathematical model are derived using Kirchhoff's laws for the circuit in Figure 3-3.

$$(1-D)^2\, i_{PV}(t) - C_{DC}\frac{dV_{DC}(t)}{dt} = (s_1 - s_2 - s_8) i_g(t) \quad (3\text{-}22)$$

$$C_c \frac{dV_c(t)}{dt} = (s_3 - s_2 - s_7) i_g(t) \tag{3-23}$$

$$L_g \frac{di_g(t)}{dt} = (s_1 - s_2 - s_8) V_{DC}(t) + (s_2 - s_3 + s_7) V_c(t) - V_g(t) \tag{3-24}$$

3.5.2 Design FCS-MPC for Systems 4 and 5

The FCS-MPC in Systems 4 and 5 and Systems 1 and 2 share the main objectives to maintain a balanced voltage of the inverter flying capacitor V_c while ensuring a unity power factor on the grid side and maintain the grid current THD below 5%. The instantaneous grid current $i_g(k)$ and inverter capacitor voltage $V_c(k)$ serve as the state variables for this process. In order to obtain the predicted values $i_g(k+1)$ and $V_c(k+1)$, the Euler forward approximation is utilized for (3-23) and (3-24) with T_S being the sampling period. The predicted values of $i_g(k+1)$ and $V_c(k+1)$ can be calculated by applying (3-25)-(3-26) to the sixteen switching states [128].

$$i_g(k+1) = i_g(k) + \frac{T_s}{L_g} \left[(s_1 - s_2 - s_8) V_{DC}(k) + (s_2 - s_3 + s_7) V_c(k) - V_g(k) \right] \tag{3-25}$$

$$V_c(k+1) = V_c(k) + \frac{T_s}{C_c} (s_3 - s_2 - s_7)\, i_g(k) \tag{3-26}$$

The cost function **C** is calculated using the values of (3-25) and (3-26). From (3-27), the value of **C** is obtained [128].

$$\boldsymbol{C} = \sqrt{\lambda \left(\frac{V_c^* - V_c(k+1)}{\Delta V_{c,max}(k)} \right)^2 + \left(\frac{i_g^*(k) - i_g(k+1)}{\Delta i_{g,max}(k)} \right)^2} \tag{3-27}$$

Where $\Delta V_{c,max}(k)$, and $\Delta i_{g,max}(k)$ are represent the maximum variations in the capacitor voltage and grid current, respectively, and can be obtained from (3-28) and (3-29).

$$\Delta V_{c,max}(k) = \frac{2 i_g(k)}{C_c} T_s \tag{3-28}$$

$$\Delta i_{g,max}(k) = \frac{2(V_{DC}(k) + V_c(k))}{L_g} T_s \qquad (3\text{-}29)$$

The factor λ represents a weighting factor, The flying capacitor reference value one-third dc link voltage, and the amplitude grid current reference value will be calculated from the DC-link PI controller, and the phase from PLL controller. The flow chart in Figure 3-11 presents the FCS-MPC algorithm of Systems 4 and 5.

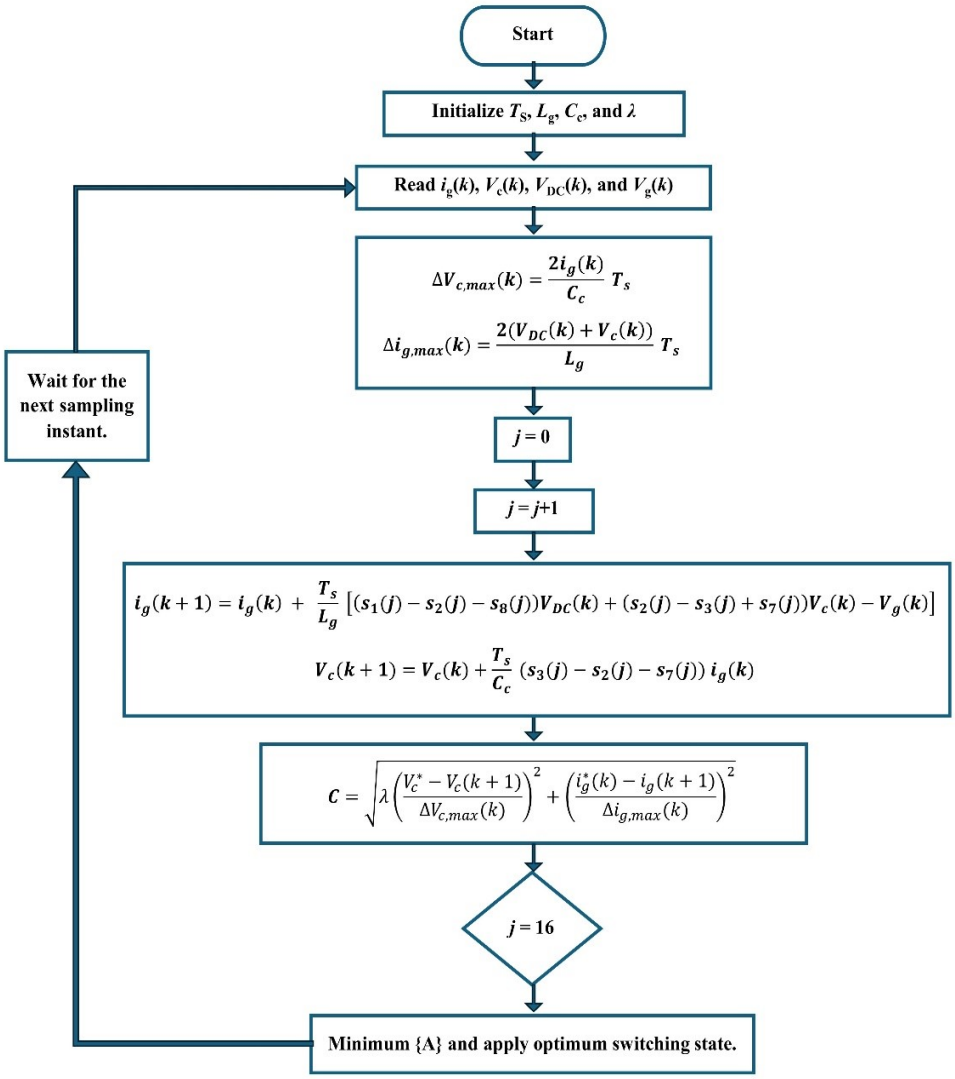

Figure 3-11. FCS-MPC Algorithm of Systems 4 and 5.

3.5.2.1 Weighting Factor Selection

The value of the weighting factor λ for the cost function (3-27) can be determined by minimizing the THD of the grid current (less than or equal to 5%) and the variation in the voltage across the PUC capacitor (less than 0.5%) [125]. The graph in Figure 3-12 shows the relationship between THD, V_c, and λ. A weighting factor of 0.1 was chosen, resulting in a THD of 2.60% and a capacitor voltage variation of 0.16%.

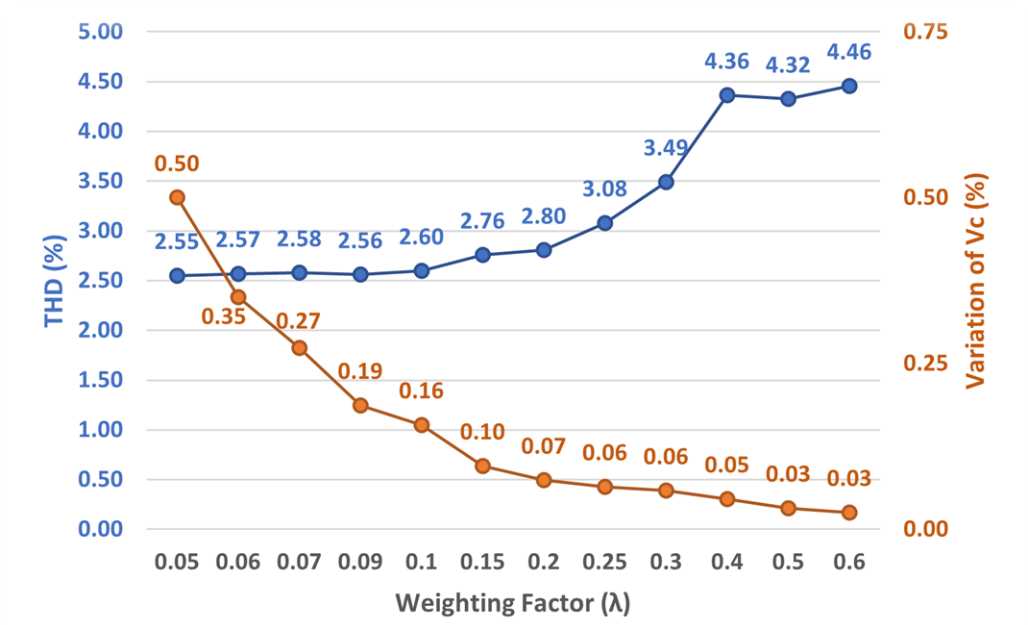

Figure 3-12. THD (%) and ΔVc (%) vs Weighting Factor (λ)

3.5.3 Design FCS-MPC for System 6

The FCS-MPC in System 6 has the same objective as FCS-MPC in Systems 3 and 4 but with extra PV LC mitigation aim which will be done by controlling the CMV across the PV panel PC (V_{cm}), so a new state variable will be added V_{cm}. The $V_{cm2}(k)$ can be calculated using the (3-30) - (3-33) equations that derived from Figure 3-4.

$$V_{an}(k) = V_{ao}(k) + V_{on}(k) \tag{3-30}$$

$$V_{an}(k) = (s_1 - s_2 - s_8)V_{DC}(k) + (s_2 - s_3 + s_7)V_c(k) \tag{3-31}$$

$$V_{on}(k) = V_{cm2}(k) \tag{3-32}$$

$$V_{ao}(k) = V_{DC}(k) \times s_1 \quad (3\text{-}33)$$

Substitute (3-30) - (3-32) in (3-33) to the value for CMV (3-34).

$$V_{cm2}(k) = (-s_2 - s_8)V_{DC}(k) + (s_2 - s_3 + s_7)V_c(k) \quad (3\text{-}34)$$

From Equation (3-34) the predictive value for CMV obtained (3-35)

$$V_{cm2}(k+1) = (-s_2 - s_8)V_{DC}(k+1) + (s_2 - s_3 + s_7)V_c(k+1) \quad (3\text{-}35)$$

According to (3-35) the $V_{DC}(k+1)$ has to be calculated, so by applying Euler forward approximation for (3-22), the predicted value $V_{DC}(k+1)$ obtained as depicted in (3-36).

$$V_{DC}(k+1) = V_{DC}(k) + \frac{T_s}{C_{DC}}\left[(1-D)^2 \times i_{PV}(k) - (s_2 + s_8 - s_1)i_g(k)\right] \quad (3\text{-}36)$$

The cost function **D** is calculated using the values of (3-25), (3-26), and (3-35). The value of **D** is obtained from (3-37).

$$\boldsymbol{D} = \sqrt{\lambda_1 \left(\frac{V^*_{cm2}(k) - V_{cm2}(k+1)}{\Delta V_{cm2,max}(k)}\right)^2 + \lambda_2 \left(\frac{V^*_c - V_c(k+1)}{\Delta V_{c,max}(k)}\right)^2 + \left(\frac{i^*_g(k) - i_g(k+1)}{\Delta i_{g,max}(k)}\right)^2} \quad (3\text{-}37)$$

To reduce the LC, the voltage variation across the CM capacitor must be minimized so the reference value (V^*_{cm2}(k)) chosen to be $V_{cm2}(k)$, and the V_{cm2} maximum variation ($\Delta V_{cm2,max}$) is ($V_{DC}(k) + V_c(k)$), besides, λ_1 *and* λ_2 are the weighting factors. The FCS-MPC System 6 algorithm presented in Figure 3-13.

3.5.3.1 Weighting Factor Selection

To ensure the optimal functioning of the FCS-MPC, precise tuning of the parameters λ_1 and λ_2 is crucial in Equation (3-37). The goal of the FCS-MPC is to keep the grid current THD% below 5% following the IEEE-519-2014 Standard, the RMS leakage current below 300 mA as per the DIN VDE 0126-1-1 Standard, and the CSC capacitor voltage variation below 0.5%.The weighting factors are adjusted based on these constraints. The variance is then calculated using (3-21).

The results of the simulations performed using varying weighting factors are shown in Figure 3-14. The simulation range for λ_1 is from 0.3 to 0.6, while for λ_2, it is between 0.05 and 0.2 . The optimal values for λ_1 and λ_2 are 0.5 and 0.08, respectively. These values lead to the lowest overall error values.

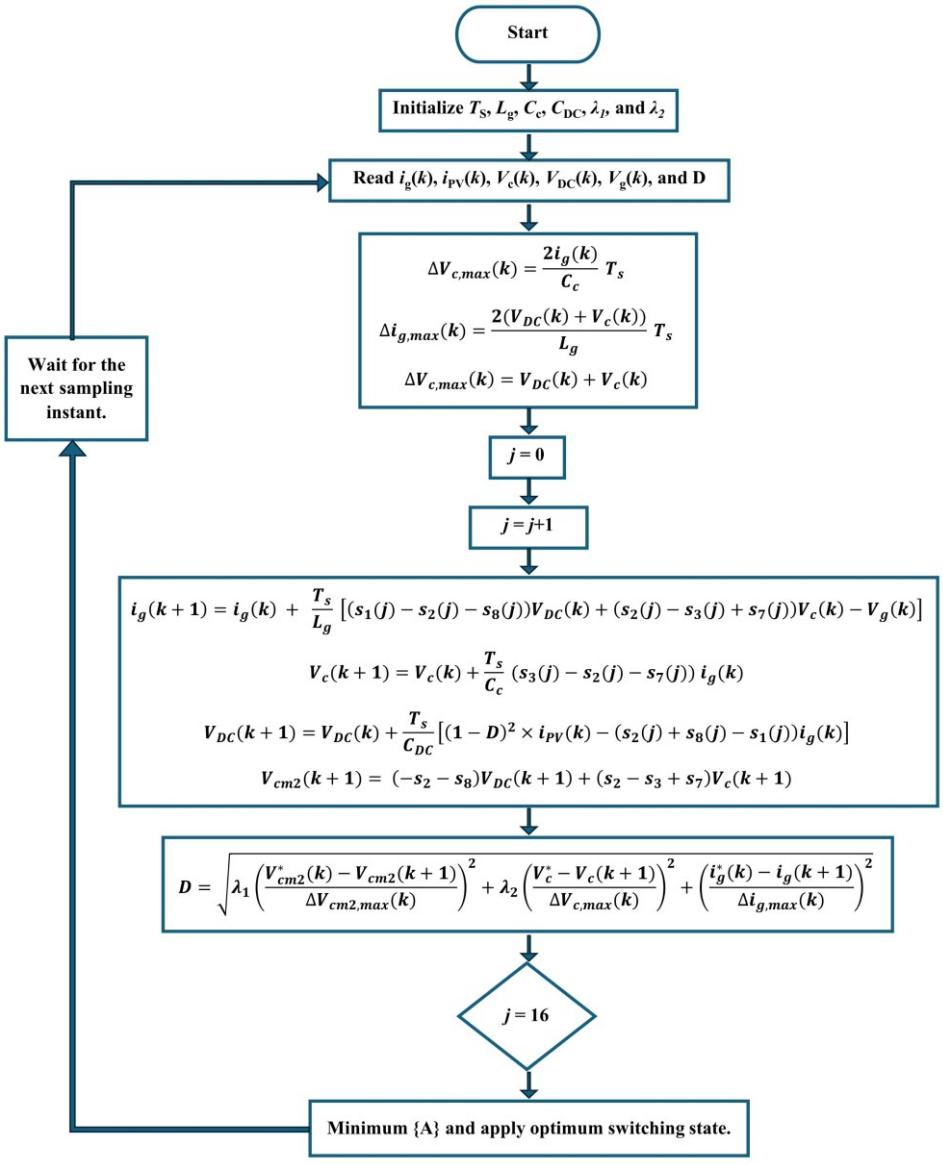

Figure 3-13. FCS-MPC Algorithm of System 6

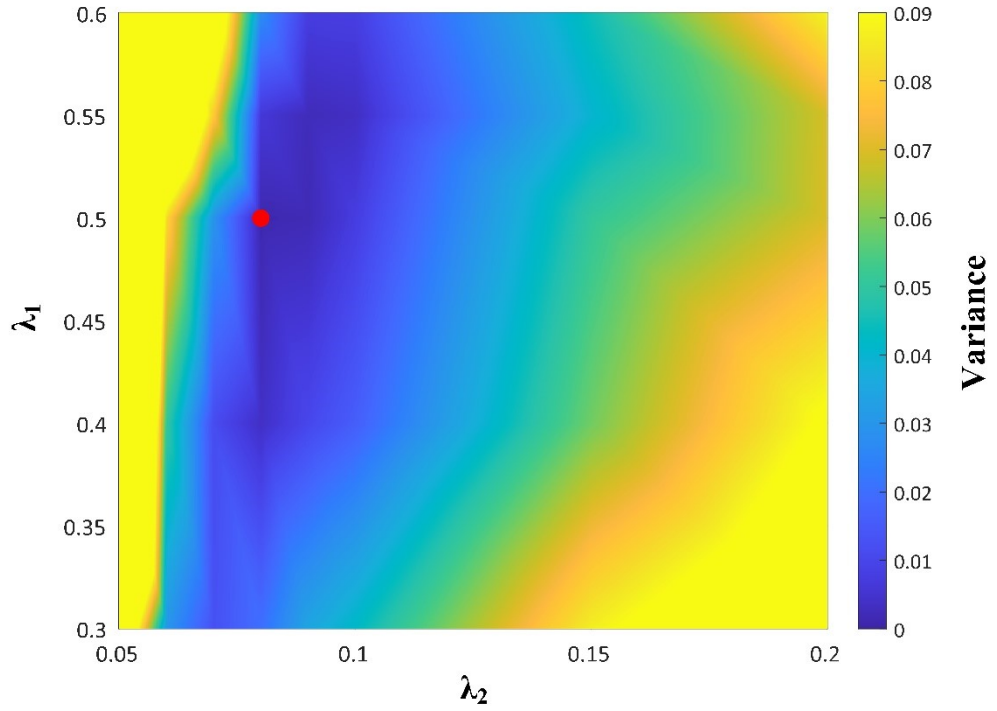

Figure 3-14. Heatmap plot for different λ_1 and λ_2 Vs. the variance

CHAPTER 4: SIMULATION RESULTS

4.1 Introduction

This chapter presents simulation results and assesses the feasibility and efficiency of the six designed systems. It comprises seven sections, the first six presenting the results for each system, while the last section summarizes and compares all the results. The software Matlab/Simulink was used to test the designs, and fixed values were initialized for all systems, which are presented in Table 4-1.

Table 4-1. Simulation Parameters Values

Parameter	Value
L_g	80 mH
V_g	$240*\sqrt{2}$ V
T_s	40 µs
C_c	1000 µF
V_c	123 V
C_{DC}	3000 µF
V_{DC}	369 V
Irradiation (t=0 to t=3)	1000 W/m^2
Irradiation (t=3 to t=6)	800 W/m^2
Temperature	25 ^{o}C

4.2 Results of System 1

The circuit simulation shown in Figure 3-1 was performed using input solar irradiance of 1000 W/m2 for three seconds, followed by 800 W/m2 for another three seconds, with a fixed temperature of 25 ^{o}C. During the simulation, it was necessary for the PV output voltage and current to remain constant with minimal variation. The PV voltage remained stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The QBC boosted the PV voltage ten times from 36.9 V to 369 V. The DC-Link voltage remained constant at around 369V, indicating that the DC-Link PI controller was functioning correctly. Figure 4-1 shows the solar irradiation plot, as well as the PV current and voltage and the DC-Link voltage.

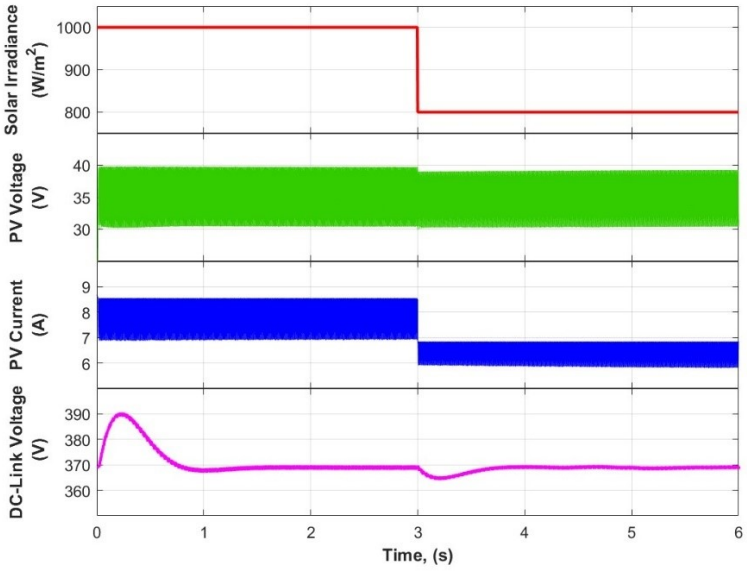

Figure 4-1. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-2 displays the seven-level output voltage of the PUC inverter and the PUC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.25%.

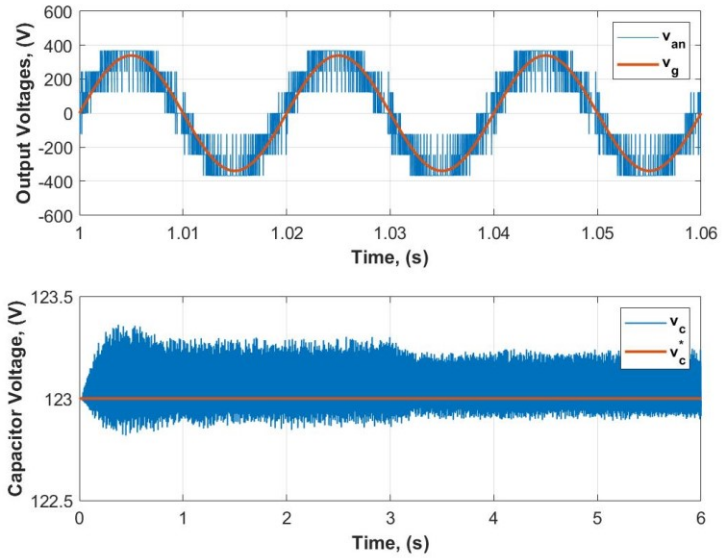

Figure 4-2. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-3 shows that at 1000 W/m^2 solar irradiance, the grid current THD% is 2.34%, while at 800 W/m^2, it is 2.67%.

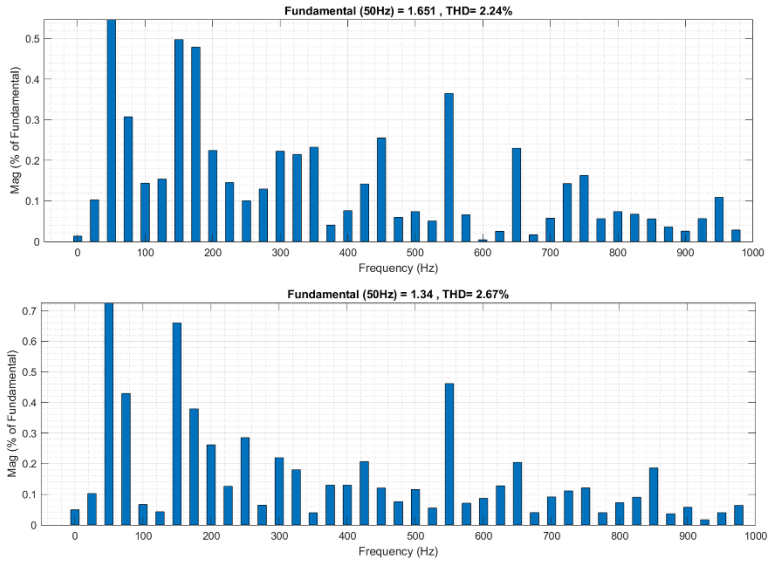

Figure 4-3. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The grid voltage and current signals are in phase with zero power factor, as present in Figure 4-4. In addition, the DC-Link PI controller ensures power transfer from the PV to the grid side, as illustrated in Figure 4-4.

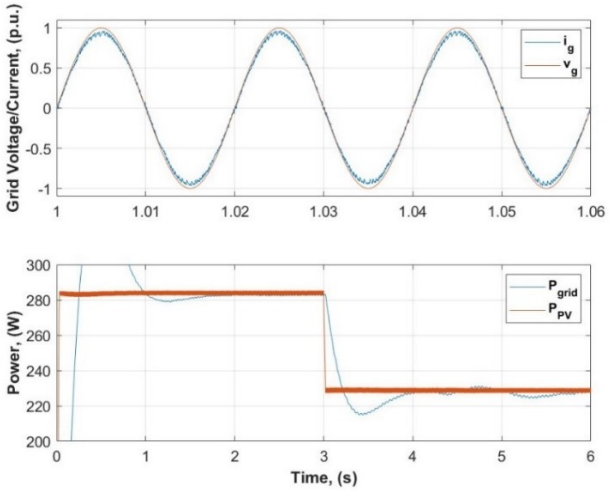

Figure 4-4. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

4.3 Results of System 2

The circuit depicted in Figure 3-2 was simulated with the same input irradiance and temperature as in the System 1 simulation. The results are presented in Figure 4-5; the plot shows the input solar irradiance and corresponding PV voltage, current, and DC-link voltage responses. The output PV voltage and current remained constant with minimal variation. The PV voltage remained stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The DC-Link voltage remained steady at around 369V, indicating that the DC-Link PI controller was functioning correctly.

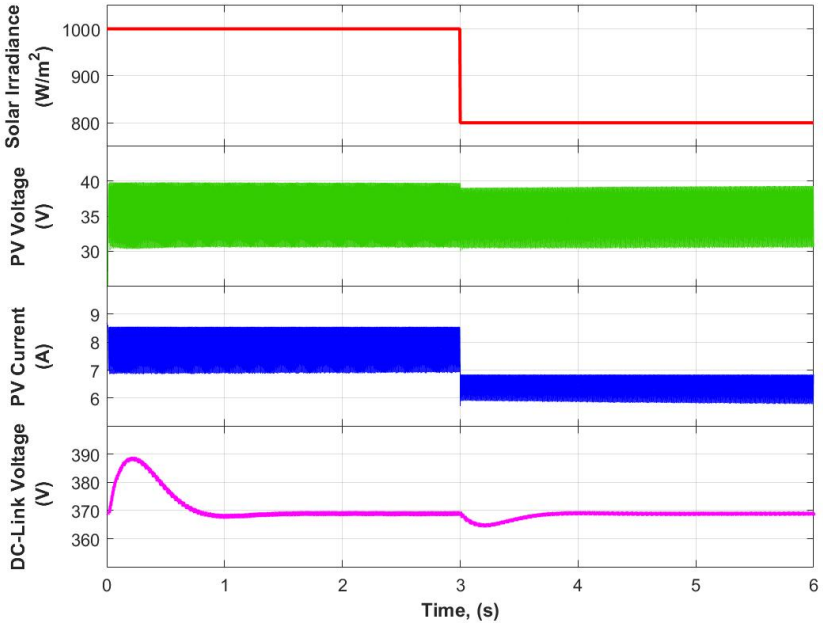

Figure 4-5. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-6 displays the seven-level output voltage of the PUC inverter and the PUC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.23%.

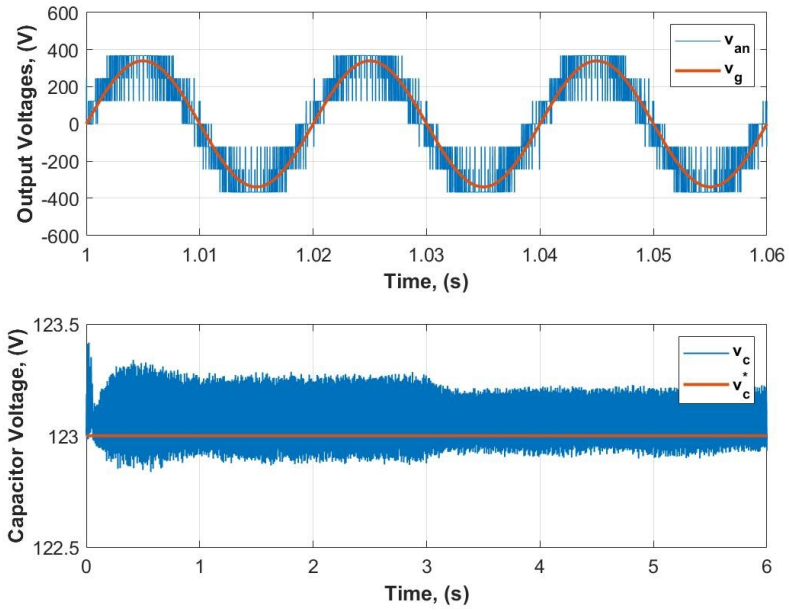

Figure 4-6. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-7 shows that at 1000 W/m2 solar irradiance, the grid current THD is 2.43%, while at 800 W/m2, it is 3.04%.

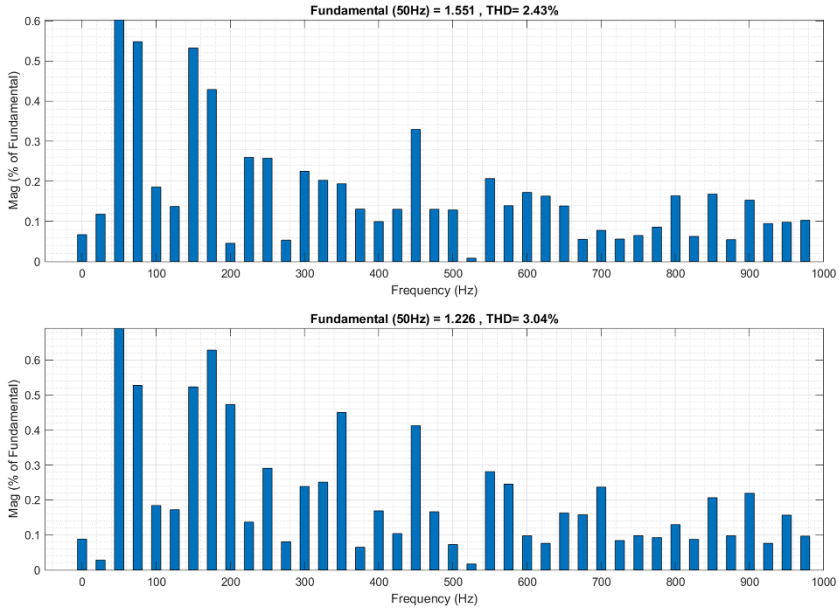

Figure 4-7. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The grid voltage and current signals are in phase with zero power factor, as

present in Figure 4-8. In addition, the DC-Link PI controller ensures power transfer from the PV to the grid side, as illustrated in Figure 4-8.

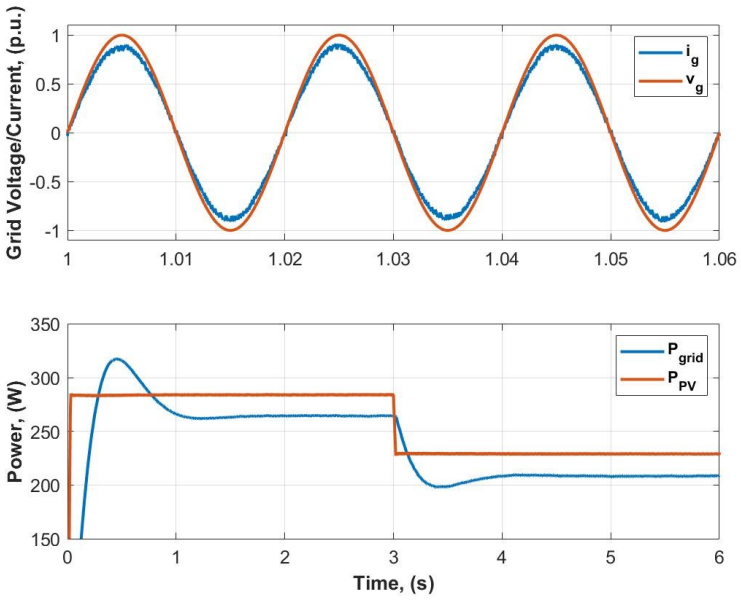

Figure 4-8. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

The PV LC fluctuates within a range of ±1.53A and the RMS value equals 0.35A, As depicted in Figure 4-9.

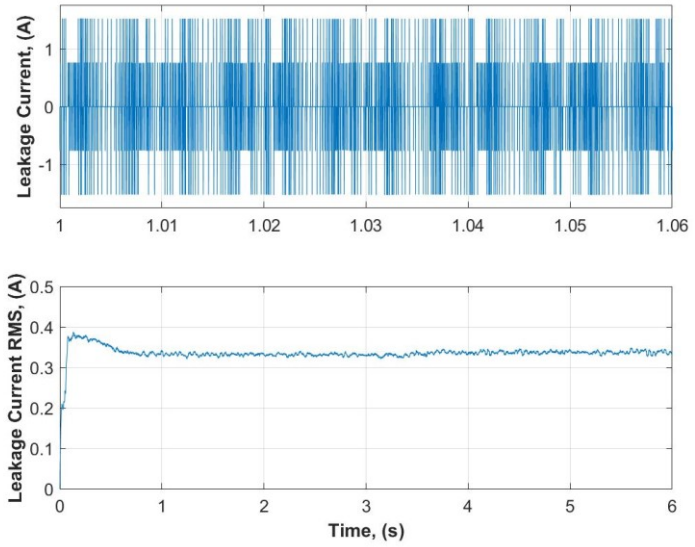

Figure 4-9. Simulation Results; Upper: PV Panel LC, Lower: PV Panel LC RMS.

4.4 Results of System 3

The circuit in Figure 3-2 was tested through a simulation with a solar irradiance of 1000 W/m2 for three seconds, followed by 800 W/m2 for another three seconds, while maintaining a fixed temperature of 25 C. The main goal of the simulation was to ensure that the output PV voltage and current remained steady with minimal fluctuations. During the simulation, the PV voltage was stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The QBC amplified the PV voltage ten times, from 36.9 V to 369 V, while the DC-Link voltage remained constant at around 369V, indicating that the DC-Link PI controller was functioning correctly. Figure 4-10 shows the solar irradiation plot, the PV current and voltage, and the DC-Link voltage.

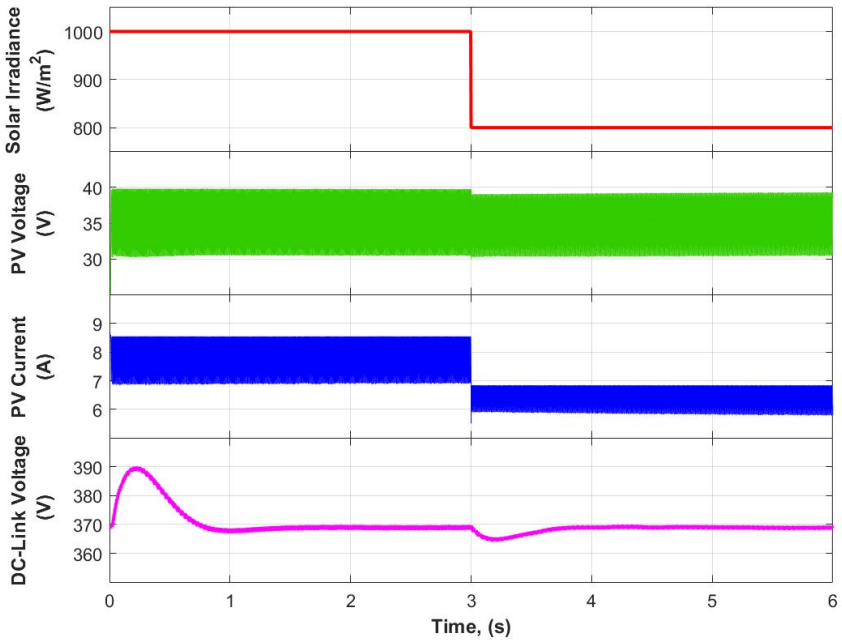

Figure 4-10. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-11 displays the seven-level output voltage of the PUC inverter and the PUC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.2%.

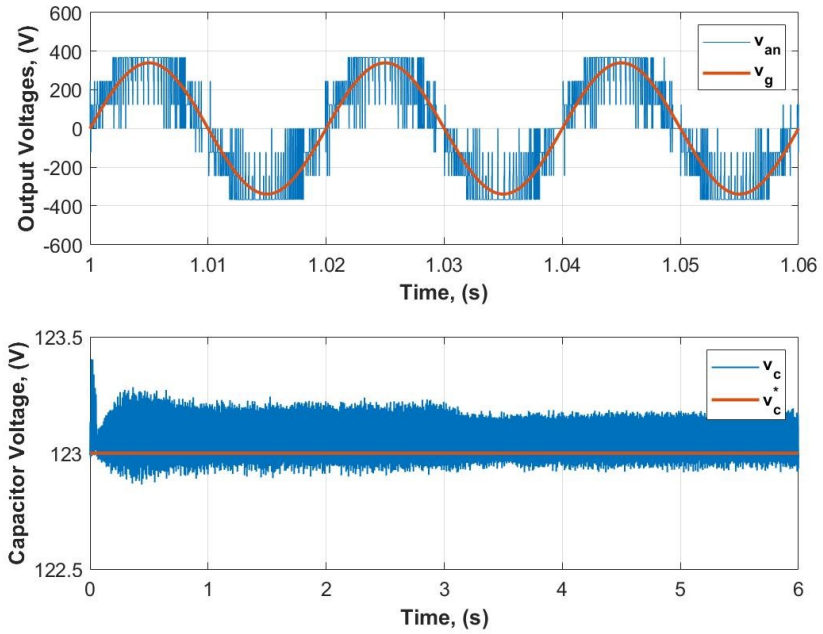

Figure 4-11. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-12 shows that at 1000 W/m2 solar irradiance, the grid current THD is 3.42%, while at 800 W/m2, it is 4.17%.

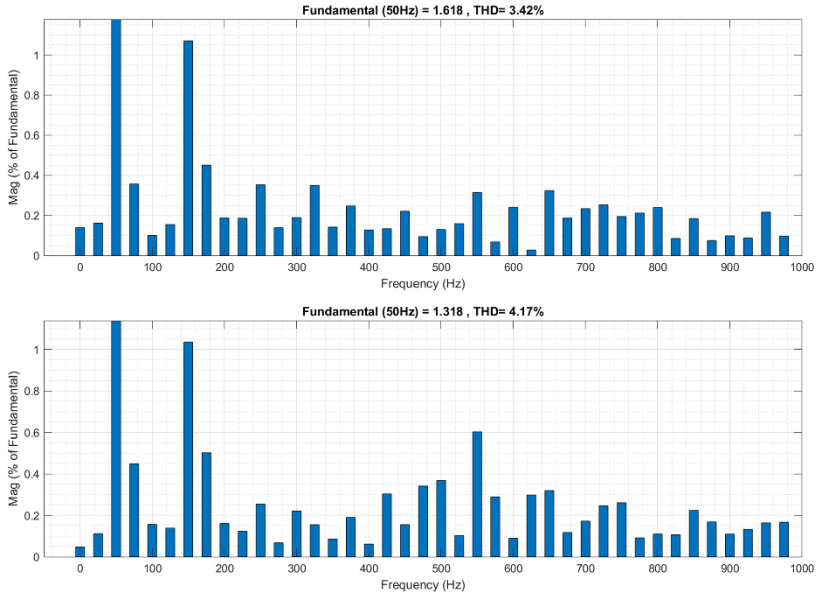

Figure 4-12. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The voltage and current signals are in phase with zero power factor, as present in Figure 4-13. In addition, the DC-Link PI controller ensures power transfer from the PV to the grid side, as illustrated in Figure 4-13.

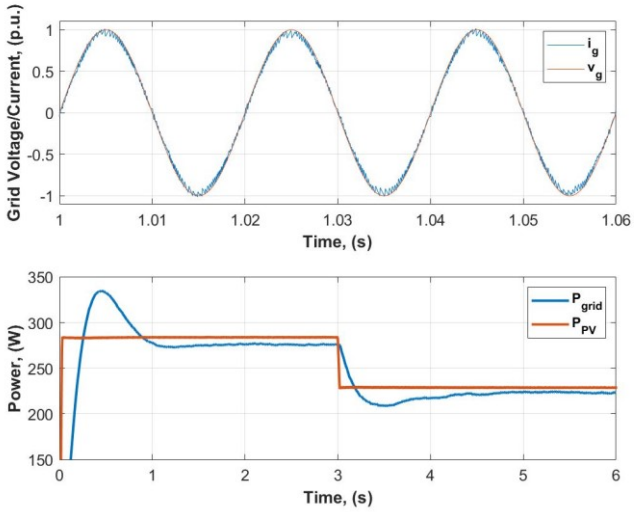

Figure 4-13. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

The PV LC fluctuates within a range of ± 1.53A and the RMS value equals 0.22A, As depicted in Figure 4-14.

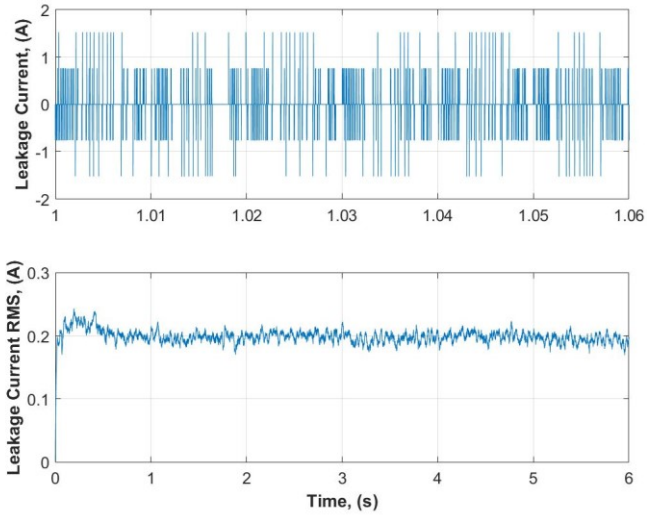

Figure 4-14. Simulation Results; Upper: PV Panel LC, Lower: PV Panel LC RMS.

4.5 Results of System 4

The circuit depicted in Figure 3-3 was simulated with the same input irradiance and temperature as in the previous simulations. The results are presented in Figure 4-15; the plot shows the input solar irradiance and corresponding PV voltage, current, and DC-link voltage responses. The output PV voltage and current remained constant with minimal variation. The PV voltage remained stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The DC-Link voltage remained steady at around 369V, indicating that the DC-Link PI controller was functioning correctly.

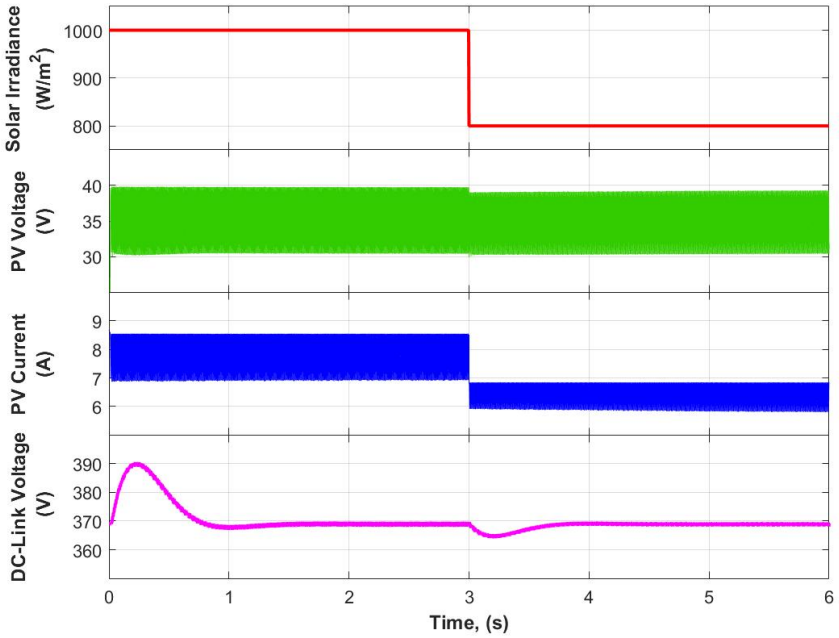

Figure 4-15. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-16 displays the nine-level output voltage of the CSC inverter and the CSC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.16%.

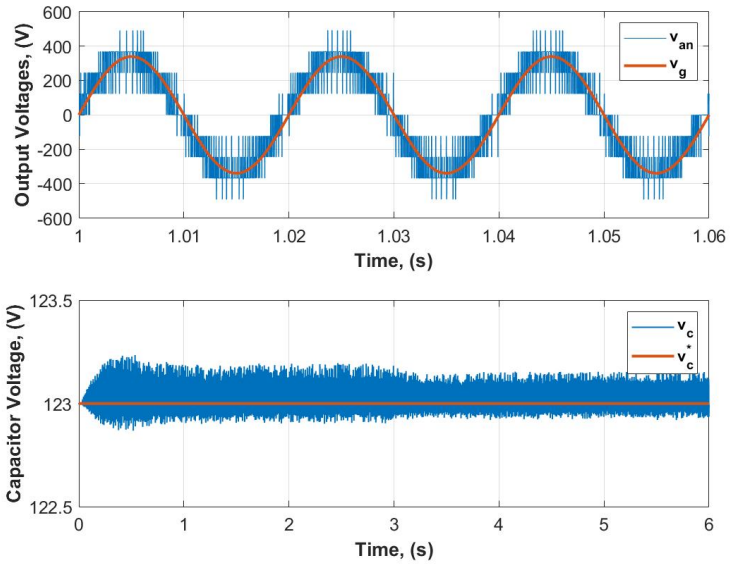

Figure 4-16. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-17 shows that at 1000 W/m2 solar irradiance, the grid current THD is 2.19%, while at 800 W/m2, it is 2.66%.

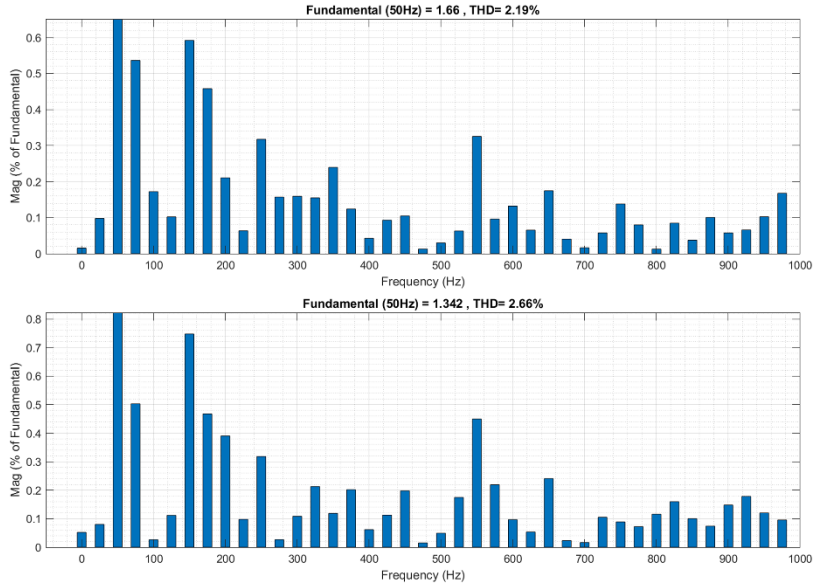

Figure 4-17. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The grid voltage and current signals are in phase with zero power factor, as present in Figure 4-18. In addition, the DC-Link PI controller ensures power transfer

from the PV to the grid side, as illustrated in Figure 4-18.

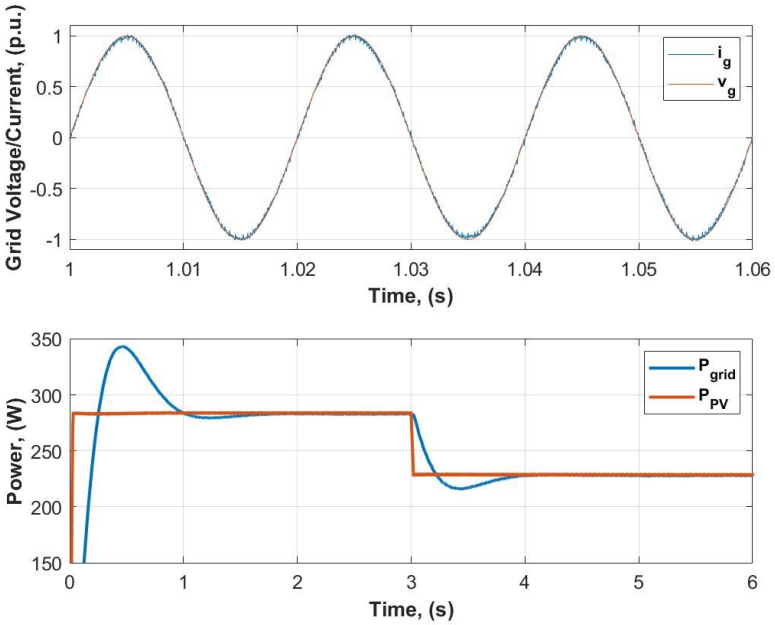

Figure 4-18. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

4.6 Results of System 5

The circuit depicted in Figure 3-4 was simulated with the same input irradiance and temperature as in the previous simulations. The results are presented in Figure 4-19; the plot shows the input solar irradiance and corresponding PV voltage, current, and DC-link voltage responses. The output PV voltage and current remained constant with minimal variation. The PV voltage remained stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The DC-Link voltage remained steady at around 369V, indicating that the DC-Link PI controller was functioning correctly.

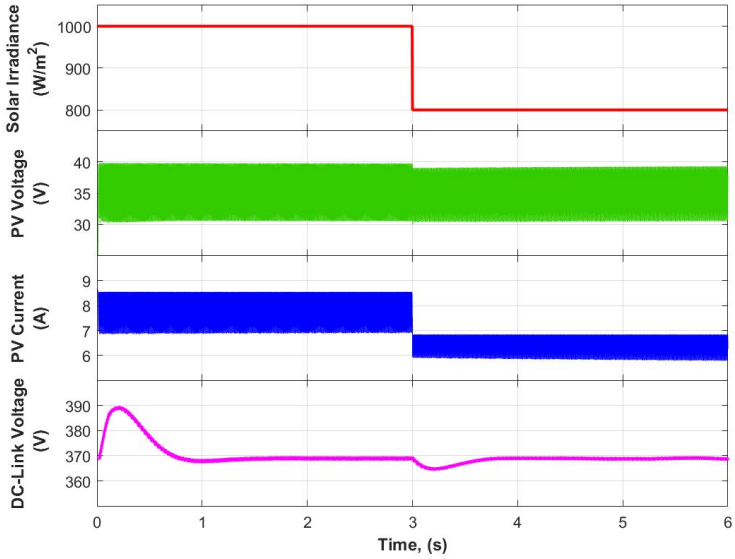

Figure 4-19. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-20 displays the nine-level output voltage of the CSC inverter and the CSC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.15%.

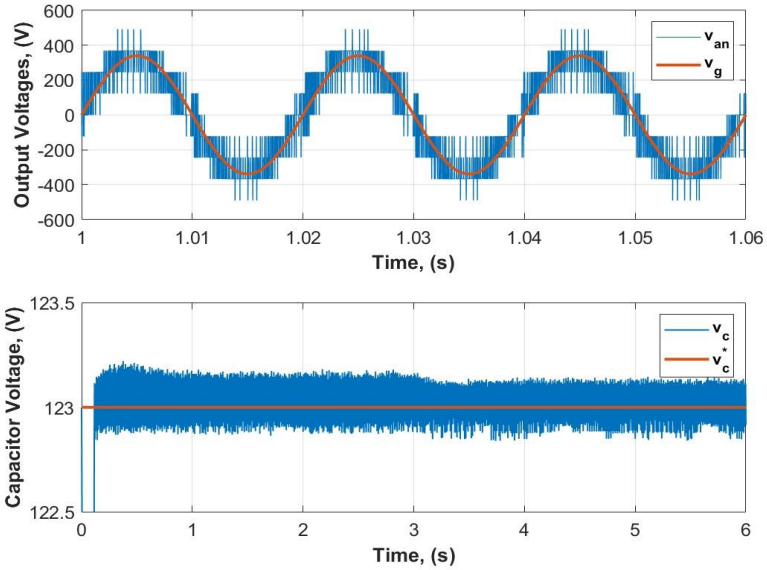

Figure 4-20. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-21 shows that at 1000 W/m2 solar irradiance, the grid current THD is 2.39%, while at 800 W/m2, it is 3.03%.

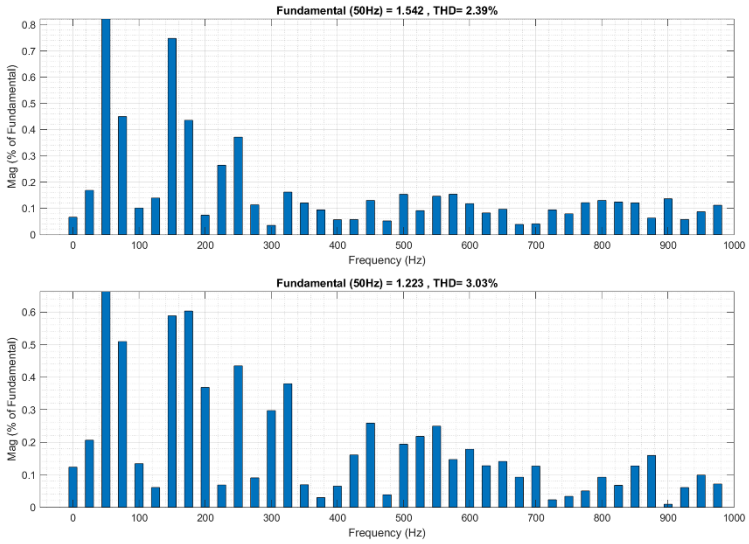

Figure 4-21. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The grid voltage and current signals are in phase with zero power factor, as present in Figure 4-22. In addition, the DC-Link PI controller ensures power transfer from the PV to the grid side, as illustrated in Figure 4-22.

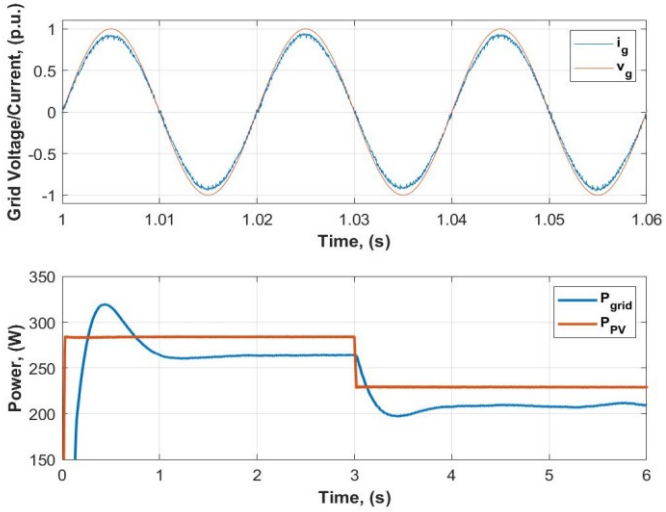

Figure 4-22. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

The PV LC fluctuates within a range of ± 2.3A and the RMS value equals 0.36A, As depicted in Figure 4-23.

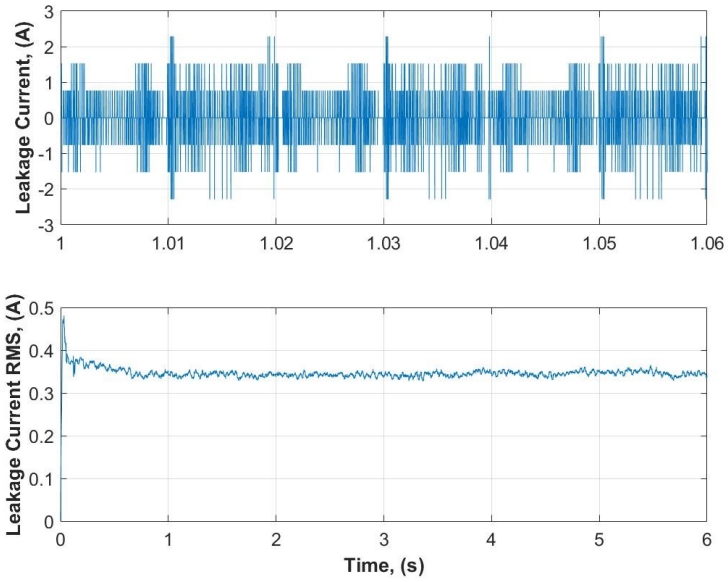

Figure 4-23. Simulation Results; Upper: PV Panel LC, Lower: PV Panel LC RMS.

4.7 Results of System 6

The circuit depicted in Figure 3-4 was simulated with the same input irradiance and temperature as in the previous simulations. The results are presented in Figure 4-24; the plot shows the input solar irradiance and corresponding PV voltage, current, and DC-link voltage responses. The output PV voltage and current remained constant with minimal variation. The PV voltage remained stable at the MPP, which was 36.9V with slight variation, while the PV current was 8.13 A. The DC-Link voltage remained steady at around 369V, indicating that the DC-Link PI controller was functioning correctly.

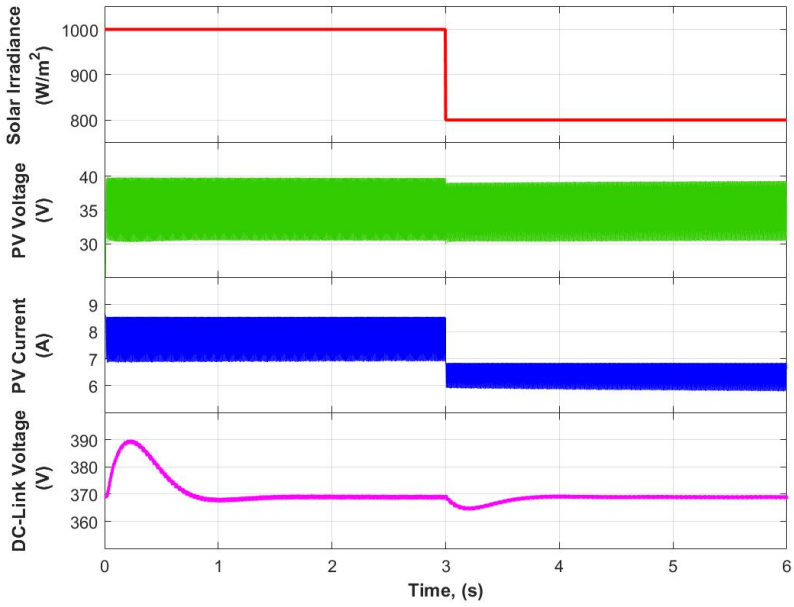

Figure 4-24. Input Solar Irradiance and Corresponding PV Voltage, Current, and DC-Link Voltage Responses

Figure 4-25 displays the nine-level output voltage of the CSC inverter and the CSC capacitor voltage, which is set at one-third of the DC-Link voltage, with a variation of about 0.2%.

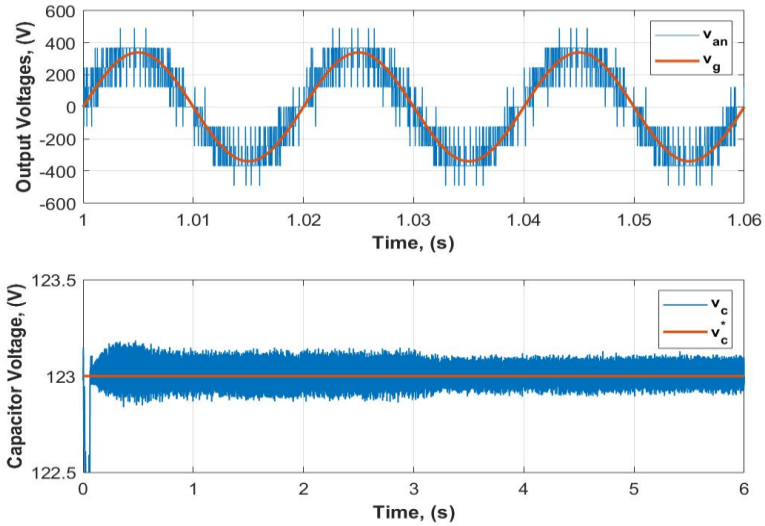

Figure 4-25. Simulation Results; Upper: inverter output voltage (v_{an}) and grid voltage (v_g), Lower: the inverter capacitor voltage (v_c) and its reference (v_c^*)

Figure 4-26 shows that at 1000 W/m2 solar irradiance, the grid current THD is 2.99%, while at 800 W/m2, it is 3.6%.

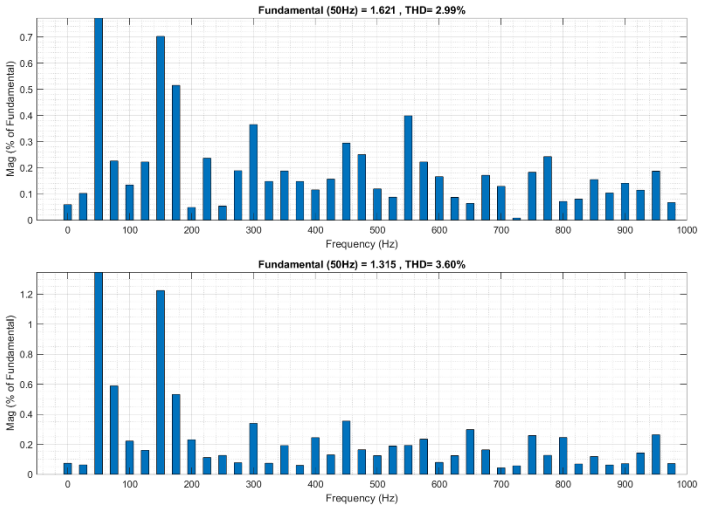

Figure 4-26. Harmonic spectrum with grid current THD%; Upper: solar irradiance at 1000 W/m^2, Lower: solar irradiance at 800 W/m^2.

The grid voltage and current signals are in phase with zero power factor, as present in Figure 4-27. In addition, the DC-Link PI controller ensures power transfer from the PV to the grid side, as illustrated in Figure 4-27.

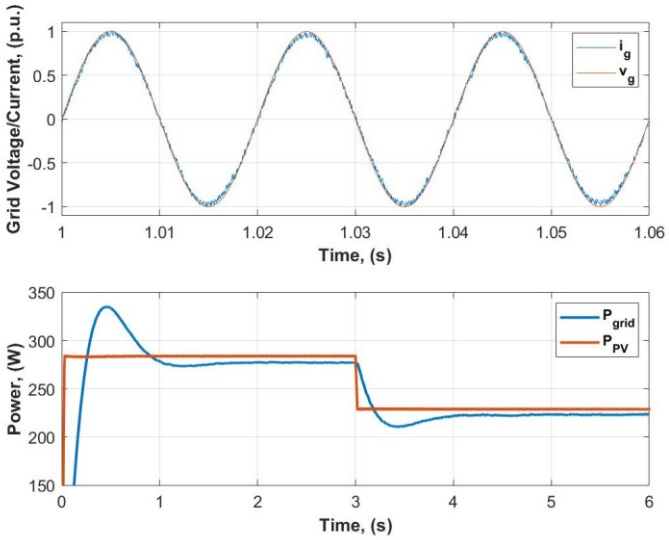

Figure 4-27. Simulation Results; Upper: Grid voltage (v_g) and Current (i_g), Lower: grid power (P_g) and the PV power (P_{PV}).

The PV LC fluctuates within a range of ±1.53A and the RMS value equals 0.2A, As depicted in Figure 4-28.

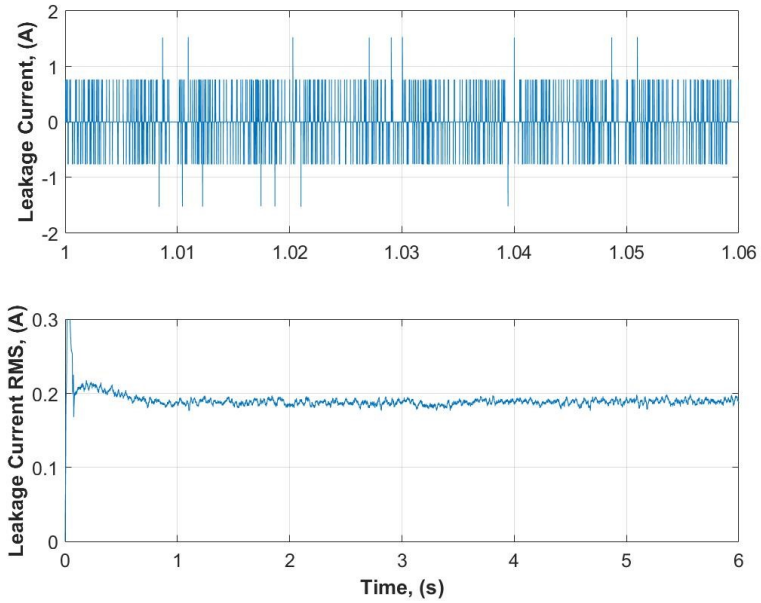

Figure 4-28. Simulation Results; Upper: PV Panel LC, Lower: PV Panel LC RMS.

4.8 Result Summary and Discussion

The systems in all simulations are function properly, As shown in Table 4-2. At 1000 W/m^2, the THD in Systems 1 and 4 is around 2.20%. It slightly increases in Systems 2 and 5 to around 2.40%; in Systems 3 and 6, the THD rose to around 3.42% and 2.99%. This slight increase is predicted as a new variable added to the control system. The inverter capacitor voltage variation in all systems did not exceed 25%. System 1 and System 4's efficiency is high, around 98.10%. Adding PC in Systems 2 and 5 affected the efficiency in the systems and dropped to around 90%. After mitigating the LC in Systems 3 and 6, the efficiency is enhanced, which concludes that the LC in the system affects the performance and increases the losses. This loss appears because of the LC circulation in the conducted loop, which results in energy being dissipated within the system rather than being transferred to the grid side. The LC was mitigated from 0.34 A to 0.22 in Systems 2 and 3 and from 0.36 to 0.2 in Systems 5

and 6.

The proposed controller achieved all control targets the LC RMS below 300 mA as per DIN VDE 0126-1-1 Standard, THD is below 5% as IEEE-519-2014 Standard, maintain inverter capacitor constant at one-third of DC-Like voltage, maintain MPP at PV panel, and maintain DC-Link voltage constant.

Table 4-2. Simulation Results Summary

Solar Irradiance	Parameter	Systems					
		1	2	3	4	5	6
1000	THD (%)	2.24	2.43	3.42	2.19	2.39	2.99
	Capacitor Voltage Variation (%)	0.25	0.23	0.20	0.16	0.15	0.12
	Efficiency (%)	98.1	92.2	96.2	98.5	91.6	96.5
	Leakage Current Maximum (A)	-	1.53	1.54	-	2.30	1.53
	Leakage Current RMS (A)	-	0.34	0.22	-	0.36	0.20
800	THD (%)	2.67	3.04	4.14	2.66	3.03	3.60
	Capacitor Voltage Variation (%)	0.20	0.19	0.15	0.13	0.13	0.11
	Efficiency (%)	98.2	90.1	95.8	98.8	89.6	96.3
	Leakage Current Maximum (A)	-	1.53	1.54	-	2.30	1.53
	Leakage Current RMS (A)	-	0.35	0.22	-	0.37	0.20

CHAPTER 5: HARDWARE-IN-THE-LOOP IMPLEMENTATION

5.1 Introduction

This chapter analyzes the feasibility and effectiveness of three PUC inverter topology-designed systems using HIL results. The HIL simulation utilized Typhoon HIL 602 and microcontroller F28379D LaunchPad. The HIL 602 device implemented the circuit part, while the microcontroller implemented the FCS-MPC. Figure 5-1 shows HIL implementation components interaction.

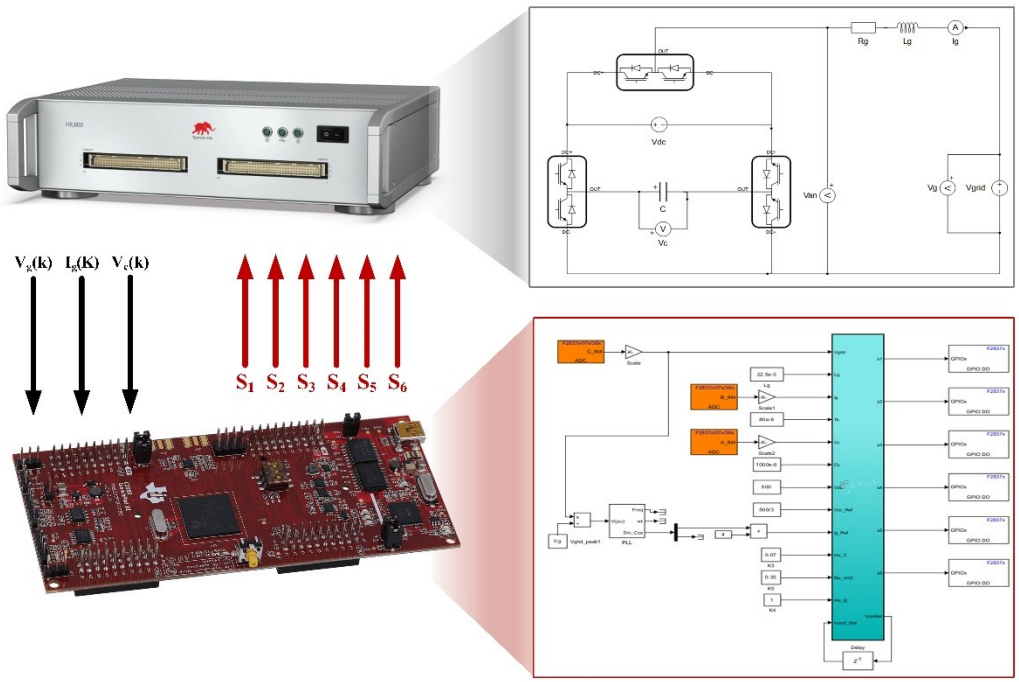

Figure 5-1. HIL implementation component interaction.

5.2 HIL Implementation

To conduct the implementation, the PV panel and DC-DC converter were replaced with a DC voltage source. The circuits used in the HIL implementation are depicted in Figure 5-2, and they were implemented using the Typhoon HIL Schematic Editor.

The Schematic Editor's measurement tools were employed to measure the values of grid current and voltage ($i_g(k)$, $V_g(k)$) and the PUC capacitor voltage ($V_c(k)$).

These signals were then sent to the microcontroller through the output analog pins.

The microcontroller received these signals via Analog-to-Digital converter (ADC) pins and inputted them into the FCS-MPC controller. The FCS-MPC generated six switch pulses sent to the HIL device via digital output pins. The HIL device received these signals and applied them to the PUC switches.

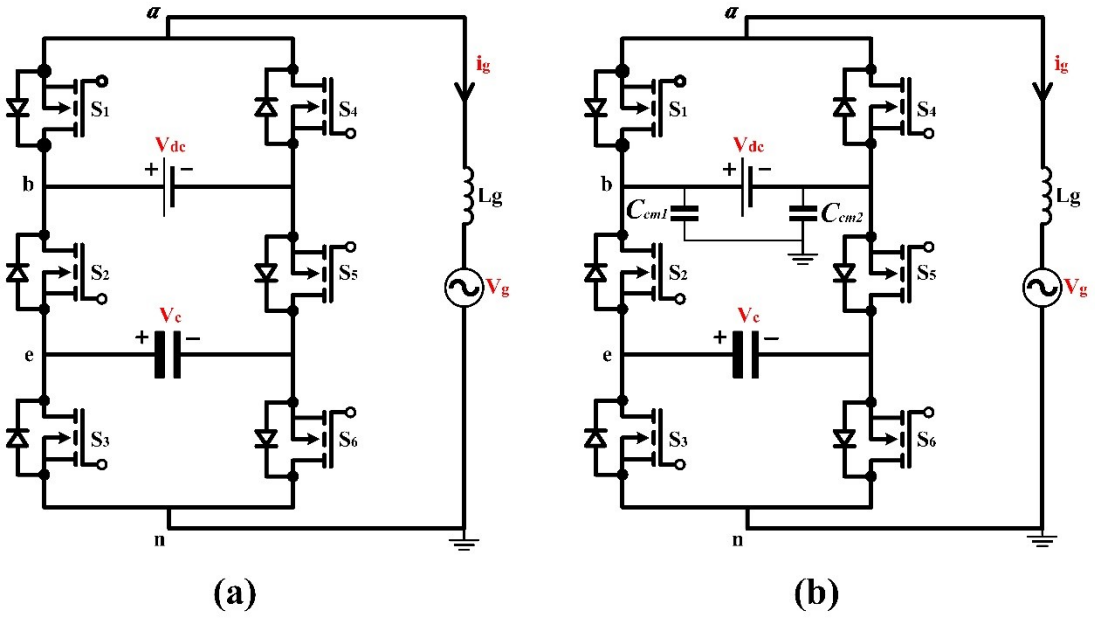

Figure 5-2. PUC inverter circuit (a) System 1 and (b) System 2 and 3

The parameter values used in the HIL implementation are presented in Table 5-1.

Table 5-1. HIL Implementation Parameters Values

Parameter	Value
L_g	22.5 mH
V_g	240*$\sqrt{2}$ V
T_s	80 µs
C_c	1000 µF
V_c	166.66 V
C_{DC}	3000 µF
Off Delay	0.3 µs

5.2.1 Results of System 1

Figure 5-3 displays the grid voltage and current in phase. The seven-levels inverter output voltage with the maximum voltage reaching 500V. Additionally, the PUC capacitor is fixed at one-third of the DC source, which is approximately 166.66V. The THD of the grid current is less than 3.8%.

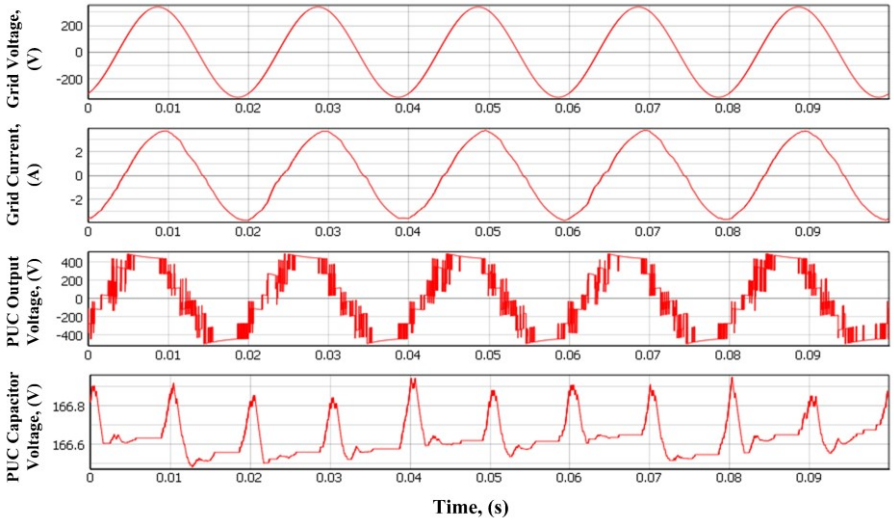

Figure 5-3. Output signal results - grid voltage, grid current, PUC output voltage, and PUC capacitor voltage.

5.2.2 Results of System 2

Figure 5-4 displays the grid voltage and current in phase. The seven-levels inverter output voltage with the maximum voltage reaching 500V. Additionally, the PUC capacitor is fixed at one-third of the DC source, which is approximately 166.66V. The THD% of the grid current is less than 4.1. The THD was affected after adding the PC to the circuit.

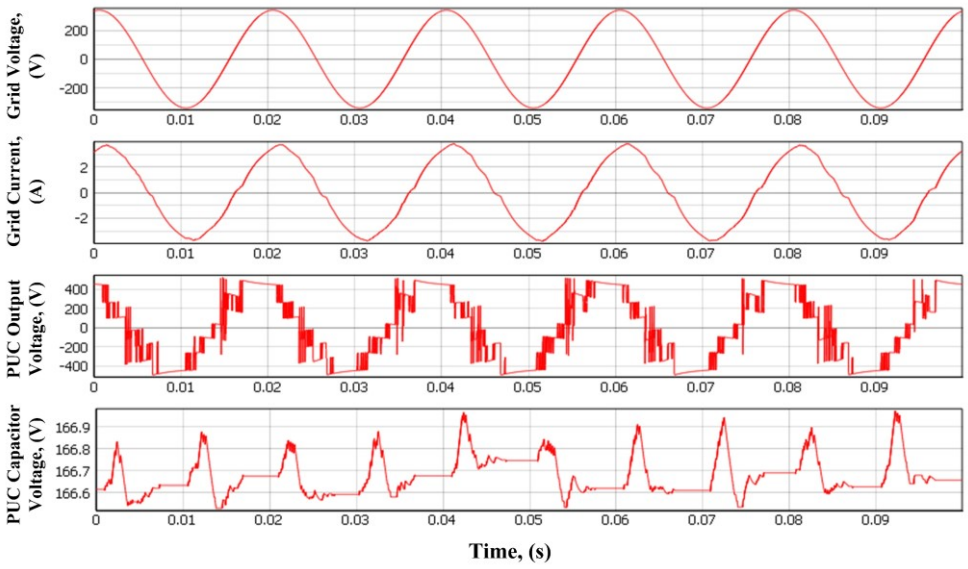

Figure 5-4. Output signal results - grid voltage, grid current, PUC output voltage, and PUC capacitor voltage.

Figure 5-5 presents the CMV and LC signals. The RMS value of the LC reaches 1.1A, and the peak current is 15A.

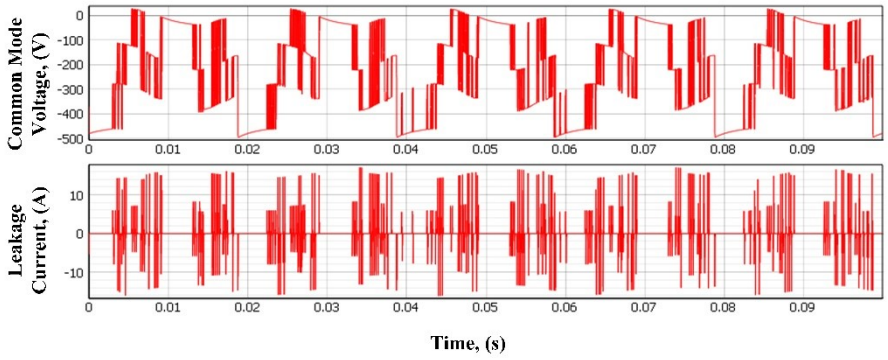

Figure 5-5. Output signal results - CMV, and instantaneous LC

5.2.3 Results of System 3

Figure 5-6 displays the grid voltage and current in phase. The seven-levels inverter output voltage with the maximum voltage reaching 500V. Additionally, the PUC capacitor is fixed at one-third of the DC source, which is approximately 166.66V. The THD of the grid current is less than 5.6%. The THD was affected after adding the CMV control part to the FCS-MPC.

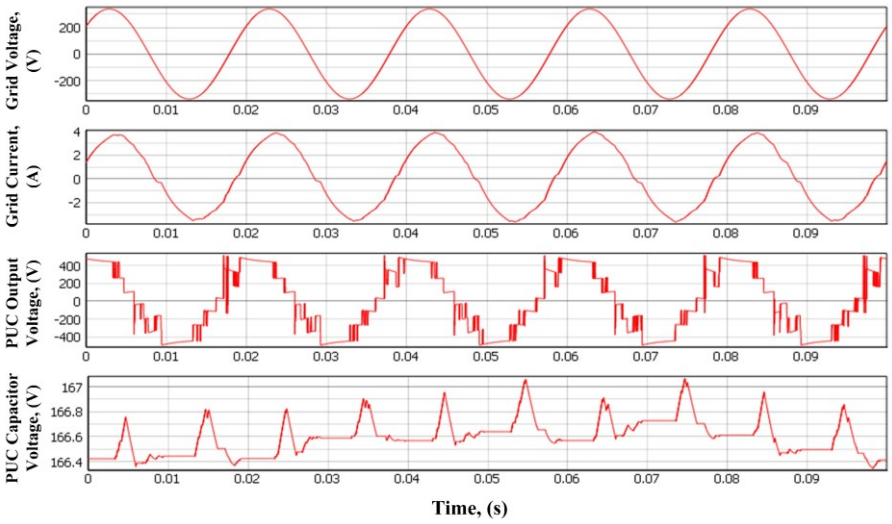

Figure 5-6. Output signal results - grid voltage, grid current, PUC output voltage, and PUC capacitor voltage.

Figure 5-7 presents the CMV and LC signals, the LC RMS mitigated from 1.1 A to 0.5 A, and the peak current 15A. the CMV variation reduced compared with System 2 in Figure 5-5.

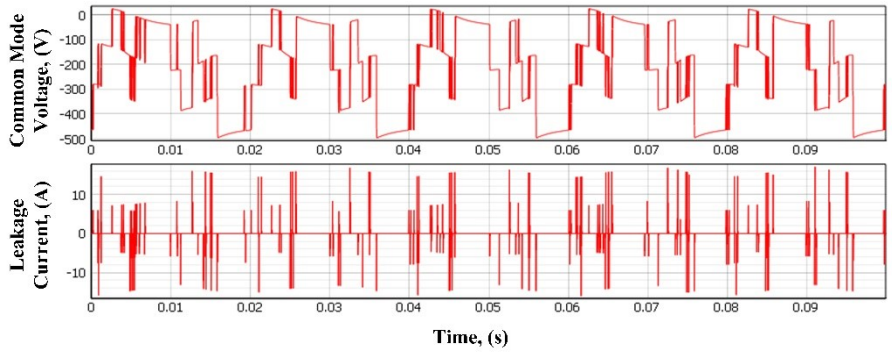

Figure 5-7. Output signal results - CMV, and instantaneous LC

CHAPTER 6: CONCLUSION AND FUTURE WORK

Grid-connected PV systems represent a promising solution for the RE sector, providing significant contributions towards the global transition to a low-carbon future. These systems come in different configurations based on the inverter and transformer components used within the system. Microinverter configurations, for example, are particularly well-suited for residential use and partial shading scenarios. This type of configuration offers expandability and flexibility in design, simple failure detection, and eliminates the mismatch losses between modules. On the other hand, transformerless configurations are an ideal choice to develop in parallel with microinverter configurations as they keep the overall system low in weight and volume while improving total efficiency by 2%. However, it is essential to note that this configuration also presents safety concerns related to the PC of the solar panel, which generates a LC between the PV panel and the grid after panel galvanic isolation.

Previous research has explored various non-isolated inverters in transformerless systems and has been extensively studied, with some papers highlighting mitigating LC using different techniques. However, it has been observed that the PUC and CSC inverters are not covered and studied in a transformerless system. Accordingly, this research focused on studying these two inverter topologies in a double-stage transformerless microinverter PV grid-connected system. The study focuses on six systems to understand the impact of PV panel LC on the PUC and CSC non-isolated inverters. Three systems are designed based on the PUC inverter, and another three are based on the CSC inverter. The analysis of these systems provides a clear understanding of the effects of PV panel LC on the system. Additionally, two FCS-MPCs are designed to mitigate the PV panel LC and tested on the two inverter topologies.

In order to evaluate the feasibility and effectiveness of the proposed controllers,

a MATLAB/Simulink simulation has been conducted. The proposed controller has successfully achieved all the control objectives, which include keeping the LC RMS below 300 mA in accordance with DIN VDE 0126-1-1 Standard, maintaining THD below 5% as per IEEE-519-2014 Standard, maintaining the inverter capacitor constant at one-third of the DC-link voltage, maintaining the MPP at the PV panel, and keeping the DC-Link voltage constant. The simulation results also indicate the impact of LC on system efficiency and grid current THD. Overall, the proposed controllers demonstrate high efficiency and effectiveness in meeting the desired control objectives.

HIL is employed to test and validate a proposed control algorithm in a three-phase inverter system. The testing results indicate that the grid voltage and current are in phase, and the inverter produces an output voltage with seven levels. Additionally, the PUC capacitor is set at one-third of the DC source. The THD of the grid current is less than 3.8% in system 1. However, in system 2, the THD% increases to 4.1% after adding PC to the circuit. In system 3, the THD further increases to 5.6% due to adding a CMV control to FCS-MPC. Furthermore, the LC RMS was mitigated from 1.1 A to 0.5 A in system 3. These findings demonstrate the importance of carefully considering the impact of PC and CMV control on the performance of PV grid-connected systems.

This research offers several opportunities for future work, including:

- The proposed controllers can be tested and validated in real-life scenarios to verify their effectiveness and practicality.
- Investigate the impact of different environmental factors, such as temperature and humidity, on the performance of the proposed controllers.
- Explore the potential of advanced control techniques, such as machine learning and artificial intelligence, to enhance the performance and efficiency of the system.

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