

# PARALLEL COMPUTING APPLIED TO COMPENSATE THE EFFECT OF AMPLIFIER BANDWIDTH IN THE DESIGN OF SWITCHED CAPACITOR NETWORKS

M.Y. Makkey\* and A.H.L. Al Mohanadi\*\*

\*Electrical Engineering Dept., Faculty of Engineering  
University of Assuit, Assuit, Egypt.

\*\*Electrical Engineering Dept., Faculty of Engineering  
Qatar University, Doha, Qatar.

## ABSTRACT

A method is described for the extraction of capacitor values for switched capacitor (SC) networks which compensate for the effect of finite amplifier bandwidth in the design of SC networks using optimization. The finite bandwidths of the amplifier distort the response of the network from the required response. It is shown that by readjusting the poles and zeros of the transfer function, the required response can be accurately restored. The values of capacitances are extracted by running a number of parallel local optimizations, each starting from different random initial conditions, on a network of transputers. This method removes the possibility of an optimization being trapped in a local minimum and ensures the stability of the design network.

## INTRODUCTION

Computer-aided design of switched capacitor networks (SCN) employing frequency independent operational amplifier as well as ideal switches, are covered in literature, [1,2,3]. The importance of the study of finite bandwidth limitations of SCN stems from the fact that it may affect the stability of the SCN as a result of the extra phase introduced, especially in feed-back loops. Recently, [4], the analysis of SCN with operational amplifier having frequency dependent gain of the form

$$A(s) = \frac{GB}{s} \quad (1)$$

has been given, where GB is the gain bandwidth product.

More recently, [5], a method has been described for the optimization of the frequency response of SCN employing an operational amplifier with a frequency dependent gain of the form of equation (1). It depends upon the minimization of the poles and zeros deviations of the distorted transfer function from their ideal locations.

It has been found, however that there are often problems in using an approach in which there is only a single local optimization. Often, the objective function formed in the optimization contains more than one minimum. The actual minimum returned by the optimization depends critically upon the initial values of the parameters being optimized. Therefore, if the values of the optimization parameters are not chosen correctly, it is possible that the optimization would end at a point which is not the global minimum, i.e. a local minimum.

One method for removing the necessity of choosing initial parameter values is to begin a number of local optimizations at random initial starting points, and then choose the best parameters producing a minimum with least error value. This approach is inefficient as it requires a high CPU time if normal sequential computing methods are used. However, if local optimizations are performed in parallel, the CPU time can be decreased to an acceptable amount.

This paper presents a method for performing multiple local optimizations in parallel on a transputer array. Moreover, this paper is concerned with the CPU time advantages by using parallel techniques.

## NETWORK RESPONSE OPTIMIZATION

The following procedure is adopted to minimize the deviation of the SCN response from its ideal one over a grid of frequency points

- 1- For the SCN topology given, obtain its transfer function as described in reference [3] assuming that the operational amplifier is ideal.
- 2- For a practical operational amplifier model, we can assume a transfer function of the form [5]

$$H(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2} + \dots + a_nz^{-n}}{1 + b_1z^{-1} + b_2z^{-2} + \dots + b_nz^{-n}} \quad (2)$$

where  $n$  is the order of the SCN [4] and the coefficients of  $H(z)$  can be easily determined.

3- For an objective function of the form

$$F = \sum_{j=1}^n \{ (x_{i,j}^2 - x_{d,j}^2)^2 + (y_{i,j}^2 - y_{d,j}^2)^2 + (w_{i,j}^2 - w_{d,j}^2)^2 + (s_{i,j}^2 - s_{d,j}^2)^2 \} \quad (3)$$

where

$$\begin{aligned} s_{i,j} &= \text{the } j^{\text{th}} \text{ zero of the ideal response} &= x_{i,j} + j y_{i,j} \\ s_{d,j} &= \text{the } j^{\text{th}} \text{ zero of the distorted response} &= x_{d,j} + j y_{d,j} \\ w_{i,j} &= \text{the } j^{\text{th}} \text{ pole of the ideal response} &= w_{i,j} + j s_{i,j} \\ w_{d,j} &= \text{the } j^{\text{th}} \text{ pole of the distorted response} &= w_{d,j} + j s_{d,j} \end{aligned}$$

evaluate the gradient vector  $F$  with respect to the capacitances of the SCN.

4- Using an optimization program (Davidon-Fletcher-Powell method of unconstrained minimization and Cubic interpolation method) [7], obtain a local minimum for equation (3).

## PARALLEL PROCESSING TECHNIQUE

The optimization program is designed to run on a network of transputers [6]. The optimization program consists of a number of local optimization programs (Davidon-Fletcher-Powell method of unconstrained minimization and Cubic interpolation method) [7], [8] and a main program that controls the local optimizations, Figure 1. These programs run concurrently on the transputer network i.e. it is not necessary that one local optimization finishes before another one can begin.

The time required to find a local minimum is much greater than that required to find the next initial optimization point, therefore the first local optimization will not end before the beginning of the next one. This process is illustrated in a simplified form in Figure 2. It can be seen that the search program is idle, waiting for a processor to become free, between some of the data transfers to the processors. It can be seen from Figure 2 that as soon as one local optimization is complete (e.g. local opt. 1), the memory space on that processor becomes available for another local optimization (local opt. 3). There is a potential for increasing the speed of the global optimization by adding more processors to the network.

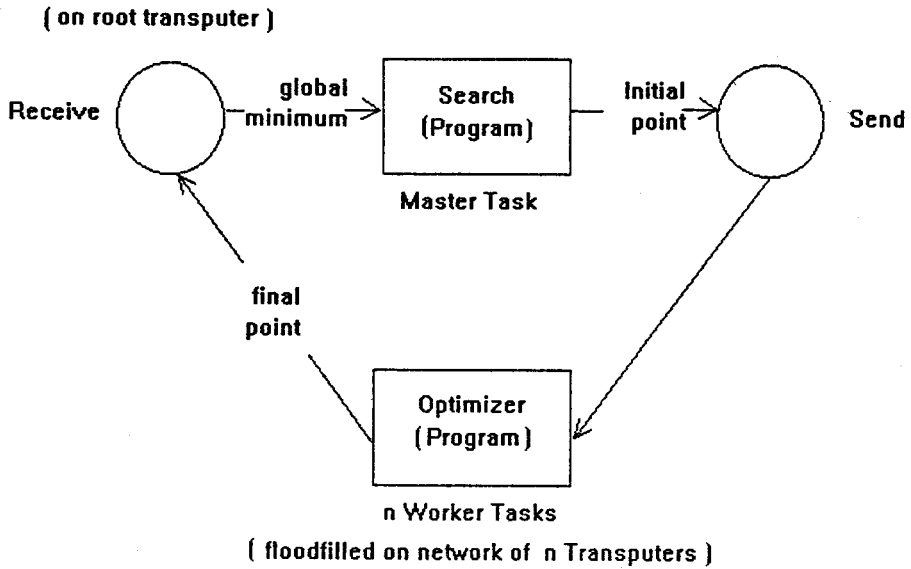


Fig. 1: Configuration of tasks on network

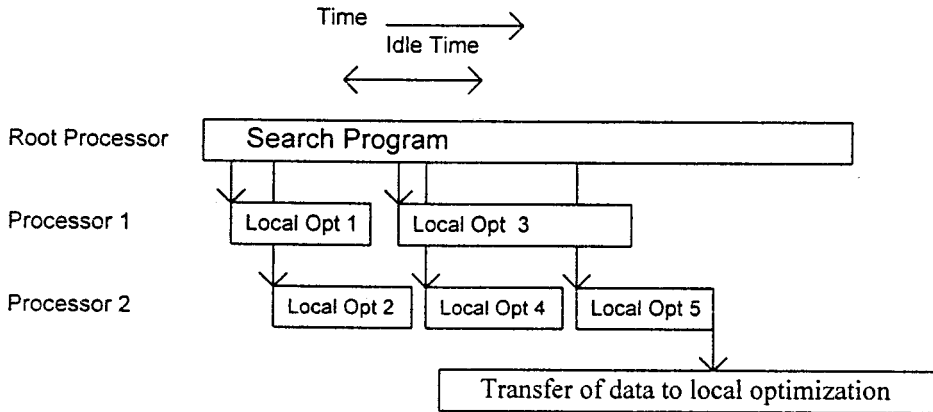
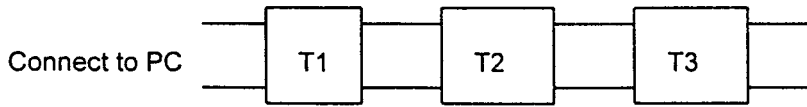


Fig. 2: Processing of tasks on transputer network. Each box represents a program running on a processor, and the length of the box represents the time taken to complete the task.

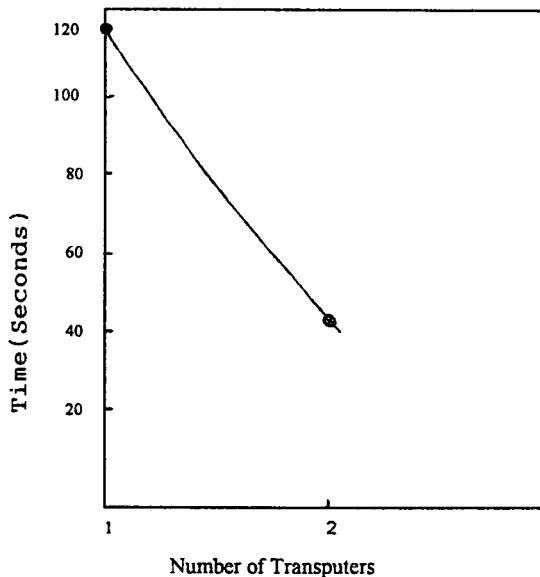
The above is a simplified explanation of the processes involved, assuming that only one local optimization runs on each transputer. In the actual transputer array, it is found that three local optimization processes run on each transputer.

The configuration of the transputers in the network is shown in Figure 3. This configuration is known as a pipeline, because data can only be transferred



**Fig. 3:** Configuration of transputers in network

in the network from each transputer to its nearest neighbor in a linear fashion. Figure 4 shows the timing for a number of local optimizations on different number of transputers.

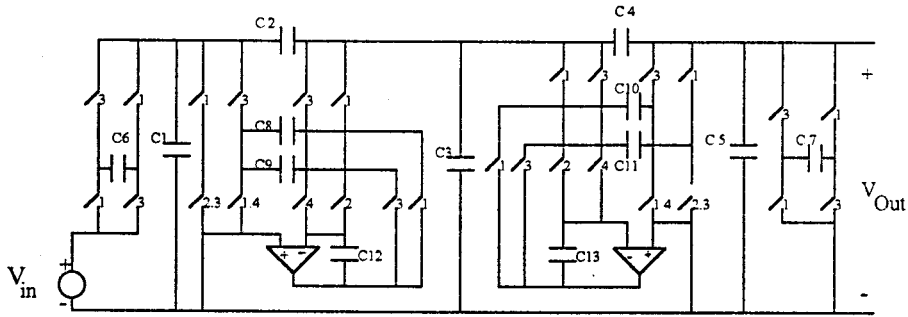


**Fig. 4:** Time to complete 5 local optimizations, averaged over 15 runs of the program, on different number of transputers

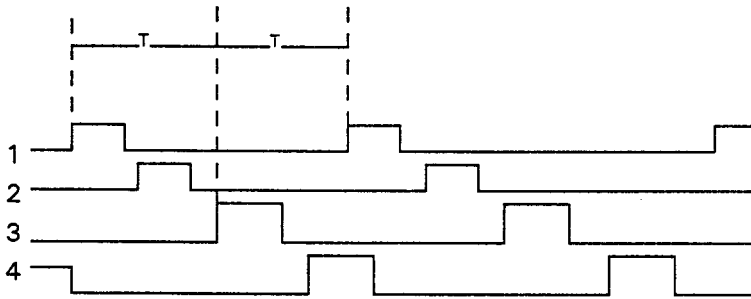
### Example

Figure 5 shows four phase 5<sup>th</sup> order Low Pass Filter that is extracted from reference [2], with the following capacitance values:

C1 = 9.3454	C2 = 1.7553	C3 = 14.453	C4 = 6.8556
C5 = 6.1225	C6 = 1.6667	C7 = 1.670	C8 = 0.9729
C9 = 0.9729	C10 = 1.6035	C11 = 1.6035	C12 = 0.9513
C13 = 1.6234.			



(a)



(b)

**Fig. 5:** a) A four-phase 5<sup>th</sup> order low pass  
b) Timing diagram

Applying the optimization procedure described before, for the case where  $GB = 48000$  and  $f_c$  (clock frequency) = 24 kHz, the resulting component values from this optimization are given in Table 1. Table 2 shows a comparison between the coefficient values and those obtained in reference [5]. Figure 6 shows the frequency response for all cases.

**Table 1**

Component	Value	Values using method in ref. [5]	Parallel computing final values
C1	9.3453	9.3419	9.4198
C2	1.7553	1.7277	1.7555
C3	14.453	14.4443	14.4107
C4	6.8556	6.8328	6.7643
C5	6.1225	6.1186	6.12215
C6	1.6667	1.5737	1.5309
C7	1.670	1.5758	1.8241
C8	0.9729	1.2793	1.21025
C9	0.9729	1.2845	1.2008
C10	1.6035	1.8002	1.8654
C11	1.6035	1.80018	1.8601
C12	0.9513	0.6824	0.6171
C13	1.6233	1.45188	1.3956
GB	Infinity	48000	48000
F	0.0	0.00019118	0.00009877

**Table 2**

Number and den. coefficient	Ideal case	Non-ideal case	Method in ref. [5]	Parallel computing
$a_0$	0.015236	0.015236	0.016442	0.015231
$a_1$	-0.030582	-0.037107	-0.032862	-0.030418
$a_2$	0.043161	0.047245	0.044463	0.041748
$a_3$	-0.028782	-0.030365	-0.029718	-0.027740
$a_4$	0.013877	0.010353	0.013514	0.012774
$a_5$	-0.00000007	0.000118	0.000165	0.000146
$b_1$	-3.341635	-3.521617	-3.366572	-3.331806
$b_2$	5.000830	5.272471	5.063385	4.968662
$b_3$	-4.025122	-4.121185	-4.102966	-3.986884
$b_4$	1.734525	1.621405	1.784943	1.713735
$b_5$	-0.316907	-0.279936	-0.330864	-0.312295

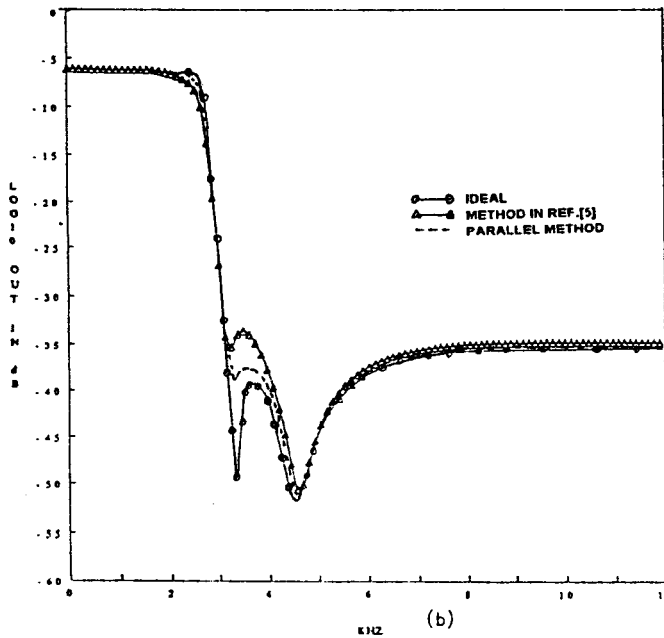
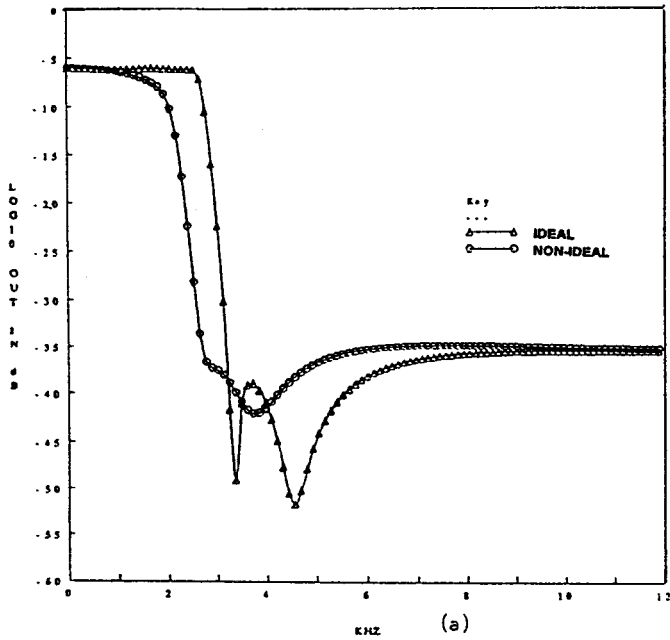


Fig. 6: Frequency response for :  
(a) Ideal and non-ideal  
(b) Ideal, method in ref. [5] and Parallel method



## CONCLUSIONS

It can be seen that a parallel processing approach to optimize the frequency response of SCN with frequency-dependent operational amplifier model is an efficient method for extracting the capacitance values of the SCN in minimum time. Adding more transputers to the network decreases the time needed for the completion of the optimization process.

## REFERENCES

1. **IEEE Press Book, 1984.** on "MOS Switched-Capacitor Filters", Ed. G. Moschytz.
2. **J. Vlach, K. Singhal and M. Martin, Sept. 1984.** "Computer -Oriented Formulation of Equations and Analysis of Switched-Capacitor Networks", IEEE Trans. on Ct. & Sys., Vol. CAS-28, pp. 753-765.
3. **Fahmy, M.K.Makkey and M.M. Doss, August, 1987.** "A Method for Frequency Domain Analysis of Switched-Capacitor Filters", IEEE Trans. on CAS, Vol. CAS-34, pp 955-960.
4. **Fahmy, M.Y.Makkey and M.I. Sobhy, Sept. 1987.** "Time and Frequency Domain Analysis of Non-ideal Switched-Capacitor Circuits", Proc. ECCD '87, pp. 83-88.
5. **Fahmy, M.Y.Makkey and M.I.Sobhy, June 1988.** "Compensation for Amplifier Finite bandwidth in the Design of Switched -Capacitor Networks, "Proc. of ISCAS'88, pp. 2471-2475 Helsinki,
6. **"Transputer Development System", 1988.** INMOS Ltd., Prentice Hall.
7. **A.H.L. Almohanadi. and M.Y.Makkey, 1991.** "Global Minimization Using Cubic Method." 13th IMACS World Congress on Computation and Applied Mathematics, Dublin, IRELAND.
8. **A.H.L. Al Mohanadi, M.Y.Makkey and A. Saleh, 1992.** "Accelerating the convergence of Qubic Interpolation Method Using Concurrent Algorithm based on the Transputer Technology", Eng. Journal of Qatar University, Vol.5, 1992.