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"ON THE DESIGN OF BIT-SLICE PROCESSORS"

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ABSTRACT

In the past decade, fixed instruction microprocessors have evolved from 4 bits to 32 bits. Their compact design and relative low cost have made them very popular with design engineers. Their use extends into a lot of applications. However, in high performance applications their usefulness becomes limited. Bit-slice devices are the answer for such applications. This paper is intended to present principles and to develop familiarity with such devices. In order to understand and appreciate the usefulness of these devices, a simple system is described. This paper discusses the design and construction of the central processing section. The generation of a multi-phase clock is also tackled.

1. INTRODUCTION

Bit-slice devices found their way into the market since the late 1970's. Their superior qualities, mainly those of speed and flexibility, cannot be ignored, their greatest impact is in the tackling of high performance problems (1-4).

Contrary to what some might believe, there exists very little relationship between a microprocessor and a bit-slice processor apart from the fact that both represent modern LSI devices. The former is a stored-program computer, usually described by an instruction set. The latter does not execute programs and is not a computer, although it may be used in building a computer. Also bit-slice architecture is defined by its control variables (1, 2).

Fixed instruction set microprocessors have found their way into a lot of applications. Being MOS devices, their small area and low cost have enabled design engineers to use them extensively. But, in such microprocessors, all computational and control capabilities are limited to what is implemented on the chip. This represents a setback especially when high performance problems must be dealt with (3).

On the other hand, most bit-slice devices are microprogrammed, enabling the designer to achieve a high degree of parallel operations in processing data. A flexible and very powerful computing machine architecture, having a variable instruction set, can thus be implemented. The flexibility of the bit-slice processor enables one to obtain speeds far beyond those realisable by fixed instruction-set MOS microprocessors. A 16-bit by 16-bit multiplication using a Z-80 microprocessor takes about 0.5 ms assuming a 2 MHz clock. A minicomputer, based around bit-slice chips, can achieve this in 5 μs.

Another asset enhances the speed achieved by these flexible structures. The chips are mostly bipolar chips which operate with faster clocks. Their bipolar nature makes them operate at the full military range i.e. (-5°C $-$ 120°C).

2. SYSTEM DESIGN

The goal of this work is to learn about the bit-slice concept and to appreciate its superior capabilities. Thus the Am 2900 family chips, from Advanced Micro Devices, were chosen as being representative components. Literature and documentation are clear and comprehensive. Also the 2900 family offers the designer a variety of different number of support chips.

3. HARDWARE ORGANISATION

A simple system consisting of a 16-bit processing section, a control section and a timing section is chosen.

4. THE PROCESSING SECTION

The Am 2900 is a 4-bit RALU, four chips were used to construct a 16-bit processor. The connection diagram is shown in Figure (1). To latch the output, two octal D-FF chips, type 74LS373, are used. The output is read on LEDs.

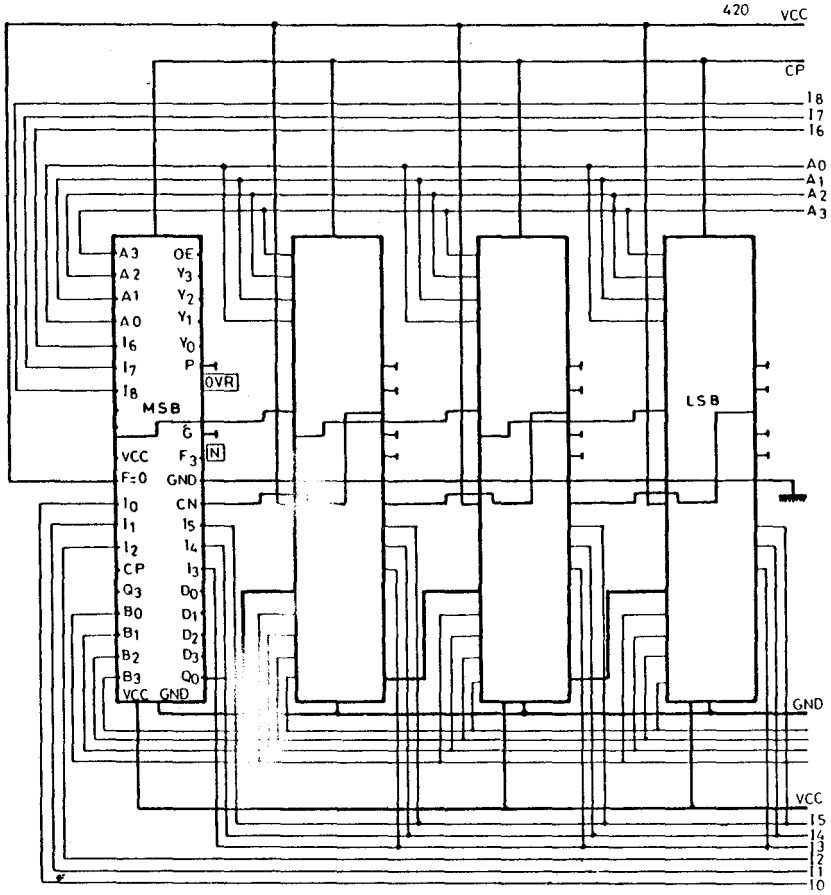

Fig. 1: Interconnection of 4 x 2901.

5. THE CONTROL SECTION

The control section is the heart of the system. A good design makes an efficient, elaborate and powerful system. The control system is made up of three subsystems.

The first subsystem comprises the sequencers. Two AM 2909 chips are connected to give eight address lines, thus enabling the address of 256 words in the control storage. As seen in Figure (2), the OR-lines are grounded as there is no need of implementing multiway branching. The R-lines receive an instruction op-code which is intended to give the first address of a microinstruction in order to implement a macroinstruction. On the other hand the D-lines receive the address from the current microinstruction and this is usually meant to perform branching operations.

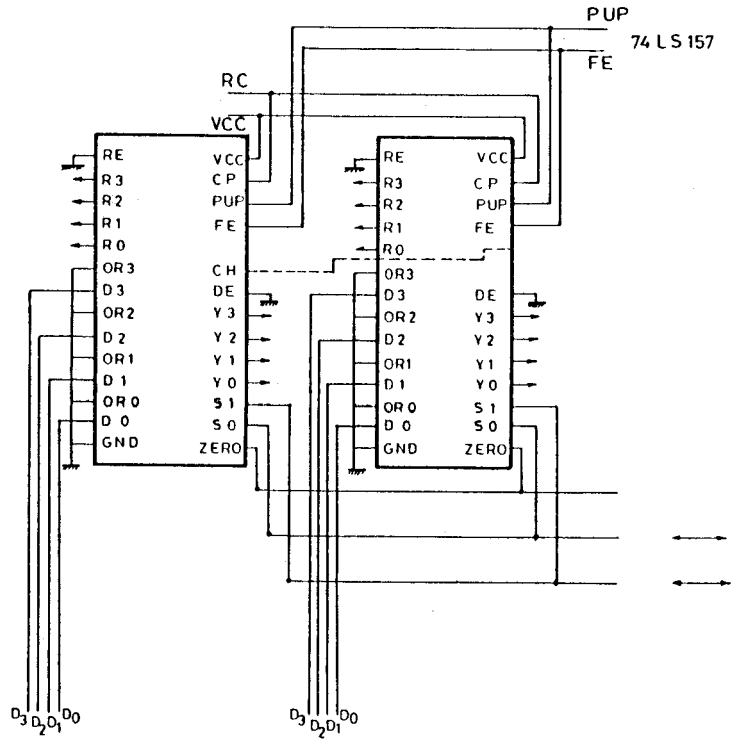

Fig. 2: Interconnection of 2 x 2909.

Eight PROMs, each 256 words deep and 4-bits wide, make up the second subsystem which is the control storage. The 32 bits microinstruction word is connected to the processing section (A, B, and I lines), sequencer (D lines), and the decoding logic in order to determine the next address selection. Figure (3) illustrates the microinstruction word.

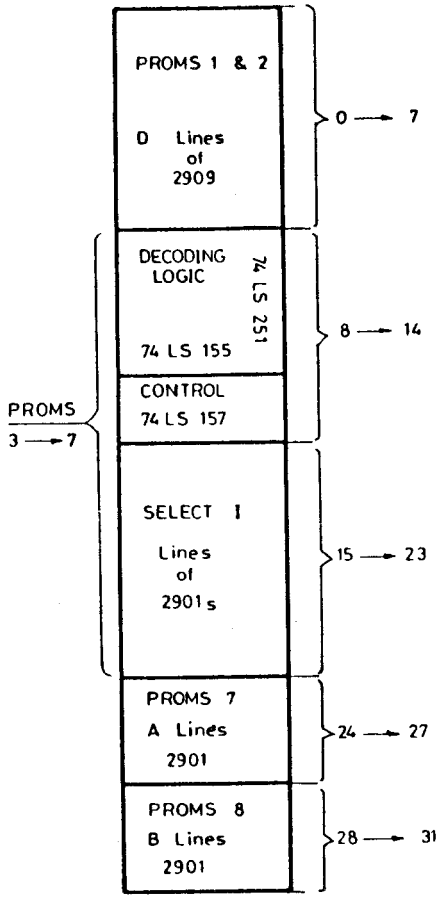

Fig. 3: Microinstruction Format.

The third sybsystem is the decoding logic. From the information it receives from the microinstruction word and the status word from the ALU, the decoding logic indicates to the sequencer the next address. Due to the unavailability of Am 29811, a powerful combinational microprogrammable next address selection LSI chip, MSI/SSI chips are used to build the required decoding logic. Figure (4) shows such a circuit which has five functions namely; CONTINUE, BRANCH to A(Reg), BRANCH to A(D), CALL A(D) and RETURN. These are expected to be sufficient for an educational system which is intended to demonstrate for the student the basic functions.

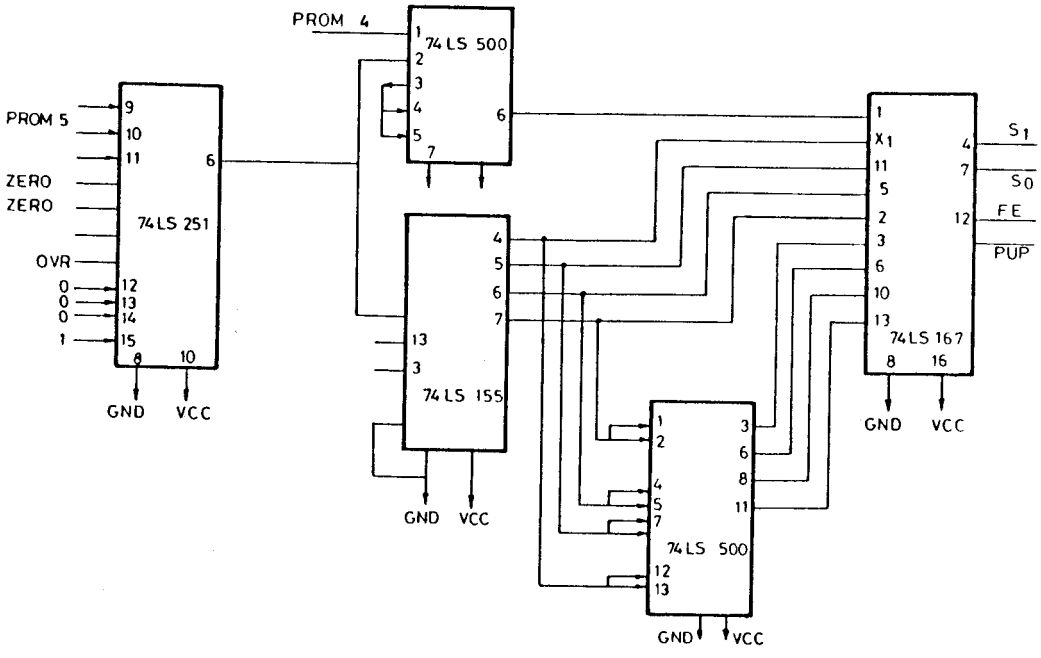

Fig. 4: Decoding Logic Unit.

6. THE TIMING SECTION

The timing section is built around the clock generator and driver Am 2925, together with some SSI chips. The Am 2925 is crystal controlled and has a microprogrammable clock cycle length to provide significant speed up over fixed clock cycle approaches. One of the main characteristics of this chip is its ability to operate in single step mode. This has been made use of, especially that it provides monitoring of the execution step by step. The microcode 101 has been used to generate the waveforms shown in Figure (5).

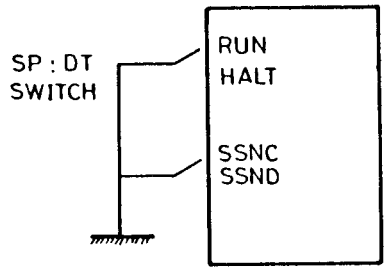

Fig. (5-a): Single Step Mode.

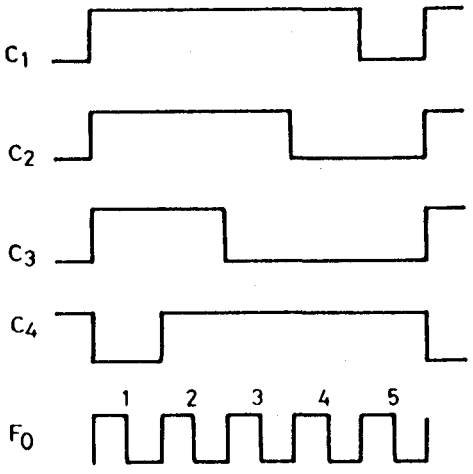

Fig. (5-b).

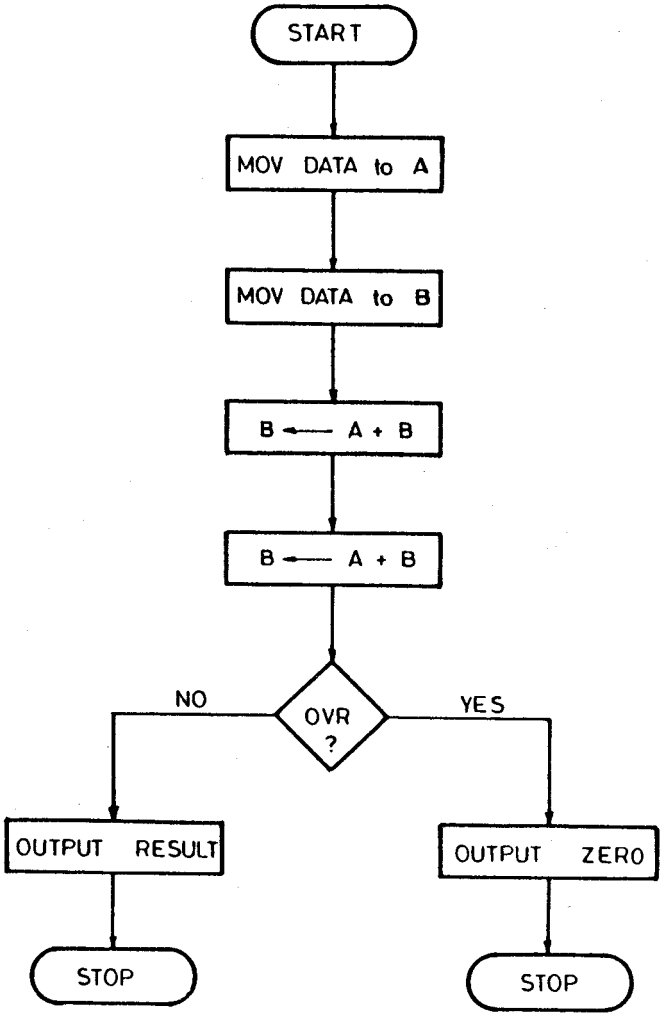

Fig. 6: Test Programme.

7. RESULTS

When first experimenting, the clock pulses were issued to the RALU before enabling the octal latches. It was observed that this initiated a racing condition. The (A+B) operation was always executed as (A+A+B). By issuing the time sequence, explained in the previous section, correct results are obtained.

To demonstrate that the system is operating correctly, a very simple program whose flowchart is given in Figure (6), was microprogrammed. The single step mode is used to follow up the program execution step by step. The program was executed many times sending different data to the ALU. In all cases the system responded correctly.

8. CONCLUSION

An inexpensive educational system, especially designed to help in the teaching and learning process of bit-slice processors, was portrayed. It emphasises the flexibility of the bit-slice approach and its basic concepts. The board permits experimentation with pipelining and microprogramming. The student or the researcher can also experiment with special as well as general purpose instruction sets.

It should be pointed out that the flexibility and properties of the system can be further enhanced by using the Am 29811 chip.

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