

DESIGN AND IMPLEMENTATION OF A MICROPROCESSOR CONTROLLED DIGITAL FILTER

By

K. M. AHMED and M. ABDEL MEGED*
Department of Physics, Faculty of Science,
Qatar University, Doha, Qatar

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ABSTRACT

The construction and implementation of a microprocessor controlled real time recursive digital filter have been given. The system designed could also be applied to a variable coefficients system such as ADAPTIVE FILTER and it makes use of a programmable LSI digital filter and detect "FAD" chip. High flexibility of such system has been proved by the realization of recursive IIR filter with different types and different orders. A wide sampling ranges could be achieved by altering the clock frequency of the filter.

INTRODUCTION

According to the availability of the digital computer as a research tool in all branches of science and technology, and the existence of analogue to digital converter (ADC) and digital to analogue converter (DAC), many filtering operations became widely used and could be carried out digitally rather than with analogue circuits.

The rapid advances in silicon technology, specially the advent of LSI and VLSI circuits, in particular microprocessors have enabled substantial reduction to be made in both the size and the cost of high speed digital signal processing techniques. This allows digital and adaptive filters to be designed in small, powerful single chip devices with realistic sampling rates which enables them to act as a real-time programmable processors. One of these LSI circuits is the digital filter and detect (FAD) chip, employed in the present work, designed as a general purpose device suitable for filtering noisy signals and detecting tones in the audio frequency band (British Telecom Lab., 1982).

*Permanent Address: Physics Department, Faculty of Science, Tanta University, Egypt.

In many practical applications of digital filtering, it is desirable to change the filter characteristics during its operation. Especially in real time filtering, this requires that the filter coefficients can be changed without computation intensive optimization procedure (Jarske, 1988).

The main aim in the present work is to construct a flexible programmable digital **IIR** filter system employing the **FAD IC** as the heart of the system. Such flexibility allows the realization of the system with different types, different orders and selectable sampling rates. This system could be applied to a variable coefficients systems such as **ADAPTIVE FILTERS**. A microprocessor software developed to control the whole system.

The principal motivation for the choice of digital **IIR** filter is the significant reduction in computational load and storage requirements, and therefor hardware saving possible versus **FIR** filters.

The structure of such that filter in the time domain may be described by the following linear difference equation:

$$y(n)T = \sum_{i=0}^N a_i x(n-i)T + \sum_{i=1}^M b_i y(n-i)T$$

and the pulse transfer function of the filter is given by

$$G(Z) = \left(\sum_{i=0}^N a_i Z^{-i} \right) / \left(1 + \sum_{i=1}^M b_i Z^{-i} \right)$$

Where a_i and b_i represent non-recursive and recursive coefficients respectively (Terrell, 1983).

This paper introduces the hardware configuration of the developed filter system, as illustrated by the block diagram in (Fig. 1). Interfacing considerations and problems associated with efficient hardware implementation of the filter operation are also discussed.

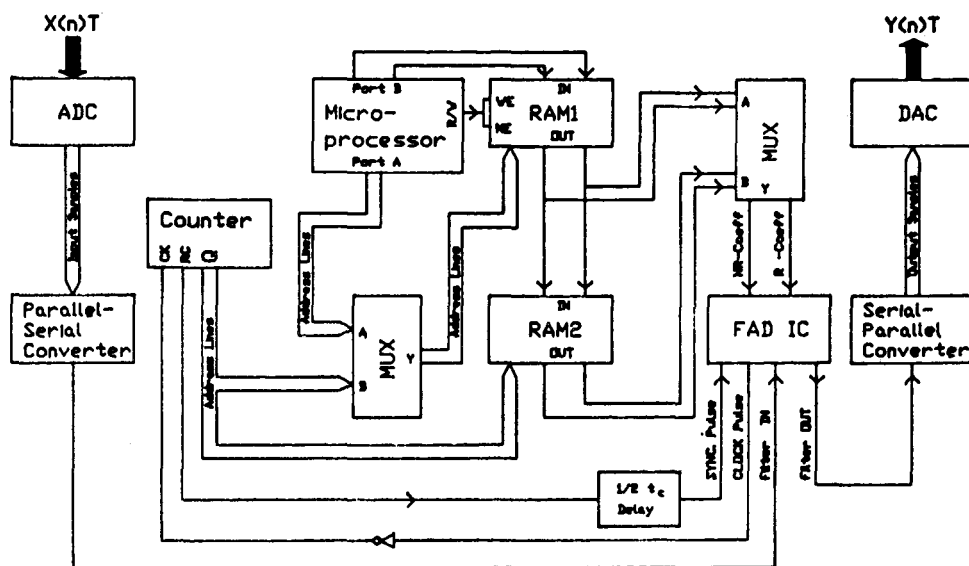


Fig. 1: The IIR Digital Filter System Block Diagram

TECHNIQUES

1. FAD IC ASPECTS

The FAD IC is assembled in a 24 pin DIL and has serial I/O. It is realized as a second order recursive canonic form which consists of four 16*13 serial/parallel multipliers, shift registers as delay elements and a number of adders (British Telecom Lab., 1982).

The transfer function of such filter is given by

$$G(Z) = S (1 + A Z^{-1} + B Z^{-2}) / (1 - a Z^{-1} - b Z^{-2})$$

where **A** and **B** define non-recursive coefficients, **a** and **b** define recursive coefficients, and **S** is the input scaling factor. In order to save computation time, these coefficients are fed, in serial, to the FAD IC in pipeline technique. In practical application the coefficients should be applied for all computation cycles, one computation cycle (**T**) is defined as the time required for serial/parallel coefficient multipliers to operate on their input words and is 32 clock cycles of the FAD IC.

The results obtained by (Liu, 1971) indicated that realizing high order filters with either parallel or cascade forms is considerably more accurate and reduces round-off noise than the direct realization of the same filter. Thus higher order

filters in the **FAD IC** can be built by cascading a number of second order sections. Delays of **1T** and **8T** are provided on the chip to realize second order and sixteenth order filters respectively without the need for external hardware delay requirements. Different orders up to 16 with the same sampling rate could be achieved by forcing to zero the coefficients of the unused sections.

2. COEFFICIENTS FEEDING

A temporary storage (**RAM**) for the filter coefficients has been employed in the design instead of permanent devices in order to implement a flexible system. Such flexibility allows the realization of **IIR** filter with different types and transfer functions, and can be developed as an adaptive filter.

To accomplish the filtering operation with the adequate performance, the **FAD IC** must be fed with one bit of recursive and non-recursive coefficient, in serial, each clock cycle with the aid of the microprocessor. Since such operation exceeds the capability of the microprocessor, so it is interfaced to two separate sets of high speed **RAMs** namely, **RAM1** and **RAM2**, with multiplexed address lines between the microprocessor and a special counter. Each set consist of two **256X1 RAM ICs** with separate input-output lines, as illustrated in (Fig. 1).

In general, for both, fixed and updated (variable) coefficients, feeding operation is carried out in two phases:

The first phase concerns with writing the coefficients into **RAM1** with the aid of the microprocessor as follows:

An assembly language routine was developed to write one bit of each set of coefficient serially into **RAM1** simultaneously, which is addressed through the **PIA** of the microprocessor.

In order to synchronize the microprocessor and **RAM1**, so that **READ/WRITE** control pulses are activated simultaneously. The $\overline{R/\overline{W}}$ line of the microprocessor and \overline{WE} line of **RAM1** are linked together. In regard to the fact that the speed of writing one bit of each coefficient, every clock cycle, by the microprocessor is not sufficient. Therefore **RAM1** is disabled whenever $\overline{R/\overline{W}}$ pulse goes HIGH. This could be achieved by connecting the **MEMORY ENABLE** control input \overline{ME} to $\overline{R/\overline{W}}$ pulse as well, as illustrated by the timing diagram in (Fig. 2). During this time the data stored in **RAM1** does not perturb the **FAD** coefficient's lines.

During the write process, **RAM2**, operated in the **READ** mode, is addressed by a special counter clocked at the frequency of the **FAD IC** and initialized every computation period (**8T**). In that case, the coefficients are transfered, bit by bit, every clock cycle, from **RAM2** to the **FAD IC**.

The write process progresses until all 256 bits are allocated in the appropriate

addressed positions in RAM1.

The second phase concerns with transferring the coefficients in RAM2, which is essential in implementing the adaptive system, the data stored in RAM1 are transferred into RAM2 and simultaneously into the FAD, by addressing both memories by the same counter as shown in (Fig. 1). The state of the control inputs of both RAMs associated with this process are illustrated by the timing diagram in (Fig. 2).

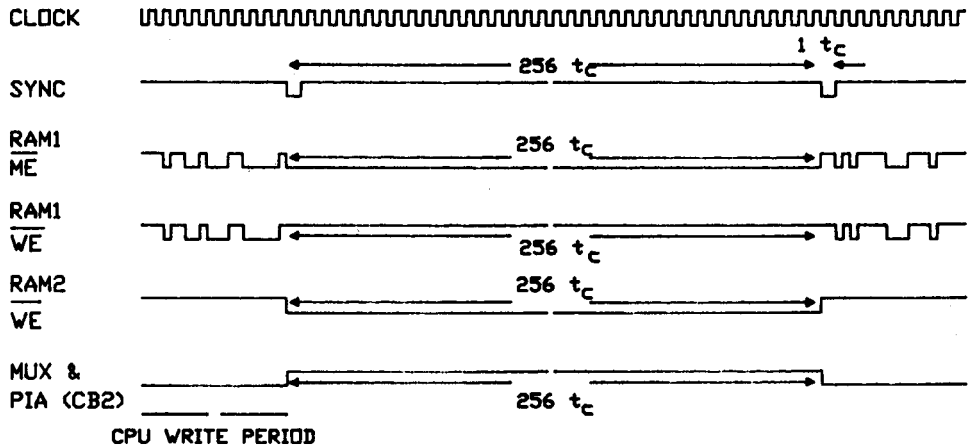


Fig. 2: The IIR Digital Filter System Timing Diagram

3. INPUT-OUTPUT INTERFACING

Most real word quantities are analogue and need some way of communicating with the digital system or vice versa. In this work a 12-bit ADC and DAC with conjunction of parallel-to-serial and serial-to-parallel shift registers are employed to interface the system input and output respectively, refer to (Fig. 1).

By using a 12-bit ADC, a considerable quantization error (Q) reduction could be achieved according to the formula $Q = 1 / (2^n - 1)$ (Liu, 1971, Kwan, 1979), where n is the number of bits.

4. SOFTWARE IMPLEMENTATION

As mentioned before, the realization of the filter system implies a hardware design supported by an assembly language programme. By running such programme, the CPU initializes the PIA and organizes its I/O ports in the desirable directions. Then the CPU starts organizing coefficients bits in the appropriate locations and a stream of coefficients, comprising control bits and scaling factor, are written into RAM1, and consequently into RAM2 and the FAD IC.

The input samples, generated by the ADC, enter the FAD every computation period occupying the first half computation cycle. The filter output samples are valid after a delay of (8 T) where it will be converted to analogue form by the DAC.

RESULTS AND DISCUSSION

The following experimental results obtained by applying real signals to the filter input, demonstrate the good performance, flexibility and the efficiency of the designed IIR filter system.

Firstly, (Fig. 3) demonstrates the Amplitude/Frequency response for eight order low-pass filter at cutoff frequency of 2KHz, which is in agreement with the desired characteristics.

Secondly, the experimental results showing the cancellation performance of the system are illustrated in (Fig. 4). A composite signal made up of two sinusoids with different frequencies (700 Hz, and 3 KHz) is applied to the above low-pass filter input. The low frequency signal (700 Hz) was reproduced at the filter output.

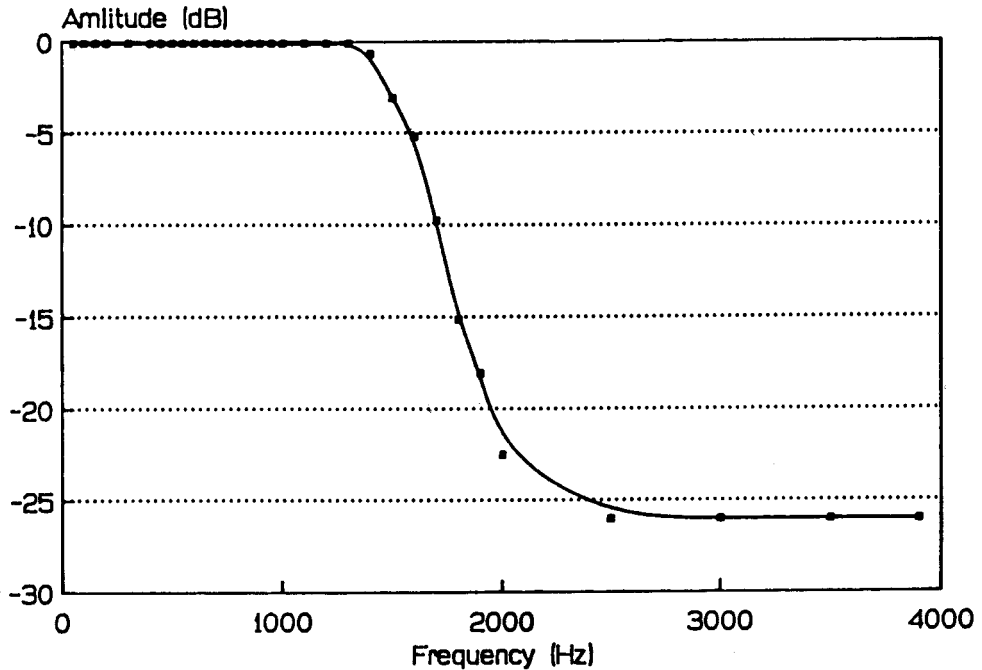


Fig. 3: Amplitude/Frequency Response for Low-Pass Digital Filter

Time domain and frequency domain (frequency spectrum) representation of both input and output signals are given.

Finally, high-pass filter with different orders have been realized using the low to high-pass filter transformation (Oppenheim, 1975):

$$Z^{-1} = - (Z^{-1} + \alpha) / (1 + \alpha Z^{-1})$$

where $\alpha = - \cos ((w + \theta)/2) / \cos ((w - \theta)/2)$,

θ and ω are the cutoff frequencies of the low and the desired high-pass filters respectively. The basic high-pass second order building block is formulated by

$$G(Z) = (1 + A_h Z^{-1} + B_h Z^{-2}) / (1 - a_h Z^{-1} - b_h Z^{-2})$$

where A_h , B_h , a_h , and b_h are the high-pass filter coefficients.

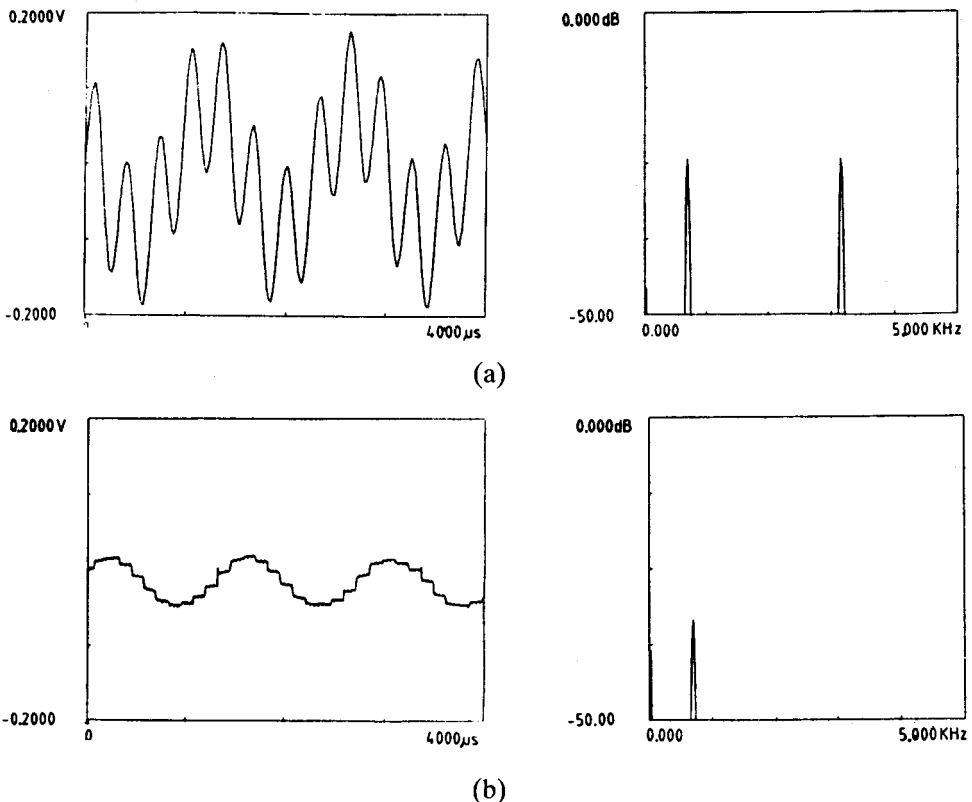


Fig. 4: Experimental results showing the cancellation performance of the IIR filter system

- (a) Input signal and spectrum
- (b) Output signal and spectrum

In order to compute the non-recursive coefficients, the following formulas have been driven:

$$A_h = (- A (1 + \alpha^2) + 2 \alpha (B + 1)) / C$$

$$B_h = (\alpha^2 - A \alpha + B) / C$$

where $C = B \alpha^2 - A \alpha + 1$

Similarly the recursive coefficients a_h and b_h can be driven by replacing A with $-a$ and B with $-b$ in the above equations, where A , B , a , and b represent the corresponding low-pass filter coefficients.

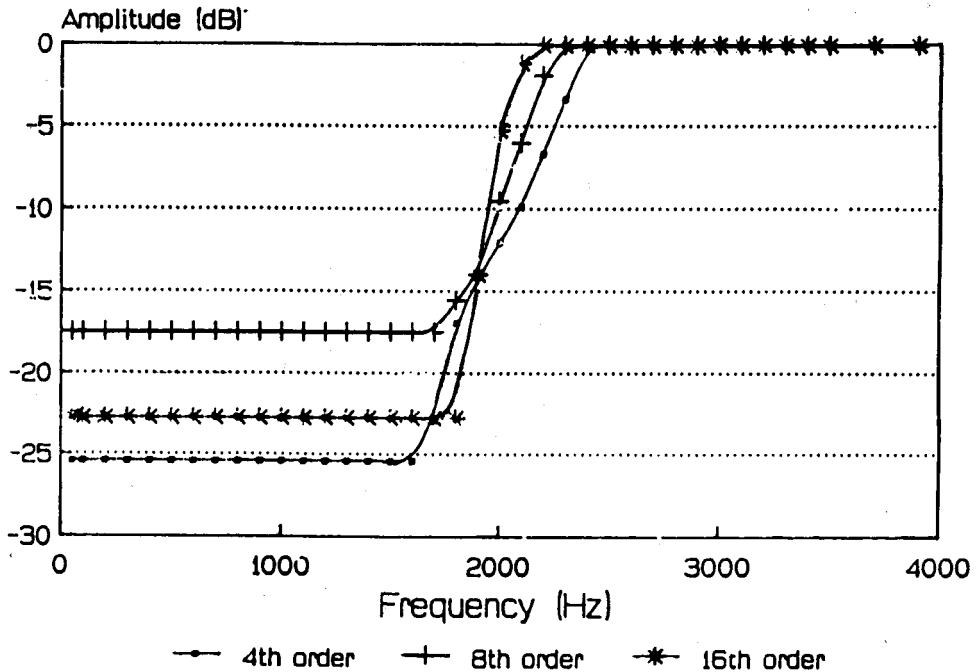


Fig. 5: Amplitude/Frequency Response for High-Pass Digital Filters

These coefficients, represented in two's complement form, have been computed by developing a high level language programme. (Fig. 5) represents the Amplitude/Frequency response of 4, 8, and 16 order high-pass filters. It is obvious that the filter order is proportional to the inverse of the transition between stop and pass bands.

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تصميم المرشحات الرقمية باستخدام العاملات الميكرووية

قدرية محمد علي أحمد و محمود مصطفى كامل عبد المجيد

اشتمل هذا البحث على تصميم وتنفيذ إحدى المرشحات الرقمية التي يتم التحكم بها بواسطة العاملات الميكرووية (الميكروبروسسورز) . تتم عملية الترشيح بحساب الدالة $T(n) \gamma$ والتي تعتمد على تغذية المرشح بمعاملات خاصة يتم حفظها في ذاكرة مناسبة . هذه المعاملات تعتمد على نوع المرشح المراد تنفيذه ، بالإضافة إلى ادخال القيم الرقمية المناظرة للإشارات القياسية المطلوب ترشيحها .

يتميز هذا التصميم بمرونة عالية تسمح بتنفيذ العديد من المرشحات بأنواع ورتب مختلفة ، كذلك إدخال الإشارات القياسية بترددات مختلفة ، كما يمكن تطبيق هذا النظام في المرشحات الانضباطية . يتم التحكم في هذا النظام عن طريق توصيله بأحدى الميكروبروسسورز والتي يتم برمجتها بهدف تغذية المرشح بالمعاملات اللازمة .

نظراً لعدم توافق سرعة الميكروبروسسورز مع السرعة العالية نسبياً واللازمة لتغذية دوائر الترشيح بالمعاملات ، إستدعت الحاجة لإستخدام ذاكرتين منفصلتين لإجراء هذه العملية على مرحلتين : في المرحلة الأولى يقوم الميكروبروسسور بتغذية الذاكرة الأولى بالمعاملات الجديدة بينما تعمل الذاكرة الثانية على تغذية المرشح بالمعاملات المخزونة بها . أما في المرحلة الثانية فيتم نقل المعاملات من الذاكرة الأولى إلى الذاكرة الثانية والمرشح في آن واحد بسرعة دوائر الترشيح مما يحافظ على إستمرارية أداء المرشح بدون توقف .

للقوف على كفاءة وأداء النظام الذي تم تصميمه إشتمل البحث على تطبيقات لإشارات حقيقية على النحو التالي :

- ١ - إستخدام النظام كمرشح ترددات منخفضة مع التحليل الترددي لاشارتي الدخل والخرج للمرشح لبيان كفاءته في التخلص من الإشارات غير المرغوب فيها .
- ٢ - دراسة العلاقة بين كفاءة مرشح الترددات العالية ورتبته .